EVALUATION KIT AVAILABLE

MAX11068

12-Channel, High-Voltage Sensor, Smart Data-Acquisition Interface

General Description

The MAX11068 is a programmable, highly integrated, high-voltage, 12-channel, battery-monitoring smart data-acquisition interface. It is optimized for use with batteries used in automotive systems, hybrid electric battery packs, electric cars, and any system that stacks long series strings of secondary metal batteries. This highly integrated battery sensor incorporates a simple state machine and a high-speed I²C bus for SMBus™-laddered serial communication.

The MAX11068 analog front-end combines a 12-channel voltage measurement data-acquisition system with a high-voltage switch bank input. All measurements are done differentially across each cell. The full-scale measurement range is from 0 to 5.0V, with full stated accuracy guaranteed from 0.5V to 4.7V. The input mux/switch bank allows for differential measurement of each cell in a series stack. A high-speed, 12-bit successive approximation (SAR) A/D converter is used to digitize the cell voltages. All 12 cells can be measured in less than 107µs. The MAX11068 uses a two-scan approach for collecting cell measurements and correcting them for errors. The first phase of the scan is the acquisition phase where the voltages of all 12 cells are acquired. The second phase is the error-cancellation phase where the ADC input is chopped to remove errors. This two-phase approach yields excellent accuracy over temperature and in the face of extreme noise in the system. The MAX11068 incorporates an internal oscillator that generates a 6.0MHz system clock with ±3.0% accuracy.

The MAX11068 consumes less than 2.0mA from the power supply while in data-acquisition modes. This current is reduced to 75µA in standby mode and less than 1µA in shutdown mode. The device is packaged in a 38-pin, 9.7mm x 4.4mm x 1.0mm TSSOP package that is lead free and RoHS compliant and is designed to operate over the AEC-Q100 Grade 2, -40°C to +105°C temperature range.

Applications

High-Voltage, Multicell Series-Stacked-Battery Systems

Electric and Hybrid Electric Vehicle (HEV) Battery Packs

Electric Bikes

High-Power Battery Backup Systems

SuperCap Backup Systems

Power Tools

SMBus is a trademark of Intel Corp.

Features

- **12-Cell Battery Voltage Measurement with Temperature Monitoring**
  - **Up to 12 Lithium-Ion (Li+), NiMH, or Super-Cap Cells**
  - **Two Auxiliary Analog Inputs for Temperature Measurement**
- **High-Accuracy I/Os**
  - **Excellent ±0.25% Voltage-Measurement Accuracy**
  - **≤ 5mV Offset Voltage**
- **Integrated 12-Channel Data-Acquisition System**
  - **12-Channel High-Voltage Mux to ADC**
  - **Differential Cell-Voltage Measurement**
  - **12-Bit Precision, High-Speed SAR ADC**
  - **12 Cell Voltages Measured Within 107µs**
- **Battery-Fault Detection**
  - **Overvoltage and Undervoltage Digital Threshold Detection**
  - **Cell Sense Line Open-Circuit Detection**
  - **High/Low Temperature Digital Threshold Detection**
- **12 Integrated Cell-Equalization Switches**
  - **Support Up to 200mA**
- **Integrated 6V to 70V Input Linear Regulator**
- **Integrated 25ppm/°C, 2.5V Precision Reference**
- **Integrated Level-Shifted, I²C-Compliant SMBus Ladder Interface**
  - **Supports Multiple Devices, Up to 31 SMBus-Ladder-Connected ICs**
  - **Communications Protocol with Autoaddressing**
  - **Fault-Tolerant Hardware Handshake and Data CRC Checking**
- **Three General-Purpose Digital I/O Lines**
- **Ultra-Low Power Dissipation**
  - **Standby Mode Quiescent Current Drain 75µA**
  - **Shutdown Mode Leakage Current 1µA**
- **Operating Temperature Range from -40°C to +105°C (AEC-Q100 Grade 2)**
- **38-Pin, Lead-Free/RoHS-Compliant TSSOP Package (9.7mm x 4.4mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11068GUU+	-40°C to +105°C	38 TSSOP
MAX11068GUU/V+	-40°C to +105°C	38 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V Denotes an automotive qualified part.

ABSOLUTE MAXIMUM RATINGS

HV, VDD_U, GND_U, DCIN to AGND	-0.3V to +80V
HV to C12	-0.3V to +6V
C1–C12 to AGND	-0.3V to (V_{HV} + 0.3V)
C(N+1) to C(N)	-0.3V to +9.0V
C0 to AGND	-0.3V to +4.0V
$\overline{SHDN}$ to AGND	-0.3V to +60V
VAA to AGND	-0.3V to +4.0V
VDD_L to GND_L	-0.3V to +4.0V
VDD_U to GND_U	-0.3V to +6.0V
GND_U to GND_L	-0.3V to +80V
AGND to GND_L	-0.3V to +0.3V
AUXIN1, AUXIN2, THRM to AGND	-0.3V to +6.0V
REF to AGND	-0.3V to (VAA + 0.3V)
SCL_L, SDA_L, $ALRM_L$ to GND_L	-0.3V to (VDD_L + 0.3V)
SCL_U, SDA_U, $ALRM_U$ to GND_U	-0.3V to (VDD_U + 0.3V)
CP+ to AGND	(GND_U - 1.0V) to (VDD_U + 1.0V)
CP- to AGND	-0.3V to (GND_U + 0.3V)
GPIO0, GPIO1, GPIO2	-0.3V to (VDD_L + 0.3V)
ESD Rating (HBM, Note 1) C0–C12, AUXIN1, AUXIN2, REF, VAA, VDD_U, GND_U, VDD_L, GND_L, DCIN, $\overline{SHDN}$, CP+, CP-, HV, SCL_U, SDA_U, $ALRM_U$, SCL_L, SDA_L, $ALRM_L$, GPIO0, GPIO1, GPIO2	±2kV
Maximum Continuous Current into Any Pin	20mA
ESD Diode Maximum Average Power Dissipation for Hot Plug (Note 2)	$14.4/\sqrt{\tau}$ W
Continuous Power: Multilayer Board	1269.8mW
Continuous Power: Single-Layer Board (derating 15.9mW/°C above +70°C)	1095.9mW
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-55°C to +150°C
Junction Temperature (continuous)	+150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Note 1: Human Body Model to Specification MIL-STD-883 Method 3015.7.

Note 2: Maximum average power dissipation for time period τ. Peak current must never exceed 2A. τ is one time constant (in µs) of hot-plug current waveform through a given diode. For example, if τ is 330µs, the maximum average diode power dissipation is 0.793W. Actual average power dissipation must be calculated from current waveform for the application circuit.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. V_{GNDU} = V_{DCIN} = 18V to +60V, typical values are at T_A = +25°C, unless otherwise specified from -40°C to +105°C per the application circuit in Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
C0–C12 INPUTS						
Differential Cell Input-Voltage Range	$VCELL_{XIN}$	Any 2 inputs CN+1 to CN for C12–C0 (Note 2)	0.5		4.7	V
Cell Input Common-Mode Voltage Range (Note 5)	VC_{XIN}	Input C1 referred to AGND	0.7		7.0	V
		Inputs C2 through C[TOP] referred to AGND	0.7			
		C[TOP] referred to AGND			GND_U	
		C0 referred to AGND	-0.05		+0.05	
Input-Leakage Current	I_{CXIN}	ADC off; C(N) to C(N+1) = 5V	-1.0		+1.0	µA
		ADC ON; C(N) to C(N+1) = 3V		±10.0		
ADC Resolution	ADC_{BITS}	LSB size is +1.22mV	12			Bits
Channel- Conversion Time	t_S	Highest enabled input		11.34		µs/ Channel
		Enabled inputs except highest		7.66		
Channel Accuracy		T_A = +25°C (Note 4); V_{CELL} = 3.0V	-5		+5	mV
		-10°C < T_A < +50°C; V_{CELL} = 3.0V (Note 3)	-10		+10	
		-40°C < T_A < +85°C; V_{CELL} = 3.0V (Note 3)	-15		+15	
		-40°C < T_A < +105°C; V_{CELL} = 3.0V	-20		+20	

ELECTRICAL CHARACTERISTICS (continued)

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. V_{GNDU} = V_{DCIN} = 18V to +60V, typical values are at T_A = +25°C, unless otherwise specified from -40°C to +105°C per the application circuit in Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Nonlinearity	DNL	No missing codes at 12 bits		±1.0		LSB
Channel Offset Error	$CELLV_{OS}$	Cells 1 through 12	-5		+5	mV
Channel Gain Error	$CELLA_V$	Cells 1 through 12	-1.0		+1.0	%
Cell-Balancing Switch Resistance		R_{SWITCH} from C(N) to C(N+1) when enabled	1.5	6	20	Ω
AUXIN1, AUXIN2 INPUTS						
Absolute Differential Input Range	VAUXINXIN	AUXIN1, AUXIN2 to AGND; ADC REF = THRM	0		V_{THRM}	V
Common-Mode Input-Voltage Range		Inputs AUXIN1/2 referred to AGND	0		V_{THRM}	V
Input-Leakage Current	I_{AUXIN}	ADC off; input voltage = 3.3V	-1.0		+1.0	µA
ADC Resolution			12			Bits
Conversion Time	t_S			10		µs/ AUX_ Input
Accuracy		T_A = +25°C	-0.5		+0.5	%
		-40°C < T_A < +105°C	-1.0		+1.0	
Differential Nonlinearity	DNL	No missing codes at 12 bits		±1.0		LSB
Offset Error	$AUXV_{OS}$	AUXIN1, AUXIN2	-8		+8	mV
Gain Error	$AUXA_V$	AUXIN1, AUXIN2	-1.0		+1.0	%
THRM Switch Resistance	R_{THRM}	THRM to VAA (Note 3)	5	18	28	Ω
VOLTAGE REFERENCE						
Output REF Voltage	$REFV_{OUT}$	T_A = +25°C	2.45	2.50	2.55	V
REF Output Short-Circuit Current	I_{REF-SC}			±12.5		mA
Temperature Coefficient	ΔREF/ ΔTEMP			±25		ppm/°C
Initial Drift	Change after 1000hr burn-in			120		ppm
LOGIC INPUTS AND OUTPUTS (GPIO AND $\overline{SHDN}$)						
$\overline{SHDN}$ Voltage High			1.8			V
$\overline{SHDN}$ Voltage Low					0.5	V
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 3.4V			1	µA
		$V_{\overline{SHDN}}$ = 30V		5.15	18	
		$V_{\overline{SHDN}}$ = 56V		12.6	45	
GPIO Input Voltage Low					0.8	V
GPIO Input Voltage High			2.4			V
I/O Leakage Current		I/O pins programmed to high impedance	-1	+2	+6.2	µA
GPIO Output Voltage Low		I_{SINK} = 3mA			0.4	V
GPIO Output Voltage High		I_{SOURCE} = 3mA	VDD_L - 0.5			V

ELECTRICAL CHARACTERISTICS (continued)

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. V_{GNDU} = V_{DCIN} = 18V to +60V, typical values are at T_A = +25°C, unless otherwise specified from -40°C to +105°C per the application circuit in Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR +3.4V (VAA)						
Input Voltage Range	V_{DCIN}	0 < I_{LOAD} < 8mA	6.0		70	V
Output Voltage	V_{VAA}	0 < I_{LOAD} < 8mA; 6V < V_{DCIN} < 70V	3.25	3.4	3.55	V
Short-Circuit Current		VAA = 0V, 6V < V_{DCIN} < 30V			60	mA
Power-On Reset Threshold (Note 3)		Falling VAA	2.85	2.95	3.05	V
		Rising VAA	2.9	3.0	3.1	
		POR threshold hysteresis	0.01	40	80	mV
Thermal Shutdown		Rising temperature		+145		°C
Thermal-Shutdown Hysteresis				15		°C
CHARGE PUMP +3.4V						
Output Voltage	V_{VDDU} - V_{GNDU}	I_{LOAD} = 0 at 0.1µF CP+ to CP-	3.2	3.4	3.55	V
		1mA = I_{LOAD} at 0.1µF CP+ to CP-	3.2	2.5	3.55	
Charge-Pump Efficiency		I_{VDDU}/I_{GNDU} - I_{VDDU} at 2.7V, VDD_U - GND_U	60	89	99	%
Charge-Pump Undervoltage Threshold	V_{CPUV}		2.0	2.7	3.2	V
INTERNAL OSCILLATORS (32.768kHz, 6.0MHz)						
Internal 32.768kHz Oscillator Frequency	f_{WD-OSC}		32.113	32.768	33.423	kHz
Internal 6.0MHz Oscillator Frequency	f_{HF-OSC}		5.82	6.0	6.18	MHz
I²C LOWER PORT SCL_L, SDA_L, $ALRM_L$ (Relative to GND_L, VDD_L = Nominal 3.4V)						
SDA_L, SCL_L Input Voltage Low					0.3 x V_{VDDL}	V
SDA_L, SCL_L Input Voltage High			0.7 x V_{VDDL}			V
SDA_L, SCL_L Input Hysteresis			0.2	0.1 x V_{VDDL}	0.5	V
SDA_L, $ALRM_L$ Output Voltage Low		At sink = 3mA			0.4	V
SDA_L, SCL_L Leakage Current		V_{SDAL} = V_{SCLL} = 1.5V			1.0	µA
SDA_L, Managed Resistance	R_{ACTIVE_EDGE}	Active edge	0.5	1	3	kΩ
		Managed passive state	35	50	75	
		Off passive state		1		MΩ
	t_{ONE_SHOT}	t_{ONE_SHOT} (active edge pulse)	150	250	380	ns
SDA_L 1-TAU Capacitance	C_{1_TAU}	SDA_L rises to 70% within active edge time when loaded with this capacitance	120	280	550	pF
$ALRM_L$ Output High Voltage		At source = 3mA	VDD_L - 0.4			V
$ALRM_L$ Heartbeat Frequency		OSC = 32.768kHz ±2.0%	16,000	16,384	16,711	kHz
Lower Port Input Capacitance		SCL_L, SDA_L, $ALRM_L$		15		pF

ELECTRICAL CHARACTERISTICS (continued)

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. V_{GNDU} = V_{DCIN} = 18V to +60V, typical values are at T_A = +25°C, unless otherwise specified from -40°C to +105°C per the application circuit in Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I^{2}C UPPER PORT SCL_U, SDA_U, $ALRM_U$ (Relative to GND_U, VDD_U)						
SDA_U, $ALRM_U$ Input Voltage Low					0.3 x V_{VDDU}	V
SDA_U, $ALRM_U$ Input Voltage High			0.7 x V_{VDDU}			V
SDA_U, $ALRM_U$ Input Hysteresis			0.05	0.1 x V_{VDDU}	0.4	V
SDA_U, SCL_U Output Voltage Low		At sink = 3mA			0.4	V
SDA_U, SCL_U Leakage Current		V_{SDAU} = V_{SCLU} = 1.5V	-1	±1.0	+1	µA
SDA_U, Managed Resistance		Active edge	0.5	1	3	kΩ
		Managed passive state	30	50	75	kΩ
		Off passive state		1		MΩ
	t_{ONE_SHOT}	t_{ONE_SHOT} (active edge pulse)	150	250	480	ns
SDA_U 1-TAU Capacitance		SDA_U rises to 70% within active edge time when loaded with this capacitance, i.e., choose 100pF to guarantee 3τ rising edge	120	280	550	pF
$ALRM_U$ Clamp Current		V_{ALRMU} = VDD_U + 0.15V			1	µA
		V_{ALRMU} = GND_U - 0.15V			1	
$ALRM_U$ Clamp Voltage		250µA current pulling below GND_U	GND_U -0.49			V
		250µA current pulling above VDD_U			VDD_U + 0.49	V
Upper Port Input Capacitance		SCL_U, SDA_U, $ALRM_U$		8		pF
Port-to-Port Level Delay					1	µs
Interface Startup		From $\overline{SHDN}$ or from POR		3		ms
I^{2}C TIMING CHARACTERISTICS						
I^{2}C Clock Frequency	f_{I2C}		10		200	kHz
Bus Timeout Period	$t_{TIMEOUT}$	Timeout for maximum clock low/high time		27.4		ms
Bus Free Time	t_{BUF}	Master to slave delay from a STOP to the next START command	500			µs
Bus Hold Time	t_{HD-STA}	Master hold time after a START command	350			µs
Bus START Command Setup Time	t_{SU-STA}	Repeated START setup time	1			µs
Bus STOP Command Setup Time	$t_{SU-STOP}$	STOP condition setup time	100			ns
SDA Data Hold Time	SLAVE PORT t_{HD-DAT}	Transmit	500			ns
		Receive	-30			
	MASTER PORT t_{HD-DAT}	Transmit	400			
		Receive (Note 7)	400			

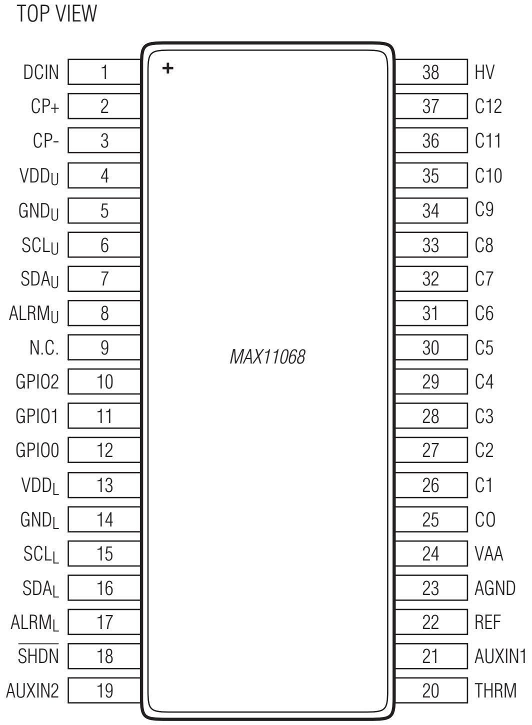
ELECTRICAL CHARACTERISTICS (continued)

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. V_{GNDU} = V_{DCIN} = 18V to +60V, typical values are at T_A = +25°C otherwise specified from -40°C to +105°C per the application circuit in Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Data Setup Time	SLAVE PORT t_{SU-DAT}	Transmit (Note 7)	250			ns
		Receive	250			
	MASTER PORT t_{SU-DAT}	Transmit (Note 7)	250			
		Receive	1000			
SCL_L Low Time	t_{LOW}		1.25			µs
SCL_L High Time	t_{HIGH}		1.25			µs
Remastered Clock Minimum High Time	$t_{MCL-MIN}$		1			us
LEVEL-SHIFT TIMING						
Level Shift Delay (SDA_L to SDA_U or SDA_U to SDA_L)	t_{LS-DAT}	Rising or falling edge at 1.5V threshold; pin-to-pin delay with 100pF loading	400		1100	ns
Level Shift Delay (SCL_L to SCL_U)	t_{LS-CLK}	Rising or falling edge at 1.5V threshold; pin-to-pin delay with 100pF loading	600		800	ns
POWER-SUPPLY REQUIREMENTS DCIN						
Current Consumption (**Note:** IDD_Q testing is done in production test with a coverage of 71%)	I_{DCIN} Acquisition Mode	High-voltage mux enabled, ADC converting 12 channels; V_{DCIN} = 30V		3.0	6	mA
	I_{HV} Acquisition Mode			4.1	9.6	
	I_{DCIN} Cell-Balancing Mode	Cell balancing enabled for four switches, LDO, REF, and OSC running; V_{DCIN} = V_{GNDU} = 6V		70		µA
	I_{GNDU} Cell-Balancing Mode			63		
	I_{DCIN} Standy Mode	No conversions or cell balancing; LDO, REF, and OSC running, $\overline{SHDN}$ = 1		55	150	
	I_{GNDU} Standby Mode			20	130	
	I_{DCIN} Shutdown Mode	$\overline{SHDN}$ = 0		0.25	2	
	I_{GNDU} Shutdown Mode			0.3	2	

Note 3: Guaranteed by design and not production tested.
Note 4: Differential input voltage range for which channel gain and offset error applies.
Note 5: Common-mode level at each pin required for specified operation of the high-voltage mux.
Note 6: Offset and gain error are calibrated at +25°C and 3.0V per cell at the factory, assuming that VC_{XIN} is met.
Note 7: This is a derived specification. No characterization required. These specifications involve the clock low time and clock high time used.

Pin Configuration



TSSOP
9.7mm x 4.4mm

Pin Description

PIN	NAME	FUNCTION
1	DCIN	DC Power-Supply Input. DCIN supplies the internal 3.4V regulator, which provides low-voltage power to the device. Bypass DCIN to GND with a 1µF capacitor.
2	CP+	Charge-Pump Capacitor Plus Input for the Internal Charge Pump. Connect a 0.1µF high-voltage capacitor between CP+ and CP-.
3	CP-	Charge-Pump Capacitor Minus Input for the Internal Charge Pump. Connect a 0.1µF high-voltage capacitor between CP+ and CP-.
4	VDD$_U$	Level-Shifted Upper I^{2}C Port Digital Supply for Use in Communicating with an Upper, Neighboring Battery Module. This is a regulated output voltage from the internal charge pump that is level shifted above the DCIN pin voltage level.
5	GND$_U$	Level-Shifted Upper I^{2}C Port Ground. This pin is the reference level and ground return for VDD$_U$ and also the supply input for the charge pump. It should be tied to the DCIN takeoff point on the battery stack as shown in the application diagrams.
6	SCL$_U$	Level-Shifted Upper Port I^{2}C Clock Line. SCL$_U$ is the I^{2}C clock line communicating with the upper neighboring battery module. This pin swings between VDD$_U$ and GND$_U$.
7	SDA$_U$	Level-Shifted Upper Port I^{2}C Bidirectional Serial Data Line. SDA$_U$ is the I^{2}C data line communicating with the upper neighboring battery module. This pin swings between VDD$_U$ and GND$_U$.

Pin Description (continued)

PIN	NAME	FUNCTION
8	ALRM_U	Upper Port Alarm Input. Overvoltage, undervoltage, over/undertemperature, cell mismatch, and communication fault. The alarm signal is laddered. This signal is referenced to VDD_U and GND_U. Connect this signal to VDD_U through a pullup resistor.
9	N.C.	Not Internally Connected/Test I/O. Leave open; do not connect any external circuit to this pin.
10	GPIO2	General-Purpose I/O 2. This pin swings between VDD_L and GND_L.
11	GPIO1	General-Purpose I/O 1. This pin swings between VDD_L and GND_L.
12	GPIO0	General-Purpose I/O 0. This pin swings between VDD_L and GND_L.
13	VDD_L	Lower Port I^2C + 3.4V Digital Supply Input. Connect to VAA and decouple to GND_L with a 0.47µF capacitor.
14	GND_L	Lower Port I^2C Common or Ground. A star ground connection to AGND is recommended.
15	SCL_L	Lower Port I^2C Clock. SCL_L is the I^2C clock line communicating with the lower neighboring battery module. This pin swings between VDD_L and GND_L.
16	SDA_L	Lower Port I^2C Data I/O. SDA_L is the I^2C serial data line communicating with the lower neighboring battery module. This pin swings between VDD_L and GND_L.
17	ALRM_L	Lower Port Alarm Output. Overvoltage, undervoltage, over/undertemperature, cell mismatch, and communication faults. The alarm signal is laddered and driven from the highest module down to the lowest. The alarm output is nominally a clocked heartbeat signal that provides a 16kHz clock when no alarm is present and is held at logic-high during an alarm. This signal swings between VDD_L and GND_L.
18	$\overline{\text{SHDN}}$	Active-Low Shutdown/Input. This pin completely shuts down the MAX11068 internal regulators and oscillators when the pin is less than +0.6V as referenced to AGND. The I^2C bus is nonresponsive when shutdown is asserted. $\overline{\text{SHDN}}$ for the first pack should be driven by the host controller through the recommended interface circuit. $\overline{\text{SHDN}}$ for laddered modules should be tied to the lower neighboring battery module through the recommended interface circuit. The shutdown pin is 60V tolerant for connection directly to the top of the battery stack.
19	AUXIN2	Auxiliary Analog Input 2. A low-voltage analog input pin with a full-scale range of AGND to VAA that can be used for monitoring an external NTC or general-purpose measurements. This channel uses the VAA voltage as the reference voltage for the ADC conversion. When used with the THRM pin and a resistor-divider, ratiometric measurements can be made.
20	THRM	External Thermistor Bias Output. This is a switched connection for supplying a bias voltage from the internal +3.4V regulator (VAA) to an external NTC device for measuring the temperature of the battery module. This pin can supply up to 2mA from the VAA regulator.
21	AUXIN1	Auxiliary Analog Input 1. A low-voltage analog input pin with a full-scale range of AGND to VAA that can be used for monitoring an external NTC or general-purpose measurements. This channel uses the VAA voltage as the reference voltage for the ADC conversion. When used with the THRM pin, ratiometric measurements can be made.
22	REF	+2.5V Voltage Reference. Bypass REF to AGND with a 1µF capacitor placed close to the device.
23	AGND	Analog Ground. Should be tied to the negative terminal of cell 1.
24	VAA	+3.4V Analog Supply Output. Connect to VDD_L and bypass with a 1.0µF capacitor to AGND.
25	C0	Cell 1 Minus Connection. Bypass to AGND with a 1.0µF capacitor.
26	C1	Cell 2 Minus Connection and Cell 1 Plus Connection
27	C2	Cell 3 Minus Connection and Cell 2 Plus Connection
28	C3	Cell 4 Minus Connection and Cell 3 Plus Connection
29	C4	Cell 5 Minus connection and Cell 4 Plus Connection

Pin Description (continued)

PIN	NAME	FUNCTION
30	C5	Cell 6 Minus Connection and Cell 5 Plus Connection
31	C6	Cell 7 Minus Connection and Cell 6 Plus Connection
32	C7	Cell 8 Minus Connection and Cell 7 Plus Connection
33	C8	Cell 9 Minus Connection and Cell 8 Plus Connection
34	C9	Cell 10 Minus Connection and Cell 9 Plus Connection
35	C10	Cell 11 Minus Connection and Cell 10 Plus Connection
36	C11	Cell 12 Minus Connection and Cell 11 Plus Connection
37	C12	Cell 12 Plus Connection. Top of battery module stack.
38	HV	High-Voltage Bias Pin. HV is biased through a diode connection to the charge pump. It is used internally to supply the high-voltage mux. Connect to DCIN through a 3.3µF capacitor.

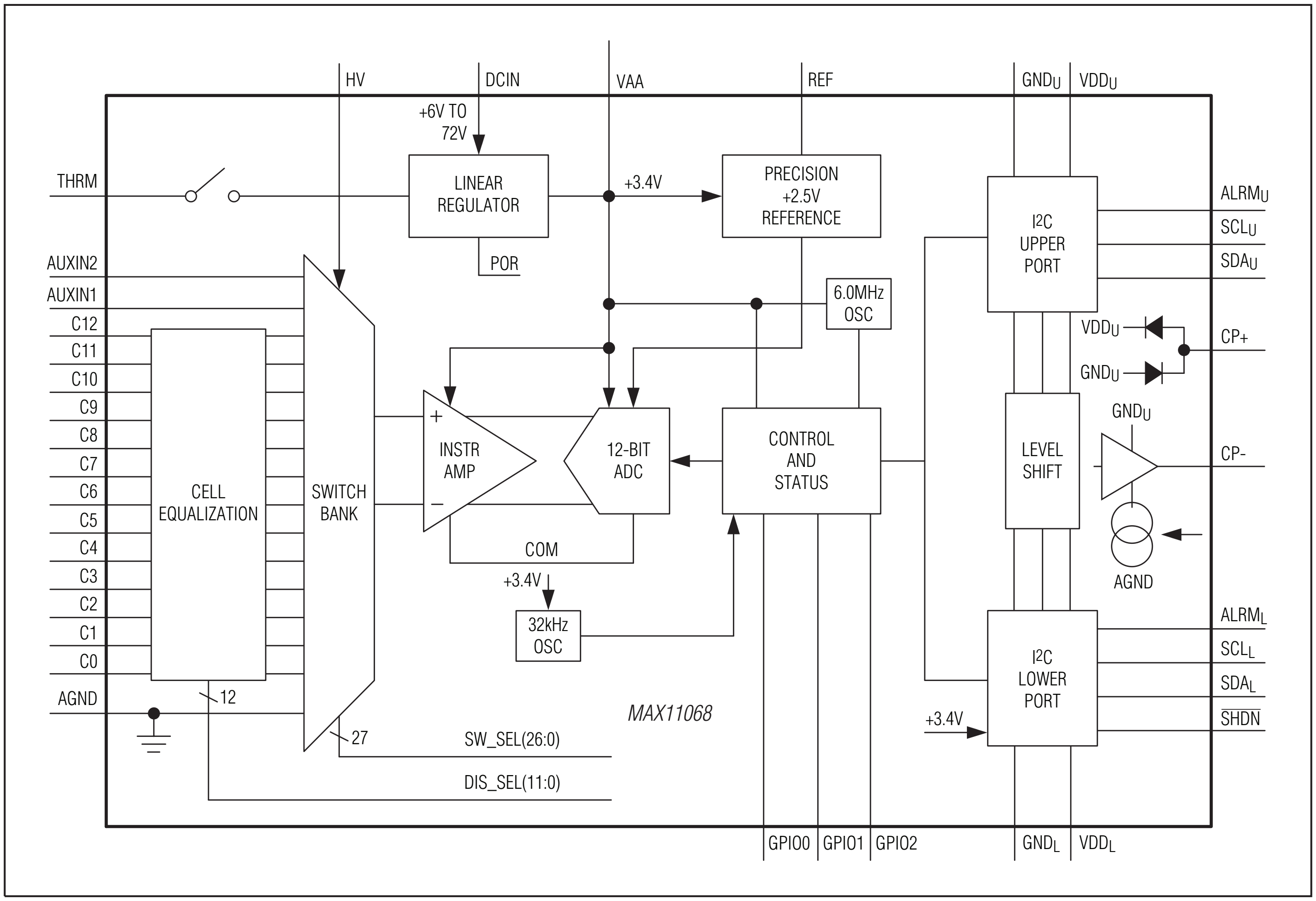


Figure 1. Functional Diagram

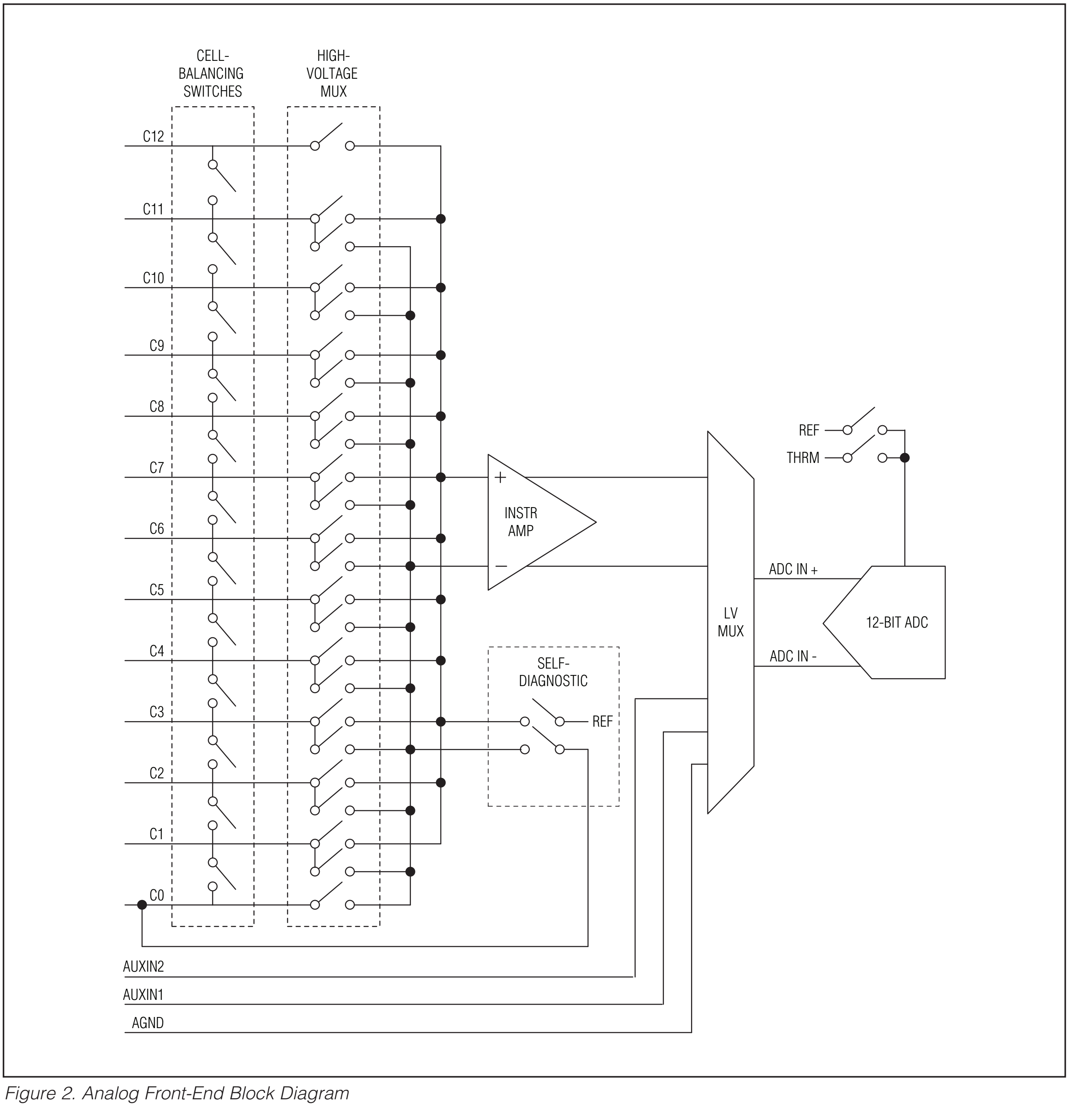
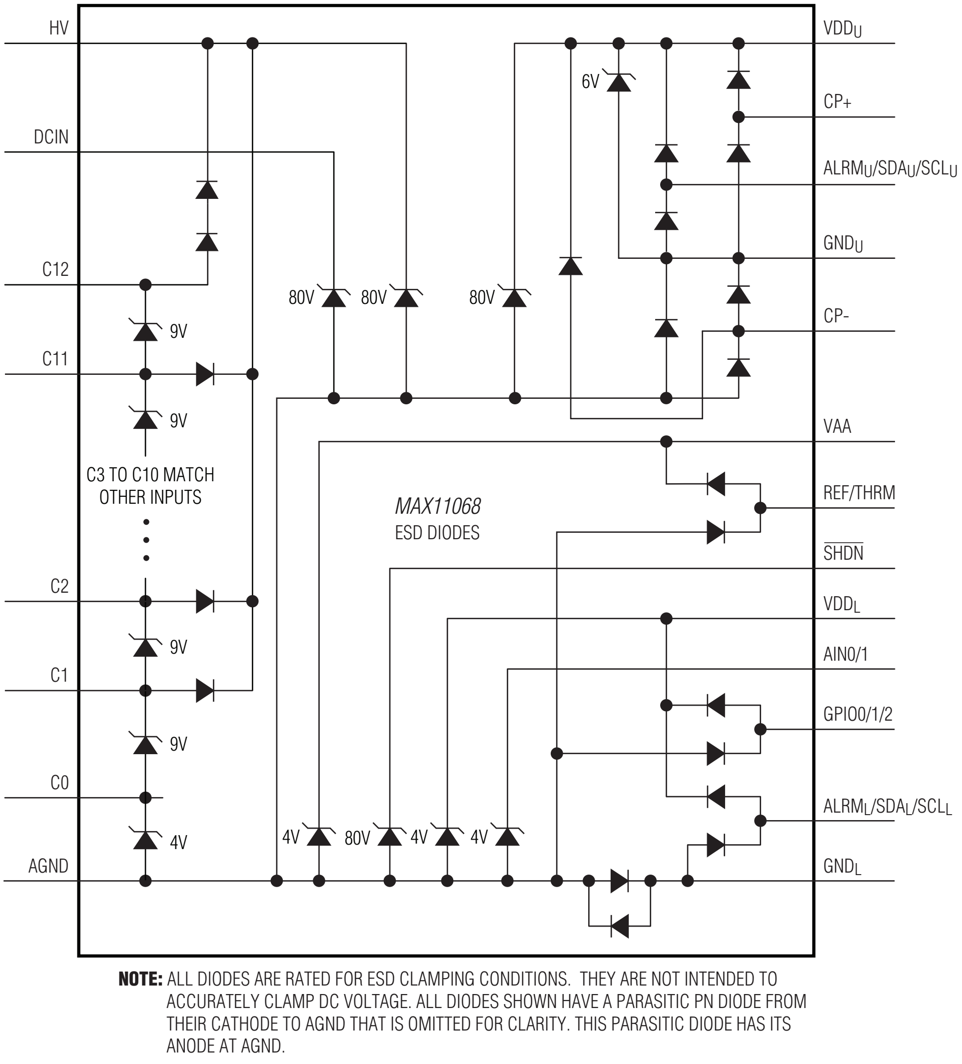


Figure 2. Analog Front-End Block Diagram



NOTE: ALL DIODES ARE RATED FOR ESD CLAMPING CONDITIONS. THEY ARE NOT INTENDED TO ACCURATELY CLAMP DC VOLTAGE. ALL DIODES SHOWN HAVE A PARASITIC PN DIODE FROM THEIR CATHODE TO AGND THAT IS OMITTED FOR CLARITY. THIS PARASITIC DIODE HAS ITS ANODE AT AGND.

Figure 3. MAX11068 ESD Diode Diagram

Typical Operating Circuit Diagrams

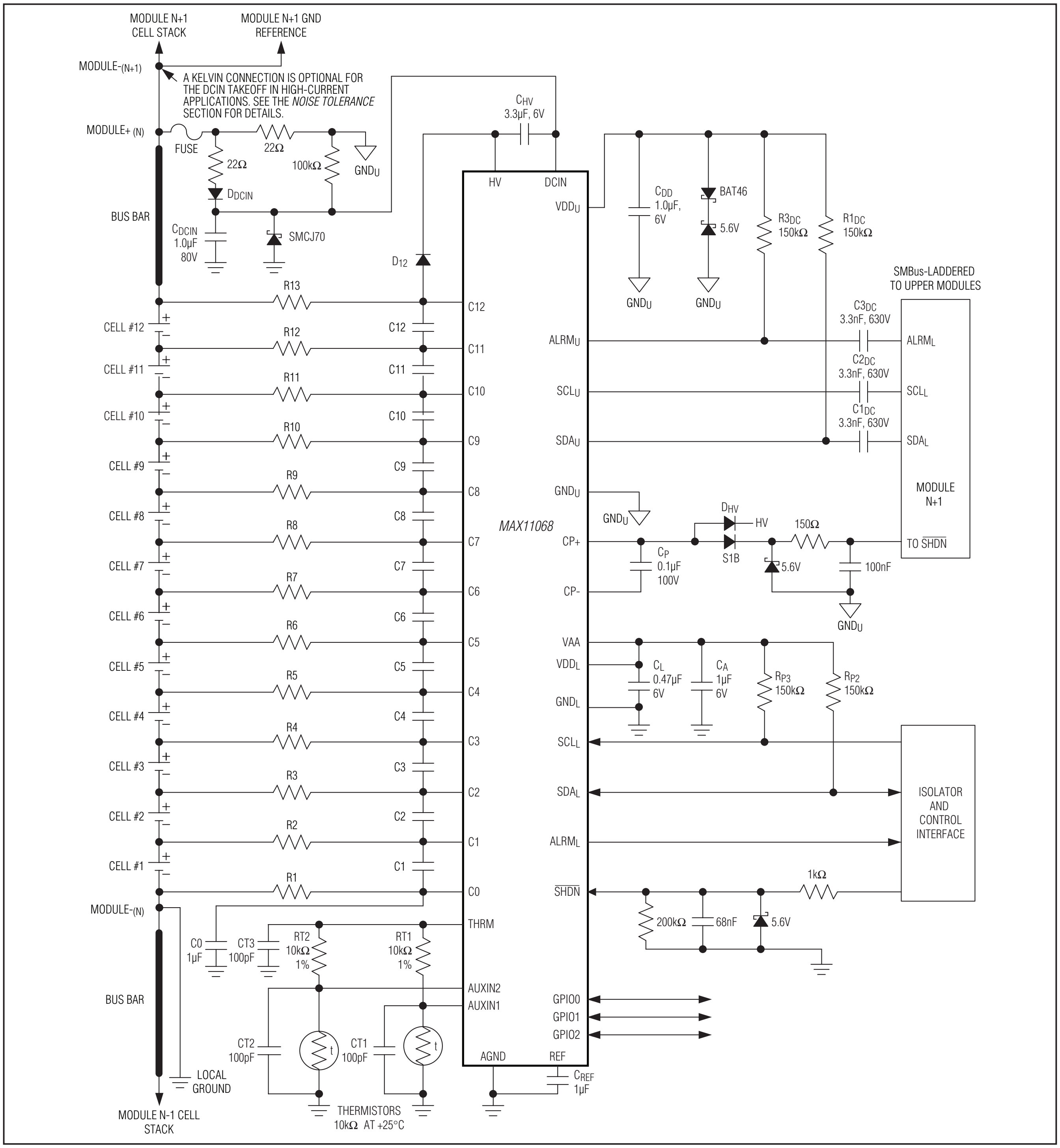


Figure 4. Operating Circuit Diagram for a 12-Cell System

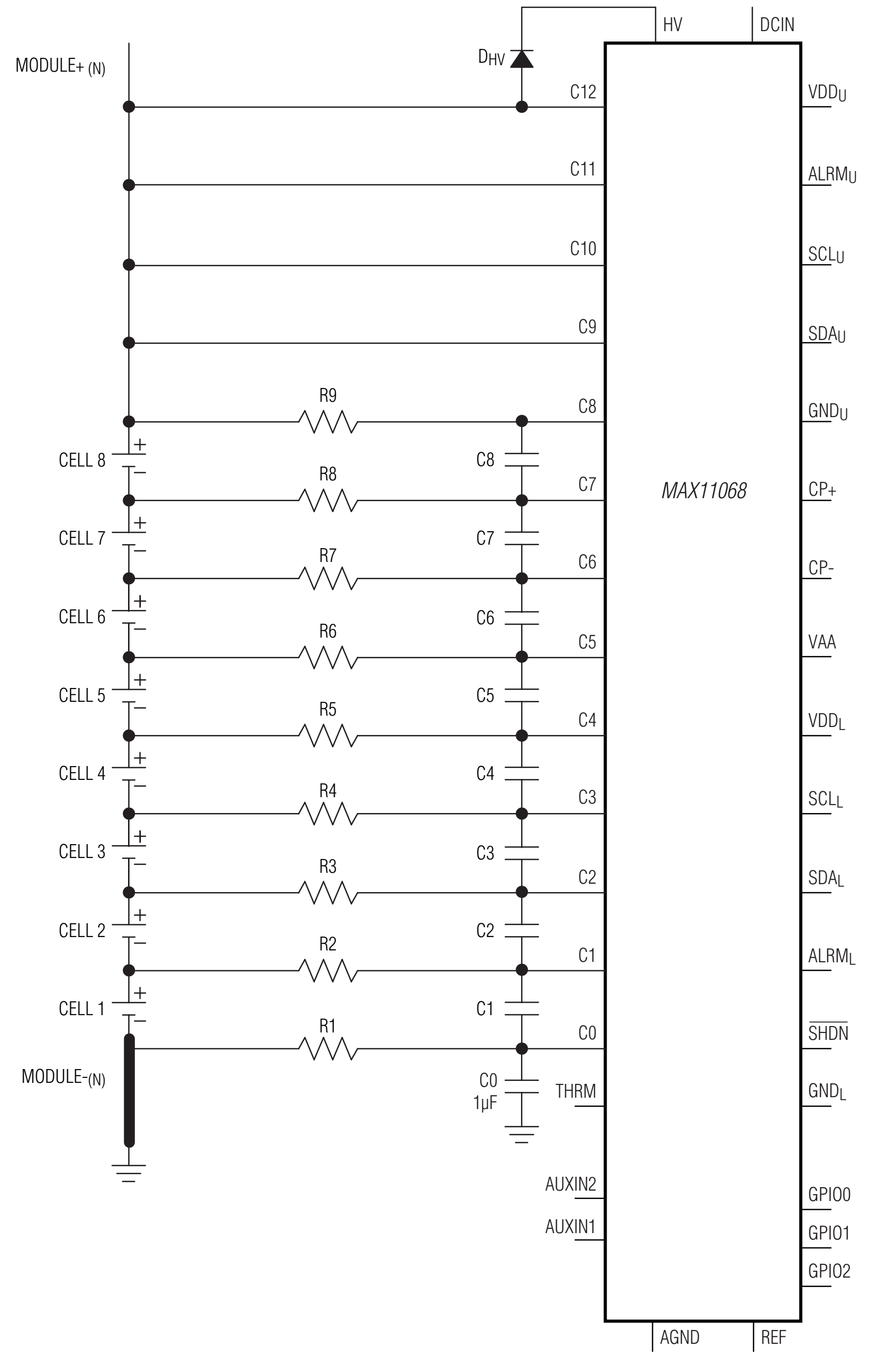


Figure 5. Simplified Operating Circuit Diagram for an 8-Cell System

Detailed Description

The MAX11068 has two auxiliary analog inputs that can be used to measure external resistance temperature detector (RTD) components. A negative temperature coefficient (NTC) RTD can be configured with the AUXIN1 or AUXIN2 analog inputs to accurately monitor module or battery-cell temperature. An internal temperature monitor on the die is used to detect thermal overload and disables the MAX11068 cell-balancing switches and linear regulator should the +145°C thermal limit be exceeded.

The MAX11068 has 12 built-in cell-balancing/discharge switches that can support up to 200mA cell discharge currents. The MAX11068 package can support up to 1.2W of power dissipation, which limits the number of balancing/discharge switches that can be enabled when using a 200mA set current to three nonconsecutive cells at no more than +75°C ambient temperature. With a 110mA cell set current, all 12 internal cell switches can be enabled at the same time. The balancing switches can also be used to detect an open circuit on any of the cell sense wire connections.

The MAX11068 contains a 25ppm/°C precision bandgap reference and an internal regulator that creates the supply for the analog front end and the interchip, level-shifted, communication bus. The regulator can operate from a 6.0V to 72V supply input. The external shutdown pin can be used to reset the MAX11068.

The MAX11068 incorporates an I^{2}C physical interface for interchip communication and control. The I^{2}C bus system is designed to allow SMBus laddering of up to 31 devices without the need for any interchip isolation. These bidirectional serial buses can withstand large differences in interchip grounds and system noise. The built-in level-shifting and predefined command protocol provide a low-cost, flexible, and reliable communication bus. Command-up forwarding relays communication along the bus from chip to chip for fast response. A 1µs delay is incurred in relaying command messages, bounding the maximum delay in response to a command to 1µs multiplied by the number of chips used in the stack minus 1. For a 31-chip stack, a maximum 30µs delay is incurred before the top module responds. This means that up to 372 cells can be measured with an elapsed measurement time from start to finish of 137µs. For a 16-chip stack, a 15µs delay is incurred. This allows measurement of up to 192 cells with an elapsed measurement time from start to finish of 122µs.

The MAX11068 incorporates an internal oscillator that generates a 6.0MHz system clock with ±3.0% accuracy.

Architectural Overview

The MAX11068 is a complete data-acquisition system on a chip designed for rugged, high-voltage measurement applications. It can measure up to 12 channels of voltages from batteries or SuperCaps with a high-accuracy, high-speed SAR ADC. Two auxiliary input channels may be configured for general-purpose measurements or as specialized temperature conversion inputs when used with RTD devices. Simple, yet fast and powerful digital command and control is implemented through unique, high-performance, level-shifted I^{2}C communication ports. This allows SMBus laddering the communication and control bus on up to 31 battery modules using the MAX11068.

Battery Pack Architectures

Battery packs are designed in a modular fashion to allow for multiple configurations, and fast and flexible assembly. This reduces cost by streamlining the build or repair process. The definition of a battery pack is a system comprising one or more battery modules connected in either a series or matrix configuration to create a high-voltage power source. Transportation or high-power battery-backup-system applications typically use many series-connected battery modules to generate voltages of up to several hundred volts. This voltage can then be inverted and transformed to levels suitable for the given load. A battery module is a series of cells configured as a subsystem that can be combined with other modules to build a high-voltage pack. For the MAX11068, the minimum cell count per module is limited by the 6.0V input requirement of the regulator, while the maximum cell count is 12. The 6.0V minimum requirement usually limits configurations to at least two lithium-ion (Li+), six NiMH, or six SuperCap cells per module. Figure 6 is the module system with redundant fault-detection application schematic.

Battery packs used in transportation applications may be composed of various battery technologies (NiMH, Li+, SuperCap, or lead acid) and typically include an electronic battery-management system (BMS), environment control, and several safety features. Figure 7 shows the electric vehicle system (EVS).

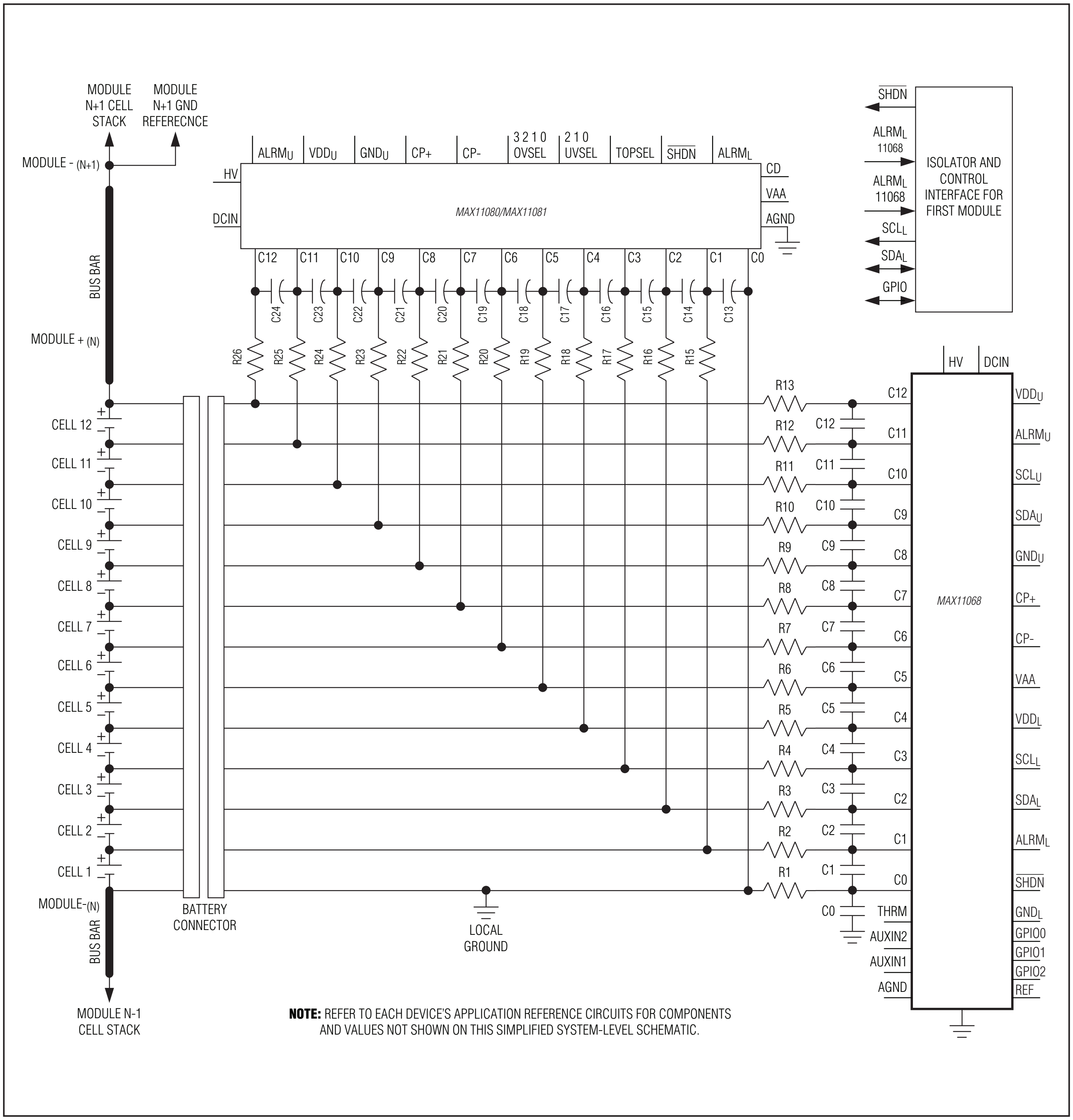
In hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), electric vehicles (EVs), or fuel-cell vehicles (FCVs), cell counts can range from 36 cells to 200 cells using Li+ batteries and up to as high as 200 to 500 cells using NiMH batteries. SuperCaps are typically used in fast-charge holding applications such as regenerative braking energy storage.

There are two fundamental battery-pack management architectures that can be realized with the MAX11068:

- Distributed module communication
- SMBus-laddered module communication

A distributed module system deploys a point-to-point connection from each battery module back to a master microcontroller in the BMS. Because the battery modules operate from the high-voltage battery stack, galvanic isolation must be used when communicating with the master microcontroller. Figure 8 shows the distributed communication battery pack.

An SMBus-laddered module system deploys a serial communication bus that travels through each battery module and is then accessed at one entry point in the system by the master microcontroller in the BMS. The SMBus ladder method reduces cost and requires at most a single galvanic isolator between the high-voltage batteries and the main power net. Galvanic isolation may not be required in certain low-voltage applications. See Figure 9.



NOTE: REFER TO EACH DEVICE'S APPLICATION REFERENCE CIRCUITS FOR COMPONENTS AND VALUES NOT SHOWN ON THIS SIMPLIFIED SYSTEM-LEVEL SCHEMATIC.

Figure 6. Battery Module System with Redundant Fault-Detection Application Schematic

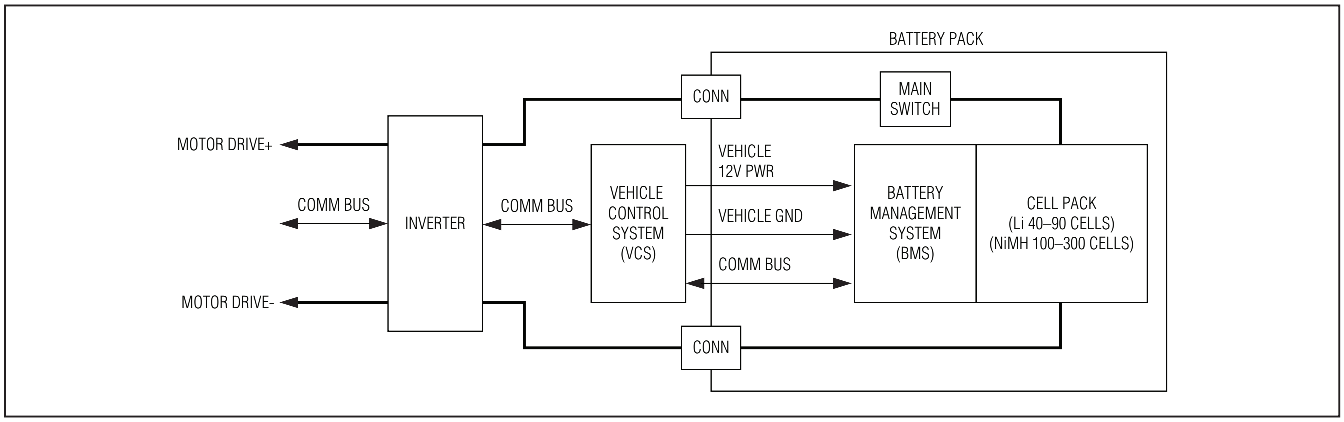


Figure 7. Electric Vehicle System

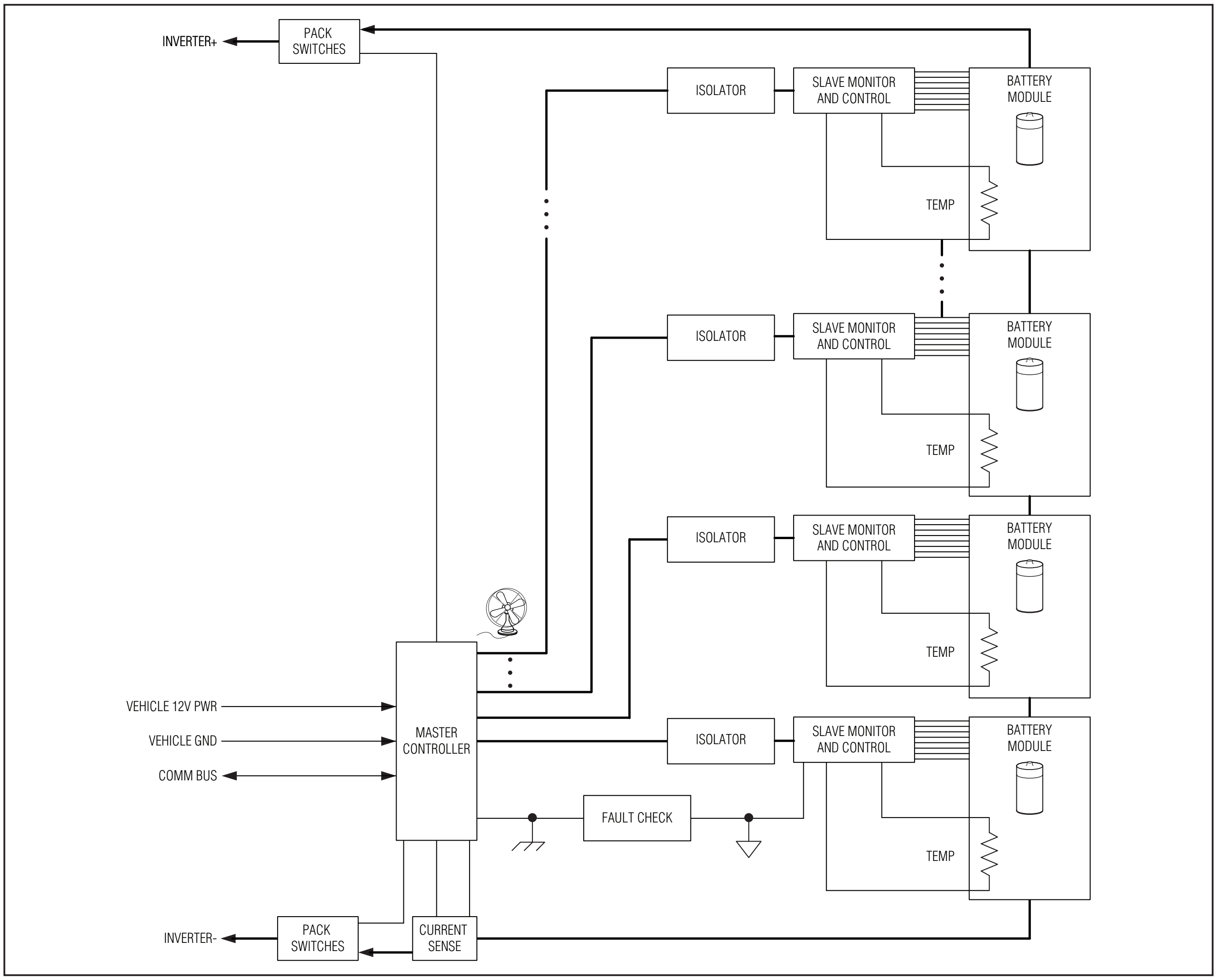


Figure 8. Distributed Communication Battery Pack

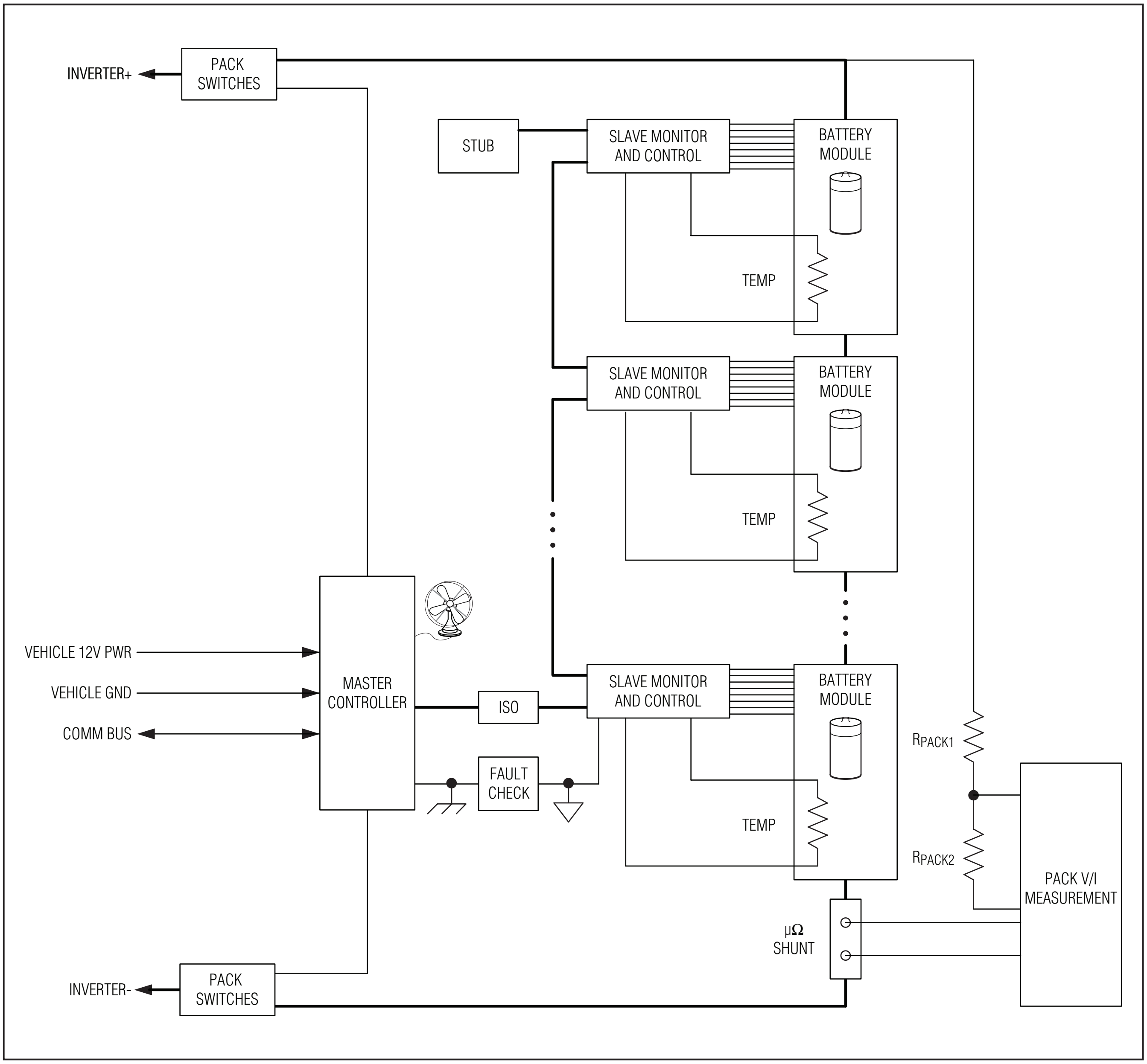


Figure 9. SMBus-Laddered Battery Module Communication

Battery-Management System (BMS)

The BMS in an electric vehicle monitors cell voltage, pack current, and temperature. The BMS is composed of two components. The first is the master controller of the system that handles all communication with the VCS. It also handles state of charge, state of health, and fault-management features of the battery pack. The second component is the data-monitoring function, which gathers information on the conditions of the battery cells, takes voltage/current/temperature measurements, and signals safety faults.

The slave monitor controller (SLC) is directly connected to the series stack battery cells. The SLC measures cell voltages and module temperature, as well as controls the cell-charge equalization feature that keeps all cells balanced to equal states of charge. The SLCs are also designed to report alarm conditions such as cell overvoltage or undervoltage, sense wire-open circuits, and in the case of Li+ battery chemistries, overtemperature situations. The SLCs are managed by the master controller. The master controller orchestrates all data acquisition and cell-balancing tasks in the slaves. The master also measures the pack current coincident to voltage measurements so that state of health of the battery pack can be determined. Measurement of the current through the pack is made across a low-value shunt resistor or hall sensor.

Cell Inputs C0–C12

The MAX11068 contains 13 analog inputs that are used for the differential measurement of as many as 12 battery cells. Each differential cell input can withstand up to 9.0V and can be included in the measurement cycle through the cell-channel scan-enable bits of the CELLEN register (address 0x09). Cell inputs are measured differentially and level shifted down to the internal ADC by a high-voltage mux and ADC preamp. The common-mode range of the cell inputs from C2 to C12 is 0.5V to V_{HV} - 2.9V. Common-mode range for C1 is limited to 7.0V and for C0 it is limited to voltages within 50mV of AGND for proper measurements. The absolute maximum differential input between two inputs must always be observed, which is 9.0V.

The application circuit shows RC filtering for each cell input. The values of the resistors are chosen in large part depending on the cell-balancing functionality that is desired. The capacitor value chosen complements the resistor values to provide lowpass filtering of the ADC measurement. Capacitor values should be in the 100nF to 1µF range.

The first cell position between C1 and C0 must be populated for all applications with a voltage of at least 500mV. This ensures accurate measurements for all other cell positions as defined by the ADC specifications. When implementing a module configuration with fewer than 12 cells, the first cell position should always be used, and then other cell positions may be used in any configuration. Any unused cell positions should have their inputs shorted together. Random connection of cells or the high-voltage supplies during module configuration does not cause adverse effects.

Measurement Scanning

When a cell is enabled for acquisition by setting the associated scan-enable bits in the CELLEN register (address 0x09), the appropriate cell differential input is scheduled for conversion. The auxiliary input channels along with the self-diagnostic channel may be similarly enabled using their enable bits in the ADCCFG register (address 0x08).

Conversion begins with the setting of the SCAN bit in the SCANCTRL register. The setting of the SCAN bit may be accomplished using either the WRITEALL command or the WRITEDEVICE command, depending on whether all devices are expected to perform the conversion. If the ADC is still busy from a previous acquisition scan, the scan command is ignored. Each module in a system begins the measurement scan cycle as soon as it receives the scan signal. The measurement order of the inputs during a cycle is as follows:

1) All enabled cell inputs phase 1, descending order (12–1)
2) All enabled cell inputs phase 2, descending order (12–1)
3) Self-diagnostic measurement phase 1, if enabled
4) Self-diagnostic measurement phase 2, if enabled
5) All enabled auxiliary inputs phase 1, ascending order (AUXIN1, AUXIN2)

The complete acquisition of the cell voltages takes place in two phases, which is shown in Figure 10. The first phase is the raw cell-voltage acquisition. In this stage, the ADC scans through all the enabled cell input channels, starting with the highest cell.

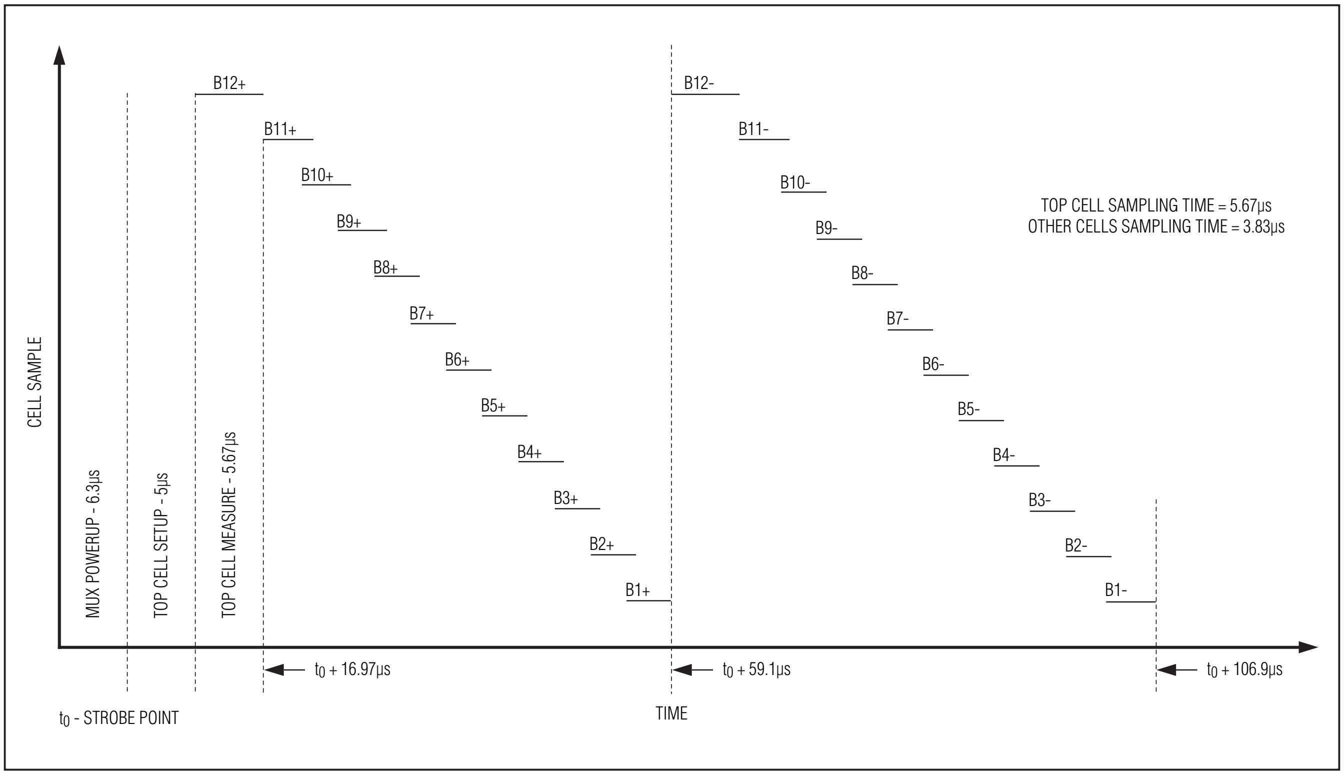


Figure 10. Cell-Scanning Timing

The second stage in the channel-scanning process is the correction phase, where the front-end amplifier chops out any offset and reference-induced errors. This provides a high-accuracy cell voltage result. In this stage, the channels are converted in the same highest to lowest order as the initial measurement. The module-to-module sampling points differ by the communication forwarding delay from the I^{2}C command. With the measurements from the two scan phases complete, the ADC data is then offset corrected, averaged, and updated in the cell data registers.

After the cell-measurement cycle is complete, the self-diagnostic channel is acquired when enabled. It is a two-phase measurement as described for the cell-voltage inputs, with each phase measured one immediately after the other. Finally, the enabled auxiliary inputs are measured. They are measured in a single conversion, with results reported in the AIN1 and AIN2 registers. The auxiliary channels have a configurable option to increase settling time that is set in the lower byte of the ACQCFG register (address 0x0C). The configured extra settling time is implemented just before the conversion for each AUXIN channel that is enabled for measurement. So, when both auxiliary channels are measured, the extra settling time occurs twice. Extra settling time is not needed by the MAX11068 ADC; it is only for the benefit of the external application circuit.

Calculating Measurement Time

The first requirement for performing a measurement conversion is setting the SCAN bit. This can be done by using the WRITEALL or WRITEDEVICE commands. The write commands require 5 full bytes of data, plus 5 acknowledge bits and the start and stop bits. This totals 47 bits of data sent by the host, which would require 235µs at a 200kHz I^{2}C clock rate.

The timing of the cell measurements is shown in Figure 10. At the start of the measurement cycle, there is a measurement setup time prior to the measurement of the highest cell totaling 11.3µs. The highest cell measured requires a sampling time of 5.67µs, while the rest of the inputs are sampled at 3.83µs per channel. When all 12 channels are enabled, the 12-cell voltages for one phase are acquired in 47.8µs, not including the measurement setup time. The total acquisition time for 12 cells is 106.9µs

For every module in the battery pack, a 1µs communication delay is incurred while the scan command is forwarded up the SMBus ladder. Therefore, the difference in the scan completion time from the first module to the last module in a chain is no more than 1µs x (no. of modules in the chain - 1) as shown in Figure 11.

Taking the module conversion time and combining it with the communication delay, the overall sampling window of the system can be calculated:

$$\text{Sampling window} = 11.3\mu s + (5.67\mu s + (\text{no. of cells enabled per module} - 1) \times 3.83\mu s) \times 2 \text{ phases} + ((\text{no. of modules per pack} - 1) \times 1\mu s \text{ per module})$$

So, for a battery pack that uses 12 cells per module and a system with four modules (total cell count = 48), the sampling window would be:

$$\text{Sampling Window} = 11.3 + (5.67 + 11 \times 3.83\mu s) \times 2 + ((4 \text{ Modules} - 1) \times 1\mu s)$$

$$\text{Sampling Window} = (106.9\mu s) + (3\mu s) = 109.9\mu s$$

Thus, from the time the first device receives the scan command until the last device completes its measurement conversion, 109.9µs elapse.

The final aspect of the measurement conversion is the retrieval of data from all devices. A READALL command is the only way to transfer data from each device. Since up to 12 cells are measured, the READALL command must be performed for each cell whose data must be transferred. For each READALL command, there are 5 total bytes of overhead. These include the broadcast address byte, the command code byte (register address to be read), the I^2C address byte, the data check byte, and the packet-error check (PEC) byte. Each of these bytes has an acknowledge bit associated with it. The register data from each device consists of 2 more bytes plus 2 acknowledge bits. Finally, the overall data stream consists of 3 more bits, start, stop, and repeated start. Thus, for a read of a single register from all modules, the total bit count is:

$$\text{READALL bit count} = 3 + 5 \times 8 + 5 + \text{no. of modules} \times (2 \times 8 + 2) = 120$$

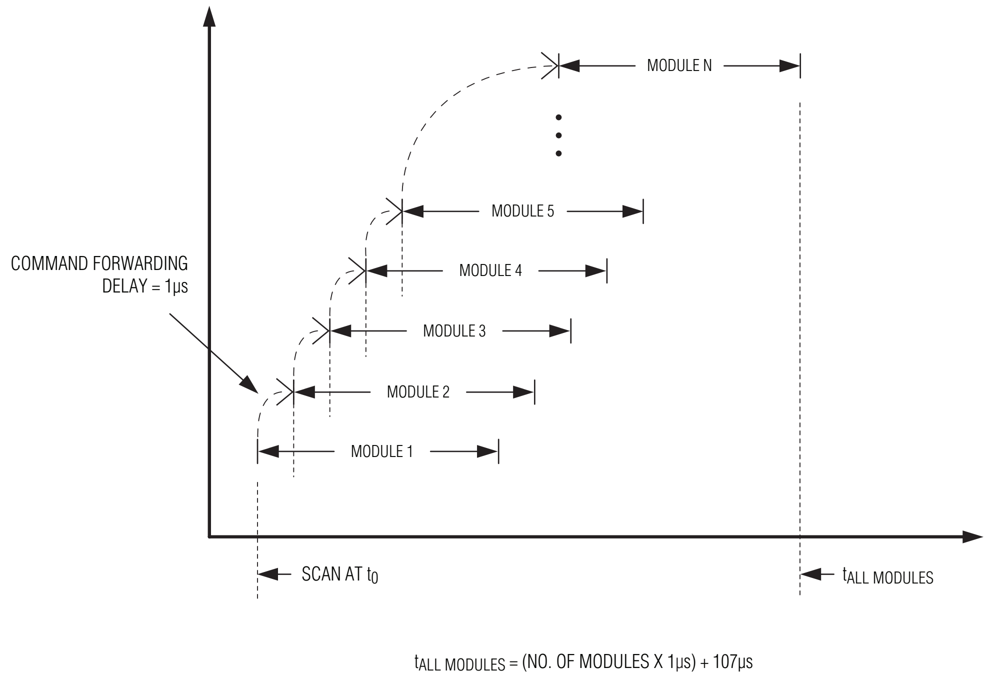


Figure 11. Measurement Scan Timing for a Multimodule System

For the example with four modules and 12 cells per module, the total READALL bit count would be 120 bits per cell or 1440 bits for all 12 cells. At a 200kHz I^2C clock rate, the total time for this command would be 7.2ms.

The overall time from the host issuing the scan command to the last data being received by the host includes the write time for the scan command, the measurement conversion time, and the time for the READALL command. For this 12-cell, four-module, 200kHz I^2C example the total is:

$$235\mu s + 106.9\mu s + 7200\mu s = 7.542ms$$

Effectively, the number of complete 12-cell measurements that can be acquired and transferred back to the host is no more than 132 per second. If the data from every measurement is not transferred back to the host, then significantly more measurements may be taken per second. Enabling the auxiliary or self-diagnostic channels would decrease the effective sampling rate.

Cell Overvoltage and Undervoltage

The MAX11068 incorporates cell-voltage monitoring with alert and alarm capability for diagnosing system status. After each ADC voltage conversion, cell-voltage data is stored in the cell-data registers. Only data registers for cell positions that were enabled for the previous measurement scan are updated. Cells that were not in the measurement scan retain their previous value. The data is also analyzed for the minimum, maximum, and total cell-voltage values, as well as for overvoltage and undervoltage conditions.

The maximum and minimum cell voltage readings are stored in the upper 12 bits of the MAXCELL and MINCELL registers (addresses 0x11 and 0x12). Also stored in the lowest 4 bits of those registers is the cell number corresponding to the data reading. Where multiple cells had the same minimum or maximum reading, the highest cell position having that reading is reported. The sum total value of cell data whose measurements were enabled in the last scan is stored in the TOTAL register (address 0x10) as a 16-bit value. Where a conversion is initiated with no enabled cell inputs, the MINCELL, MAXCELL, and TOTAL registers retain their current value.

Cell-voltage data is also compared against programmable cell overvoltage and undervoltage thresholds. These thresholds are configured through the overvoltage and undervoltage set and clear threshold registers (addresses 0x18 to 0x1B). Alerts, when enabled, are triggered as cell voltage data passes through the set threshold level. Conversely, alerts are cleared when the cell voltage data passes through the clear threshold level. If the voltage data is equal to a relevant cell threshold limit, no action occurs. Therefore, if the set threshold level is placed at full scale for the overvoltage alert or at zero scale for the undervoltage alert, the alert cannot trigger and is effectively disabled. The two thresholds, set and clear, for each condition allow for digital hysteresis to be configured in the alarm trigger. Figure 12 is a diagram of the programmable overvoltage and undervoltage thresholds.

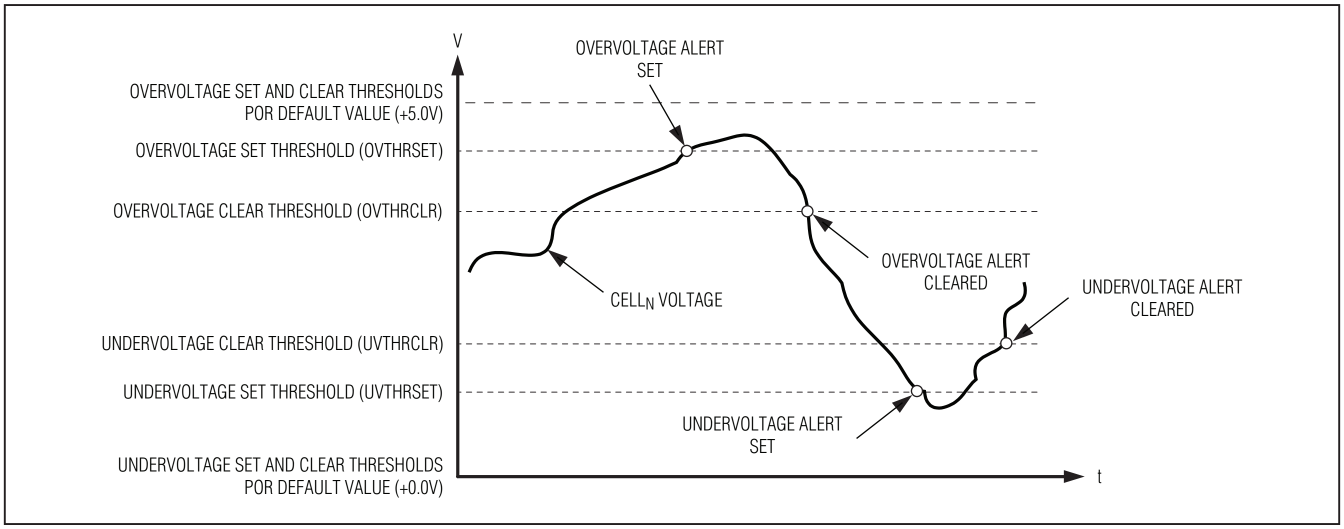


Figure 12. Programmable Overvoltage and Undervoltage Thresholds Diagram

Alerts may be enabled on a per-cell basis. Local enable bits OVEN and UVEN are found in each cell's data register (addresses 0x20 to 0x2B). These bits are mapped to the equivalent bits of the OVALRTEN and UVALRTEN registers (address 0x06 and 0x07). If these bits are enabled for a given cell, the cell reports its overvoltage or undervoltage alert status to the appropriate alert status register (addresses 0x04 and 0x05). The alert status is updated whenever new cell measurement data is available. If either of these two alerts are active for a cell, that cell's corresponding ALRTCELL register bit (address 0x03) is also set. All voltage alert status register bits are zero when no alert is present and cannot be manually cleared. To clear an active voltage alert, the alert condition must be removed and a new measurement must be taken or the alert must be disabled.

The global ALRTOV and ALRTUV bits in the STATUS register (address 0x02) are set when any cell has an active alert as indicated in the ALRTOVCELL or ALRTUVCELL registers. All alerts are automatically cleared following the next conversion cycle when the alert conditions no longer exist. Using this tiered approach to alert reporting, the system host may quickly establish whether any voltage alerts are active and, if necessary, determine exactly which cells and conditions are affected.

The mismatch alert is another status condition flag that can be enabled to signal when the minimum and maximum cell voltages are mismatched by more than a programmed amount. The alert is enabled by setting the ALRMMMTCHEN bit of the ADCCFG register. The MSMTCH register (address 0x1C) sets the 12-bit threshold for the mismatch alert, ALRTMSMTCH. Whenever MAXCELL - MINCELL > MSMTCH, the ALRTMSMTCH bit in the STATUS register is set. The alert bit is cleared when new conversion data does not violate the threshold condition.

Cell Balancing

The basic cell-balancing circuit for the MAX11068 incorporates the use of internal 6Ω switches and external resistors to set an equalization discharge current that is dependent on cell voltage. Figure 13 shows the basic circuit used with the internal cell-balancing switches.

The following limitations must be taken into account when using the basic circuit:

- Maximum power dissipation allowed in the package
- Measurement during cell balancing
- Current variation due to enabled adjacent cell switches
- Protection from open-circuit faults in the battery stack destroying the MAX11068

Managing Power

The MAX11068 contains 12 independently controlled switches that have a typical on-resistance (R_{SW}) of 6Ω with ±50% variation due to process and temperature. The package used for the MAX11068 is a 38-pin TSSOP package with a maximum power limit (P_{MAX}) of 1.2698W and a junction-to-ambient thermal resistance of +63°C/W for a multilayer board. These parameters are the fundamental limits for the package-power dissipation and require careful consideration when using the internal cell-balancing switches since the switches are the dominant power consumers in the device. For operating margin, it is recommended targeting a maximum power level that is 70% of the absolute maximum rating. The maximum die junction temperature that is allowed is +150°C. A built-in overtemperature protection circuit protects the die at a junction temperature of +145°C, however. When the overtemperature limit is reached, the internal cell-balancing switches are disabled. The associated cell-balancing switch enable bits in the Balancing Switch Control register (BALCFG at address 0x0B) are not directly affected, but the resulting power down of the linear regulator may cause a power-on reset (POR) condition, which would reset the BALCFG register and deassert all switch-enable bits. The maximum number of cell-balancing switches that can be enabled at any one time is calculated as shown below:

$$\text{Maximum number of enabled switches} = (0.7 \times P_{MAX}) / ((I_{BALANCE})^2 \times R_{SW})$$

where:

$I_{BALANCE} = V_{CELL}/((2 \times R_{EQ}) + R_{SW})$

$P_{MAX} = 1.2698\text{W}$

$R_{SW} = 6\Omega$, typical

Table 1 lists example results obtained based on the formula above.

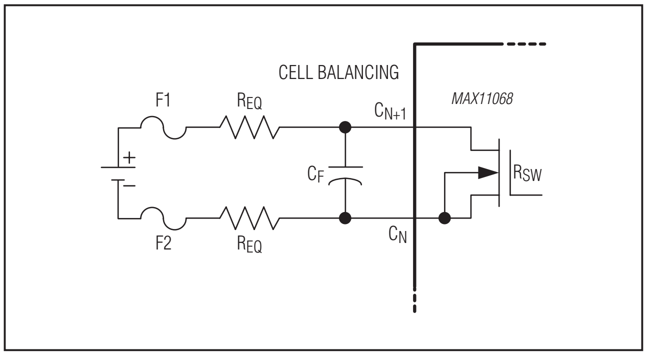


Figure 13. Cell-Balancing Switch Network

Table 1. Cell-Balancing Circuit Parameter Variation

CELL NAME	MIN	TYP	MAX	UNITS	HIGH-SIDE ACCURACY (%)	LOW-SIDE ACCURACY (%)
R_{EQ}	5.1	5.2	5.3	Ω	1	-1
C_F	9	10	11	µF	10	-10
R_{SW}	3	6	9	Ω	50	-50
V_{CELL}	4.1	4.1	4.1	V	NA	NA
$I_{BALANCE}$	308	250	210	mA	16	-23
$FILTER_{3dB}$	3435	3061	2755	Hz	—	—
t_{SETTLE} at C_{N+1} (Note 1)	0.6	0.8	1.1	ms	—	—
Max No. of Switches On (Note 2)	3	2	2	Switches	—	—

Note 1: t_{SETTLE} is five time constants after the cell-balancing switch is disabled.

Note 2: Nonadjacent cell switches.

Based on the calculations, up to two nonadjacent internal cell-balancing enabled switches are supported for a discharge current of 250mA per cell. At least a 0.5W rated R_{EQ} is required to handle the 250mA nominal current and its worst-case range of 210mA to 308mA.

Measurements During Cell Balancing

When using the internal cell-balancing switches, the measured voltage on the C_N to C_{N+1} input is reduced by the external R_{EQ} resistors. For accurate cell-voltage measurements, disabling the internal cell-balancing switch is required. These switches are not disabled automatically during a conversion. After the internal cell-balancing switch is disabled, allow the input voltage to settle for a time period (t_{SETTLE}), which is determined by external components C_F and R_{EQ}, before performing a cell-measurement sequence:

$$t_{SETTLE} = 10 \times R_{EQ} \times C_F$$

Current Variation Due to Enabled Adjacent Cell Switches

If adjacent internal cell-balancing switches are enabled, the discharge current would be much higher than the desired value. Figure 14 shows the adjacent enabled balancing switches and the resulting discharge current (I_{DIS}):

$$I_{DIS} = (V_{CELL5} + V_{CELL4})/(2 \times R_{EQ} + (2 \times R_{SW}))$$

From the I_{DIS} equation, it is apparent that the discharge current grows with the number of adjacent active internal cell-balancing switches. This is because the cell voltages across the active switches and the R_{SW} values are growing proportionally, but R_{EQ} remains fixed no matter how many adjacent switches are active. Consequently, the numerator of the discharge current equation grows faster than the denominator with increasing active switch count and discharge current increases. Unless this is accounted for by the host controller, the package power-dissipation limit could be reached unexpectedly and damage to the device could occur. To avoid this possibility, it is recommended to use an odd or even switch-enable control scheme for the internal cell-balancing switches.

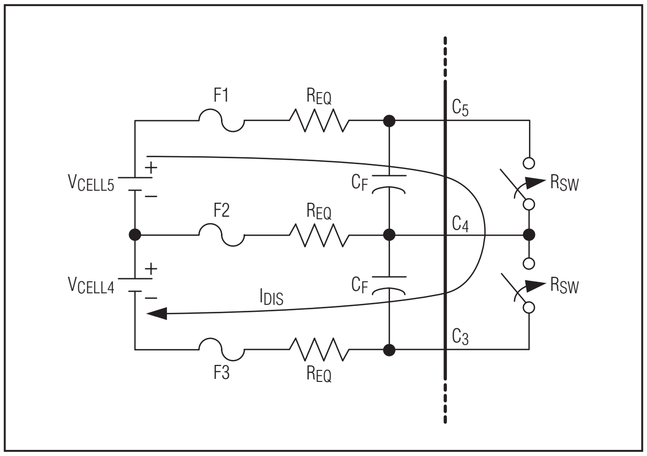


Figure 14. Discharge Current Path for Adjacent Enabled Balancing Switches

Protection from Open-Cell Faults

There are two methods of protecting the MAX11068 from damage due to an open circuit occurring in a series battery stack:

- An external fuse placed in series with the internal or external cell-balancing circuit protects against high-voltage damage. If an external MOSFET is used, as in the circuits described below, the high-value resistors protect the MAX11068 inputs from damage during an open-cell condition.
- Detection of any cell dropping below ground or violating the undervoltage condition indicates an open-cell condition and that the electric motor is supplying voltage to the battery pack. To prevent damage, the switches connecting the battery stack to the load should be opened immediately after the undervoltage flag asserts.

External Cell-Balancing Circuit

The MAX11068 allows external cell balancing to be implemented by using the internal switch to control the bias network of an external transistor. When the internal switch is closed, the external resistors R_{BIAS1} and R_{BIAS2} form the bias network used to turn on the external bipolar or MOSFET transistor. The discharge current of the battery is set with resistor R_{EQ}. The following sections describe different external cell-balancing circuits in more detail. Figure 15 is a simplified external cell-balancing circuit.

External Cell Balancing with a Bipolar Transistor

When using an external bipolar transistor, it is recommended to select one with current gain (h_{FE}) greater than 100 and a V_{CE} voltage that is rated to the overall pack voltage to avoid damage should an open circuit occur in the cell stack. If a bipolar transistor with a lower voltage rating is chosen, then series fuses are recommended to protect the circuit. Typical component values for a 500mA cell discharge current are (see Figure 16):

$R_{BIAS} = 80\Omega$

$R_{EQ} = 8\Omega$

Bipolar transistor = MJD50 (for high-voltage tolerance) or MMBTA05 (for low cost and low voltage)

External Cell Balancing with a MOSFET

When using an external MOSFET, it is recommended to select one with low V_{GS} (typically around 1.2V) and a V_{DS} voltage that is rated to the overall pack voltage to avoid damage should an open circuit occur in the cell stack. If a MOSFET with lower voltage rating is chosen, series fuses are recommended to protect the circuit. See Figure 17. Typical component values for a 500mA cell discharge current are:

$R_{BIAS1} = 10k\Omega$

$R_{GATE} = 470\Omega$

$R_{EQ} = 8\Omega$

MOSFET = NTK3134N (for low cost, low voltage)

External cell balancing with a MOSFET switch results in little to no cell-to-cell interaction. The R_{BIAS} resistor value combined with the input bias current requirements does add a small measurement error of less than 1mV worst case for a 10kΩ R_{BIAS} value.

The recommended NTK3134N FETs have built-in gate-protection diodes. During hot-plug conditions, inrush current flows through R_{BIAS} and internal ESD diodes to charge the HV to DCIN capacitor. This current creates a negative V_{GS} voltage that can turn on the gate-protection diodes and possibly damage the transistor devices. A series resistor of no less than 470Ω should be placed in series with the transistor gate to make the circuit robust under cell hot-plug conditions. For other transistors, the negative V_{GS} condition must be controlled so that it is tolerated by the devices.

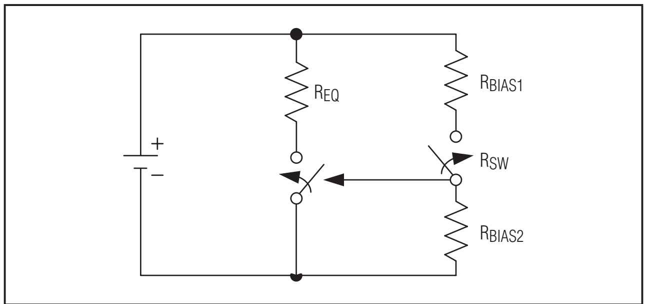


Figure 15. Simplified External Cell-Balancing Circuit

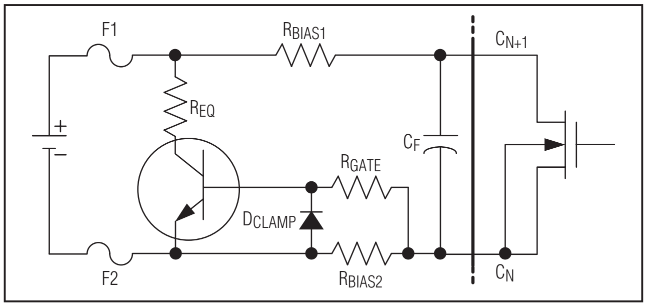


Figure 16. External Cell-Balancing Circuit with a Bipolar Transistor

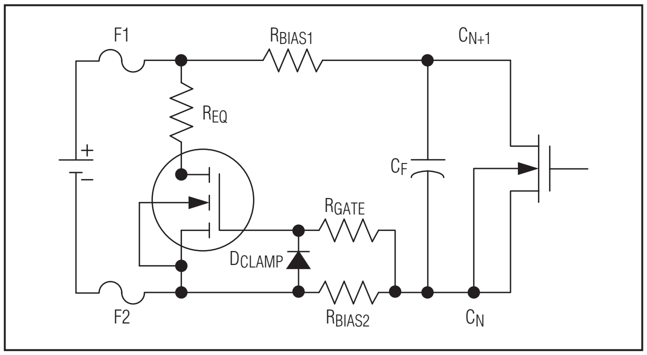


Figure 17. External Cell-Balancing Circuit with a MOSFET Transistor

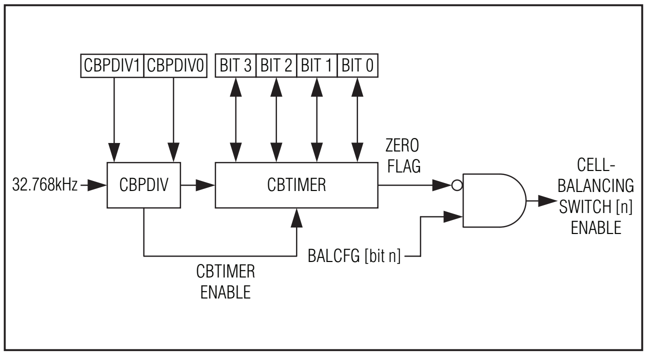


Figure 18. Cell-Balancing Timer Block Diagram

Cell-Balancing Watchdog Timeout

The MAX11068 implements a watchdog-style timeout feature for the cell-balancing switch enables. A countdown timer is clocked at a rate specified by a predivider. The full range of possible timeout values is 0 to 240s. In the event of unexepected communication loss, the cell-balancing switches are safely disabled after the timer reaches zero. The timeout disables the cell switches with a signal separate from those of the BALCFG register. Thus, the BALCFG register value is not affected by the cell-balancing timeout condition. Figure 18 shows the timeout circuit block diagram.

The cell-balancing timeout feature consists of a 4-bit countdown timer and a predivider with 2 control bits for range selection. Both the timer and predivider are programmed through the MSB of the ACQCFG register (address 0x0C). The predivider sets the effective LSB time period of the timer. The user-selectable choices are shown in Table 2.

The cell-balancing timer counts down at the rate specified by the predivider, CBPDIV[1:0]. The timer starts when the CBPDIV control bits are written to one of the three enabled settings. The CBTIMER[3:0] bits are readable and writeable and return the value of the timer as sampled during the acknowledge bit time of the register address bit of the READALL command. The host application should periodically rewrite the ACQCFF register value to ensure that this value does not unintentionally go to zero. The timeout can be set to any value within the timer range specified by the CBPDIV setting by choosing the appropriate value to write to the CBTIMER byte. If the value of the CBTIMER does reach zero, the cell-balancing switches are disabled until the timer is either disabled or is refreshed by writing a nonzero value. If the timer is enabled by writing the CBPDIV bits while the CBTIMER value is at 00h, the cell-balancing switches are not disabled. The first transition of CBTIMER to the 00h value when the timer is enabled disables the balancing switches.

Table 2. Cell-Balancing Predivider Settings

CBPDIV[1:0] SETTING	TIMER LSB PERIOD (s)	TIMER RANGE (MIN TO MAX) (s)
00	Timer disabled	Timer disabled
01	1	1 to 15
10	4	4 to 60
11	16	16 to 240

Internal Regulator and Charge Pump

The MAX11068 incorporates a linear regulator for generating the internal supply from DCIN. The regulator can accept a supply voltage on the DCIN pin from 6.0V to +70V, which it regulates to 3.3V to run the voltage-measurement system, control logic, and low-side communication interface. The regulator is designed to supply up to 10mA of current. When the $\overline{\text{SHDN}}$ pin and die temperature protection are not active and a sufficient voltage is applied to DCIN, the output of the regulator becomes active. The regulator is paired with a power-on POR circuit that senses its output voltage and holds the MAX11068 in a reset state until the internal supply has reached a sustainable threshold of +3.0V (±5%). The internal comparator has built-in hysteresis that can handle noise on the supply line, as well as slow supply ramps of 1V/s. Since secondary metal batteries are never fully discharged to 0V, the MAX11068 is designed for a hot-swap insertion of the battery cells. Once the POR threshold is reached, the internal RESET signal disables. A status bit, RSTSTAT in the STATUS register (address 0x02), is set when power is restored to the digital logic following a reset event to denote that a reset has occurred. It should be checked and cleared by the system controller so that any future reset condition can be resolved. Figure 19 is the internal low-dropout regulator block diagram.

The MAX11068 power-up sequence is shown in Figure 20. Starting with no DC power applied, the device waits for a power source and then waits until the $\overline{\text{SHDN}}$ signal is deactivated. If the internal die temperature limit is not exceeded, the regulator is enabled. The regulator begins to regulate the DCIN input voltage down to 3.3V. After VAA has reached the rising POR threshold, the internal POR signal is deasserted and the various sections of the device begin to initialize, starting with the 32kHz oscillator. An additional 280μs after the oscillator becomes active, the digital logic becomes active and the charge pump begins operating. The charge pump reaches full regulation in approximately 3ms depending on the external circuit components used, at which time the MAX11068 is ready for operation. When the charge pump achieves regulation of 3.4V between VDD$_U$ and GND$_U$, it switches to a standby mode until the voltage drops by 20mV to minimize operation during light loading. The specification accuracies and full operation of the MAX11068 are not guaranteed until a minimum of 6.0V is applied to the DCIN pin. The regulator has built-in short-circuit protection in case of a fault condition. Figure 21 shows asynchronous regulator disable events and Figure 22 shows the POR event sequence.

The regulator incorporates a thermal-shutdown feature. If the MAX11068 die temperature rises above +145°C, the device shuts down by disabling the internal regulator. The cell-balancing switches are also independently disabled in case an external power source maintains power to the digital logic through VDD$_L$. The settings of the BALCFG register are not directly altered by the overtemperature condition, but unless VDD$_L$ is supplied from a source other than VAA, the POR event caused by the regulator shutting down resets all registers to their default values. After a thermal shutdown event, the die temperature must cool 15°C below the shutdown temperature before the device reenables the regulator.

Figure 23 shows a more detailed view of the charge pump and the supply and ground references for the regulator and charge pump. The charge pump is driven by a 4mA current source, I$_{PUMP}$.

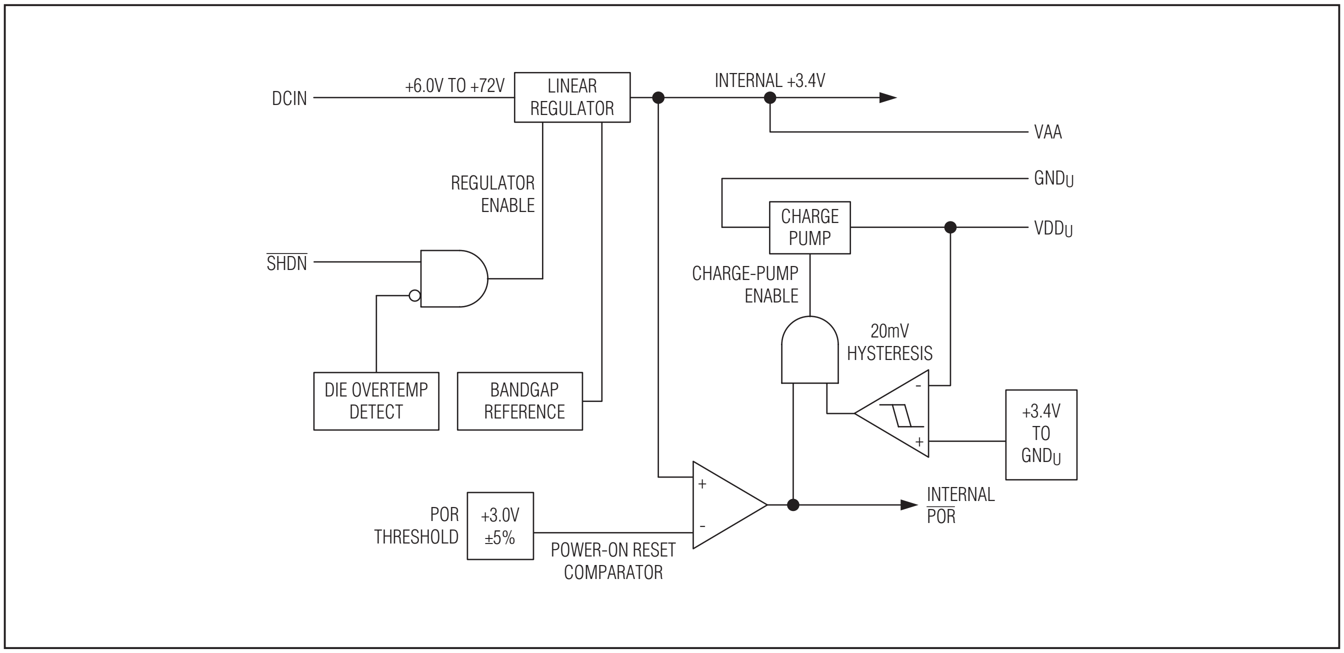


Figure 19. Internal Low-Dropout Regulator Block Diagram

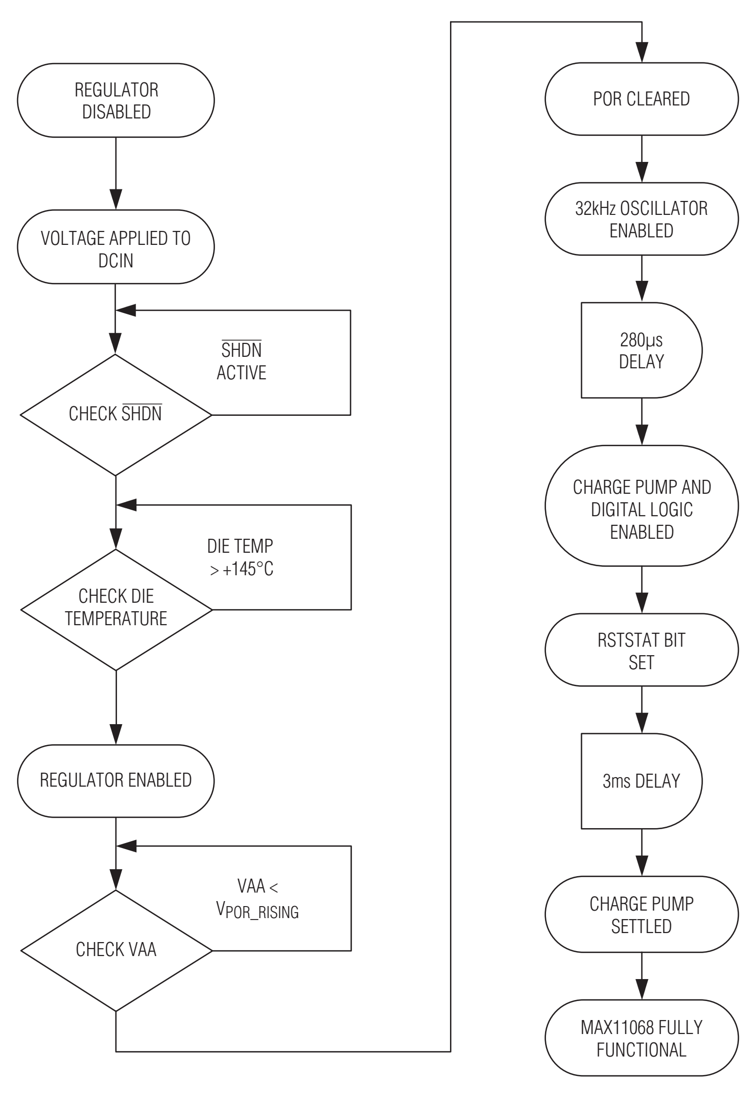


Figure 20. Power-Up Sequence

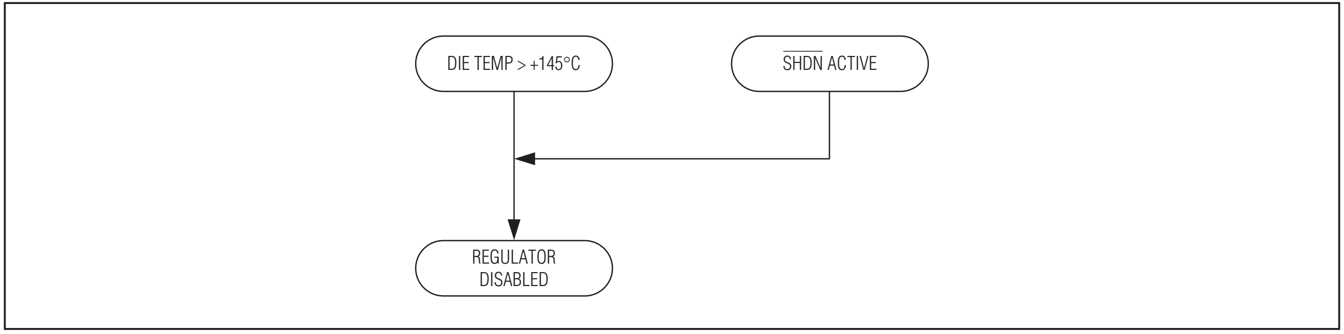


Figure 21. Asynchronous Regulator Disable Events

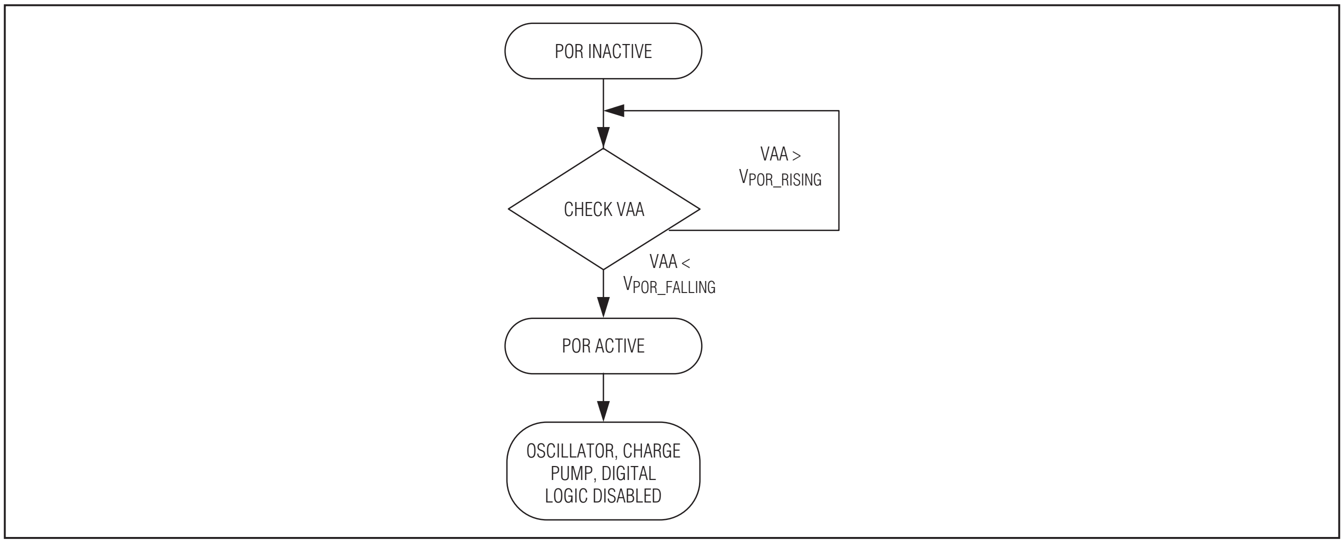


Figure 22. Power-On-Reset Event Sequence

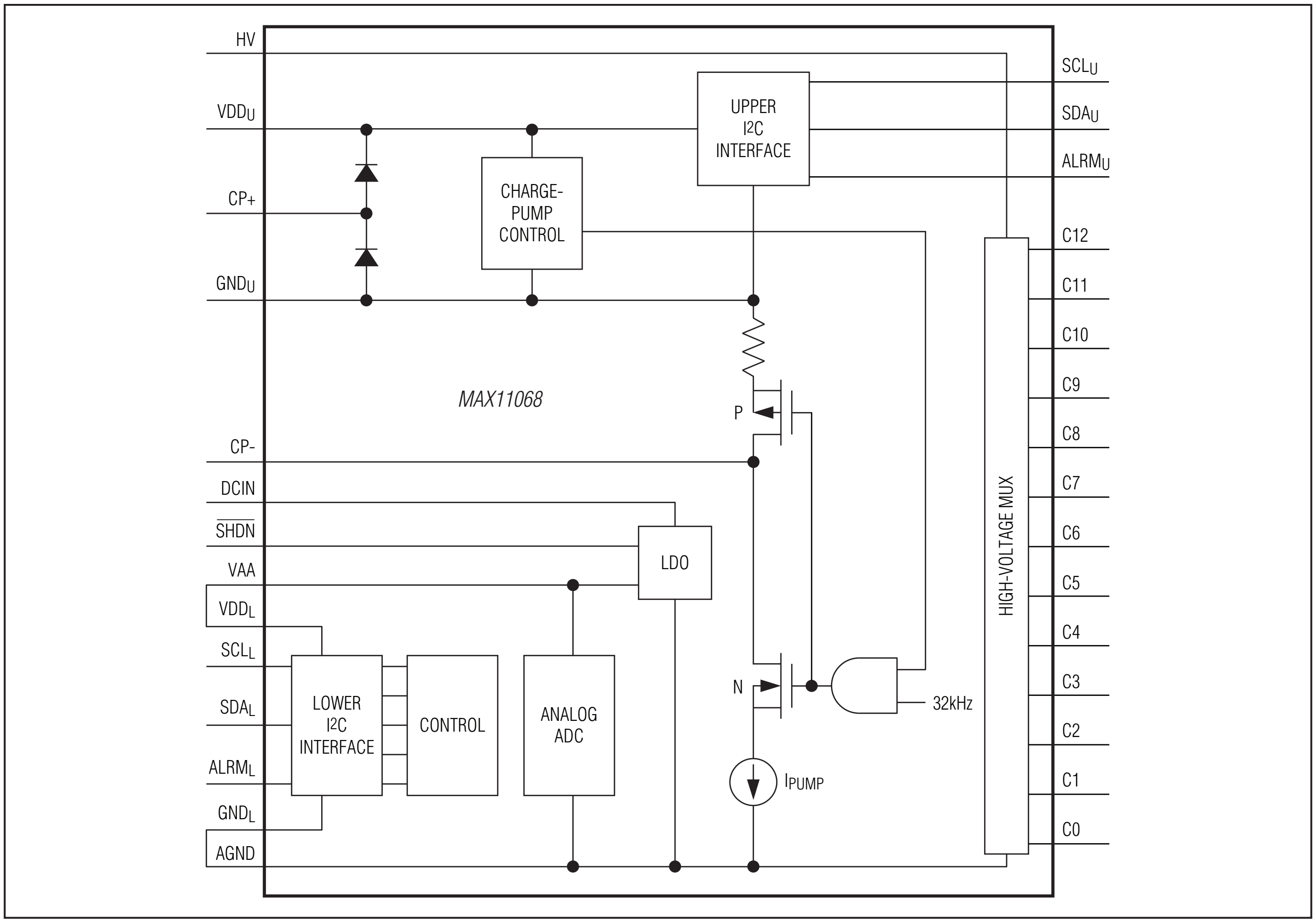


Figure 23. Detailed View of Supply and Ground Connections

DCIN Pin Application Circuit

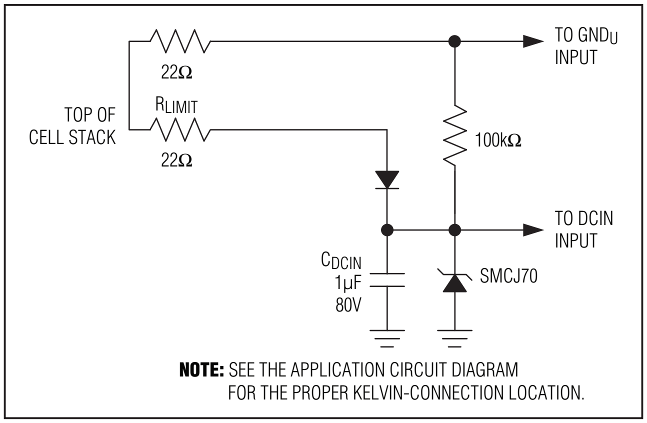
The DCIN pin is the input to the linear regulator. For maximum performance, it should be protected from any overvoltage conditions and also properly decoupled for peak transient current demands of the linear regulator. Figure 24 shows a recommended protection and decoupling circuit.

Since the linear regulator must supply load peaks to the ADC and other low-voltage circuitry, the DCIN pin must be properly decoupled to ensure proper performance. A 1µF high-voltage, high-quality ceramic capacitor should be used at the pin. The series diode, D1, prevents discharge of the DCIN decoupling capacitor during negative transients.

During regenerative braking conditions, a surge voltage is produced by the electric motor. The MAX11068 is designed to tolerate an absolute maximum of 80V under this condition. The MAX11068 should be protected against higher voltages with an external voltage suppressor such as the SMCJ70A. This protection circuit also helps to reduce power spikes that can occur during the insertion of the battery cells.

Precision Internal-Voltage Reference

The MAX11068 incorporates a precision, low-temperature coefficient, internal-voltage reference. The reference is used in the MAX11068 to set the full-scale range of the ADC. The REF pin is not designed to drive any external loads, and should be configured with an external 1µF capacitor to AGND only. This capacitor should be mounted as close as possible to the REF pin.



NOTE: SEE THE APPLICATION CIRCUIT DIAGRAM FOR THE PROPER KELVIN-CONNECTION LOCATION.

Figure 24. DCIN Overvoltage Protection and Decoupling Circuit

Auxiliary Analog Inputs and External Thermistor Supply Pin

The auxiliary analog inputs (1 and 2) can be used to monitor analog voltages with a full-scale range of 0 to THRM (3.4V). The full-scale range of the ADC for the auxiliary channel measurements is the THRM pin voltage referenced to AGND. The AUXIN1/2 pins are single-ended inputs that are measured against the AGND pin. A scan of the AUXIN inputs is first configured by enabling conversion of one or both inputs through the AIN1EN and AIN2EN bits of the ADCCFG register (address 0x08). After enabling the channels for measurement, a scan is initiated by setting the SCAN bit of the SCANCTRL register to 1. Conversions on the enabled auxiliary channels commence after the conversions for the cell input channels are complete. Conversion results are available in the AIN1 and AIN2 registers (addresses 0x40 and 0x41).

The AUXIN1/AUXIN2 pins can also be used in conjunction with the thermal supply pin (THRM) to monitor external RTD devices. The THRM pin has an internal switch connected to the internal-voltage regulator of the MAX11068. The purpose of the switch is to save power when a measurement of an external temperature-sensing device is not needed. During normal operation, the THRM pin is disabled. When the AIN1EN or AIN2EN bits of the ADCCFG register (address 0x08) are enabled and a measurement scan is initiated, a voltage source taken from the internal regulator is connected to the THRM pin. This occurs as soon as the scan signal is received and before any cell or auxiliary channel measurements have taken place. The THRM pin biases the RTD network so that the effect of temperature on the RTD component can be measured as a voltage by the ADC. Figure 25 is the external temperature-sensor configuration.

Since the THRM pin is not driving the AIN pin application circuit at all times, in some cases it may be necessary to adjust the settling time seen by the AIN pins before the measurement is started. A customized delay can be programmed through the ACQCFG register (address 0x0C) AINCFG bits to allow the application circuit extra time to settle before taking the ADC measurement for the AIN pins. The AINCFG bits have a resolution of 5.3µs, which is also the minimum delay value. The maximum delay is 339.2µs. The programmed delay from the ACQCFG register is implemented just before the measurement is taken on an AIN channel. If both channels are enabled for measurement, the delay is implemented twice, once just before each channel's measurement.

Care must be taken when selecting the AINCFG settling time value if the load on VDD_U is more than that specified by the typical application circuit diagrams. During the entire measurement cycle, the charge pump is disabled and the VDD_U voltage is supported only by the decoupling capacitor stored charge. If an extra load is placed on VDD_U and the AINCFG value is set too high, the VDD_U voltage may decay below levels that support error-free communication.

The recommended RTD network is a 10kΩ resistor in series with a 10kΩ NTC thermistor. For an NTC thermistor, the resistance increases as the temperature decreases. They are typically specified by a resistance at +25°C (R_0) and also by a factor called beta. To first order, the resistance at a temperature T in Kelvin can be found from:

$$R = R_0 e^{(\beta(1/T - 1/T_0))}$$

A typical value of beta for an NTC thermistor might be approximately 3400. By determining the resistance of the thermistor at the desired temperature thresholds, the voltage at the auxiliary inputs can be calculated. This voltage can then be converted to a digital threshold value using the ADC step size of 0.83mV/LSB, whose derivation follows below.

Once the ADC power-up delay and any cell measurements and the self-diagnostic measurement have completed, the auxiliary channel-acquisition cycle begins. First, AUXIN1 is measured, if enabled, followed by AUXIN2, if enabled.

Each individual voltage reading from the completed acquisition is stored in the appropriate AIN1 (address 0x40) or AIN2 (address 0x41) register. Since the ADC is 12 bits with a full-scale voltage of 3.4V, each LSB is approximately 0.83mV. Overall, a conversion on the AUXIN1 and/or AUXIN2 input completes in 10µs when only one of the auxiliary inputs are enabled and in 17µs when both are enabled. When the result is stored, it is compared against the under- and overtemperature thresholds saved in registers 0x1E and 0x1F, respectively.

Separate alert bits ALRTTHOT and ALRTTCOLD in the STATUS register (address 0x02) may be enabled to indicate when one of these temperature thresholds has been violated. Individual over- and undertemperature enables (HOTEN and COLDEN) for each of the two auxiliary analog channels are found in the AIN1 and AIN2 data registers. The alert bits are automatically cleared if the alert condition is cleared on subsequent conversions.

The overtemperature and undertemperature alarm enable bits ALRMOTEN and ALRMUTEN found in the ADCCFG register (address 0x08) determine whether alerts result in an alarm. When 1 of these bits is enabled, the respective alert causes an alarm signal to occur on the $ALRM_L$ pin.

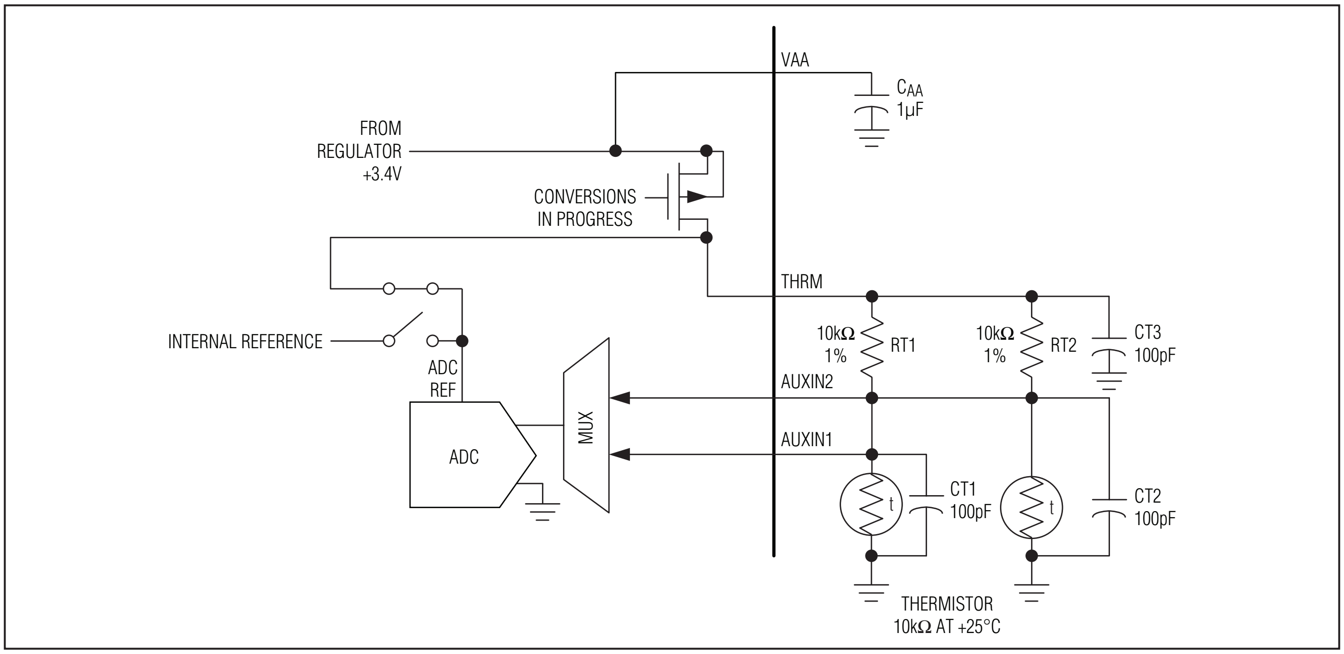


Figure 25. External Temperature-Sensor Configuration

Self-Diagnostics

The MAX11068 incorporates the capability to check the health of its internal voltage reference and regulator output. The results are stored in the DIAG register. Conversions are enabled by setting the DIAGEN bit of the ADCCFG register (address 0x08). They are initiated immediately following the cell conversions. For the self-diagnostic measurement, the ADC reference is taken from the internal THRM pin connection. This makes the full-scale range of the self-diagnostic measurement 3.4V. The reference voltage is measured differentially against the internal voltage on C0 through an instrumentation amp, the low-voltage mux, and finally the internal ADC. The instrumentation amp has a gain of 1/2 that must be taken into account when calculating the expected diagnostic result. The complete block diagram for the self-diagnostic measurement is shown in Figure 26.

The expected value of the self-diagnostic measurement varies depending on the regulator output voltage, the reference voltage itself, and the accuracy of the ADC. When discussing the DIAG measurement values, the least significant nibble of the DIAG register is ignored since only the three most significant nibbles contain real data. To first order, the expected value of the self-diagnostic measurement is:

$$\mathrm{DIAG} = \big((\mathrm{REF} - \mathrm{C0}) \times 0.5/\mathrm{VAA}\big) \times 4096$$

Since the specified regulator voltage can vary by approximately ±10%, the expected result of the self-diagnostic varies proportionally. For typical values of REF = 2.5V and VAA = 3.4V, the nominal DIAG value for normal operation is 5E1h with a tolerance of ±150 LSBs (±0x96). Typical devices may vary from this value due to trim differences. Table 3 shows typical values and ranges for the DIAG value for various fault and no-fault conditions.

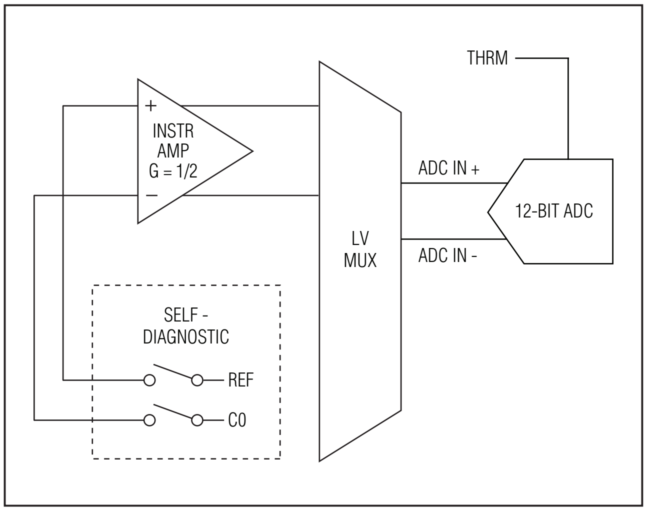


Figure 26. Block Diagram of Self-Diagnostic Mode Connections

In a typical application, the self-diagnostic measurement should be performed and stored when the system is operated for the first time. By periodically performing a new measurement, the results can be compared against the original value to verify that the system is operating at the expected performance level. As shown in Table 2, a change on the order of ≤ 4 LSBs can be expected across the full temperature range.

The REF pin also has a special failure-mode effects analysis (FMEA) detector to alert when an open-circuit may exist. The alert is the ALRTREF bit of the FMEA register. It detects when the REF pin has an oscillating voltage condition, which is a symptom of an open circuit on the pin.

Table 3. DIAG Typical Values and Ranges

FAULT CONDITION	DIAG VALUE (TYPICAL)	DIAG VALUE RANGE (TYPICAL)	VARIATION FROM INITIAL VALUE (LSB)
None	0x5E1	0x54B to 0x677	+4 to -4
C0 is open	0x1DA to 0x1DC	0x1DA to 0x1DC	—
REF is shorted to AGND	0x292 to 0x293	0x292 to 0x293	—
REF pin is open or floating	0x3C1 to 0x7AE	Use ALRTREF in the FMEA register	—

Noise Tolerance

High-power batteries are often used in noisy environments subject to high dv/dt supply noise and EMI noise. For example, the supply noise of a power inverter driving a high-horsepower motor produces a large square wave at the battery terminals, even though the battery is also a high-power battery. Typically, the battery dominates the task of absorbing this noise, since it is impractical to put hundreds of farads at the inverter. Supply noise between two modules occurs due to the very large current transients that are often present in high-power battery systems. Even very-low-impedance connections of only a few milliohms between the various battery modules and the load can produce substantial voltage noise that would not allow an AC-coupled ground-referenced I²C communication system to work reliably. Voltage noise is also induced through the batteries' impedance, which cannot be easily reduced. A unique level-shifting SMBus ladder communication architecture solves these problems by referencing the communication signals from one module to the next from a common voltage that is shared by both modules. The supply noise seen by the communication interface is thus greatly reduced and is then able to be rejected completely in most cases.

In a typical application of up to approximately 200A to 400A, the GND_U supply may be connected to the top of the battery stack without the communication path experiencing adverse affects from bus-bar-induced noise. In some high-current applications where the load current is greater than 400A, or the module interconnect impedance is more than a couple milliohms, further precautions may be necessary to ensure optimal performance. In these cases, the extreme current levels across even tiny interconnect impedances can result in significant noise due to the GND_U reference connection. Applications with one or more of the following conditions may benefit from connecting GND_U with a Kelvin style:

- The bus bar impedance is greater than 1mΩ to 2mΩ.
- Battery pack current steps are greater than 400A in less than 100µs.
- The RC time constant at cell 12 does not match the time constant at DCIN.

In applications that meet these conditions, a Kelvin connection should be made from GND_U to AGND of the next-higher module. For applications that do not have these conditions, the Kelvin-style connection is optional. This connection can reject noise induced across the bus bar to further improve noise immunity for the I²C interface. Figure 27 demonstrates how to properly Kelvin-connect modules for maximum noise immunity. This method requires careful attention to the mechanical design of the module, since an extra module terminal connection is required. DCIN and C12 should not share a common terminal of a module for Kelvin-connected modules.

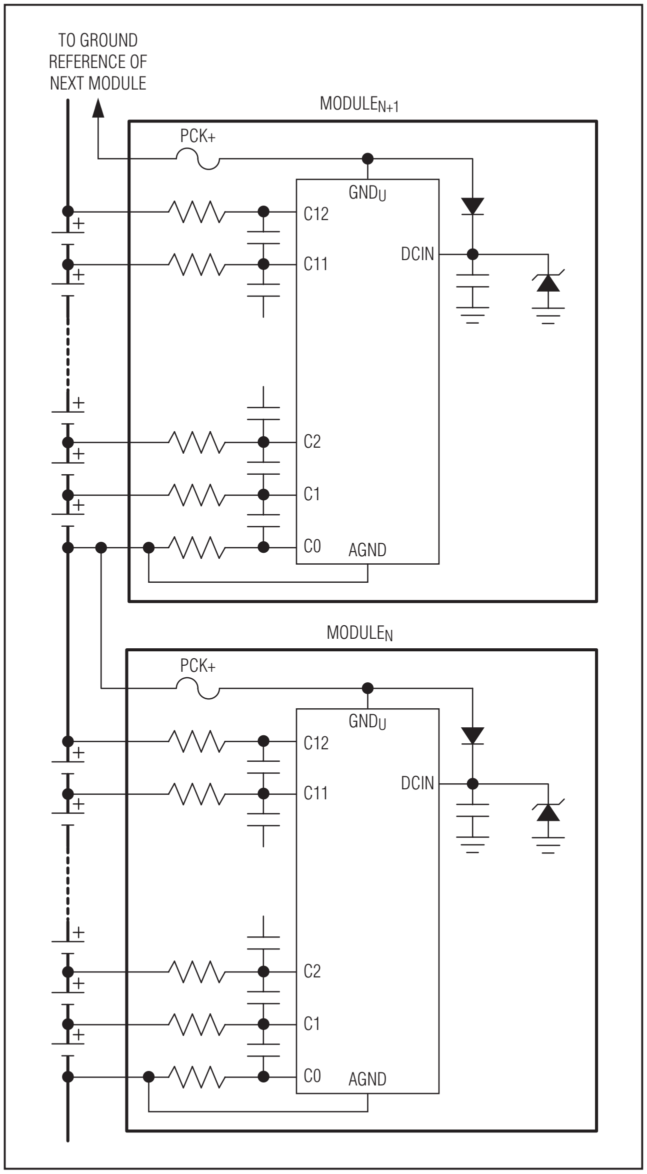


Figure 27. Module-to-Module DCIN Kelvin Connection

Register Map

Table 4. I^{2}C Register Map

REGISTER ADDRESS	REGISTER NAME	R/W	DESCRIPTION	POR STATE
MANAGEMENT FUNCTIONS				
0x00	VERSION	R	Contains coded information corresponding to the device model number and die version, where n is the least significant byte denoting the die revision code.	0x068
0x01	ADDRESS	R/W	A read of this register returns the I^{2}C address of the device and the device address of the last device in the SMBus ladder. Perform a ROLLCALL command (special case of READALL) to this address to determine the number of devices in the stack.	0x1FA0
0x02	STATUS	R/W	Read for status flags; write 0s to clear status flags.	0x8000
0x03	ALRTCELL	R/W	Read for cell-alert status flags.	0x0000
0x04	ALRTOVCELL	R/W	Read for overvoltage cell-alert status flags.	0x0000
0x05	ALRTUVCELL	R/W	Read for undervoltage cell-alert status flags.	0x0000
0x06	ALRTOVEN	R/W	Overvoltage cell-alert enables for cells 1–12.	0x0000
0x07	ALRTUVEN	R/W	Undervoltage cell-alert enables for cells 1–12.	0x0000
0x08	ADCCFG	R/W	Aux channel enable, alarm enable, and scan control.	0x0000
0x09	CELLEN	R/W	Cell measurement enable.	0x0000
0x0A	GPIO	R/W	GPIO2 to GPIO0 configuration.	0x0000
0x0B	BALCFG	R/W	Cell-balancing switch control.	0x0000
0x0C	ACQCFG	R/W	Acquisition time control configuration register for the auxiliary analog inputs.	0x0000
0x0D	SCANCTRL	R/W	Measurement scan control.	0x0000
0x0E	FMEA	R/W	Failure-mode effects analysis status and control.	0x0000
0x0F	BROADCAST ADDRESS	R/W	Broadcast address.	0x0040

Table 4. I^{2}C Register Map (continued)

REGISTER ADDRESS	REGISTER NAME	R/W	DESCRIPTION		POR STATE
SUMMARY AND ALERT FUNCTIONS					
0x10	TOTAL	R	Result for a sum total of all CELL_N measurements in the scan.		0x0000
0x11	MAXCELL	R	Result for the highest/maximum cell voltage measured during the scan.		0x000F
0x12	MINCELL	R	Result for the lowest/minimum cell voltage measured during the scan.		0x000F
0x18	OVTHRCLR	R/W	Overvoltage clear threshold	When any ADC cell conversion is completed, the value is compared with OVTHRSET, OVTHRCLR, UVTHRSET, and UVTHRCLR. The difference between UVTHRSET and UVTHRCLR or OVTHRSET and OVTHRCLR is effectively a digital hysteresis for the alert threshold. If: **CELL_N > OVTHRSET or CELL_N < UVTHRSET** The corresponding alert bits are set. The overvoltage alert bit is cleared when: **CELL_N < OVTHRCLR** The undervoltage alert bits are cleared when: **CELL_N > UVTHRCLR**	0xFFF0
0x19	OVTHRSET	R/W	Overvoltage set threshold		0xFFF0
0x1A	UVTHRSET	R/W	Undervoltage set threshold		0x0000
0x1B	UVTHRCLR	R/W	Undervoltage clear threshold		0x0000
0x1C	MSMTCH	R/W	Cell mismatch threshold	When a scan of conversions is completed, a mismatch alert is generated if the result of: **MAXCELL - MINCELL > MSMTCH** Set MSMTCH = 0xFFFF to disable mismatch alerts.	0xFFF0
0x1E	AINOT	R/W	Auxiliary input overtemperature threshold.		0x0000
0x1F	AINUT	R/W	Auxiliary input undertemperature threshold.		0xFFF0
MEASUREMENTS					
0x20	CELL1	R/W	Result for ADC conversion of C1.		0x0000
0x21	CELL2	R/W	Result for ADC conversion of C2.		0x0000
0x22	CELL3	R/W	Result for ADC conversion of C3.		0x0000
0x23	CELL4	R/W	Result for ADC conversion of C4.		0x0000
0x24	CELL5	R/W	Result for ADC conversion of C5.		0x0000
0x25	CELL6	R/W	Result for ADC conversion of C6.		0x0000
0x26	CELL7	R/W	Result for ADC conversion of C7.		0x0000
0x27	CELL8	R/W	Result for ADC conversion of C8.		0x0000
0x28	CELL9	R/W	Result for ADC conversion of C9.		0x0000
0x29	CELL10	R/W	Result for ADC conversion of C10.		0x0000
0x2A	CELL11	R/W	Result for ADC conversion of C11.		0x0000
0x2B	CELL12	R/W	Result for ADC conversion of C12.		0x0000
0x40	AIN1	R/W	Result for ADC conversion of AUXIN1.		0x0000
0x41	AIN2	R/W	Result for ADC conversion of AUXIN2.		0x0000
0x44	DIAG	R	Result for ADC conversion for the diagnostic front-end test (used for self-test).		0x0000

Register Descriptions

The MAX11068 contains 38 registers that control and report the operational status of the device (see Tables 5 through 34).

Table 5. VERSION—IC Version Register Description (Address 0x00)

BIT	NAME	FUNCTION
D15	0	MAX11068 model number designator, 0x068
D14	0	
D13	0	
D12	0	
D11	0	
D10	1	
D9	1	
D8	0	
D7	1	
D6	0	
D5	0	
D4	0	
D3	VER3	MAX11068 mask revision version number; Revision 3.0 = 0x7h
D2	VER2	
D1	VER1	
D0	VER0	

Table 6. ADDRESS Register Description (Address 0x01)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	LA4	The last address bits are used to support the SMBus ladder alarm feature and the error-checking bytes of the READALL command. These bits are set by the SETLASTADDRESS command and correspond to the A[4:0] device address bits of the last device in the chain. Once properly set in all nodes, the alarm heartbeat function begins.
D11	LA3	
D10	LA2	
D9	LA1	
D8	LA0	
D7	1	Write ignored; read back 1.
D6	0	Write ignored; read back 0.
D5	A0	I^2C device address. A0 is the LSB. The first A[0:4] device address in the SMBus ladder is set with the HELLOALL command. The HELLOALL command is then propagated up the SMBus ladder and automatically incremented for each device, up to a maximum of 31 nodes. This gives each device a unique A[0:4] address.
D4	A1	
D3	A2	
D2	A3	
D1	A4	
D0	0	Write ignored; read back 0.

Table 7. STATUS Register Description (Address 0x02)

BIT	NAME	FUNCTION
D15	RSTSTAT	Reset Status: RSTSTAT = 1 after a power-reset event. Clear RSTSTAT to 0 after power-up and after a successful HELLOALL command to detect any future resets. Writing a 1 to this bit has no effect. PEC errors should be ignored until this bit is cleared.
D14	ALRTOV	Cell Overvoltage Alert: ALRTOV = 1 when a corresponding overvoltage has occurred. Check the ALRTOVCELL register to determine which cell is responsible. This is a read-only bit. All voltage alerts are automatically cleared when the next conversion occurs and the alert condition disappears.
D13	ALRTUV	Cell Undervoltage Alert: ALRTUV = 1 when a corresponding undervoltage has occurred. Check the ALRTUVCELL register to determine which cell is responsible. This is a read-only bit. All voltage alerts are automatically cleared when the next conversion occurs and the alert condition disappears.
D12	ALRTMSMTCH	Mismatch Alert: ALRTMSMTCH = 1 when MAXCELL - MINCELL > MSMTCH threshold: This is a read-only bit. All voltage alerts are automatically cleared when the next conversion occurs and the alert condition disappears.
D11	ALRTTCOLD	Undertemperature Alert: Set when AIN1 > AINUT or AIN0 > AINUT. This is a read-only bit. All temperature alerts are automatically cleared when the next conversion occurs and the alert condition disappears. The comparison with AINUT assumes an NTC thermistor is used as part of the suggested application circuit.
D10	ALRTTHOT	Overtemperature Alert: Set when AIN1 < AINOT or AIN0 < AINOT. This is a read-only bit. All temperature alerts are automatically cleared when the next conversion occurs and the alert condition disappears. The comparison with AINOT assumes an NTC thermistor is used as part of the suggested application circuit.
D9	ALRTPEC	Packet Error Check Alert: Indicates a communication failure occurred due to a slave or master PEC error. The PEC is a CRC-8 error check byte, calculated on all message bytes except the ACK, NACK, START, and STOP bits. The ALRTPEC bit must be cleared by writing a 0 to this bit location to detect future PEC failures. Writing a 1 to this bit has no effect.
D8	ALRTACK	Acknowledge Communication Alert: Indicates a communication fault due to an unexpected slave or master NACK in the ACK/NACK bit position. ALRTACK must be cleared by writing this bit to 0 to detect future NACK events. Writing a 1 to this bit has no effect.
D7	ALRTFMEA	FMEA Status Alert: Indicates that there is an FMEA alert. This bit is the logical OR of the alert bits in the FMEA register. Check the FMEA register to determine which alerts are active.

Table 7. STATUS Register Description (Address 0x02) (continued)

BIT	NAME	FUNCTION
D6	0	Write ignored; read back 0.
D5	0	
D4	0	
D3	0	
D2	0	
D1	ALRTAIN2	AIN1 Fault: Indicates a fault condition (over- or undertemperature) was detected on the AIN1 analog input. A fault occurs when the AIN1 input exceeds the set levels in the AINOT and AINUT registers. This bit is cleared automatically when the alert condition disappears following a new measurement. Writing a 1 to this bit has no effect.
D0	ALRTAIN1	AIN0 Fault: Indicates a fault condition (over- or undertemperature) was detected on the AIN0 analog input. A fault occurs when the AIN0 input exceeds the set levels in the AINOT and AINUT registers. This bit is cleared automatically when the alert condition disappears following a new measurement. Writing a 1 to this bit has no effect.

Table 8. ALRTCELL—Per-Cell Alert Status Register Description (Address 0x03)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	ALRTCELL12	Alert Cell Fault: ALRTCELL$_N$ is set when the corresponding cell is overvoltage or undervoltage. The register bits are the logical OR of the corresponding ALRTOVCELL and ALRTUVCELL register bits. All voltage alerts are automatically cleared when the alert condition disappears.
D10	ALRTCELL11	
D9	ALRTCELL10	
D8	ALRTCELL9	
D7	ALRTCELL8	
D6	ALRTCELL7	
D5	ALRTCELL6	
D4	ALRTCELL5	
D3	ALRTCELL4	
D2	ALRTCELL3	
D1	ALRTCELL2	
D0	ALRTCELL1	

Table 9. ALRTOVCELL—Per-Cell Overvoltage Alert Register Description (Address 0x04)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	ALRTOV12	Alert Cell Overvoltage Fault: ALRTOV[N] bits are set when the corresponding cell is overvoltage. All voltage alerts are automatically cleared when the alert condition disappears.
D10	ALRTOV11	
D9	ALRTOV10	
D8	ALRTOV9	
D7	ALRTOV8	
D6	ALRTOV7	
D5	ALRTOV6	
D4	ALRTOV5	
D3	ALRTOV4	
D2	ALRTOV3	
D1	ALRTOV2	
D0	ALRTOV1	

Table 10. ALRTUVCELL—Per-Cell Undervoltage Alert Register Description (Address 0x05)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	ALRTUV12	Alert Cell Undervoltage Fault: ALRTUV[N] bits are set when the corresponding cell is undervoltage. All voltage alerts are automatically cleared when the alert condition disappears.
D10	ALRTUV11	
D9	ALRTUV10	
D8	ALRTUV9	
D7	ALRTUV8	
D6	ALRTUV7	
D5	ALRTUV6	
D4	ALRTUV5	
D3	ALRTUV4	
D2	ALRTUV3	
D1	ALRTUV2	
D0	ALRTUV1	

Table 11. ALRTOVEN—Per-Cell Overvoltage Alert Enable Register Description (Address 0x06)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	OVALRTEN12	Overvoltage Cell-Alert Enable: Overvoltage alert enable bits for cells 1–12. Set the corresponding bit to enable alert notification for overvoltage events on that cell input. Set to 0 to disable alarm notification for a cell or to clear the associated cell alarm. Alert notification is not affected by the status of the alarm enable bits. This alert enable bit for each cell is also accessible through bit 1 of the CELLEN register.
D10	OVALRTEN11	
D9	OVALRTEN10	
D8	OVALRTEN9	
D7	OVALRTEN8	
D6	OVALRTEN7	
D5	OVALRTEN6	
D4	OVALRTEN5	
D3	OVALRTEN4	
D2	OVALRTEN3	
D1	OVALRTEN2	
D0	OVALRTEN1	

Table 12. ALRTUVEN—Per-Cell Undervoltage Alert Enable Register Description (Address 0x07)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	UVALRTEN12	Undervoltage Cell Alert Enable: Undervoltage alert enable bits for cells 1–12. Set the corresponding bit to enable alarm notification for undervoltage alerts on that cell input. Set to 0 to disable alarm notification for a cell or to clear the associated cell alarm. Alert notification is not affected by the status of the alarm enable bits. This alert enable bit for each cell is also accessible through bit 0 of the CELLEN register.
D10	UVALRTEN11	
D9	UVALRTEN10	
D8	UVALRTEN9	
D7	UVALRTEN8	
D6	UVALRTEN7	
D5	UVALRTEN6	
D4	UVALRTEN5	
D3	UVALRTEN4	
D2	UVALRTEN3	
D1	UVALRTEN2	
D0	UVALRTEN1	

Table 13. ADCCFG—ADC Configuration Register Description (Address 0x08)

BIT	NAME	FUNCTION
D15	SCAN	Start conversions scan set with 1 to initiate an ADC scan of the enabled cell channels. A new measurement scan is initiated as long as the ADC is not busy with a previous scan. Otherwise, the scan start is ignored. This bit always reads back 0. The SCAN bit of the SCANCTRL register has the same function and is the recommended register control for initiating a scan.
D14	ALRMMMTCHEN	Voltage Mismatch Alarm Enable Mask: Set ALRMMMTCHEN = 1 to force a mismatch alert, ALRTMSMTCH, to generate an alarm. Set ALRMMMTCHEN = 0 to prevent a mismatch alert from generating an alarm.
D13	ALRMOVEN	Overvoltage Alarm Enable Mask: Set ALRMOVEN = 1 to force an overvoltage alert, ALRTOV, to generate an alarm. Set ALRMOVEN = 0 to prevent an overvoltage alert from generating an alarm.
D12	ALRMUVEN	Undervoltage Alarm Enable Mask: Set ALRMUVEN = 1 to force an undervoltage alert, ALRTUV, to generate an alarm. Set ALRMUVEN = 0 to prevent an undervoltage alert from generating an alarm.
D11	ALRMUTEN	Undertemperature Alarm Enable Mask: Set ALRMUTEN = 1 to force an undertemperature alert, ALRTTCOLD, to generate an alarm. Set ALRMUTEN = 0 to prevent an undertemperature alert from generating an alarm.
D10	ALRMOTEN	Overtemperature Alarm Enable Mask: Set ALRMOTEN = 1 to force an overtemperature alert, ALRTTHOT, to generate an alarm. Set ALRMOTEN = 0 to prevent an overtemperature alert from generating an alarm.
D9	ALRMPEC	Packet-Error Check (PEC) Alarm Enable Mask: Set ALRMPEC = 1 to force a packet-error check alert, ALRTPEC, to generate an alarm. Set ALRMPEC = 0 to prevent a packet-error check alert from generating an alarm.
D8	ALRMACK	Acknowledge Communication Fault Alarm Enable: Set ALRMACK = 1 to force an acknowledge communication fault alert, ALRTACK, to generate an alarm. Set ALRMACK = 0 to prevent an acknowledge communication check alert from generating an alarm.
D7	Unused	Unused Bit: Reads back written value.
D6	Unused	
D5	Unused	
D4	DIAGEN	Self-Test Diagnostic Enable: Enable reference channel diagnostic conversion. Used for internal diagnostic self-test. Set to 1 to enable the measurement to occur during the measurement cycle.
D3	Unused	Unused Bit: Reads back written value.
D2	Unused	
D1	AIN2EN	AUXIN2 Channel Conversion Enable: Enables a conversion on the AUXIN2 input. After a conversion is completed, the results are compared to the over- and undertemperature thresholds.
D0	AIN1EN	AUXIN1 Channel Conversion Enable: Enables a conversion on the AUXIN1 input. After a conversion is completed, the results are compared to the over- and undertemperature thresholds.

Table 14. CELLEN—Cell-Scan Enable Register Description (Address 0x09)

BIT	NAME	
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	CELL12EN	Cell Channel Scan Enable: Set the cell enable bit to 1 to enable the corresponding channel in the measurement cycle. Set to 0 to disable a cell measurement for a scan. Disabled channels do not have their measurement values changed by a scan.
D10	CELL11EN	
D9	CELL10EN	
D8	CELL9EN	
D7	CELL8EN	
D6	CELL7EN	
D5	CELL6EN	
D4	CELL5EN	
D3	CELL4EN	
D2	CELL3EN	
D1	CELL2EN	
D0	CELL1EN	

Table 15. GPIO—General-Purpose I/O Register Description (Address 0x0A)

BIT	NAME	FUNCTION
D15	Unused	Unused Bit: Reads back written value.
D14	DIR2	Input/Output Direction: Write the DIR bits to 1 to set the GPIO pin drivers to output. Write the DIR bits to 0 to set the drivers as a high-impedance input. The bits default to a 0 and the high-impedance input state.
D13	DIR1	
D12	DIR0	
D11	Unused	Unused Bit: Reads back written value.
D10	GPIO2	GPIO Pin Logic State: When reading this byte, the GPIO[N] bits always return the logic state of each GPIO pin.
D9	GPIO1	
D8	GPIO0	
D7	0	Write ignored; reads 0.
D6	0	
D5	0	
D4	0	
D3	Unused	Unused Bit: Reads back written value.
D2	GPIO2OUT	The GPIO[N]OUT bits configure the GPIO pin output driver-logic level. These bits only determine the driver state when the driver is set to be an output by the DIR bits and have no affect on the GPIO pins if the DIR bits are set to the input state.
D1	GPIO1OUT	
D0	GPIO0OUT	

Table 16. BALCFG—Cell-Balancing Configuration Register Description (Address 0x0B)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	BAL12	Cell-Balancing/Discharge Switch Enable: Select cell-balancing/discharge switches to activate. Set BAL[N] to 1 to enable the cell-balancing switch between C_{N-1} and C_N. Clearing to 0 disables the balancing/discharge switch. The switches are separately disabled by signals from the die overtemperature detection circuit and the cell-balancing watchdog timer.
D10	BAL11	
D9	BAL10	
D8	BAL9	
D7	BAL8	
D6	BAL7	
D5	BAL6	
D4	BAL5	
D3	BAL4	
D2	BAL3	
D1	BAL2	
D0	BAL1	

Table 17. ACQCFG—Acquisition Configuration Register Description (Address 0x0C)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	CBPDIV1	Cell-Balancing Timer Predivider: Sets the step size of the cell-balancing timer LSB. 00 = Disabled, no timeout for the cell-balancing switch on-time. 01 = 1s; timer range is then 1s to15s. 10 = 4s; timer range is then 4s to 60s. 11 = 16s; timer range is then 16s to 240s.
D12	CBPDIV0	
D11	CBTIMER3	Cell-Balancing Timer: Acts as a safety watchdog timeout for the cell-balancing switches. The timer counts down at a rate set by the CBPDIV bits. When the timer reaches 0, all cell-balancing switches are disabled. The timer should be periodically rewritten with a timeout value to keep the cell-balancing switches enabled. When the timer value is read, the value reported is latched during the 9th bit time following the ACQCFG register address of the READALL command.
D10	CBTIMER2	
D9	CBTIMER1	
D8	CBTIMER0	
D7	0	Write ignored; read back 0.
D6	0	

Table 17. ACQCFG—Acquisition Configuration Register Description (Address 0x0C) (continued)

BIT	NAME	FUNCTION
D5	AINCFG5	Auxiliary Analog Input-Acquisition Time Configuration: Custom acquisition settling time for AUXIN1/AUXIN2. The auxiliary analog channels acquisition settling time can be set from 5.3µs up to 339.2µs with a count increment of 5.3µs/count. This is to allow extra settling time if the application circuit requires it since the THRM pin becomes active only during the measurement sequence. AINCFG default is 0x000, which equals an acquisition time of 5.3µs. The full settling time is added prior to the measurement for each enabled auxiliary channel.
D4	AINCFG4	
D3	AINCFG3	
D2	AINCFG2	
D1	AINCFG1	
D0	AINCFG0	

Table 18. SCANCTRL—Measurement Scan Control Register Description (Address 0x0D)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	0	
D10	0	
D9	0	
D8	0	
D7	0	
D6	0	
D5	0	
D4	0	
D3	0	
D2	0	
D1	0	
D0	SCAN	Start Conversions Scan: Set to 1 to initiate an ADC scan of the enabled cell channels. A new measurement scan is initiated as long as the ADC is not busy with a previous scan. Otherwise, the scan signal is ignored. This bit always reads back 0.

Table 19. FMEA—Failure-Mode Effects Analysis Status and Control Register Description (Address 0x0E)

BIT	NAME	FUNCTION
D15	ALRMCPUV	Charge-Pump Undervoltage Alarm Enable Mask: Set ALRMCPUV = 1 to force a charge-pump alert, ALRTCPUV, to generate an alarm. Set ALRMCPUV = 0 to prevent a charge-pump alert from generating an alarm.
D14	ALRMHBEAT	Heartbeat Frequency Alarm Enable Mask: Set ALRMHBEAT = 1 to force a heartbeat frequency alert, ALRTHBEAT, to generate an alarm. Set ALRMHBEAT = 0 to prevent a heartbeat frequency alert from generating an alarm.
D13	Unused	Unused Bit: Reads back written value.
D12	ALRMREF	REF Pin Open-Circuit Alarm Enable Mask: Set ALRMREF = 1 to force a REF pin open-circuit alert, ALRTREF, to generate an alarm. Set ALRMREF = 0 to prevent a REF pin open-circuit alert from generating an alarm.
D11	Unused	Unused Bit: Reads back written value.
D10	Unused	Unused Bit: Reads back written value.
D9	ALRMVDDL	VDDL Open-Circuit Alarm Enable Mask: Set ALRMVDDL = 1 to force a VDD_L open-circuit alert, ALRTVDDL, to generate an alarm. Set ALRMVDDL = 0 to prevent a VDD_L open-circuit alert from generating an alarm.
D8	ALRMGNDL	GND_L Open-Circuit Alarm Enable Mask: Set ALRMGNDL = 1 to force a GND_L open-circuit alert, ALRTGNDL, to generate an alarm. Set ALRMGNDL = 0 to prevent a GND_L open-circuit alert from generating an alarm.
D7	ALRTCPUV	Charge-Pump Undervoltage Alert: Indicates that the charge-pump output voltage has fallen below the undervoltage threshold V_{CPUV}. This bit is not set before the RSTSTAT bit is cleared. Writing a 1 to this bit has no effect. This bit must be written to 0 to clear the alert condition.
D6	ALRTHBEAT	Heartbeat Frequency Alert: Indicates that the alarm heartbeat signal has a frequency error of more than ±12.5% relative to the 32.768kHz oscillator divided by 2. This bit is not set before the RSTSTAT bit is cleared. Writing a 1 to this bit has no effect. This bit must be written to 0 to clear the alert condition.
D5	Unused	Unused Bit: Reads back written value.
D4	ALRTREF	REF Pin Open-Circuit Alert: Indicates that the REF pin is oscillating, most likely due to a missing decoupling capacitor or open-circuit condition. The detection test occurs just after a valid measurement scan is initiated. After each ADC strobe, there is a time of 4/32kHz where logic transitions are counted. ALRTREF is set for four positive transitions. If there are no strobes, ALRTREF cannot be set.
D3, D2	Unused	Unused Bit: Reads back written value.
D1	ALRTVDDL	VDD_L Pin Open-Circuit Alert: Indicates that an open circuit is detected on the VDD_L pin. This bit is not set before the RSTSTAT bit is cleared. Writing a 1 to this bit has no effect. This bit must be written to 0 to clear the alert condition.
D0	ALRTGNDL	GND_L Pin Open-Circuit Alert: Indicates that an open circuit is detected on the GND_L pin. This bit is not set before the RSTSTAT bit is cleared. Writing a 1 to this bit has no effect. This bit must be written to 0 to clear the alert condition.

Table 20. BROADCAST ADDRESS—Broadcast Address Register Description (Address 0x0F)

BIT	NAME	FUNCTION
D15	0	Write ignored; read back 0.
D14	0	
D13	0	
D12	0	
D11	0	
D10	0	
D9	0	
D8	0	
D7	BRDCST7	Broadcast Address: This byte contains the communication bus broadcast address. The LSB, BRDCST0, is not used and can be considered a don't care. The default is 0040h.
D6	BRDCST6	
D5	BRDCST5	
D4	BRDCST4	
D3	BRDCST3	
D2	BRDCST2	
D1	BRDCST1	
D0	BRDCST0	

Table 21. TOTAL—Total Cell Voltages Data Register Description (Address 0x10)

BIT	NAME	FUNCTION
D15	SUM15	16-bit sum total value of all cells enabled in the measurement scan.
D14	SUM14	
D13	SUM13	
D12	SUM12	
D11	SUM11	
D10	SUM10	
D9	SUM9	
D8	SUM8	
D7	SUM7	
D6	SUM6	
D5	SUM5	
D4	SUM4	
D3	SUM3	
D2	SUM2	
D1	SUM1	
D0	SUM0	

Table 22. MAXCELL—Maximum Cell Reading Register Description (Address 0x11)

BIT	NAME	FUNCTION
D15	D11	12-bit ADC conversion result of the highest cell-voltage reading.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	CH3	Cell number of the maximum cell voltage acquired. If multiple cells have the same maximum value, this field contains the highest cell number with that measurement.
D2	CH2	
D1	CH1	
D0	CH0	

Table 23. MINCELL—Minimum Cell Reading Register Description (Address 0x12)

BIT	NAME	FUNCTION
D15	D11	12-bit ADC conversion result of the lowest cell-voltage reading.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	CH3	Cell number of the minimum cell voltage acquired. If multiple cells have the same minimum value, this field contains the highest cell number with that measurement.
D2	CH2	
D1	CH1	
D0	CH0	

Table 24. OVTHCLR—Overvoltage Clear Threshold Register Description (Address 0x18)

BIT	NAME	FUNCTION
D15	D11	12-bit limit for the reset threshold of overvoltage-alert detection. An alert that is issued when the overvoltage set threshold is exceeded by a cell voltage is not cleared until the voltage falls below this lower threshold. The overvoltage alert is updated on each new measurement scan of the cell voltages by comparing against the threshold values. This alert-clearing threshold builds in digital hysteresis to the overvoltage detection.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

Table 25. OVTHRSET—Overvoltage Set Threshold Register Description (Address 0x19)

BIT	NAME	FUNCTION
D15	D11	12-bit limit for the triggering threshold of overvoltage-alert detection. An alert for a given cell is issued when this set threshold is exceeded by the cell voltage and the alert is not cleared until the cell voltage falls below the clear threshold. The overvoltage alert is updated on each new measurement scan of the cell voltages by comparing against the overvoltage threshold values. This alert setting threshold is a critical maximum cell-voltage level.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

Table 26. UVTHRSET—Undervoltage Set Threshold Register Description (Address 0x1A)

BIT	NAME	FUNCTION
D15	D11	12-bit limit for the triggering threshold of undervoltage-alert detection. An alert for a given cell is issued when the cell voltage falls below this set threshold and the alert is not cleared until the cell voltage rises above the clear threshold. The undervoltage alert is updated on each new measurement scan of the cell voltages by comparing against the undervoltage threshold values. This alert-setting threshold is a critical minimum cell-voltage level.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

Table 27. UVTHRCLR—Undervoltage Clear Threshold Register Description (Address 0x1B)

BIT	NAME	FUNCTION
D15	D11	12-bit limit for the reset threshold of undervoltage-alert detection. An alert that is issued when the undervoltage set threshold is tripped by a cell voltage is not cleared until the voltage rises above this clearing threshold. The undervoltage alert is updated on each new measurement scan of the cell voltages by comparing against the threshold values. This alert-clearing threshold builds in digital hysteresis to the undervoltage detection.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

Table 28. MSMTCH—Cell Mismatch Threshold Register Description (Address 0x1C)

BIT	NAME	FUNCTION
D15	D11	12-bit threshold limit for mismatch alert. If: **MAXCELL - MINCELL > MSMTCH** then the ALRTMSMTCH alert bit in the STATUS register is set. If the MSMTCH threshold is set to 0xFFF0, no alert is possible; this immediately clears the alert status. For all other MSMTCH threshold value changes, the alert status does not change until after the next measurement scan.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

Table 29. AINOT—Auxiliary Analog Input Overtemperature Threshold Register Description (Address 0x1E)

PIN	NAME	FUNCTION
D15	D11	12-bit threshold limit for an undervoltage alert on the AUXIN1 and AUXIN2 inputs. When the auxiliary analog inputs are used with an NTC thermistor as part of the recommended circuit, this register can be used to store the overtemperature threshold. This threshold may also be used as a general undervoltage trip point for the auxiliary inputs. The ALRTTHOT bit in the STATUS register is set if: **AIN1 OR AIN0 < AINOT** The polarity of this comparison assumes that an NTC thermistor is used in the application circuit.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

Table 30. AINUT—Auxiliary Analog Input Undertemperature Threshold Register Description (Address 0x1F)

PIN	NAME	FUNCTION
D15	D11	12-bit threshold limit for an overvoltage alert on the AIN0 and AIN1 inputs. When the auxiliary analog inputs are used with an NTC thermistor as part of the recommended circuit, this register can be used to store the undertemperature threshold. This threshold may also be used as a general overvoltage trip point for the auxiliary inputs. The ALRTTCOLD bit in the STATUS register is set if: **AIN1 OR AIN2 > AINUT** The polarity of this comparison assumes that an NTC thermistor is used in the application circuit.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

Table 31. CELL$_N$ Data Register Description (Addresses 0x20 to 0x2B)

PIN	NAME	FUNCTION
D15	D11	12-bit ADC conversion result from CELL$_N$.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	Write ignored; read back 0.
D1	OVEN	Enable overvoltage alerts for this cell channel: Maps to the ALRTOV(N-1) bit.
D0	UVEN	Enable undervoltage alerts for this cell channel: Maps to the ALRTUV(N-1) bit.

Table 32. AIN1—Auxiliary Analog Input 1 Data Register Description (Address 0x40)

PIN	NAME	FUNCTION
D15	D11	12-bit ADC conversion result on the AUXIN1 channel.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	Write ignored; read back 0.
D1	COLDEN	Enable undertemperature or overvoltage alerts for this channel.
D0	HOTEN	Enable overtemperature or undervoltage alerts for this channel.

Table 33. AIN2—Auxiliary Analog Input 2 Data Register Description (Address 0x41)

PIN	NAME	FUNCTION
D15	D11	12-bit ADC conversion result on the AUXIN2 channel.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	Write ignored; read back 0.
D1	COLDEN	Enable undertemperature or overvoltage alerts for this channel.
D0	HOTEN	Enable overtemperature or undervoltage alerts for this channel.

Table 34. DIAG—Diagnostic Data Register Description (Address 0x44)

PIN	NAME	FUNCTION
D15	D11	12-bit ADC conversion result on the diagnostic data value. This diagnostic tests the tolerance of the reference, the stability of the internal regulator, and the open/short status of cell input C0. The converter delivers the data value based on the following formula: **DIAG = ((REF - C0) x 0.5)/VAA x 4096** The nominal value for normal operation is 5E1h with a tolerance of ±150 LSBs. The REF open case also has a special FMEA detector that has a separate alert, ALRTREF, in the FMEA register.
D14	D10	
D13	D9	
D12	D8	
D11	D7	
D10	D6	
D9	D5	
D8	D4	
D7	D3	
D6	D2	
D5	D1	
D4	D0	
D3	0	Write ignored; read back 0.
D2	0	
D1	0	
D0	0	

I^{2}C Interface

Overview

The MAX11068 uses an SMBus ladder I^{2}C physical interface with customized I^{2}C command protocol to communicate with the host system and from module to module. Each device contains two I^{2}C ports, one master and one slave. The slave port is the lower port, referenced to the chip ground, and communicates with the host master or the master from a device lower on the SMBus ladder. The upper port is a master port that is level shifted and referenced to GND$_U$. It drives communication with devices higher on the SMBus ladder and gathers information to be passed back toward the host. The two ports act together with the help of a digital controller to bridge two separate links of the SMBus ladder. Each link between master and slave of interconnected MAX11068 devices can be thought of as its own bus under the control of the master side device. A standard I^{2}C hardware master found in many microcontrollers or a master implemented with firmware and general-purpose I/O pins is all that is required to successfully implement the physical communication bus. This level-shifted dual-port scheme allows modules to be easily stacked without the need for costly and complex galvanic isolation of the communication lines while providing very-high-noise rejection.

I^{2}C Physical Interface Operation

The physical I^{2}C interface for each MAX11068 device consists of a master block and a slave block. The master block is level shifted and referenced to the GND$_U$ supply voltage. A digital controller manages each block and coordinates the passing of commands and data between the two as needed. The two standard I^{2}C interface pins for all ports are SCL for the serial data clock and SDA for the serial data line. Additional status pins used to complement the I^{2}C communication in the MAX11068 are the ground-referenced ALRM$_L$ output and the level-shifted ALRM$_U$ input. These pins act as an SMBus-laddered interrupt signal that the host can use to determine the health of the bus. To support the level-shifted I/O pins, a level-shifted supply, VDD$_U$, is generated by an internal charge pump and referenced to GND$_U$. This supply provides a pullup voltage to the level-shifted bus communication signals. Figure 28 shows the simplified view of the I^{2}C physical interface from the perspective of the first device in an SMBus ladder.

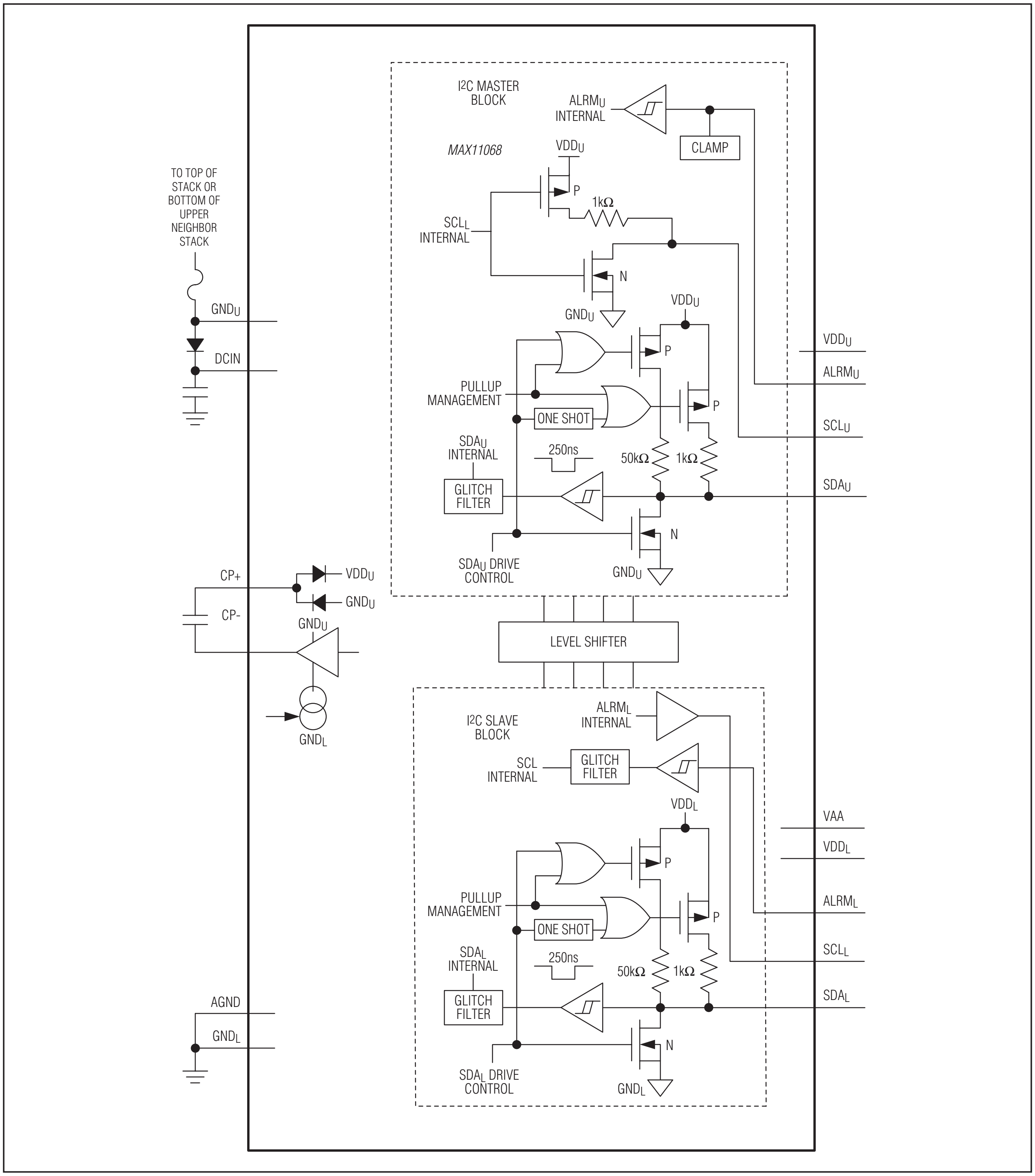


Figure 28. I^{2}C Physical Interface Block Diagram

Each port contains a bidirectional SDA pin with managed internal pullup drivers. The SCL pin for the lower slave port is an input only, while the upper port master SCL pin has a 1kΩ pullup driver. Glitch filters and Schmitt trigger buffers are present on the input signals to minimize communication errors. The alarm signal input is Schmitt trigger with a current and voltage-clamping circuit while the lower port alarm output is a push-pull driver. Each port is designed to operate in an AC- or DC-coupled bus configuration. All signal pins have a weak 150kΩ pullup to their respective VDD supply to establish the customary idle state of the I²C bus. The following operating description assumes the AC-coupled circuit shown in Figure 28.

Since the SDA signal path must be bidirectional, managing the handoff of roles between transmitting nodes and receiving nodes is critical to data integrity. At the same time, the bus must be able to drive a certain capacitive load size to maintain specified timing performance. To meet these requirements, a managed resistance pullup system with a strong pulldown driver is implemented in both the master and slave blocks. When the SDA pin for a given block is the driver of a signal edge on the line, it first connects both a 1kΩ resistor and a 50kΩ resistor from its VDD supply to SDA to initiate the active edge. This strong pullup provides extra drive strength initially to speed the charging of the parasitic capacitances connected to the SDA pin and is active for the time period $t_{ONE\text{-}SHOT}$, which is typically 250ns. A parameter, C_{1_TAU}, specifies the maximum capacitance that may be present on the SDA pin so that the SDA voltage level transitions to within 70% of its nominal value within the time period of the one-shot active edge. When the one-shot period is over, the 1kΩ resistor is disconnected and the 50kΩ pullup remains to complete the active edge transition. This weaker pullup continues to actively drive the line until the particular SDA pin is no longer in a transmitting state. During the acknowledge bit time, the SDA pin that had been receiving data is able to use its pulldown driver to overcome the 50kΩ pullup driven by the transmitting device and successfully acknowledge the transmission. Internal circuitry prevents the coupling capacitors from accumulating charge and causing a DC drift on the signals.

When the host or a device master drives the AC-coupled SCL line with a signal edge, the high-frequency edge passes to the slave side of the coupling capacitor where it is received at the SCL input pin. Since the 150kΩ passive pullup resistor value is large, the time constant of the pullup's effect during communication when paired with the typical 3.3nF AC-coupling capacitor is large compared to the specified range of the I²C clock period. Using resistor values lower than 150kΩ or changing the coupling-capacitor value could affect the margin of the bus timing specifications at some communication frequencies. Since the SCL signal is unidirectional, no internal pullup resistor manipulation for the driver circuit is necessary. As with the SDA pins, internal circuitry prevents the coupling capacitors from accumulating charge.

I²C Command Summary

The MAX11068 supports seven different commands. There are two main cycle formats, one for READALL and the other for the rest of the commands. Several commands require the host to send a PEC byte or for the chain to send a PEC byte to the host. This is an implementation of the SMBus PEC algorithm, which is a CRC-8 process where all bits in the packet are cycled through the CRC engine. Table 35 is the I²C command list.

Table 35. I²C Command List

FUNCTION	DESCRIPTION	PEC BYTE
HELLOALL	This command sets the device address of the first part in the chain. All other parts in the chain are then assigned an automatically incremented address as this command is forwarded from module to module. The HELLOALL command should be issued after any power cycle or shutdown event.	None
ROLLCALL	Reads 2 bytes from each device in the chain, which includes the address byte. When 0xFF is returned, the host has the addresses of all devices. The ROLLCALL command should be issued after the HELLOALL command.	None
SETLASTADDRESS	The host informs all devices of the device count determined by the ROLLCALL command so that each device can know when to expect and generate PEC bytes. The SETLASTADDRESS command should be issued after the ROLLCALL command.	Required from host
WRITEALL	Broadcasts a common command to all enabled devices in the chain.	Required from host
READALL	Reads the available data from the device register specified by the command code byte for each device in the chain.	Sent to host
WRITEDEVICE	Writes data only to a specified target device.	Required from host

I²C Communication Cycle Formats

The following cycle formats are used for the MAX11068 command set.

Write Word Format

START	DEVICE OR GLOBAL ADDRESS	WR	ACK	COMMAND CODE/ REGISTER ADDRESS	ACK	DATA LOW [7:0]	ACK	DATA HIGH [15:8]	ACK	STOP
	7 bits			8 bits		8 bits		8 bits		

ReadAll Format, Single Device

START	DEVICE OR GLOBAL ADDRESS	WR	ACK	COMMAND CODE/ REGISTER ADDRESS	ACK	SR	ADDRESS	RD	ACK	DATA LOW [7:0]	ACK	DATA HIGH [15:8]	NACK	STOP
	7 bits			8 bits			7 bits			8 bits		8 bits		

I²C Command Protocol Descriptions

Conventions

The following conventions are used in the description of the I²C command protocols.

Binary values are prefixed with the notation 0b, e.g., 0b11101000.

Hexadecimal values are prefixed by the notation 0x, e.g., 0xE8.

In the timing diagrams, standard I²C notations have been used:

- S represents a START condition (pulls SDA low while SCL is high).
- P represents a STOP condition (pulls SDA high while SCL is high).
- Sr represents a repeated START condition. This is identical to a START condition except that it has not followed a STOP condition.
- A represents a positive acknowledge (ACK). The data receiver drives the SDA line low.
- N represents a negative acknowledge (NACK). The data receiver drives the SDA line high.
- W represents the R/Wb bit set low for a write transaction.
- R represents the R/Wb bit set high for a read transaction.
- X represents a don't-care value for a data bit.
- N.C. represents an I²C link that is a no connect.

The diagrams also represent the direction of SDA by shading the data when the slave is the data source. For example, when the I²C master performs a write, it sends the data bits and receives the acknowledge bit. So, the data bits have a clear background and the acknowledge bit is shaded. When the I²C master performs a read, it receives the data bits and sends the acknowledge bit. So, the data bits have a shaded background and the acknowledge bit is clear.

Address Byte Encoding

All commands begin with an I²C address byte immediately following a START or repeated START condition. Each MAX11068 responds to the following bytes after a START condition:

- Broadcast address
- WRITEDEVICE command containing the device address
- HELLOALL command

The format for these bytes is shown in Table 36.

The broadcast address is an address value to which all enabled devices respond. This address is used for ROLLCALL, WRITEALL, and READALL commands. The broadcast address B[7:0] is programmable through the BRDCST bits of the BROADCAST ADDRESS register (address 0x0F), but B[0] is not used since it falls in the position of the I²C R/Wb bit. The default broadcast address is 0x40. The I²C general-call address 0x00 is not supported and the MAX11068 does not respond to messages sent to that address unless the BRDCST bits are set to this value.

The device address is unique to each part within the chain of devices. This address is used during HELLOALL and WRITEDEVICE commands, and is essential in determining which device is the last in the SMBus ladder. The HELLOALL command sets the address of all de-vices by initializing the address of the first device in the chain and autoincrementing the addresses of remaining devices up the chain. When the MAX11068 is not used on a dedicated I²C bus, the other devices on the bus should not be configured to use addresses with a 1 as the MSB. The broadcast address must also be chosen to avoid conflicts with the HELLOALL and WRITEDEVICE commands, as well as any other devices on the bus.

Table 36. I²C Address Byte Encoding

I²C ADDRESS BIT	7	6	5	4	3	2	1	R/Wb
Broadcast Address (default value)	B7 0	B6 1	B5 0	B4 0	B3 0	B2 0	B1 0	1/0 1/0
HELLOALL	1	1	A0	A1	A2	A3	A4	0
WRITEDEVICE	1	0	A0	A1	A2	A3	A4	0

HELLOALL Command

The purpose of the HELLOALL command is to initialize the device stack and assign a unique device address to each MAX11068 in the SMBus ladder. It should be issued after any power cycle or shutdown event to reconfigure all addresses. The HELLOALL command is a standard I²C address byte where the first 2 bits must be 1s, the next 5 bits specify the desired address of the first MAX11068 device in the SMBus ladder, and the last bit is the standard I²C R/Wb bit. This bit should always be 0 for this command. The starting address A[0:4] is specified least significant bit first. Since the device address consists of 5 bits, it has a maximum value of 32, while the maximum number of SMBus-laddered devices is 31. The device address A[0:4] wraps to 0 if it exceeds the maximum value of 0x1F during a HELLOALL command. The WRITEDEVICE command, which uses the device address, however, does not properly communicate with devices whose address is less than that of device 1. Therefore, the starting address used by the HELLOALL command should always be set such that the last device's address A[0:4] is no greater than 0x1F. When using the maximum number of devices, the address A[0:4] of the first device must be initialized to 0x00 or 0x01 to meet this requirement.

When the HELLOALL command is first issued by the host, the address specified is stored to the A[0:4] bits of the ADDRESS register (address 0x01) in the first SMBus ladder device. The command is then forwarded to the next device in the chain with the A[0:4] bits of the address byte incremented by 1 LSB. This continues for each active device in the SMBus ladder. A typical starting address is 0x01, which in this example would make the HELLOALL address byte value 0b1110000 = 0xE0. Figure 29 is the I²C address byte for the HELLOALL command and Figure 30 shows the HELLOALL command SMBus ladder sequences with four modules.

In the case of a four-module SMBus ladder, the fourth MAX11068 upper I²C port is not connected to anything. Therefore, it receives a NACK when it transmits the HELLOALL command. This sets the ALRTACK status bit, which should be cleared by the host.

ROLLCALL Command

The ROLLCALL command is used to determine the number of devices in the stack. It should be issued after the HELLOALL command following any power cycle or shutdown event. The format for this command is similar to the READALL command except that 0xFF is returned in place of the PEC and data check bytes. The ROLLCALL command is always a read of the ADDRESS register (address 0x01). This register cannot be read in any other way. Figure 31 shows the I²C communication sequence for the ROLLCALL command as viewed by the host controller and Figure 32 is the ROLLCALL command SMBus ladder sequences with two modules.

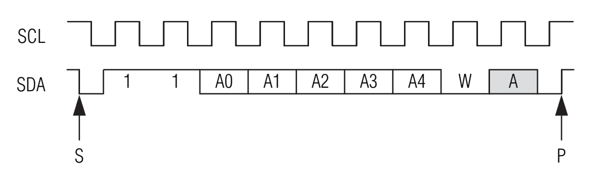
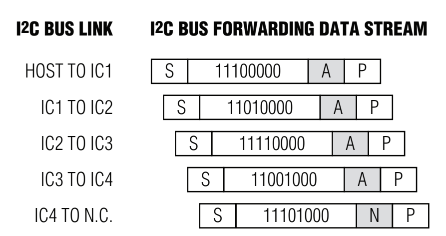
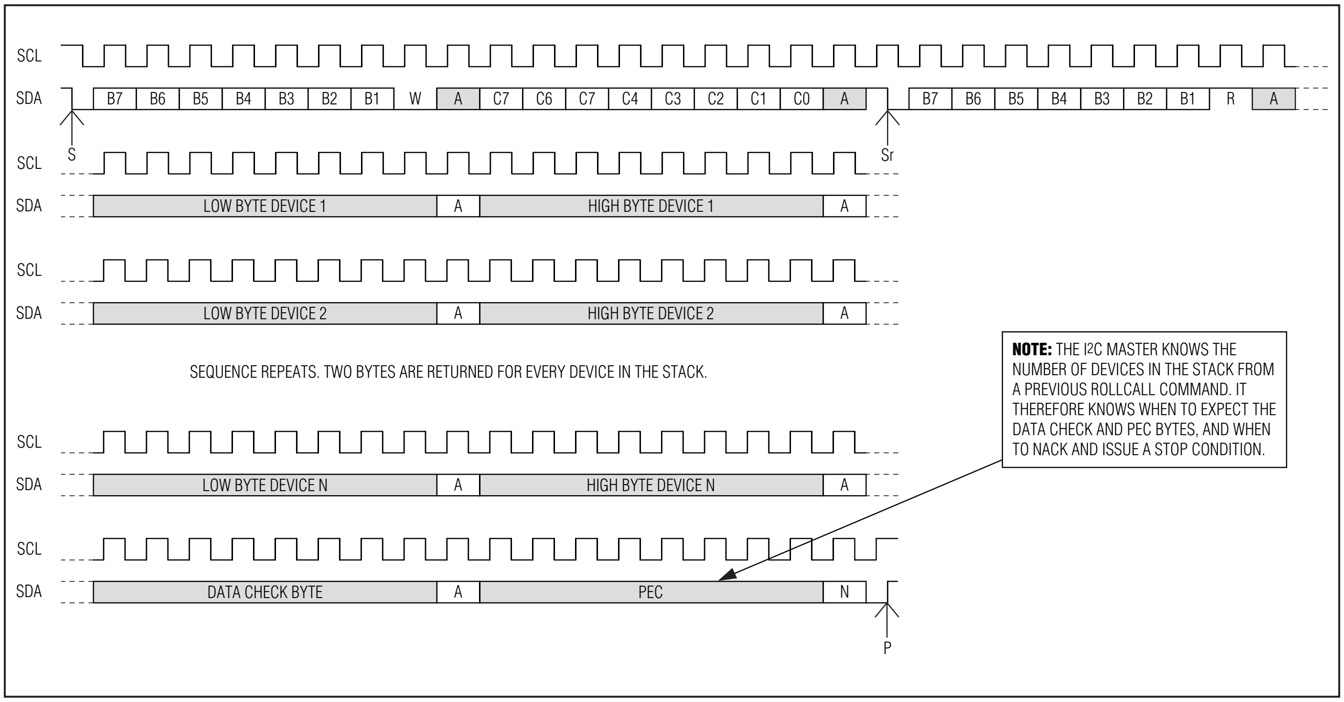


Figure 29. I²C Address Byte for the HELLOALL Command



NOTE: SHOWN IS THE 1µs FOWARDING DELAY FROM ONE BUS LINK LEVEL TO THE NEXT. NOT DRAWN TO SCALE. STARTING ADDRESS OF A[4:0] = 0x01.

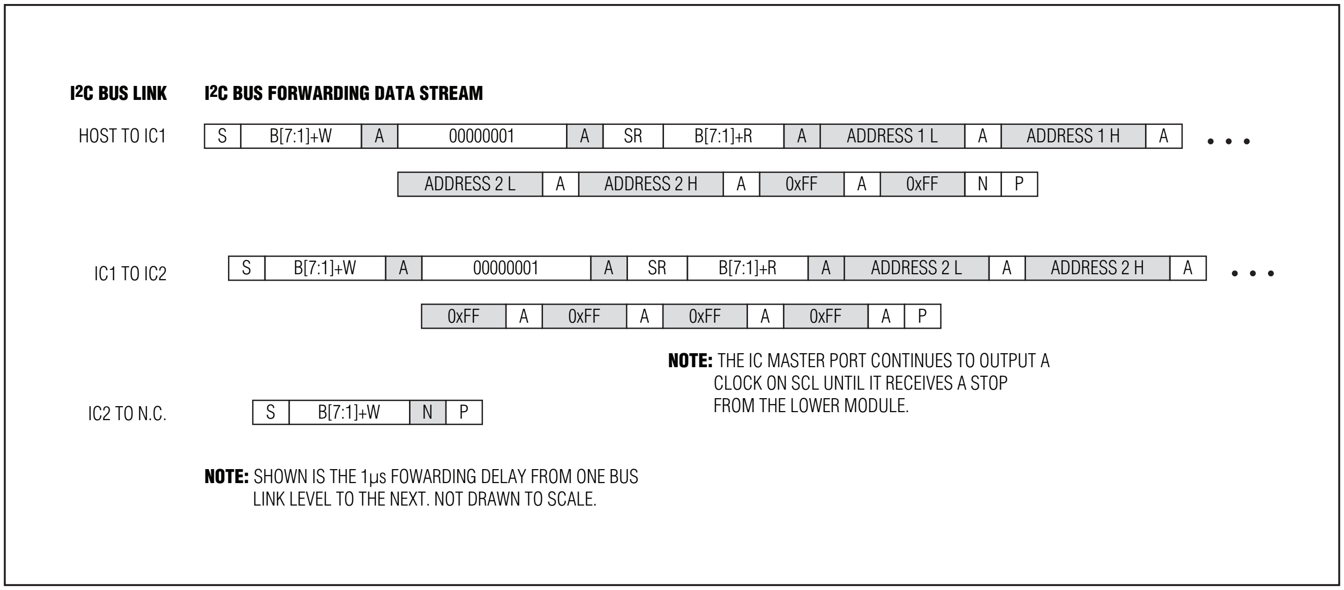
Figure 30. HELLOALL Command SMBus Ladder Sequences with Four Modules



SEQUENCE REPEATS. TWO BYTES ARE RETURNED FOR EVERY DEVICE IN THE STACK.

NOTE: THE I2C MASTER KNOWS THE NUMBER OF DEVICES IN THE STACK FROM A PREVIOUS ROLLCALL COMMAND. IT THEREFORE KNOWS WHEN TO EXPECT THE DATA CHECK AND PEC BYTES, AND WHEN TO NACK AND ISSUE A STOP CONDITION.

Figure 31. I²C Communication Sequence for the ROLLCALL Command as Seen by the Host



NOTE: THE IC MASTER PORT CONTINUES TO OUTPUT A CLOCK ON SCL UNTIL IT RECEIVES A STOP FROM THE LOWER MODULE.

NOTE: SHOWN IS THE 1µs FOWARDING DELAY FROM ONE BUS LINK LEVEL TO THE NEXT. NOT DRAWN TO SCALE.

Figure 32. ROLLCALL Command SMBus Ladder Sequences with Two Modules

The ROLLCALL command is formatted like the READALL cycle format. First, the broadcast address is sent on the bus as an I^{2}C address byte with the R/Wb bit configured as a write. Next, the command 0x01 for the ADDRESS register is sent. This address is always the target of the ROLLCALL command. Following the broadcast address and command byte, a repeated start is performed. Next, the host sends another broadcast address byte with the last bit set to 1 for an I^{2}C read. All command bytes are forwarded up the SMBus ladder. After receiving the broadcast address byte for the read, each device in the chain starting with the first device responds by sending both bytes of their ADDRESS registers. When each device is done sending its own data, it passes the data of the device above it in the chain. The SCL signal provides a clock to all devices in the chain until the host issues a stop event. Therefore, when devices no longer have valid register data to forward, they will continue to forward bytes consisting of 0xFF since the SDA lines are pulled to a logic-high level. When the host receives 2 bytes of 0xFF, it should recognize that no more devices are present and send the NACK/stop sequence. The stop propagates up the SMBus ladder to halt the transfer of data. The host is then able to examine all the bytes received and determine the number of valid devices that are connected, in addition to the address of the last device. If a device is connected to the chain but not powered, its data is 0x0000 since the SDA line is not pulled up by the VDD supplies. This allows the host processor to determine that a device is present, but not communicating properly or is faulty. Because of the way in which data is shifted from the last device in the chain back to the first device and then to the host, the bus forwarding delay of the ROLLCALL command is masked and no delay is perceived by the host once it begins receiving data from device 1.

As an example, if a HELLOALL command was issued previously with a starting address of 0x01, the first device returns in response to the ROLLCALL command the device address 0x01 encoded as 0b10100000 = 0xA0. The second device returns a device address of 0x02, which is encoded 0b10010000 = 0x90 and so on. The last address byte is indeterminate during readback with this command, and should not be relied upon.

SETLASTADDRESS Command

This command is used to tell each MAX11068 in an SMBus ladder which device address is the last one. Each device must know this information to properly place the PEC byte in the data stream during relevant communication operations. The I^{2}C master establishes the last device identity by using the ROLLCALL command, which should always precede SETLASTADDRESS. Once the last device address is known, the host initiates the SETLASTADDRESS command to write this information to the LA[4:0] bits of the ADDRESS register (address 0x01). As with all data bytes in the I^{2}C stream, the last address byte is encoded MSB first. Figure 33 shows the I^{2}C communication sequence for the SETLASTADDRESS command. Figure 34 shows the SETLASTADDRESS command SMBus ladder sequences with four modules.

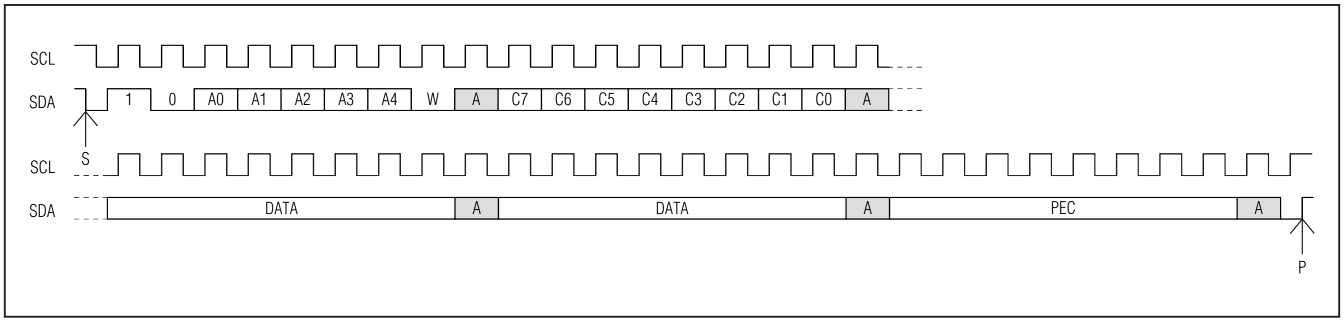


Figure 33. I^{2}C Communication Sequence for the SETLASTADDRESS Command

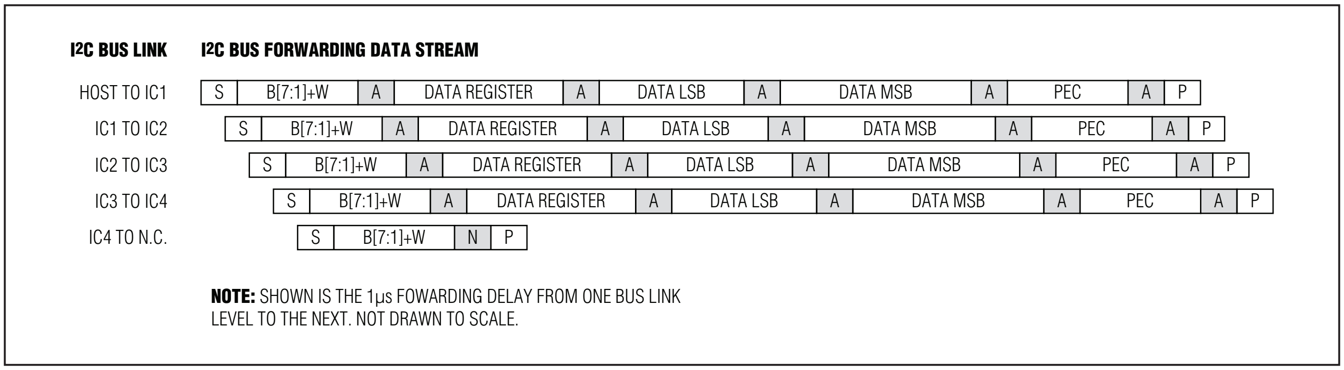


Figure 34. SETLASTADDRESS Command SMBus Ladder Sequences with Four Modules

The communication sequence for SETLASTADDRESS follows the write word format. First, the broadcast address is sent on the bus as an I^{2}C address byte with the R/Wb bit configured as a write. Next, the command code byte 0x01 for the ADDRESS register location is sent. This address is always the target of the SETLASTADDRESS command. Next, the 2 data bytes to be written to each device are sent on the bus. Only the second byte containing the LA[4:0] bit information is written into each device's ADDRESS register for the SETLASTADDRESS command. Therefore, the first data byte may have any value. After the second data byte is sent, the PEC byte, which is calculated from the first 4 bytes, is transmitted and then a stop event from the host should end the communication sequence.

For example, if the host determined by use of the ROLLCALL command that the device address byte (D[7:0] of the ADDRESS register) for the last device in the chain was 0x84 = 0b10000100, then the device address bits (packed LSB first) A[0:4] are 0b00010. This value, noting proper orientation of the LSB and MSB, is what must be written to the LA[4:0] bits of the ADDRESS register in all connected devices. To construct the last address byte, which consists of bits D[15:8] in the ADDRESS register, start with 3 zeros, and append the A[4:0] data (oriented with the MSB first), which results in 0b00001000 = 0x08. This is the byte value for this example that would be written to D[15:8] of the ADDRESS register using the SETLASTADDRESS command.

Once the last device has been configured with the last address bit data, that device acts as the source of the alarm heartbeat. All other devices relay that heartbeat, or any alarm conditions that may be present, down the chain to the host using the ALRM_L and ALRM_U pins.

WRITEALL Command

The WRITEALL command allows a given value to be written to a certain register in all active MAX11068 devices at the same time (neglecting communication delays). Since most configuration information is common to all the devices, this command allows faster setup than writing to each device individually. First, the broadcast address is sent on the bus as an I^{2}C address byte with the R/Wb bit configured as a write. Next, the command byte is sent with an MSB first value corresponding to the register address to which the data byte is written. The low data byte and then the upper data byte follow the command byte. Finally, the PEC is sent and a stop event ends the communication sequence. Figure 35 shows the I²C communication sequence for the WRITEALL command. Figure 36 shows the WRITEALL command SMBus ladder sequences with four modules.

The PEC byte must be supplied with the WRITEALL command. It is calculated from the first 4 bytes of the command. If any MAX11068 device does not receive a packet with a consistent PEC, it will not perform the command or the register writes. It will also generate a PEC alert in the status register, and this may (optionally) cause the suspension of the alarm heartbeat. Due to bus noise, it is possible for some devices to receive a consistent PEC while others may not. In this case, an enabled PEC alarm can signal the overall problem while a READALL command can check the status registers to reveal which specific devices failed to correctly receive the command. When using the WRITEALL command to change the broadcast register, it is important to verify that the command was executed by all known devices. This can be accomplished by enabling the PEC alarm and verifying that the WRITEALL was successful, or by performing a READALL after the WRITEALL and making sure a response was received from all expected devices. If a response was not received from all devices, steps should be taken to rewrite the new broadcast address or determine if a device has been removed from the stack.

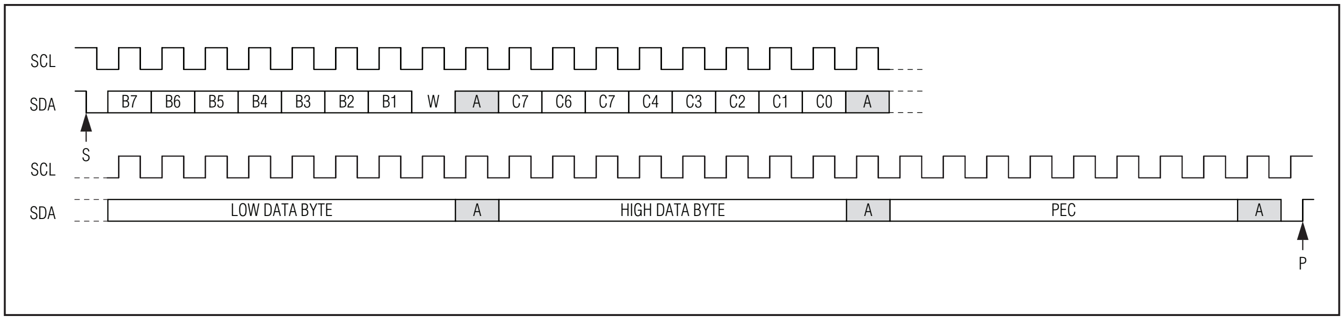


Figure 35. I²C Communication Sequence for the WRITEALL Command

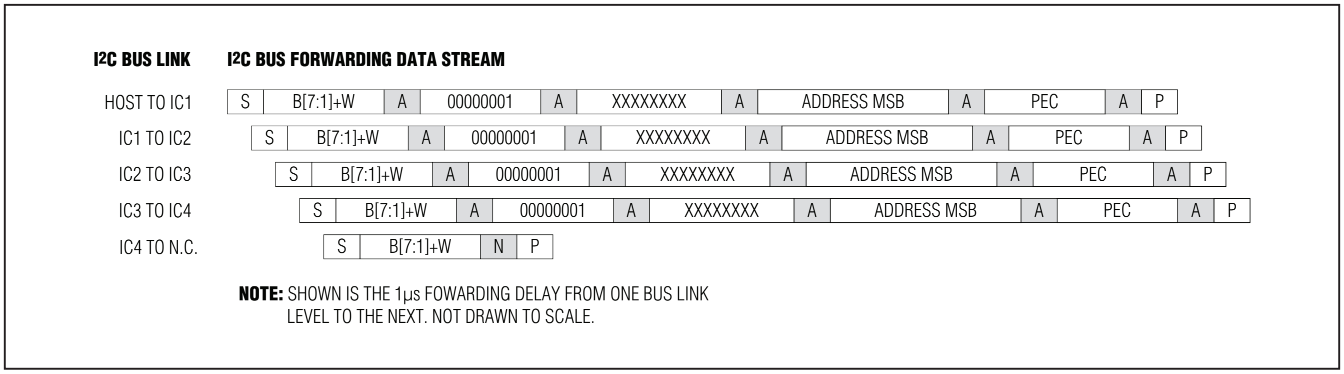


Figure 36. WRITEALL Command SMBus Ladder Sequences with Four Modules

WRITEDEVICE Command

This command allows a register in a specific device within the SMBus ladder to be written. It is similar to the WRITEALL command except that the I²C address byte contains the fixed MSbs 0b10, followed by the device address A[0:4] encoded LSB first instead of the broadcast address. Once again, a consistent PEC must be received for the command to be executed by the device. The PEC alert is set if the command was aborted. The command sequence is forwarded up the SMBus ladder until the device address sent with the command matches or exceeds the receiving device's address. If the addresses match, the device executes the command. If the command address exceeds the device's address, the command forwarding stops. This can happen if the device addresses assigned during the HELLOALL command exceeded 0x1F, or if the device addressed by the WRITEDEVICE command is no longer active. Figure 37 shows the I²C communication sequence for the WRITEDEVICE command and Figure 38 shows the WRITEDEVICE command SMBus-laddered sequences where the device address matches IC3.

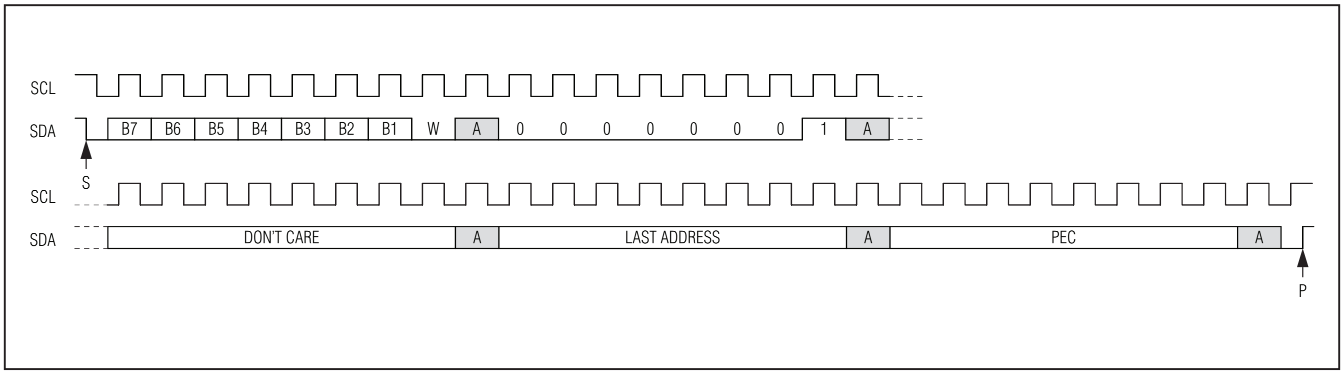


Figure 37. I²C Communication Sequence for the WRITEDEVICE Command

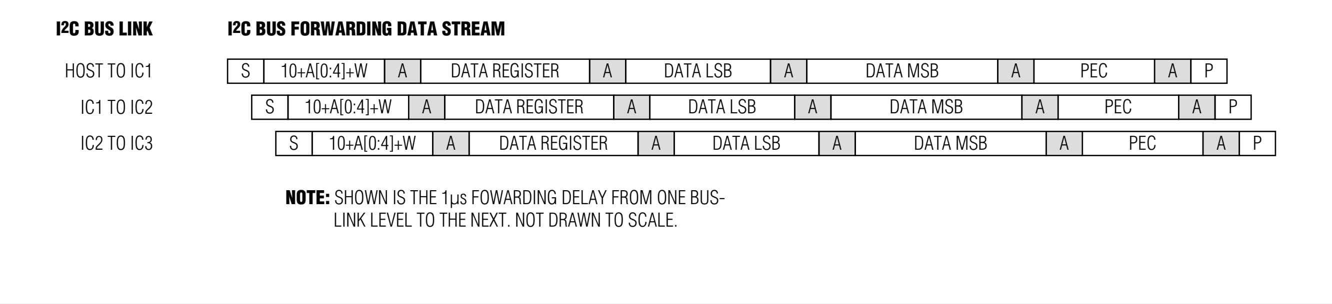


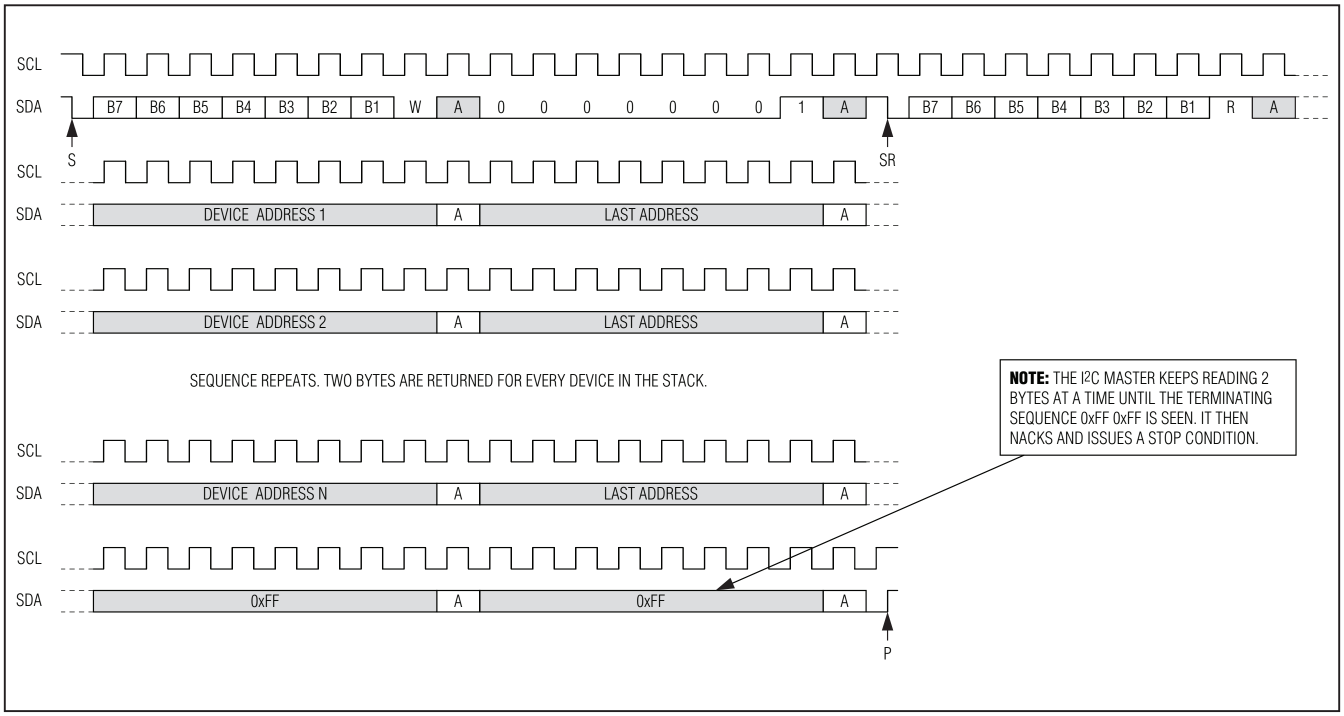
Figure 38. WRITEDEVICE Command SMBus Ladder Sequences Where the Device Address Matches IC3

READALL Command

This command is used to retrieve register information from the stack of devices and it is the only way to read register values (except for the ADDRESS register, which is handled by the ROLLCALL command). After sending the I^{2}C address byte containing the broadcast address with the R/Wb bit low and then the command byte, the READALL format requires a repeated start to change the direction of data flow. Following the repeated start, another broadcast address byte is sent with the R/Wb bit, this time set for a read. This starts the flow of device data back to the host. The data stream as viewed at the lower port interface of the first device in the stack appears as shown in Figure 39.

After the first device receives the READALL command, it begins to send the requested register data, low byte first, on the bus toward the host. Approximately 1µs later, the next device in the SMBus ladder receives the READALL command and sends its data to the upper port of the first device. The first device holds these bits until it is done sending its own data and receives an acknowledge bit, at which time it forwards the data from the second device. This process continues for each MAX11068 in the SMBus ladder. Because of the way the data is shifted from each device back toward the host, the module-to-module communication delays are effectively masked and the host sees a continuous stream of data once the first device receives the READALL command.

After the last device sends its data, it creates a data check byte and PEC byte since it knows it is the last device in the chain. The PEC byte generated by the MAX11068 uses a CRC-8 algorithm, which is what the host should use on the sent data. Each link of the SMBus ladder contains a unique data sequence. Therefore, each READALL communication between modules has a different PEC byte. The data check byte informs the host whether the entire communication succeeded by passing a flag containing the PEC error status of the entire READALL command down the chain. This makes it easier for the host controller to determine if the READALL command was successful without having to check the ALRTPEC status of each module in the



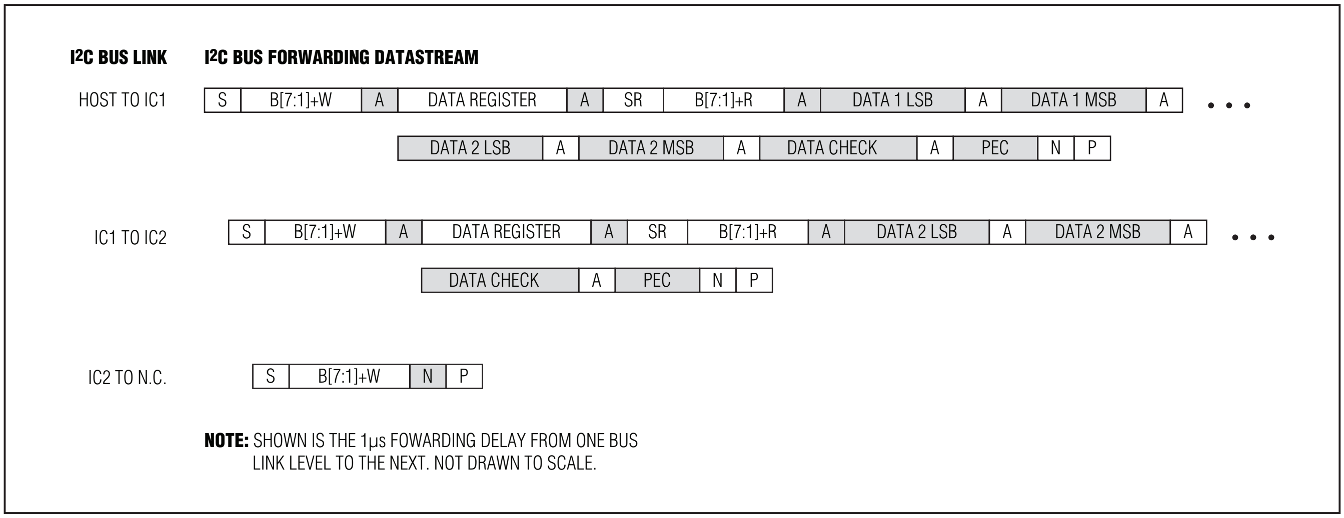
SEQUENCE REPEATS. TWO BYTES ARE RETURNED FOR EVERY DEVICE IN THE STACK.

NOTE: THE I^{2}C MASTER KEEPS READING 2 BYTES AT A TIME UNTIL THE TERMINATING SEQUENCE 0xFF 0xFF IS SEEN. IT THEN NACKS AND ISSUES A STOP CONDITION.

Figure 39. I^{2}C Communication Sequence for the ROLLCALL Command as Viewed by the Host Controller

SMBus ladder. Host processor efficiency is improved as a result. In addition, an ALRTPEC condition can be configured to generate an alarm on the alarm bus by setting the ALRMPEC bit. This alarm can be monitored by the host and provides the same information as the ALRM bit of the data check byte. The benefit of the PECERR bit is that it provides a specific ALRTPEC flag to the host as part of each READALL transaction. The data included in the calculation is the first address byte, the command byte, the address byte following the repeated start, all data sent on the bus by the device calculating the PEC, and the data check byte. For the last device, the PEC is calculated from the 3 bytes of the READALL command, the 2 data bytes that it sent, and the data check byte. The data check byte is defined in Table 37.

The MSB, ALRM, is a flag indicating whether the device sending the data check byte or a device above it in the SMBus ladder is in any alarm condition with the ALRM pin pulled high. For the data check byte sent by the last device in the chain, the ALRM bit is set according to the alarm status of the device while the PECERR bit is a 0, since this is the last device. When the next-to-last device receives the data check byte from the last device, it logically ORs this byte with its own alarm status and whether its upper port received a valid PEC byte from the last device. It sends out the data check byte after the last data byte (high byte from the last device) is sent. The LSB, PECERR, is a flag indicating whether the device sending the data check byte, or a device in a module above it, has an active ALRTPEC flag. When a device receives an invalid PEC byte at its upper I²C port, it sets PECERR, as well as ALRTPEC to 1 before sending the data check byte down the SMBus ladder. The next-to-last device recalculates the PEC byte based on the same READALL command bytes as the last device, plus all 4 data bytes belonging to the last two devices and the updated data check byte. The processing of the data check and PEC bytes continues as all information is passed from the last device in the chain to the first device. When the first device has sent all data bits, it appends the processed data check byte as each of the devices before it has done. The PEC byte is then appended having been calculated using all bytes shown in Figure 40. Any error in the process that causes an invalid PEC does not terminate the transaction. Since each intermediate device recalculates the PEC, the host may receive a valid PEC byte for invalid data, but the data check byte shows that a PEC error has occurred along the way. In that case, the host should determine where the error occurred and take appropriate actions. As mentioned, the overall data stream appears to the host as it is shown in Figure 40. In the transactions between intermediate modules, the data stream is similar except that it contains only the data bytes from itself and the modules above it. Since the module-to-module communication delay is much less than one I²C clock, and the clock itself is also delayed, there is no apparent module-to-module delay observed by the host controller as the real delay is masked in the process of shifting the data back to the host. A combination of the PEC and data check byte approaches can ensure a very high probability of transactional integrity for the READALL command.



NOTE: SHOWN IS THE 1µs FOWARDING DELAY FROM ONE BUS LINK LEVEL TO THE NEXT. NOT DRAWN TO SCALE.

Figure 40. READALL Command SMBus Ladder Sequences with Two Modules

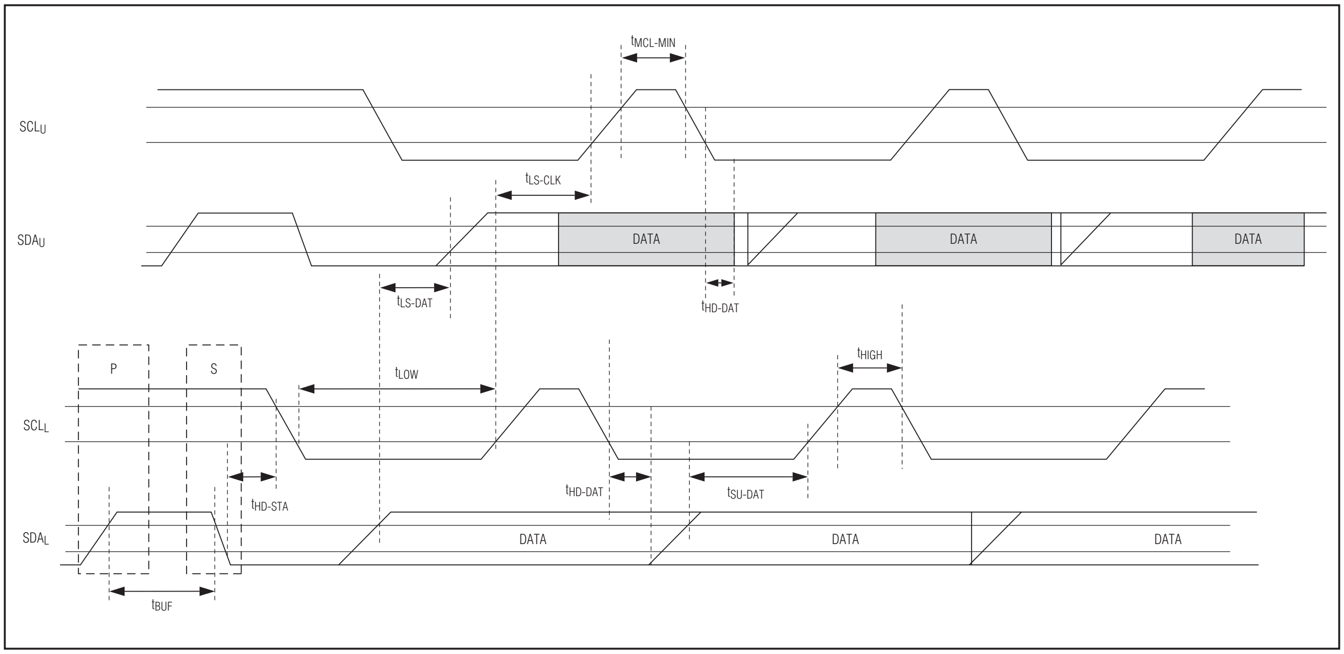


Figure 41. I^2C Lower and Upper Port Timing Diagrams

I^2C Port Timing Diagrams

Figure 41 shows the I^2C lower and upper port timing diagrams.

I^2C Functional Description

Autoaddressing

The HELLOALL command automatically assigns each device a unique address. This address can be used during a WRITEDEVICE command to write to only one selected device in the SMBus ladder, and is also read during the ROLLCALL command to identify all the unique active devices present on the bus. When all the device addresses are known, the last device in the chain can be identified and made known to all ports. It is important for each node and the host to know the relationship of devices that make up the SMBus ladder so that the PEC byte used in some command protocols can be properly located and calculated.

The device address of the first device in the SMBus ladder stack is specified with the HELLOALL command. This address is incremented by 1 before being sent to each successive downstream device. The maximum device address is 0x1Fh and the address counter wraps to 0 if the starting address was set too high for the number of devices in the chain. The SMBus-laddered devices only forward WRITEDEVICE commands that have a higher device address than their own. So, some devices are not addressable if the addresses A[0:4] written by HELLOALL are allowed to wrap past 0x1Fh.

Pack Insertion and Removal

When a pack is removed or inserted, the SMBus ladder must be reconfigured. The HELLOALL, ROLLCALL, and SETLASTADDRESS sequence should be used to reinitialize the device addresses and the address of the last device.

Communication Timeout

If the SCL_U input remains high or low for longer than 28ms, then any transaction is aborted and the device behaves as if it observed a STOP condition. The host can ensure that all devices are in a “ready-to-communicate” state by remaining idle for longer than 28ms.

Interface Speed

For optimal data transfer, the host microcontroller should make extensive use of the WRITEALL and READALL commands. One READALL or ROLLCALL command consumes the following amount of time based on the number of bits in the command protocol and the number of devices in the SMBus ladder:

$$t_{READALL} = (5 \times 8\text{ bits} + 5\text{ bits} + 3\text{ bits}) \times t_{SCL} + N_{MODULES} \times (16\text{ bits} + 2\text{ bits}) \times t_{SCL}$$

Table 37. Data Check Byte Definition

BIT	NAME	DESCRIPTION
7	ALRM	Set if the device is in an alarm condition, meaning the ALRML pin is high.
6	0	Unused, read as 0.
5	0	Unused, read as 0.
4	0	Unused, read as 0.
3	0	Unused, read as 0.
2	0	Unused, read as 0.
1	0	Unused, read as 0.
0	PECERR	During a READALL command, the slave returns PECERR = 0 if the master received a valid PEC. The slave returns PECERR = 1 if the master received an invalid PEC or the master received PECERR = 1. In this way, the system can verify communication not only one layer at a time, but also across all layers.

For 20 modules with a 200kbps I²C master data rate, it takes approximately 2.0ms to perform a READALL or ROLLCALL command for one register. Since there are 16 frequently read registers, it would take 32ms to perform a complete read of all devices for those registers. If an additional nine configuration registers are included, then 50ms are required. A 100kbps I²C master would be fast enough to perform this task in a reasonable amount of time.

WRITEALL consumes the following amount of time based on the number of bits in the command protocol, and the number of modules in the SMBus ladder:

$$\begin{aligned} t_{\text{WRITEALL}} &= (5 \times 8\text{ bits} + 5\text{ bits} + 2\text{ bits}) \times t_{\text{SCL}} \\ &+ (N_{\text{MODULES}} - 1) \times t_{\text{LEVEL-SHIFT-DELAY}} \end{aligned}$$

For 20 modules with a 200kbps I²C master data rate, this is approximately 250μs to perform a WRITEALL command for one register.

Packet-Error Checking (PEC)

The MAX11068 uses the SMBus PEC mechanism for maintaining data integrity. PEC verifies stage-to-stage communication both in the write and read directions.

During any write transaction, a device does not execute the write command internally unless the PEC is received successfully by the lower port. The host can easily ignore the PEC byte from a READALL command if the host does not intend to support PEC for read transactions. The only verification of a successful write transaction that the host receives is through the ACK bit following the PEC byte returned from the first device in the SMBus ladder. This bit indicates whether the first device received a valid write command. The success of the write command further up the chain is unknown to the host. If verification is critical, the host should follow up any write command with a READALL to verify the write by checking the register that was updated or the ALRTPEC bit of the STATUS register. The PEC alert may also be enabled to trigger an alarm through the ALRMPEC bit of the ADCCFG register (address 0x08). If no alarms are present following the write command, the host can infer that the write command was successful to all attached devices.

To support PEC, the host must implement a CRC-8 algorithm to perform calculations necessary for the PEC byte. The CRC-8 polynomial is:

$$C(x) = x^8 + x^2 + x + 1$$

All bytes including addresses, command codes, data, and for READALL, the data check byte should be processed by the CRC-8 algorithm as input bytes. START, repeated START, STOP, and ACK/NACK bits are not included in the calculation. The bits should be processed in the order they are received with MSB first. The logic implementation can be described as follows. First, the CRC is initialized to zero for a new calculation. For each input byte, the byte is first XORed with the CRC value. This byte is called the remainder. The remainder is left shifted by 1 bit and is sent to a mux as itself or XORed with the 8 least significant bits of the polynomial representation. The bit lost in the left-shift operation is able to be ignored because either it is a zero, or if it is a 1, it would be XORed with the most significant bit of the polynomial representation to yield a 0. Therefore, only an 8-bit pipeline is shown for all parts of the circuit. The MSB of the remainder controls a mux to select which operation is performed on the left-shifted version of the remainder byte. Once the remainder is operated on, it is latched and fed back to the input of the shift register through another mux. This is repeated until eight left shifts have occurred. After eight left-shift operations have been processed, the process is repeated on the next input byte using the working CRC value, which is the remainder following the left-shift operations. After all input bytes have been processed, the CRC output byte is the final result. Figure 42 shows a pseudo-code algorithm for the CRC-8 logic that can be used in a software or firmware implementation.

For write commands that require a PEC byte, the host should perform this calculation on the byte sequence that is transmitted. In applications where processing time is extremely critical, it is possible to precalculate the CRC value for the first few bytes of common commands, or sometimes even for full commands, and store these as constants. Then, when those commands are used, the microcontroller can use the stored CRC value for the precalculated portion of the message as an initial value and only calculate the portion of a message that may have changed in real time. This can save some processing time, although the PEC algorithm is designed to require a relatively small amount of processing resources in most cases. For a READALL command, the host should store the bytes of the received data stream, perform the PEC calculation on the relevant bytes, and compare the results to the received PEC byte. The PEC may also be calculated as each byte is received instead of waiting for the entire message to arrive by storing the running CRC value and passing it to the PEC calculation function for each new byte.

Example PEC Calculation

Figure 43 shows a typical WRITEALL command that is being sent by the host controller for which the PEC byte must be calculated.

```
Function PEC_Calculation(ByteList(), NumberOfBytes, CRCByte)
{
  //CRCByte is typically initialized to 0 for each ByteList.  If processing time
  //must be conserved, it is possible to precalculate the CRCByte value
  //for a known set of bytes at the beginning of a message.  Then, this
  //CRCByte value for the partial ByteList may be passed into the function
  //as the initial value along with the remaining bytes of the message
  //resulting in less computation steps.

  //Loop once for each byte in the ByteList
  For Counter1 = 0 to (NumberOfBytes –1)
  (
    //Bitwise XOR the current CRC value with the ByteList byte
    Remainder = CRCByte XOR ByteList(Counter1)

    //Process each of the 8 Remainder bits
    For Counter2 = 8 To 1 Step -1
    (
      //Determine if MSB = 1 prior to left shift
      If (Remainder And &H80) = &H80 Then
        //When MSB = 1, left shift and XOR with 8 lsbs of the polynomial
        Remainder = ((Remainder * 2) XOR &H7)
      Else
        //When MSB = 0, left shift 1 bit
        Remainder = (Remainder * 2)
      End If

      //Truncate the CRC value to 8 bits
      Remainder = Remainder And &HFF

      //Proceed to the next Remainder bit
      Next Counter2
    )

    CRCByte = Remainder

    //Operate on the next data byte in the ByteList
    Next Counter1
  )

  Return CRCByte
}
```

Figure 42. Example Pseudo-Code Algorithm for a CRC-8 PEC Calculation

Figure 43 shows 4 bytes preceding the transmission of the PEC byte. The first is the broadcast address, which is assumed to be the default of 0x40. The next byte 0x09 is the register address corresponding to the CELLEN register that is written. The last 2 bytes are the new values of the register with the LSB first. The value of 0x03FF that is written corresponds to enabling the first 10 cells for measurement. These 4 bytes shown above represent all bits included in the PEC byte calculation, and would comprise the ByteList() array from the previous pseudo-code algorithm. Applying the bytes 0x40, 0x09, 0xFF, and 0x03 in sequence to the CRC algorithm yields a final CRC result of 0x7F, which would be the value of the PEC byte that the host should send immediately following the data MSB.

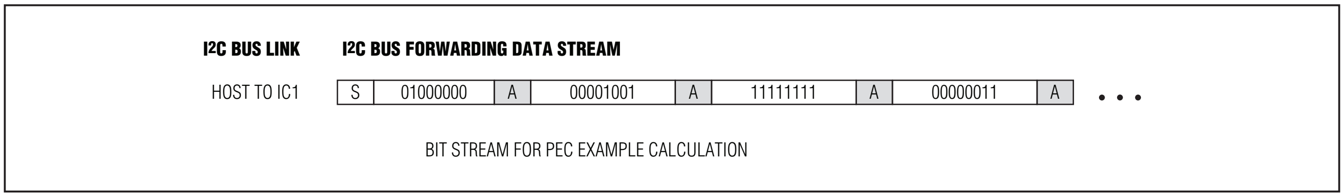


Figure 43. Example WRITEALL Bit Stream Prior to PEC Transmission

Power-On-Reset (POR) Event

A VAA voltage below the POR threshold results in an internal device reset. In this state, the charge pump is disabled, as well as the digital logic. Therefore, after VAA and VDD$_U$ have decayed below the power-on reset levels, I^{2}C communication is ignored and is not forwarded. In some cases, a parasitic power path may exist to VDD$_L$, and therefore VAA, through communication pullup resistors or logic signals from the host. These paths typically supply VDD$_L$ at one diode drop below the pullup level. As long as the pullup level is no more than one diode drop above the POR threshold, the entire device, including the digital logic remains in reset. Supplying VAA or VDD$_L$ with a power source above the reset threshold can result in active operation, even though the regulator may be disabled. When the POR is not active and VDD$_U$ and VDD$_L$ are valid, communication proceeds as normal.

Alert and Alarm Status Functions

The MAX11068 offers a comprehensive system to inform the host controller of the device's status. This is done with status alerts and status alarms. Status alerts are flag bits reporting various monitoring functions of the device. Alerts can be divided into three main groups. Cell monitoring alerts are flags that report conditions related to the cell measurement. They include:

- Cell undervoltage threshold crossed (UVTHRSET)
- Cell overvoltage threshold crossed (OVTHRSET)
- Cell voltage mismatch threshold crossed (MSMTCH)
- Auxiliary channel temperature measurement threshold crossed (AINOT, AINUT)

The second group of alert flags are communication errors. These flags report conditions related to the functioning of the SMBus ladder. They include:

- Packet error checking (ALRTPEC)
- Acknowledge error (ALRTACK)

The last group of alerts report operational failures of blocks of the IC. These flags aid in detecting conditions that signal if the device is operating correctly. They include:

- Reset status (RSTSTAT)
- Charge-pump failure (ALRTCPUV)
- Heartbeat signal out of specification (ALRTHBEAT)
- Voltage reference failure (ALRTREF)
- Lower +3.3V supply failure (ALRTVDDL)
- Lower GND failure (ALRTGNDL)

These alerts are activated when the configured thresholds are violated for a particular monitored condition or a particular function did not execute as expected. Status alerts are indicated by individual flag bits in various registers and must be read through the communication bus and processed by the host controller.

Status alarms are indicated using the alarm ladder bus comprising the ALRM$_L$ and ALRM$_U$ ports. An alarm is the result of an active alert that has been enabled to trigger an alarm. By monitoring the alarm bus with the system controller, the controller has nearly instant visibility of critical status conditions. Normally, this alarm bus carries a 16.384kHz heartbeat signal from the top device in the SMBus ladder to the bottom device. When an alarm is activated in a device, the alarming device pulls the alarm bus to logic high and interrupts the flow of the heartbeat signal. In this way, the alarm function acts as a high-priority interrupt signal to the host controller for critical events.

The topmost device in an SMBus ladder stackup is responsible for generating the heartbeat signal when it is not in an active alarm state and after the RSTSTAT bit has been cleared. The last device in the stack recognizes itself as the top module when the last address bits of the ADDRESS register (address 0x01) match its own device address. When this condition is true, usually following the SETLASTADDRESS command, and the RSTSTAT bit is clear, the top device generates the heartbeat signal. This signal is propagated down the alarm bus and is only stopped if a device replaces it with an active alarm signal. The system controller should monitor the ALRM_U of the lowest device in the SMBus ladder to determine whether an active alarm exists. The controller can then read the status of the SMBus ladder to pinpoint the location of the alerts that triggered the alarm. The heartbeat signal propagated down the SMBUs ladder is received and monitored by the upper port ALRM_U pin according to Figure 44.

Some alerts may be configured to trigger an alarm condition by using their alarm mask bits. This allows the application to choose which alerts should generate an alarm condition. Figure 45 shows how status alert signals and alarm mask bits work together to generate an alarm on the alarm bus.

Table 38 is a summary of all status alerts present in the MAX11068, the associated threshold levels or trigger condition, and the corresponding mask enable bits.

Alert bits are cleared by writing the bit to a logic zero unless they are automatically cleared when the alert condition subsides. Clearing an alert bit that caused an alarm also clears the alarm. If multiple alerts or multiple devices are triggering an alarm condition, all alerts must be cleared before the heartbeat signal is again propagated to the host controller.

When the system controller receives an active alarm indication from the alarm bus, it must poll the SMBus ladder stack to determine the source of the alarm. A READALL command should be issued to read each register that contains alert bits that are enabled to trigger an alarm. After determining the source of the alarm, appropriate actions may be taken by the application. The system controller should periodically poll all registers with alert status bits to monitor the status of the MAX11068 SMBus ladder. This ensures any important events are identified in a timely manner.

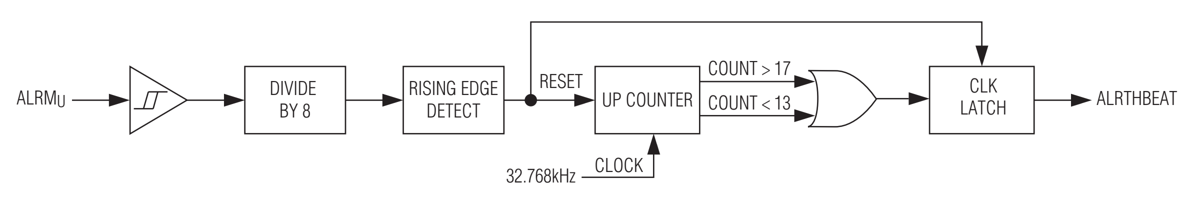


Figure 44. ALRM_U Pin and ALRTHBEAT Block Diagram

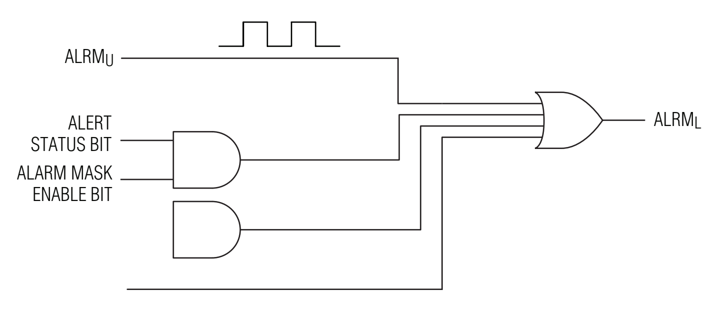


Figure 45. Logic Diagram of Alert Conditions and Associated Alarm Enable Bits

Table 38. Alert Bits with Descriptions and Corresponding Alarm Mask Bits

ALERT STATUS BIT (REGISTER.BIT)	ALERT DESCRIPTION	ALERT THRESHOLD OR TRIGGER CONDITION	ALERT CLEAR CONDITION	ALARM MASK ENABLE BIT (REGISTER.BIT)
STATUS.RSTSTAT	Device reset occurred	VAA < $V_{POR-FALL}$	Write alert bit to 0	Always enabled
STATUS.ALRTOV	Overvoltage was detected for at least one cell	Logical OR of bits in the ALRTOVCELL register	Disable active alert or remove the overvoltage condition	ADCCFG.ALRMOVEN
STATUS.ALRTUV	Undervoltage was detected for at least one cell	Logical OR of bits in the ALRTUVCELL register	Disable active alert or remove the undervoltage condition	ADCCFG.ALRMUVEN
STATUS.ALRTMSMTCH	Cell-voltage mismatch between min and max measurements	MAXCELL - MINCELL > MSMTCH	Remove the cause of the mismatch or set the threshold to 0xFFF0 to disable the comparison	ADCCFG.ALRMMMTCHEN
STATUS.ALRTTCOLD	Auxiliary input overvoltage/ undertemperature	AIN0 or AIN1 > AINUT	Disable the active alert or remove the overvoltage condition	ADCCFG.ALRMUTEN
STATUS.ALRTTHOT	Auxiliary input undervoltage/ overtemperature	AIN0 or AIN1 < AINOT	Disable the active alert or remove the undervoltage condition	ADCCFG.ALRMOTEN
STATUS.ALRTPEC	Communication PEC error	PEC byte checked for a received packet was incorrect	Write alert bit to 0	ADCCFG.ALRMPEC
STATUS.ALRTACK	Communication NACK error	A NACK was received when an ACK was expected	Write alert bit to 0	ADCCFG.ALRMACK
STATUS.ALRTFMEA	At least one alert from FMEA register is active	Logical OR of the alert bits in the FMEA register	Clear all alerts in the FMEA register	None
STATUS.ALRTAIN2	Auxiliary analog input 1 is outside one of the set thresholds	AIN1 > AINUT or AIN1 < AINOT	Disable the active alert or remove the undervoltage or overvoltage condition and take a new measurement	None

Table 38. Alert Bits with Descriptions and Corresponding Alarm Mask Bits (continued)

ALERT STATUS BIT (REGISTER.BIT)	ALERT DESCRIPTION	ALERT THRESHOLD OR TRIGGER CONDITION	ALERT CLEAR CONDITION	ALARM MASK ENABLE BIT (REGISTER.BIT)
STATUS.ALRTAIN1	Auxiliary analog input 0 is outside one of the set thresholds	AIN0 > AINUT or AIN0 < AINOT	Disable the active alert or remove the undervoltage or overvoltage condition and take a new measurement	None
ALRTCELL.ALRTCELL[n]	Specifies whether each cell has an overvoltage or undervoltage condition	Each bit [n] is a logical OR of the corresponding bit in the ALRTOVCELL and ALRTUVCELL registers	Set CELL[n].OVEN and CELL[n].UVEN to 0 or remove the overvoltage or undervoltage condition from the cell	None; use the ALRTOV and ALRTUV status bits as alarm triggers
ALRTOVCELL. ALRTOVCELL[n]	Specifies whether each cell is in an overvoltage state	CELL[n] > OVTHRSET and CELL[n].OVEN set to 1	Set CELL[n].OVEN to 0 or remove the overvoltage condition from the cell	None; use the ALRTOV status bit as an alarm trigger
ALRTUVCELL. ALRTUVCELL[n]	Specifies whether each cell is in an undervoltage state	CELL[n] < UVTHRSET and CELL[n].UVEN set to 1	Set CELL[n].UVEN to 0 or remove the undervoltage condition from the cell	None; use the ALRTUV status bit as an alarm trigger
FMEA.ALRTCPUV	The charge-pump output VDD_U has fallen below the undervoltage threshold	VDD_U - GND_U < V_{CPUV}	Remove alert condition and write alert bit to 0 alert condition	FMEA.ALRMCPUV
FMEA.ALRTHBEAT	Alarm bus heartbeat signal is out of specification	$ALRM_L$ frequency is more than 12.5% from nominal	Remove alert condition and write alert bit to 0 alert condition	FMEA.ALRMHBEAT
FMEA.ALRTREF	REF pin is oscillating, most likely due to an open-circuit condition		Remove alert condition and write alert bit to 0 alert condition	FMEA.ALRMREF
FMEA.ALRTVDDL	VDD_L pin is open circuit	VAA - VDD_L > 0.3V typical	Remove alert condition and write alert bit to 0 alert condition	FMEA.ALRMVDDL
FMEA.ALRTGNDL	GND_L pin is open circuit	GND_L - AGND > 0.3V typical	Remove alert condition and write alert bit to 0 alert condition	FMEA.ALRMGNDL

Shutdown Control

The $\overline{\text{SHDN}}$ pin of the MAX11068 is connected in a manner that allows the shutdown/wakeup command to trickle up through the series of SMBus-laddered packs. The propagation time is on the order of 3ms per module with the recommended shutdown circuit. The shutdown function is intended to be a reset and power-saving mode for the entire IC. When coming out of shutdown mode, the device goes through the power-up sequence shown for the linear regulator once the $\overline{\text{SHDN}}$ pin is above the inactive state threshold. The shutdown function must still operate when the VAA is shut down, so it cannot depend on a Schmitt trigger. A special low-current, high-voltage circuit is used to detect the state of the $\overline{\text{SHDN}}$ pin. The shutdown pin has a +1.8V threshold. When $\overline{\text{SHDN}}$ > 1.8V, the MAX11068 turns on and begins regulating VDD_U and VDD_L. If $\overline{\text{SHDN}}$ < 0.6V, the MAX11068 shuts down. Figure 46 shows the shutdown circuit interface of two SMBus ladder devices.

When $\overline{\text{SHDN}}$ is high for the device, the charge pump is enabled and begins to charge the capacitors in the interface circuit. When the voltage of the $\overline{\text{SHDN}}$ pin for device (n+1) rises above the V_{IH} threshold, that device begins its power-up sequence. This action propagates up the SMBus ladder until the last battery module is enabled. Conversely, pulling $\overline{\text{SHDN}}$ to GND_L powers down a module and thus propagates the power down to all higher SMBus-laddered modules as the charge on their $\overline{\text{SHDN}}$ capacitors is dissipated. The zener diodes provide additional ESD protection. The filter capacitors and resistors are sized to provide robust noise immunity. The diode from the CP+ pin should be S1B or a similar low-leakage type for high-temperature stability.

The $\overline{\text{SHDN}}$ pin is a high-voltage input rated to 60V. $\overline{\text{SHDN}}$ may be tied to DCIN through a resistor instead of using the interface circuit above for applications that do not require use of the shutdown mode. The resistor in that case is necessary for failure-mode effects analysis considerations. If $\overline{\text{SHDN}}$ was shorted to the $ALRM_L$ pin, the $ALRM_L$ pin must be protected from seeing the full DCIN voltage. A resistor value of 100kΩ is recommended to work across the entire DCIN voltage range.

The $\overline{\text{SHDN}}$ pin has a weak internal pulldown resistor in the order of 12MΩ. So, a 200kΩ or similar resistor from $\overline{\text{SHDN}}$ to GND_L should be installed to ensure that the $\overline{\text{SHDN}}$ pin is pulled low when the active $\overline{\text{SHDN}}$ signal is propagated up the SMBus ladder. This resistor is not needed for applications that tie $\overline{\text{SHDN}}$ high at all times.

I²C SMBus Ladder Initialization Sequence

When the MAX11068 becomes functional after any reset event, its I²C address, broadcast address, and place in the SMBus ladder are set to a default value. Prior to performing battery-monitoring tasks, each device must be configured to operate as part of the SMBus ladder. The following configuration sequence (Figure 47) is recommended to initialize the system of SMBus-laddered modules after a power cycle or change in the number of battery stack modules.

First, the HELLOALL command is sent to sequentially initialize the individual device addresses. The first device address is specified in the command byte and should be chosen carefully based on the application requirements. After a successful HELLOALL command, the ROLLCALL command should be sent. This reads the ADDRESS register of all properly communicating modules. When the host sees two consecutive 0xFF bytes, meaning that all valid data has been received, it should send a NACK and a STOP bit to halt data flow. Once the ADDRESS register data is received, the host can determine how many devices are active on the bus. After ensuring that the number of active devices matches what is expected by the application, the host should send the SETLASTADDRESS command to configure the last device in the chain to be the heartbeat initiator.

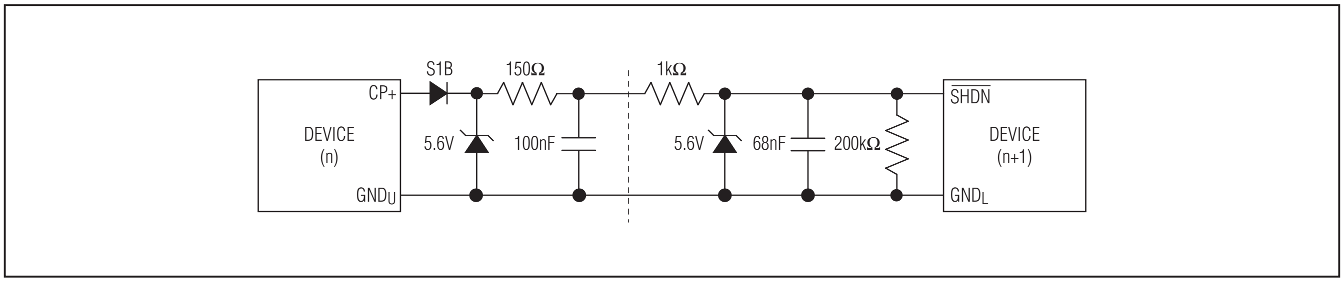


Figure 46. Shutdown Circuit Interface

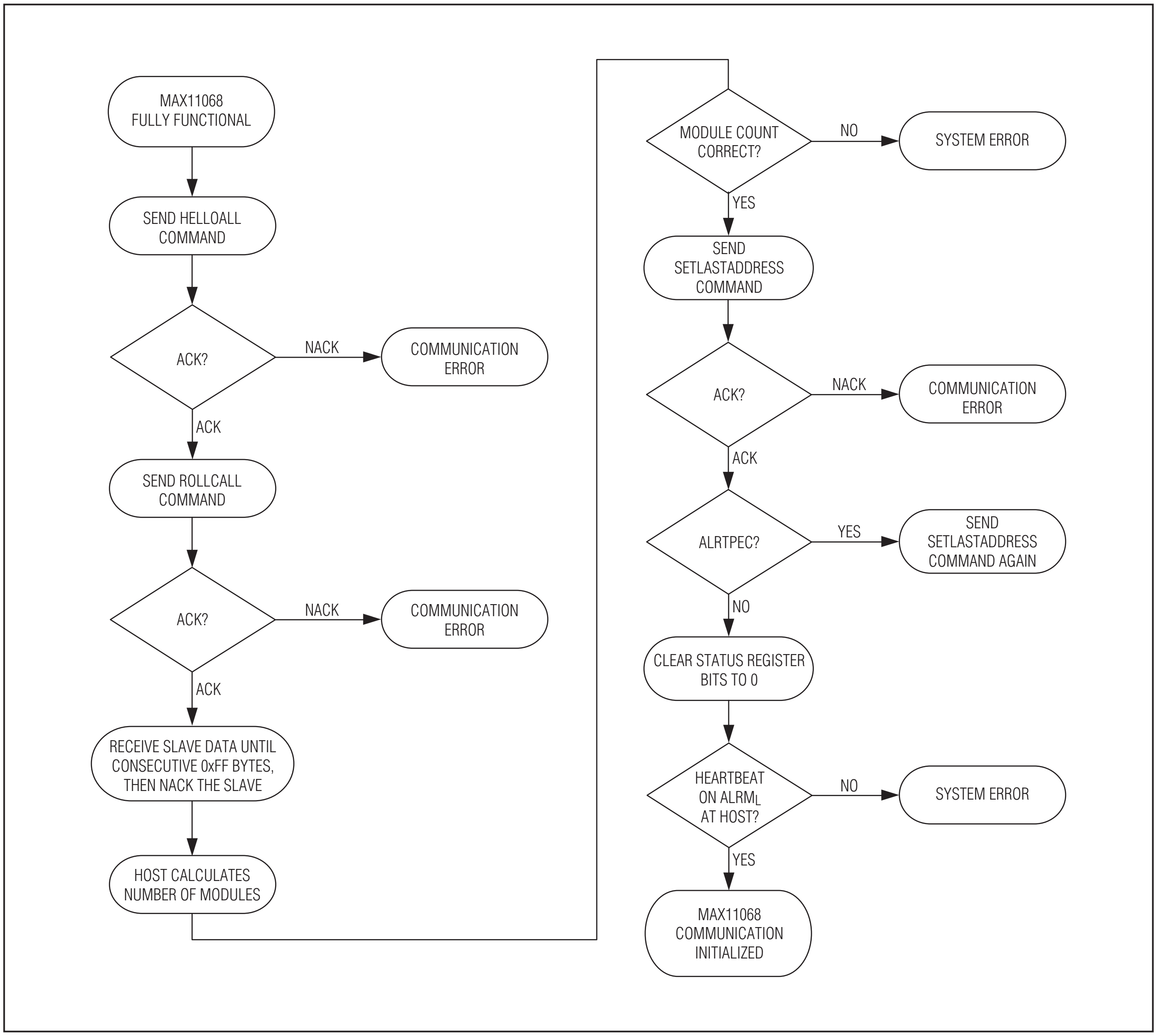


Figure 47. Communication Initialization Sequence Following Any Reset Event or Module Connection Change

After the SMBus ladder modules are configured for communication, they should be configured for operation:

1) Perform a READALL to check device status:
    a) The RSTSTAT bit should be set in all devices to signify a POR event has occurred.
    b) The last device in the chain shows an ALRTACK fault because there is no device above it to acknowledge its communication.
2) Clear the ALRTACK status for the last device using a WRITEDEVICE or WRITEALL command.
3) Clear the RSTSTAT bit on all devices so that future power-cycle events can be detected. This also allows the last device in the daisy-chain to begin generating the heartbeat signal.
4) Change configuration registers as necessary with WRITEALL commands:
    a) Change the broadcast address in register 0x0F if a different one is required.
    b) Configure the undervoltage and overvoltage cell thresholds in registers 0x18 to 0x1B.
    c) Configure the mismatch threshold if required in register 0x1C.
    d) Configure the undertemperature and overtemperature thresholds used for thermistor measurements, if required.
    e) Configure the auxiliary input-acquisition settling time in the ACQCFG register if necessary.
    f) Enable the cell input channels that are used for measurement and enable auxiliary channels that are used.
    g) Configure cell-voltage alert enables.
    h) Set desired alarm enable flags in the ADCCFG and FMEA registers.
5) When the device is fully configured, initiate a measurement conversion by setting bit 0 of the SCANCTRL register (address 0x0D).
6) When the first conversion is complete, process the cell and auxiliary input channel data and take any necessary actions.
7) Continue monitoring the system status while initiating new measurements.

Changing the Broadcast Address

If the default broadcast address must be changed for an application, the host should manage the process carefully since the READALL and WRITEALL commands rely on this address for proper operation. Although a WRITEALL command can be used to change the address at any time, it is recommended that a broadcast address change not be performed until after the SMBus ladder is fully initialized so that subsequent ROLLCALL or READALL commands may be used to verify the address change for all devices.

With the device in a fully initialized state, the new broadcast address is written to the BROADCAST ADDRESS register (address 0x0F) using a WRITEALL command, although a series of WRITEDEVICE commands may be used as well. Prior to changing the broadcast address, the host should save the original address in case it is needed later in the process. Once the WRITEALL command is issued, it must be verified. The most straightforward way of accomplishing this is to issue a ROLLCALL command and count the number of active devices using the new address. If the count matches what is expected, the broadcast address change was successful for all modules. If the count is incorrect, at least one device rejected the WRITEALL command and the count signifies which module is not responding to the new address. A WRITEDEVICE command may be used to rewrite to individual modules, or another WRITEALL command may be sent to the old broadcast address. After updating the missing modules, the ROLLCALL procedure should again be used to make sure all devices are responding to the new broadcast address. See Figure 48.

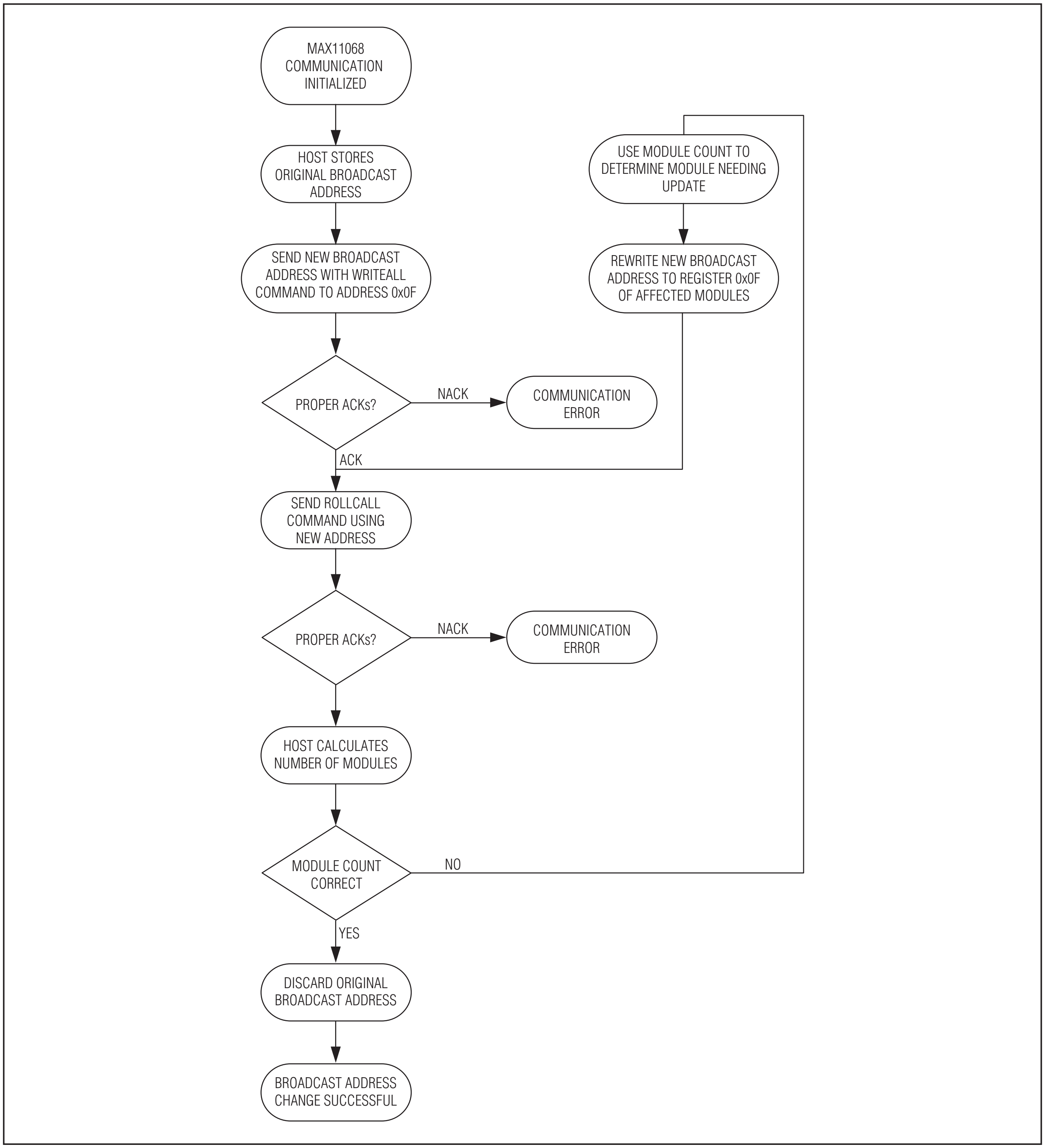


Figure 48. Broadcast Address Change Procedure

Failure Mode and Effects Analysis

High-voltage battery-pack systems can be subjected to severe stresses during in-service fault conditions and could experience similar conditions during the manufacturing and assembly process. The MAX11068 is designed with high regard to these potential states. Open and short circuits at the package level must be readily detected for fault diagnosis and should be tolerated whenever possible. A number of circuits are employed within the MAX11068 specifically to detect such conditions and progress to a known device state.

Table 39 summarizes other conditions typical in a normal manufacturing process along with their effect on the MAX11068 device. See Table 40 for the failure-mode effects analysis of the MAX11068.

Table 39. System Fault Modes

CONDITION	EFFECT	DESIGN RECOMMENDATION
PCB or IC package open or short circuit—no stack load	See pin-level failure-mode effects analysis spreadsheet available from the factory	The built-in features of the MAX11068 should ensure low failure-mode effects risk in most cases.
Random connection of cells to IC—no stack load	No effect	Circuit design of Figures 4 and 5 ensure protection against random power-supply or ground connections.
Random connection of modules—no stack load	No effect	Each module is referenced to its neighbor, so no special connection order is necessary.
Random connect/disconnect of communication bus—no stack load; AC- or DC-coupled	Communication from host to the first break in the daisy-chain bus	The level-shifted interface design of the MAX11068 ensures that the $\overline{\text{SHDN}}$, GND_U, ALRM_U communication bus can be connected at any time with no load.
Random connect/disconnect of communication bus—with stack load; AC- or DC-coupled	Communication from host to the first break in the daisy-chain bus	The level-shifted interface design of the MAX11068 ensures that the $\overline{\text{SHDN}}$, GND_U, ALRM_U communication bus can be connected at any time as long as the power bus is properly connected.
Connect/disconnect module interconnect (bus bar)—no stack load	No effect for DC- or AC-coupled communication bus	A break in the power bus does not cause a problem as long as there is no load on the stack.
Removal/fault of module interconnect (bus bar)—with stack load	No effect for AC-coupled communication bus; device damage for DC-coupled bus	An AC-coupled bus with isolation on the $\overline{\text{SHDN}}$ pin or a redundant bus bar connection should be used to protect against this case.
Removal/fault of module interconnect (bus bar)—with stack under charge	No effect for AC-coupled communication bus; device damage for DC-coupled bus	An AC-coupled bus with isolation on the $\overline{\text{SHDN}}$ pin or a redundant bus bar connection should be used to protect against this case.

Table 40. Failure-Mode Effects Analysis

PIN	NAME	ACTION	EFFECT
1	DCIN	Open or disconnected	I^{2}C lost communication. No heartbeat.
		Short to pin 2	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
2	CP+	Open or disconnected	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
		Short to pin 3	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
3	CP-	Open or disconnected	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
		Short to pin 4	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
4	VDD_U	Open or disconnected	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
		Short to pin 5	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
5	GND_U	Open or disconnected	I^{2}C lost communication. No heartbeat. ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
		Short to pin 6	The up-device cell registers are read back all 1. ALRTACK of the STATUS register is set to 1. No effect for the single device or the top device.
6	SCL_U	Open or disconnected	The up-device cell registers are read back all 1. ALRTACK and ALRTPEC of the STATUS register are set to 1. No effect for the single device or the top device.
		Short to pin 7	The up-device cell registers are read back all 1. No effect for the single device or the top device.
7	SDA_U	Open or disconnected	The up-device cell registers are read back all 1. ALRTACK of the STATUS register is set to 1. No effect for the single device or the top device.
		Short to pin 8	ALRTPEC and ALRTACK of the STATUS register are set to 1. The up-device cell registers are read back as the random number. No effect for the single device or the top device.
8	ALRM_U	Open or disconnected	ALRTHBEAT of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1. No heartbeat. No effect for the single device or the top device.
		Short to pin 9	No effect.
9	N.C.	Open or disconnected	No effect.
		Short to pin 10	No effect.
10	GPIO2	Open or disconnected	Lost the input status or no drive capability.
		Short to pin 11	If both GPIO2 and GPIO1 are configured as the input or the same status for the output, there is no effect. If they are configured as a different value as the output, it shows the output of 0V and the part is reset.

Table 40. Failure-Mode Effects Analysis (continued)

PIN	NAME	ACTION	EFFECT
11	GPIO1	Open or disconnected	Lost the input status or no drive capability.
		Short to pin 12	If both GPIO1 and GPIO0 are configured as the input or the same status for the output, there is no effect. If they are configured as a different value as the output, it shows the output of 0V and the part is reset.
12	GPIO0	Open or disconnected	Lost the input status or no drive capability.
		Short to pin 13	If the GPIO0 is configured as input or the high status for the output, there is no effect. If it is configured as low status for the output, the part is reset.
13	VDD_L	Open or disconnected	ALRTVDDL of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
		Short to pin 14	I^{2}C lost communication. No heartbeat.
14	GND_L	Open or disconnected	I^{2}C lost communication.
		Short to pin 15	I^{2}C lost communication.
15	SCL_L	Open or disconnected	I^{2}C lost communication.
		Short to pin 16	I^{2}C lost communication.
16	SDA_L	Open or disconnected	I^{2}C lost communication.
		Short to pin 17	I^{2}C lost communication. No heartbeat.
17	$ALRM_L$	Open or disconnected	No heartbeat.
		Short to pin 18	The result is dependent on the circuit that drives the $\overline{SHDN}$ pin. If the circuit has strong drive capability ($ALRM_L$ follows $\overline{SHDN}$), the heartbeat goes away. Otherwise the heartbeat is OK as the VAA charged faster than the discharge so the part keeps in the normal working mode.
18	$\overline{SHDN}$	Open or disconnected	I^{2}C lost communication as the device is shut down by the internal pulldown resistor.
		Short to pin 19	The result is dependent on the circuit that drives the $\overline{SHDN}$ pin and AUXIN2.
19	AUXIN2	Open or disconnected	The AIN2 register is around 0.
20	THRM	Open or disconnected	External temperature circuit lost the bias supply. So the AIN0 and AIN1 should be read as close to 0V. Otherwise there is no effect.
		Short to pin 21	The AIN1 register is close to full scale (0xFFF).

Table 40. Failure-Mode Effects Analysis (continued)

PIN	NAME	ACTION	EFFECT
21	AUXIN1	Open or disconnected	The AIN1 register is around 0.
		Short to pin 22	The result is dependent on the circuit setup of AUXIN1. If REF is driven to VAA, all the cell input measurements are lower by 1V. If REF is pulled low to AGND, cells 1 to 10 measurement results are all full scale (5V). The DIAG register changes to 0x296 from 0x5D4.
22	REF	Open or disconnected	Cells 1 to 12 measurement results vary from 3V to 5V. The DIAG register varies from 0x300 to 0x800. ALRTREF of the FMEA register is set to 1, ALRTFMEA of the STATUS register is set to 1.
		Short to pin 23	Cell 1 to 12 measurement results are all full scale (5V). The DIAG register changes to 0x296 from 0x5D4.
23	AGND	Open or disconnected	No effect.
		Short to pin 24	I^{2}C lost communication and no heartbeat.
24	VAA	Open or disconnected	ALRTVDDL of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
		Short to pin 25	I^{2}C lost communication and no heartbeat.
25	C0	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 26	V_{CELL1} = 1V (3V lower).
26	C1	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 27	V_{CELL2} = 0V.
27	C2	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 28	V_{CELL3} = 0V.
28	C3	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 29	V_{CELL4} = 0V.
29	C4	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 30	V_{CELL5} = 0V.
30	C5	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 31	V_{CELL6} = 0V.

Table 40. Failure-Mode Effects Analysis (continued)

PIN	NAME	ACTION	EFFECT
31	C6	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 32	V_{CELL7} = 0V.
32	C7	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 33	V_{CELL8} = 0V.
33	C8	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 34	V_{CELL9} = 0V.
34	C9	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 35	V_{CELL10} = 0V.
35	C10	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 36	V_{CELL11} = 0V.
36	C11	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 37	V_{CELL12} = 0V.
37	C12	Open or disconnected	This situation can be detected by the cell sense line open-circuit detection feature.
		Short to pin 38	ALRTCPUV of the FMEA register is set to 1. ALRTFMEA of the STATUS register is set to 1.
38	HV	Open or disconnected	V_{CELL12} = 0.6V (3.4V lower).

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
38 TSSOP	U38-1	21-0081

MAX11068

12-Channel, High-Voltage Sensor, Smart Data-Acquisition Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—