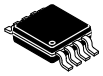
CAT5116

Log-taper, 100-tap Digital Potentiometer (POT)

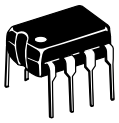
ON Semiconductor®

http://onsemi.com

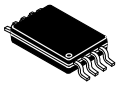
SOIC−8
V SUFFIX
CASE 751BD



MSOP−8
Z SUFFIX
CASE 846AD



PDIP−8
L SUFFIX
CASE 646AA



TSSOP−8
Y SUFFIX
CASE 948AL

Description

The CAT5116 is a log-taper single digital POT designed as an electronic replacement for mechanical potentiometers.

Ideal for automated adjustments on high volume production lines, ICs are well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5116 contains a 100-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_W.

The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting.

Wiper-control of the CAT5116 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digital POT can be used as a three-terminal resistive divider or as a two-terminal variable resistor.

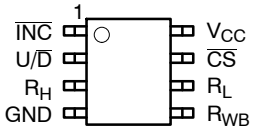
Features

- 100-position, Log-taper Potentiometer
- Non-volatile EEPROM Wiper Storage
- 10 nA Ultra-low Standby Current
- Single-supply Operation: 2.5 V – 5.5 V
- Increment Up/Down Serial Interface
- Resistance Value: 32 kΩ
- Available in 8-pin MSOP, TSSOP, SOIC and DIP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Audio Volume Control
- Sensor Adjustment
- Motor Controls and Feedback Systems
- Programmable Analog Functions

PIN CONFIGURATIONS



PDIP (L), SOIC (V), MSOP (Z)

TSSOP (Y)

(Top Views)

PIN FUNCTION

Pin Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_W	Buffered Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Functional Diagram

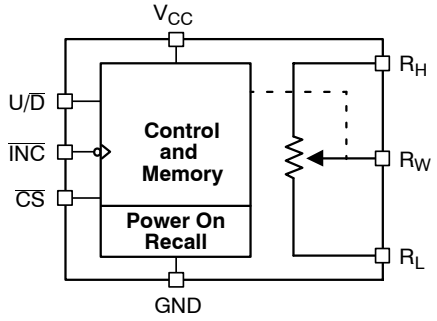


Figure 1. General

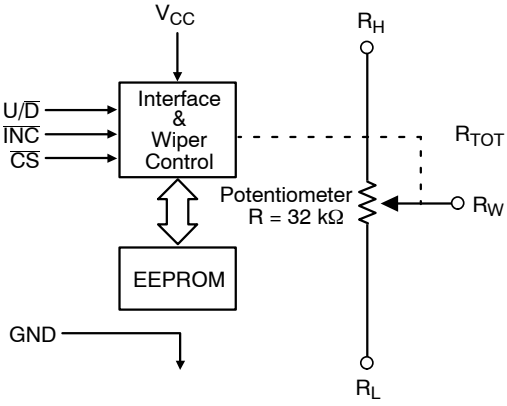


Figure 2. Block Diagram

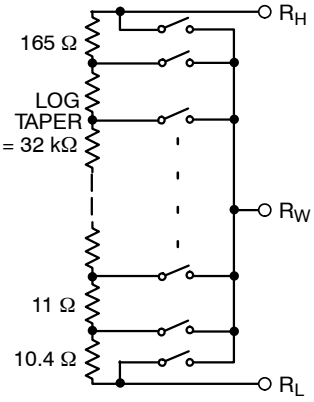


Figure 3. Potentiometer Schematic

Pin Description

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_W: Wiper Potentiometer Terminal

R_W is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. Voltage applied to the R_W terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the CAT5116 and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper.

Device Operation

The CAT5116 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_W equivalent to the mechanical potentiometer's wiper. There are 100 tap positions including the resistor end points, R_H and R_L. There are 99 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a seven-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5116 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and seven-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5116 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5116 may be deselected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

Table 1. OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby

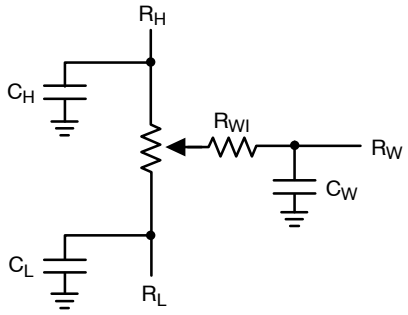


Figure 4. Potentiometer Equivalent Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V_{CC} to GND	−0.5 to +7	V
Inputs $\overline{CS}$ to GND	−0.5 to V_{CC} +0.5	V
$\overline{INC}$ to GND	−0.5 to V_{CC} +0.5	V
U/$\overline{D}$ to GND	−0.5 to V_{CC} +0.5	V
R_H to GND	−0.5 to V_{CC} +0.5	V
R_L to GND	−0.5 to V_{CC} +0.5	V
R_W to GND	−0.5 to V_{CC} +0.5	V
Operating Ambient Temperature Industrial ('I' suffix)	−40 to +85	°C
Junction Temperature (10 s)	+150	°C
Storage Temperature	+150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP} (Note 1)	ESD Susceptibility	MIL−STD−883, Test Method 3015	2000			V
I_{LTH} (Notes 1, 2)	Latch-up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL−STD−883, Test Method 1008	100			Years
N_{END}	Endurance	MIL−STD−883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} + 1 V.

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.5	–	5.5	V
I_{CC1} (Note 5)	Supply Current (Increment)	V_{CC} = 5.5 V, f = 1 MHz, I_W = 0	–	–	100	μA
		V_{CC} = 5.5 V, f = 250 kHz, I_W = 0	–	–	50	μA
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 5.5 V	–	–	1	mA
		V_{CC} = 3 V	–	–	500	μA
I_{SB1}	Supply Current (Standby)	$\overline{CS}$ = V_{CC} – 0.3 V U/$\overline{D}$, $\overline{INC}$ = V_{CC} – 0.3 V or GND	–	0.01	1	μA
LOGIC INPUTS						
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	–	–	10	μA
I_{IL}	Input Leakage Current	V_{IN} = 0 V	–	–	–10	μA
V_{IH1}	TTL High Level Input Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V	2	–	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	–	0.8	V
V_{IH2}	CMOS High Level Input Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V	V_{CC} x 0.7	–	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		–0.3	–	V_{CC} x 0.2	V
POTENTIOMETER PARAMETERS						
R_{POT}	Potentiometer Resistance			32		kΩ
R_{TOL}	Pot. Resistance Tolerance				±20	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
R_V (Note 6)	Relative Variation				0.05	
R_{WI}	Wiper Resistance	V_{CC} = 5 V, I_W = 1 mA		200	400	Ω
		V_{CC} = 2.5 V, I_W = 1 mA		400	1000	Ω
I_W	Wiper Current				1	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC				20	ppm/°C
V_N	Noise	100 kHz / 1 kHz		8/24		nV/√Hz
$C_H/C_L/C_W$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10 kΩ		1.7		MHz

3. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} + 1 V.
4. This parameter is tested initially and after a design or process change that affects the parameter.
5. I_W = source or sink.
6. Relative variation is a measure of the error in step size between taps = log ($V_{W(N)}$) – log($V_{W(N–1)}$) = 0.045 ± 0.003.

Table 5. AC TEST CONDITIONS

V_{CC} Range	2.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Levels	0.2 V_{CC} to 0.7 V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V_{CC}

Table 6. AC OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V, V_H = V_{CC}, V_L = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100	–	–	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	–	–	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	–	–	ns
t_{IL}	$\overline{INC}$ LOW Period	250	–	–	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	–	–	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	–	–	μs
t_{CPH1}	$\overline{CS}$ Deselect Time (NO STORE)	100	–	–	ns
t_{CPH2}	$\overline{CS}$ Deselect Time (STORE)	10	–	–	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	–	1	5	μs
t_{CYC}	$\overline{INC}$ Cycle Time	1	–	–	μs
t_R, t_F (Note 8)	$\overline{INC}$ Input Rise and Fall Time	–	–	500	μs
t_{PU} (Note 8)	Power-up to Wiper Stable	–	–	1	ms
t_{WR}	Store Cycle	–	5	10	ms

7. Typical values are for T_A = 25°C and nominal supply voltage.
8. This parameter is periodically sampled and not 100% tested.
9. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

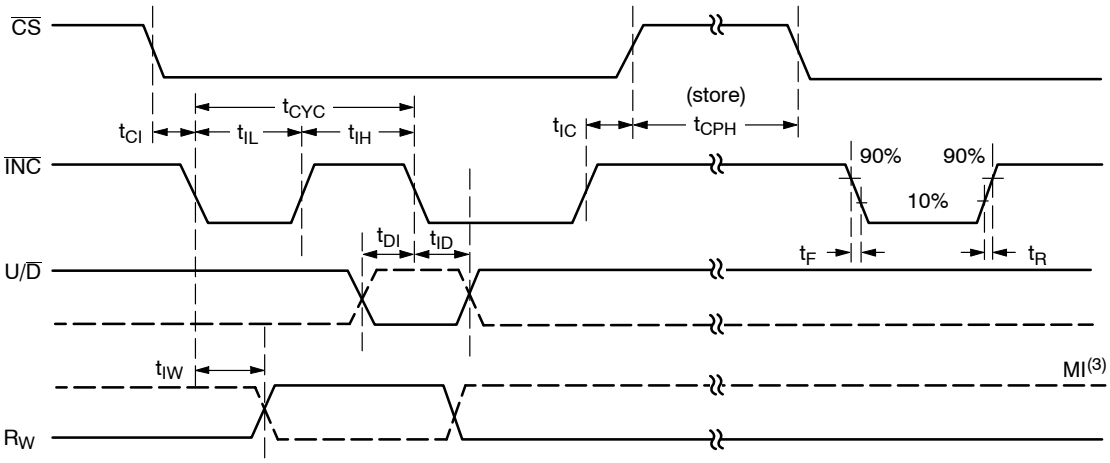


Figure 5. A.C. Timing

TYPICAL CHARACTERISTICS

(V_{CC} = 5 V, T_{AMB} = 25°C, unless otherwise specified)

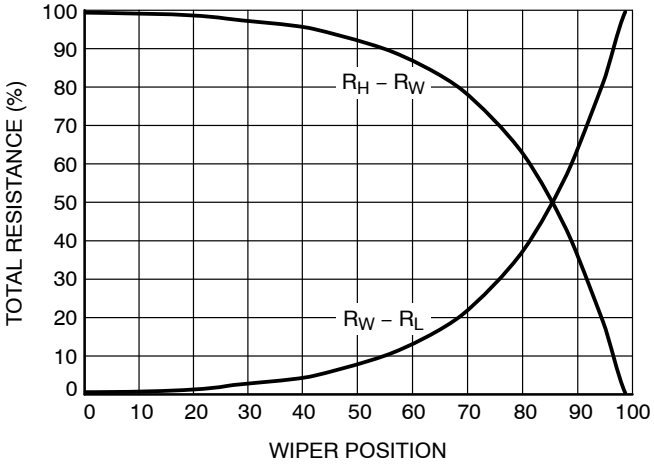


Figure 6. Wiper-Low/High Resistances vs. Wiper Position

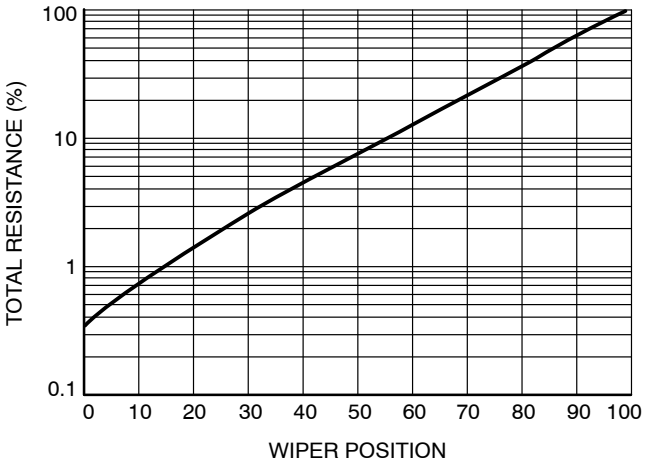


Figure 7. Wiper-Low Resistance vs. Wiper Position (Log Scale)

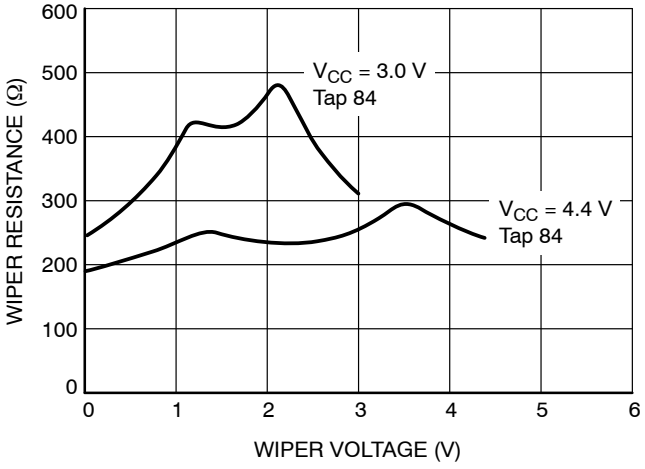


Figure 8. Wiper Resistance vs. Wiper Voltage

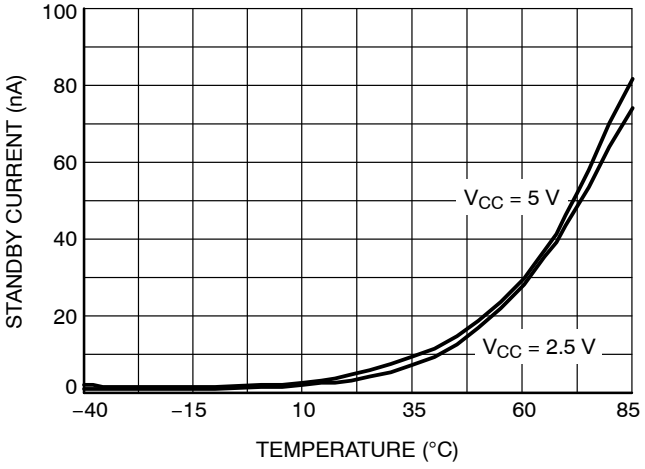


Figure 9. Standby Supply Current vs. Temperature

Table 7. ORDERING INFORMATION

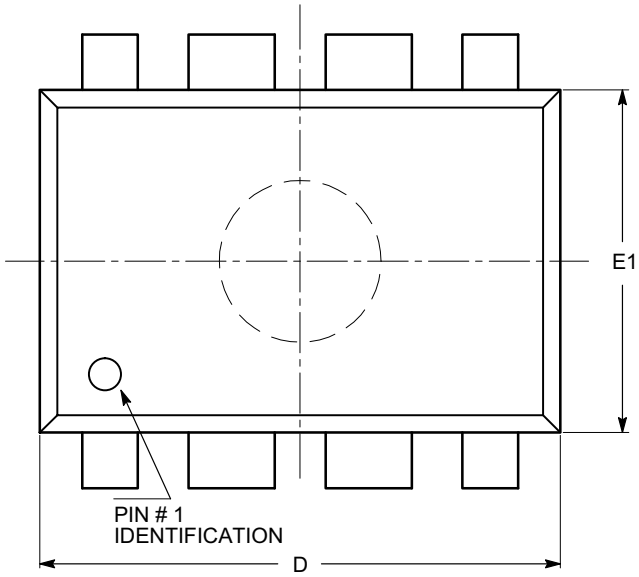
Device	Package	Shipping†
CAT5116LI−G	PDIP−8 (Pb−Free)	50 Units / Rail
CAT5116VI−G	SOIC−8 (Pb−Free)	100 Units / Rail
CAT5116VI−GT3	SOIC−8 (Pb−Free)	3000 / Tape & Reel
CAT5116YI−G	TSSOP−8 (Pb−Free)	100 Units / Rail
CAT5116YI−GT3	TSSOP−8 (Pb−Free)	3000 / Tape & Reel
CAT5116ZI	MSOP−8 (Pb−Free)	96 Units / Rail
CAT5116ZI−T3	MSOP−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.
11. All packages are RoHS-compliant (Lead-free, Halogen-free).
12. The standard lead finish is NiPdAu.
13. Contact factory for Matte-Tin finish.

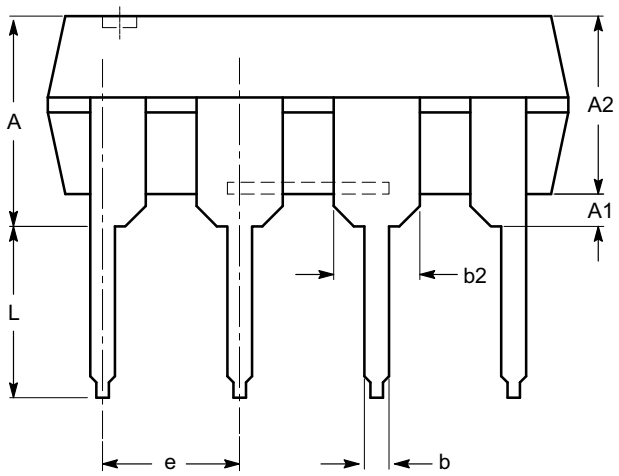
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA
ISSUE A

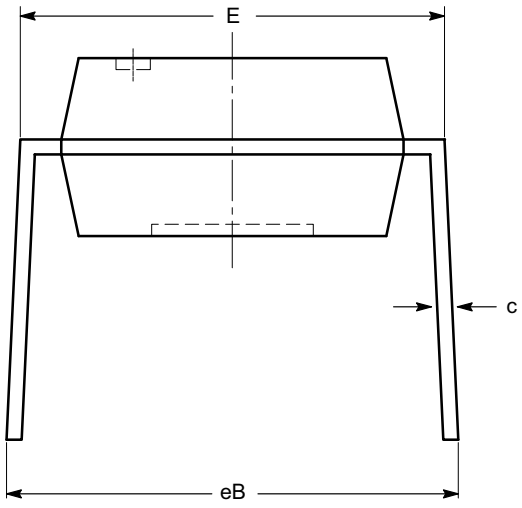


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

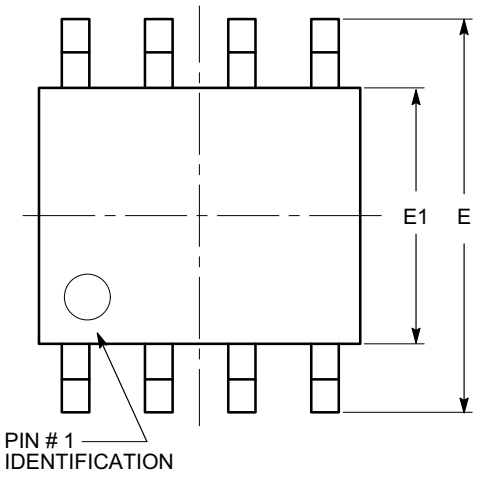


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

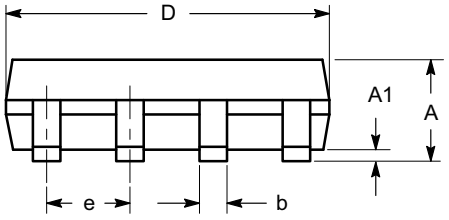
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD
ISSUE O

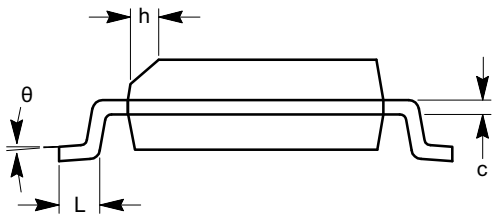


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

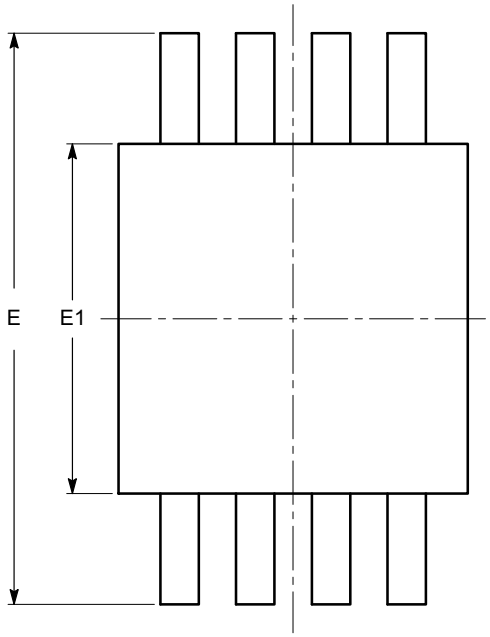


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

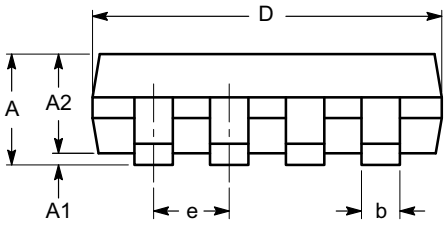
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD
ISSUE O

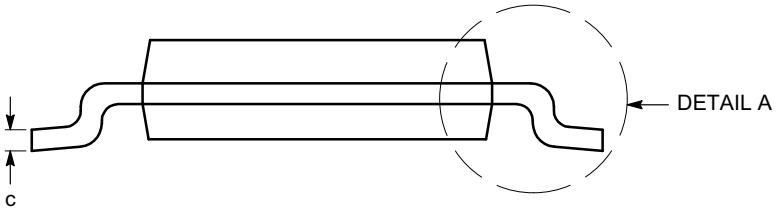


TOP VIEW

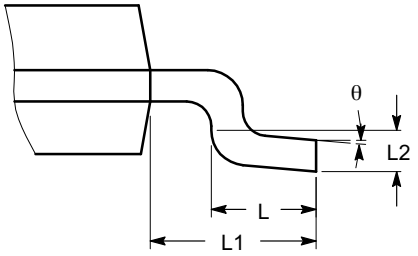
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0°		6°



SIDE VIEW



END VIEW

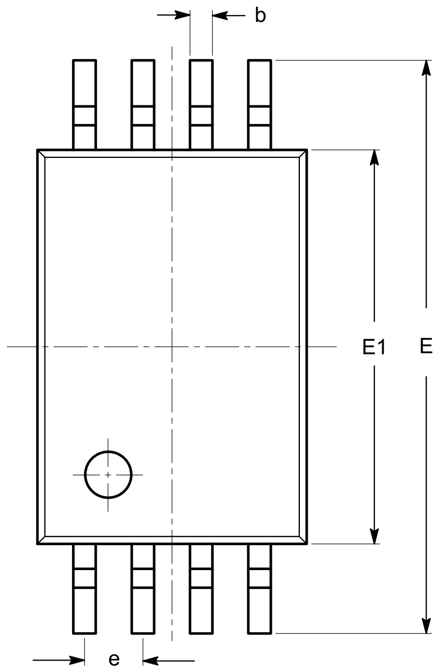


DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

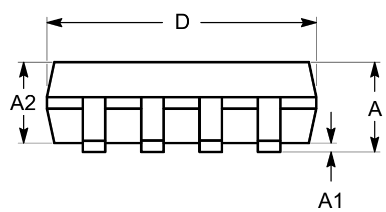
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL
ISSUE O

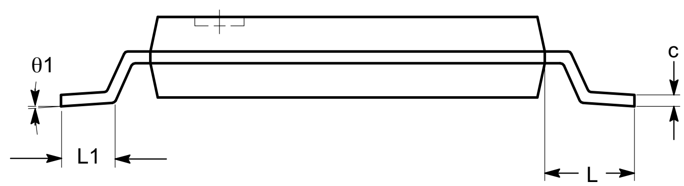


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º

TOP VIEW



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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