Features

- Wide range of operating supply voltage: 1.5V to 3.6V

- Optimized low crystal drive current oscillation for miniature crystal units

- PT7C5028BxDE series: for Wire Bonding (type   )

- PT7C5028CxDE series: for Wire Bonding (type   )

- Recommended oscillation frequency range

  ➢ Low frequency version: 20MHz to 60MHz

- Multi-stage frequency divider for low-frequency output support: 0.75MHz(min)

- Frequency divider built-in:

  ➢ Selectable by version: f0, f0/2, f0/4, f0/8, f0/16, f0/32, f0/64

- -40 to 85   operating temperature range

- Standby function

  ➢ High impedance in standby mode, oscillator stops

  ➢ CMOS output duty level(1/2VDD)

- $50 \pm 5\%$ output duty

- 15pF output drive capability

- Die form and Wafer form

Description

The PT7C5028B/C series are miniature crystal oscillator module ICs. The pad layouts are selective from 2 types depending on package structures, mounting methods, which are suitable for miniature crystal oscillators. The PT7C5028B/C series can be used to realize ultra miniature, ultra low voltage crystal oscillators.

Ordering Information

Part no.	Package type
PT7C5028Bx-5GDE	Die form
PT7C5028Bx-5GWF	Wafer form
PT7C5028Bx-6GDE	Die form
PT7C5028Bx-6GWF	Wafer form
PT7C5028Cx-5GDE	Die form
PT7C5028Cx-5GWF	Wafer form
PT7C5028Cx-6GDE	Die form
PT7C5028Cx-6GWF	Wafer form

Note: 1."x" shows the different function. See below description.

2. "-5G" show the die thickness is $130 \pm 15 \mu m$ without coating   "-6G" show the die thickness is $100 \pm 10 \mu m$ without coating.

Applications

- Used for crystal oscillator

Series Configuration
Table 1 Part No suffix description

Part No	Pad Layout Type
PT7C5028Bx	Wire Bonding (type I)
PT7C5028Cx	Wire Bonding (type II)

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Table 2 Part No suffix description

Part No	Operating supply voltage range(V)	Oscillation mode	Recommended oscillation frequency range[1](MHz)	Output frequency	Output drive capability (mA)	Standby mode	
						Oscillator stop function	Output state
PT7C5028B1/C1	1.5 to 3.6	Fundamental	20 to 60	f0[2]	4	Yes	Hi-Z
PT7C5028B2/C2				f0/2			
PT7C5028B3/C3				f0/4			
PT7C5028B4/C4				f0/8			
PT7C5028B5/C5				f0/16			
PT7C5028B6/C6				f0/32			
PT7C5028B7/C7				f0/64			

Note: * 1. The recommended operating frequency is a yardstick value derived from the crystal used for PTI characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

* 2. f0 is oscillation frequency (input frequency).

Block Diagram
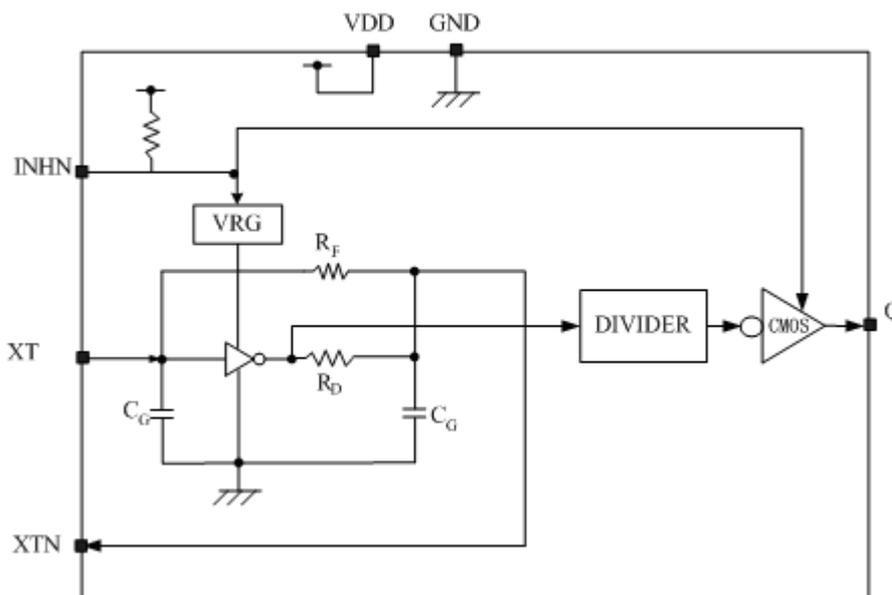
Function Description

Standby Function

When INHN goes LOW, the oscillator stops and the oscillator output on Q becomes high impedance.

INHN	Q	Oscillator
HIGH (or open)	f0 output frequency	Normal operation
Low	High impedance	Stopped

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Power-saving Pull-up Resistor

The INHN pin pull-up resistance R_{UP1} or R_{UP2} changes in response to the input level (HIGH or LOW). When INHN is tied LOW level, the pull-up resistance is large (R_{UP1}), reducing the current consumed by the resistance. When INHN is left open circuit, the pull-up resistance is small (R_{UP2}), which increases the input susceptibility to external noise. However, the pull-up resistance ties the INHN pin HIGH level to prevent external noise from unexpectedly stopping the output.

Oscillation Detector Function

The PT7C5028B/C series also feature an oscillation detector circuit. This circuit functions disable the outputs until the oscillator circuit starts and oscillation becomes stable. This alleviates the danger of abnormal oscillator output at oscillator start-up when power is applied or when INHN is switched.

Pad Configuration

PT7C5028Bx **PT7C5028Cx**
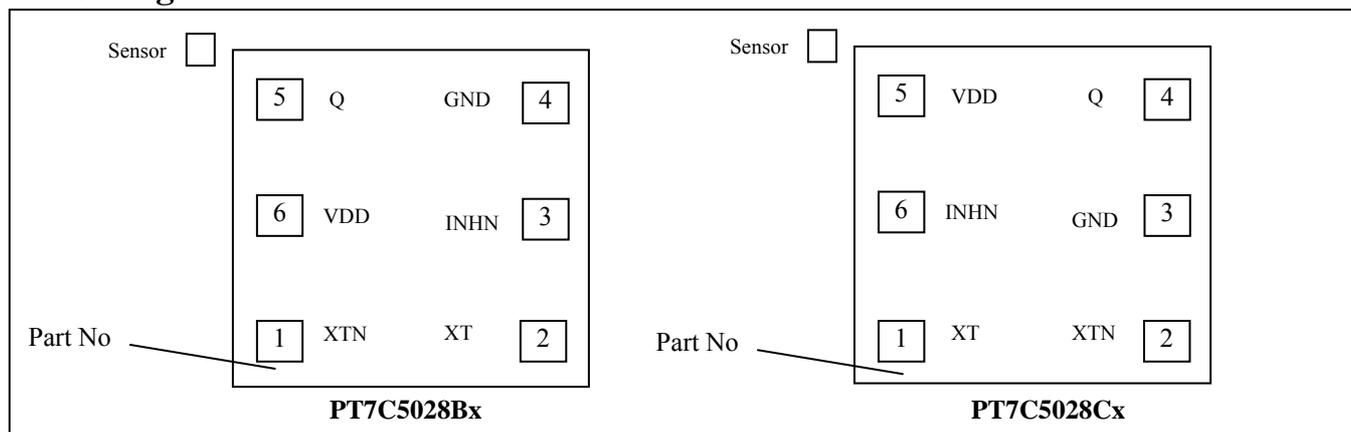
Pad Coordinate File					
Pad Name	X Coordinate	Y Coordinate	Pad Name	X Coordinate	Y Coordinate
sensor	-40	650.00			
1	79.00	79.00	4	531.00	530.99
2	531.00	79.00	5	79.00	530.99
3	531.00	282.31	6	79.00	282.31

Note: Substrate is connected to GND.
Die Size: 690μm*690μm (Including scribe line size 80μm*80μm.)
Die Thickness: 130μm±15μm and 100μm±10μm without coating.
Pad Size: 90μm*90μm

Pad Description

Sym.	Type	Description
XTN	O	Amplifier output.
XT	I	Amplifier input.
		Crystal oscillator connected between XT and XTN
INHN	I	Output state control input. High impedance when LOW. Power-saving pull-up resistor built in.
VDD	P	Supply voltage
GND	P	Ground
Q	O	Output. Output frequency determined by internal circuit to one of f0,f0/2,f0/4,f0/8,f0/16,f0/32,f0/64

Maximum Ratings

Storage Temperature ....- 65°C to +150°C
Supply Voltage range..- 0.5V to +4.0V
Input voltage range ....- 0.5V to V_{DD} +0.5V
Output voltage range ....- 0.5V to V_{DD} +0.5V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Sym.	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	C_L 15pF	1.5	-	3.6	V
V_{IN}	Input voltage	Input pins	GND	-	V_{DD}	V
T_A	Operating temperature	-	-40	+25	+85	°C
f_0	Oscillation frequency[*1]	-	20	-	60	MHz
f_{OUT}	Output frequency	C_L 15pF	0.75	-	60	MHz

Note:* 1. The recommended oscillation frequency is a yardstick value derived from the crystal used for PTI characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

DC Electrical Characteristics

V_{DD}=1.5 to 3.6V, T_A=-40 to 85   unless otherwise noted

Parameter	Sym	Conditions		Rating			Unit
				Min	Typ	Max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct3, I_{OH}=4mA		V_{DD}-0.4	-	-	V
LOW-level output voltage	V_{OL}	Q: Measurement cct3, I_{OL}=4mA		-	-	0.4	V
HIGH-level input voltage	V_{IH}	INHN, Measurement cct4		$0.7V_{DD}$	-	-	V
LOW-level input voltage	V_{IL}	INHN, Measurement cct4		-	-	$0.3V_{DD}$	V
Output leakage current	I_Z	Q: Measurement cct5, IHNH=LOW	V_{OH} =V_{DD}	-	-	20	μA
			V_{OL}=GND	20	-	-	μA
Current consumption	I_{DD}	5028× 1(f0),no load INHN=open,f0=48MHz f_{OUT}=48MHz	V_{DD} =3.3V	-	1.6	2.4	mA
			V_{DD} =2.5V	-	1.3	2.0	mA
			V_{DD} =1.8V	-	1.0	1.5	mA
		Measurement cct 1, 5028× 2(f0/64),no load INHN=open,f0=48MHz f_{OUT}=24MHz	V_{DD} =3.3V	-	1.5	2.3	mA
			V_{DD} =2.5V	-	1.2	1.8	mA
			V_{DD} =1.8V	-	0.9	1.4	mA
		Measurement cct 1, 5028× 3(f0/64),no load INHN=open,f0=48MHz f_{OUT}=12MHz	V_{DD} =3.3V	-	1.3	2.0	mA
			V_{DD} =2.5V	-	1.0	1.5	mA
			V_{DD} =1.8V	-	0.8	1.2	mA
		Measurement cct 1, 5028× 4(f0/64),no load INHN=open,f0=48MHz f_{OUT}=6MHz	V_{DD} =3.3V	-	1.1	1.7	mA
			V_{DD} =2.5V	-	0.9	1.4	mA
			V_{DD} =1.8V	-	0.75	1.15	mA
		Measurement cct 1, 5028× 5(f0/64),no load INHN=open,f0=48MHz f_{OUT}=3MHz	V_{DD} =3.3V	-	1.05	1.6	mA
			V_{DD} =2.5V	-	0.85	1.3	mA
			V_{DD} =1.8V	-	0.7	1.1	mA
		Measurement cct 1, 5028× 6(f0/64),no load INHN=open,f0=48MHz f_{OUT}=1.5MHz	V_{DD} =3.3V	-	1.0	1.5	mA
			V_{DD} =2.5V	-	0.85	1.3	mA
			V_{DD} =1.8V	-	0.7	1.1	mA
		Measurement cct 1, 5028× 7(f0/64),no load INHN=open,f0=48MHz f_{OUT}=0.94MHz	V_{DD} =3.3V	-	1.0	1.5	mA
			V_{DD} =2.5V	-	0.85	1.3	mA
			V_{DD} =1.8V	-	0.7	1.1	mA
Standby current	I_{ST}	Measurement cct1, INHN=LOW		-	-	10	μA
INHN pull-up resistance	R_{UP1}	Measurement cct6		0.4	1.5	8	MΩ
	R_{UP2}			30	70	150	KΩ
Oscillator feedback resistance	R_f	-		50	100	200	KΩ
Oscillator capacitance	C_G	Design value(a monitor pattern on a wafer is tested), Excluding parasitic capacitance		4.8	6	7.2	pF
	C_D			8	10	12	pF

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AC Electrical Characteristics

V_{DD}=1.5 to 3.6V, T_A=-40 to 85 unless otherwise noted

Parameter	Symbol	Condition		Min	Type	Max	Unit
				Rating			
				Min	Type	Max	
Output rise time	t_{r1}	Measurement cct1, C_L=15pF, $0.1V_{DD}$ to $0.9V_{DD}$	V_{DD}=2.0 to 3.6 V	-	1.3	3.0	ns
	t_{r2}	Measurement cct1, C_L=15pF, $0.2V_{DD}$ to $0.8V_{DD}$	V_{DD}=1.5 to 2.0 V	-	1.3	3.0	ns
Output fall time	t_{f1}	Measurement cct1, C_L=15pF, $0.9V_{DD}$ to $0.1V_{DD}$	V_{DD}=2.0 to 3.6 V	-	1.3	3.0	ns
	t_{f2}	Measurement cct1, C_L=15pF, $0.8V_{DD}$ to $0.2V_{DD}$	V_{DD}=1.5 to 2.0 V	-	1.3	3.0	ns
Output duty cycle	Duty	Measurement cct 1, T_A=25 ,C_L=15pF		45	50	55	%
Output disable delay time	t_{OD}	Measurement cct 1, T_A=25 ,C_L 15pF		-	-	50	μS
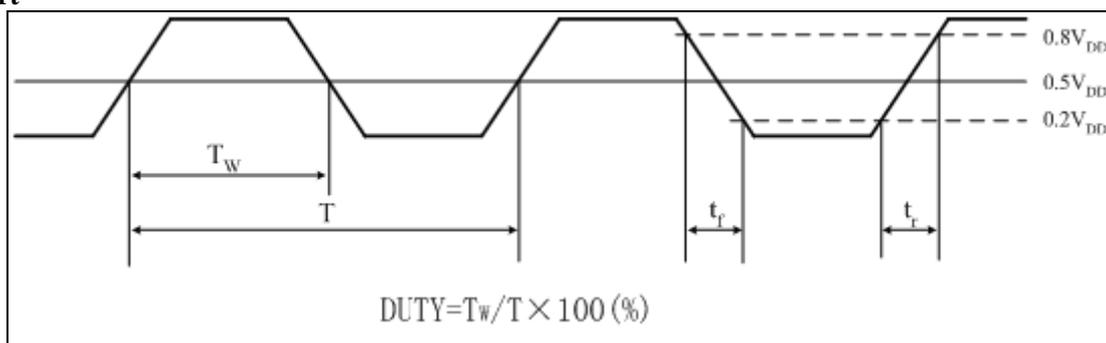
Timing chart

Figure 1: Output switching waveform
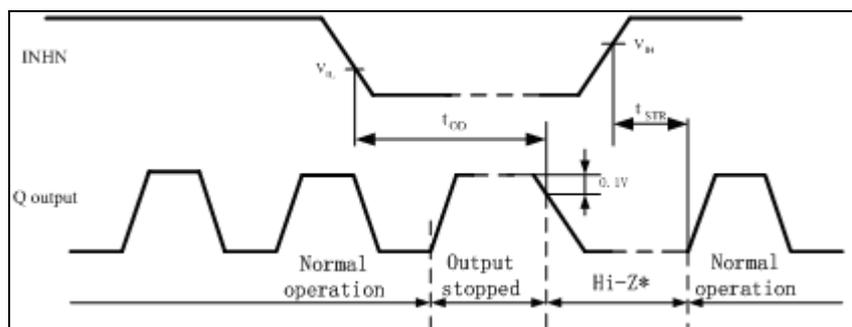
Figure 2: Output disable and oscillation start timing chart

When INHN goes HIGH to LOW, the Q output goes HIGH once and then becomes high impedance.
When INHN goes LOW to HIGH, the Q output from high impedance to normal output operation when the oscillation starts(oscillation is detected)
*) the high –impedance interval in the figure is shown as a LOW level due to the 1KΩ pull-down resistor connected to the Q pin(see "Measurement circuit 2"in the "Measurement circuits" section)

Measurement Circuit

Measurement cct1
Measurement parameter: I_{DD}, I_{ST}, Duty, t_r, t_f
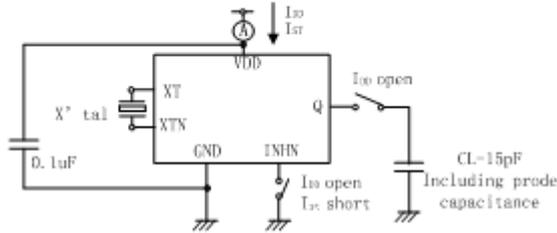
Note:The AC characteristics are observed using an oscilloscope on pin Q

Measurement cct2
Measurement parameter: t_{DD}
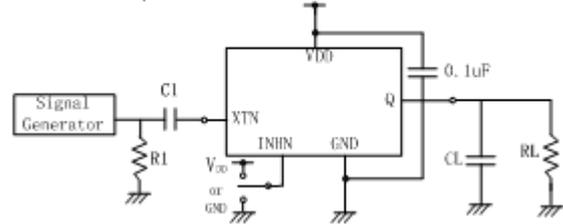
XTN input signal:1Vp-p, sina wave
C1: 0.001uF   CL:15pF
R1:50Ω   RL: 1KΩ

Measurement cct3
Measurement parameter: V_{OH}, V_{OL}
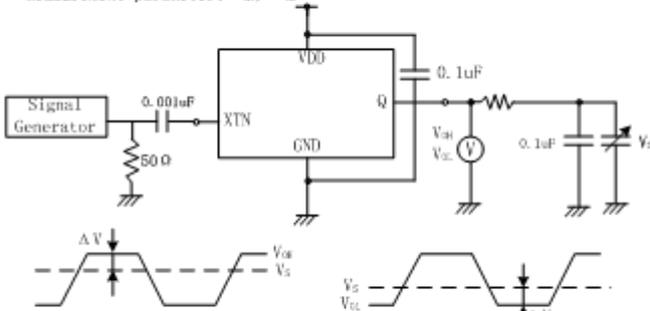
V_S adjusted such that $\Delta V=50\times I_{OH}$ V_S adjusted such that $\Delta V=50\times I_{OL}$

XTN input signal:1Vp-p, sina wave

Measurement cct4
Measurement parameter: V_{IH}, V_{IL}
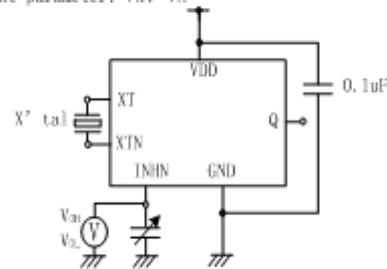
V_{IH}:Voltage is 0V to V_{DD} transition that changes the output state.
V_{IL}:Voltage is V_{DD} to 0V transition that changes the output state.
INHN has an oscillation stop function

Measurement cct5
Measurement parameter: I_Z
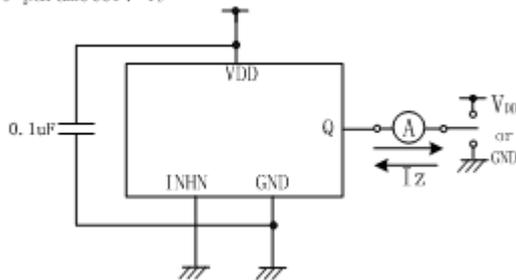
Measurement cct6
Measurement parameter: R_{UP1}, R_{UP2}

$R_{UP1}=\dfrac{V_{DD}}{I_{UP}}$ (V_{IN}=0V)

$R_{UP1}=\dfrac{V_{DD}-0.7V_{DD}}{I_{UP}}$ (V_{IN}=0.7) V_{DD}
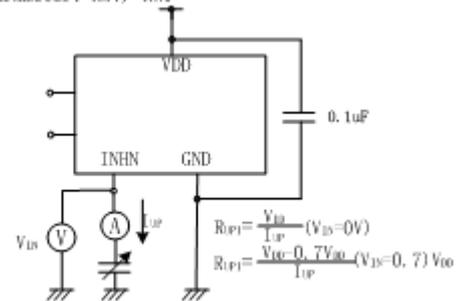
Notes

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