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Interleaved Two-Switch Forward Topology Featuring the ADP1046

FEATURES

Interleaved 2-switch forward switching power supply
12 V/25 A regulated output from 400 V dc input
Voltage feedback loop
Dynamic phase shedding
Integrated current balance between phases
I²C serial interface to PC
Software graphic user interface (GUI)
Programmable digital filters
7 PWM outputs including auxiliary PWM (for fan control)
Digital trimming
OrFET control for hot swap and redundancy
Current, voltage, and temperature sense through GUI
Digital current sharing

REFERENCE DESIGN CONTENTS

The evaluation system package contains the following items:

- User Guide UG-320
- ADP1046 300 W interleaved two-switch forward board

The USB-to-I²C dongle for serial communication (ADP1046-USB-Z) and the software CD must be ordered separately.

CAUTION

This evaluation board uses high voltages and currents. Extreme caution must be taken especially on the primary side to ensure safety for the user. It is strongly advised to power down the evaluation board when not in use. A current limited power supply is recommended as an input because no fuse is present on the board.

GENERAL DESCRIPTION

This evaluation board features the ADP1046 in a switching power supply application. With the evaluation board and software, the ADP1046 can be interfaced to any PC running Windows® 2000, Windows NT, or Windows XP via the computer's USB port. The evaluation board allows all the input and output functions of the ADP1046 to be exercised without the need for external components. The software allows control and monitoring of the ADP1046 internal registers. The board is set up for the ADP1046 to act as an isolated switching power supply with a rated load of 12 V/25 A from an input voltage ranging from 350 V dc to 400 V dc.

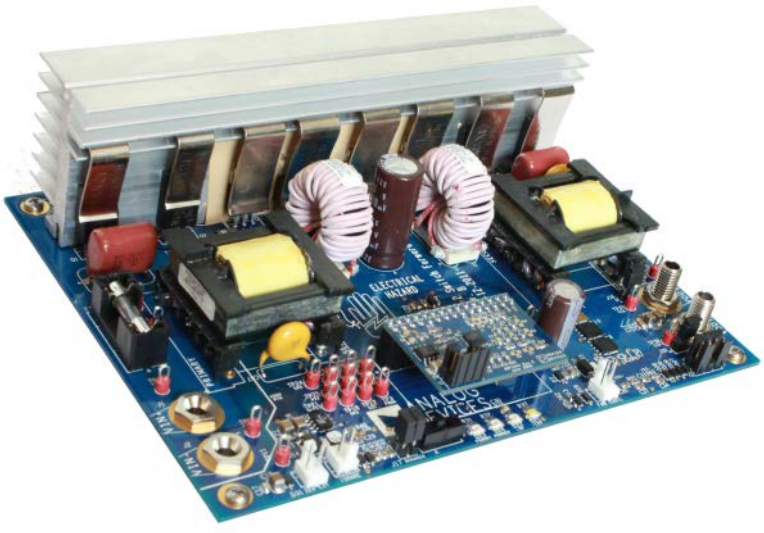

Figure 1. Picture of Printed Circuit Board

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REVISION HISTORY

8/12—Rev. 0 to Rev. A

Added Figure 74; Renumbered Sequentially ... 30
Change to Table 6 ... 40

4/12—Revision 0: Initial Version

DEMO BOARD SPECIFICATIONS

Table 1. Target Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_{IN}	350	385	400	V	
V_{OUT}	10.8	12	13.2	V	
I_{OUT}	0.0	25	25	A	With 300 LFM air flow
T_A	0	50	50	°C	Ambient temperature
Efficiency		91.5%		%	Typical reading at 385 V/25 A load
Switching frequency		148.8		kHz	
Output Voltage Ripple			100	mV	At 25 A load

TOPOLOGY AND CIRCUIT DESCRIPTION

This user guide describes the ADP1046 in a typical dc-to-dc switching power supply in an interleaved two-switch forward topology with synchronous rectification. Figure 75 and Figure 76 show the schematics of the main power stage and the peripheral connections, respectively. The daughter card schematic is shown in Figure 77. The circuit is designed to provide a rated load of 12 V/25 A from an input voltage source of 350 V dc to 400 V dc. The ADP1046 is used to provide functions such as output voltage regulation, output overcurrent protection, primary cycle-by-cycle protection, load current sharing with multiple power supplies over the share bus, and overtemperature protection.

The interleaved two-switch forward topology is essentially two two-switch forward designs running 180 degrees out of phase in parallel with each other.

The primary side consists of the input terminals (J1, J2), switches (Q1/Q2 for Phase 1, Q3/Q4 for Phase 2), the current sense transformer (T3 for Phase 1 and T4 for Phase 2) and the main power transformer (T1 for Phase 1 and T2 for Phase 2). The ADP1046 (U1 on the daughter card) resides on the secondary side and is powered via the USB 5 V with an ADP3303 LDO (U2 on the daughter card) present on the same daughter card. The gate signal for the primary switches comes from the ADP1046 through the MOSFET driver (U1) and passes through pulse transformers (T5 for Phase 1 and T6 for Phase 2). Diodes (D1/D2 for Phase 1 and D3/D4 for Phase 2) are responsible for circulating the magnetizing current of the transformer through the dc source during the off period of the switch and for clamping the maximum output voltage. C1 and C21 act as decoupling capacitors, and Y capacitors (C67, C68) reduce common-mode noise.

The secondary side power stage consists of the synchronous rectifiers (Q5 for Phase 1 and Q6 for Phase 2) and freewheeling FETs (Q7 for Phase 1 and Q9 for Phase 2). The RC series connections (R2/C2, R4/C4, R25/C22, R3/C3) act as snubbers for these FETs. The secondary-side FETs are driven by U2 and U3, which are 4 A drivers with a UVLO of 4.2 V (typical). Also present on the secondary side are the output filter inductors (L1 for Phase 1 and L2 for Phase 2) and the output capacitors (C10 and C8) placed before the OrFET (Q8, Q10). Capacitors (C15, C16) provide high frequency decoupling to lower EMI.

The OrFETs are driven by a diode (D7) and a capacitor (C13) that form a peak detector on the switch node of the transformer. The OrFET turn-off is through the GATE pin connected to the FET (Q14) that pulls the gate of the OrFET low, turning it off.

The output load current is sensed using resistors (R5, R8). Alternatively, they can also be replaced by using the Rds_on of the OrFETs (open R26 and R16, and short R38 and R39 with 5.5 kΩ/0.01% Resistors R3 and R4 on the daughter card). The output voltage is sensed at VS1 and VS2 for OrFET control and V_{OUT} for output load regulation. Jumpers (J18, J20) can be used for remote sensing.

The primary current is sensed through the CS1 pin. A Zener diode (D17) protects the pin from exceeding its absolute maximum rating. A thermistor (RTD1) is placed on the secondary side between Q7 and Q9 and acts as thermal protection for the power supply. A 20 kΩ resistor is placed in parallel with the thermistor that allows the software GUI to read the temperature directly in degrees Celsius.

The ADP1046 also features a line feedforward functionality. The switch node on the secondary side of the transformer (T1) is filtered through an RCD filter (R56, C25, D10), and a fraction of the voltage is fed into the ACSNS pin.

Also present on the secondary side is the current sharing circuitry, flag LEDs (D11 to D12), and the communications port to the software through the I^2C bus. There is a 4-pin connector for I^2C communication. This allows the PC software to communicate with the evaluation board (and with other evaluation boards through the extra 4-pin connectors) through the USB port of the PC. The user can easily change register settings on the ADP1046 and monitor the status registers. It is recommended that the USB dongle be connected directly to the PC, not via the external hub.

Instead of using an auxiliary supply, the board uses an on-board boost converter that converts the 5 V from the USB to the 12 V that powers the MOSFET drivers. Alternatively, an external 12 V connector (J6) is also present. During normal operation, the drivers are powered from the main 12 V output after the output is in regulation. The 5 V is input from the USB port and generates 3.3 V using an LDO for the ADP1046 .

The board also has a connector for a fan capable of driving ~12 V/300 mA from the main 12 V output terminal. The fan is driven by the OUTAUX PWM signal and is duty cycle modulated, providing maximum speed at maximum load.

ADVANTAGES OF INTERLEAVING

The interleaved two-switch forward (I2SF) topology is popular for its ruggedness. Because the primary switches of the two-switch forward converter are turned on and off at the same instant, this topology is free of shoot-through problems associated with other topologies such as the full bridge. With an interleaved design, care must be taken not to turn on the synchronous rectifiers (Q5 and Q7, or Q6 and Q9) while their respective primary switches are on. Interleaving technology improves circuit efficiency, reduces current ripple generated at the output, and increases its effective ripple frequency. This allows for reduction of the output filter capacitor. The interleaving approach can also significantly reduce the input filter inductor and capacitor requirement and improve dynamic response.

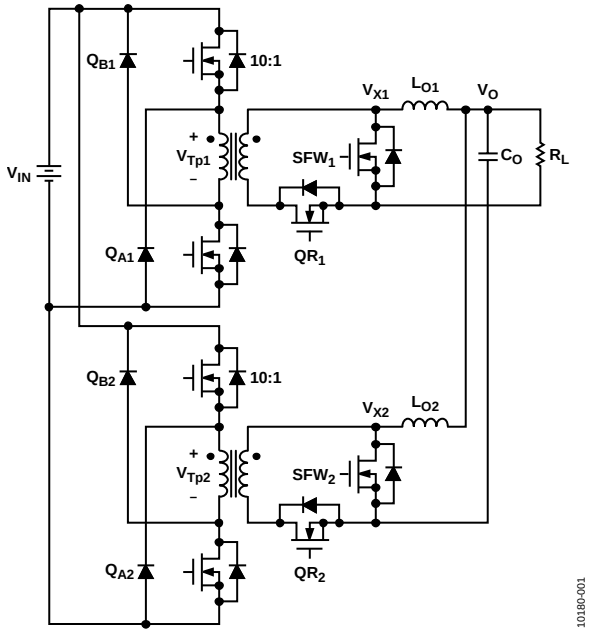

Figure 2. Topology of the Interleaved Two-Switch Forward Converter

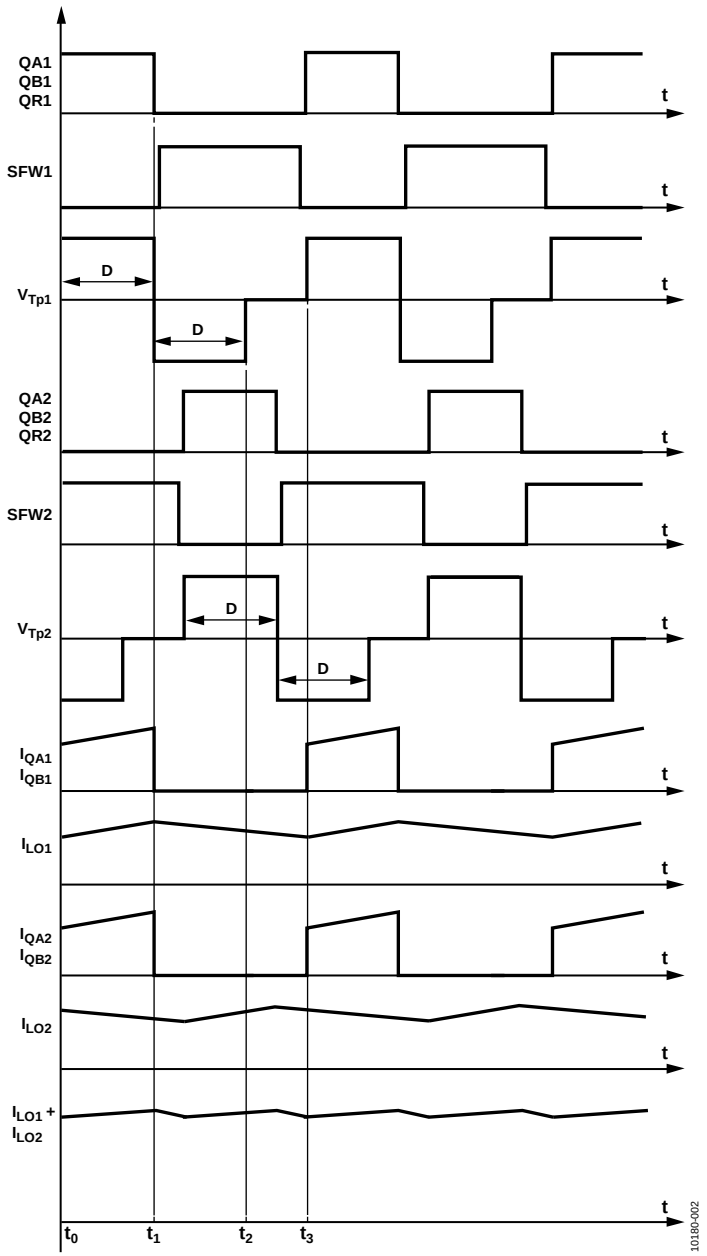

Figure 3. Summary of Key Waveforms for I2SF Topology

The key waveforms are illustrated in Figure 3. For the first phase of the two-switch forward converter, the operation can be simplified into three modes:

- Energy transfer stage (t_0 to t_1): Both primary-side switches (QA1, QB1) and the secondary-side rectifier switch (QR1) are turned on and energy is transferred from input to output
- Transformer reset stage (t_1 to t_2): In this stage, two primary-side diodes (or body diodes) conduct and apply reversed input voltage to the transformer winding to reset the transformer, while the secondary side is freewheeling (SFW2 is on).
- Dead time stage (t_2 to t_3): When the transformer is completely reset, the converter goes to the dead time stage with no current in the primary side, while the secondary-side current continues to freewheel.

The second phase operates in a similar pattern but with a 180° phase shift in the PWMs.

CONNECTORS

Table 2 lists the connectors on the board.

Table 2. Board Connectors

Connector	Evaluation Board Function
J1/J2	+400 V/−400 V input
J3/J4	+12 V/−12 V output
J6	External 12 V
J19	Fan connector
J10	I^2C connector
J7	Digital share Bus
J5	Daughter card connector

The pinout of the USB dongle is shown in Table 3.

Table 3. I^2C Connector Pin Descriptions

Pin No.	Evaluation Board Function
1	5 V
2	SCL
3	SDA
4	Ground

Figure 4. I^2C Connector (Pin 1 on Left)

SETTINGS FILES AND EEPROM

The ADP1046 communicates with the GUI software using the I²C bus.

The register settings (having extension .46r) and the board settings (having extension .46b) are two files that are associated with the ADP1046 software (see Appendix III—Register File (ADP1046_I2SF_032011.46r) and Appendix IV—Board File (ADP1046_I2SF_032011.46b)). The register settings file contains information such as the overvoltage and overcurrent limits, soft start timing, and PWM settings that govern the functionality of the part. The ADP1046 stores all settings in the EEPROM.

The EEPROM on the ADP1046 does not contain any information about the board, such as current sense resistor, output inductor, and capacitor values. This information is stored in a board setup file (extension .46b) and is necessary for the GUI to display the correct information in the **Monitor** window as well as the **Filter Settings** window (not shown). The entire status of the power supply, such as the ORFET and enable/disable of the synchronous rectifiers, primary current, output voltage, and output current, can thus be digitally monitored and controlled using software only. Always make sure that the correct board file is loaded for the board currently in use.

Each ADP1046 chip has trim registers for the temperature, input current, output voltage, output current, and ACSNS. These can be configured during production and are not overwritten whenever a new register settings file is loaded. This is done to retain the trimming of all the ADCs for that corresponding environmental and circuit condition (for example, component tolerances and thermal drift). A guided wizard called the **Auto Trim** can be used to trim the previously mentioned quantities of the trim registers (for example, temperature, input current, output voltage) so that the measurement value matches the values displayed in the GUI, which allows ease of control through the software. Click **Voltage Settings** or **CS2 Settings** in the **Setup** window (see Figure 9) to access the **Auto Trim** wizard.

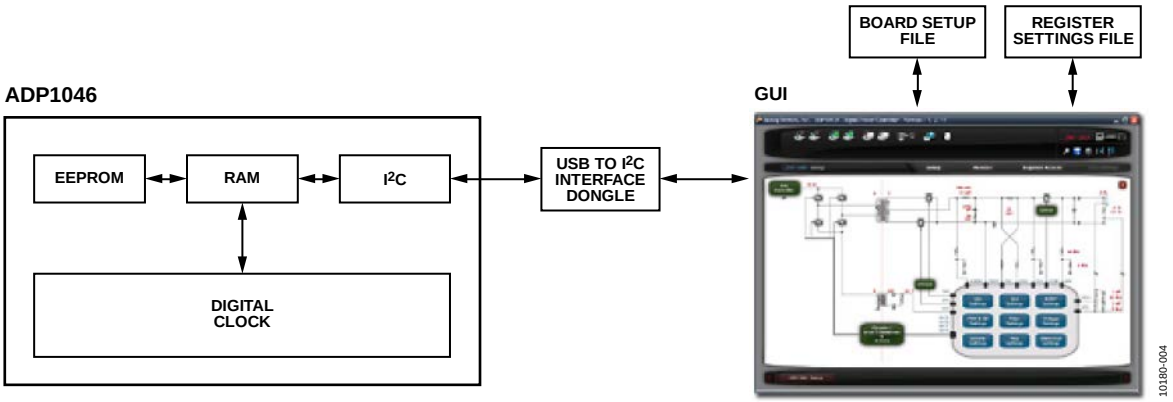

Figure 5. ADP1046 and GUI Interaction

EVALUATION BOARD

EQUIPMENT

- DC power supply (350 V to 400 V, 400 W)
- Electronic load (25 A/300 W)
- Oscilloscope with differential probes
- PC with ADP1046 GUI installed
- Precision digital voltmeters (HP34401or equivalent) for measuring dc voltage

SETUP

Do not connect the USB cable to the evaluation board until the software has finished installing.

1. Install the ADP1046 software by inserting the installation CD. The software setup starts automatically, and a guided process installs the software as well as the drivers for the USB-to-I²C adapter, which allows communication of the GUI with the IC.
2. Insert the daughter card into Connector J5, as shown in Figure 6.
3. Ensure that the PSON switch (SW1 on schematic; see Figure 76) is turned to the off position. It is located on the bottom left half of the board.
4. Connect one end of the USB dongle to the board and the other end to the USB port on the PC using the USB-to-I²C interface dongle. The white LED, D21, should turn on.

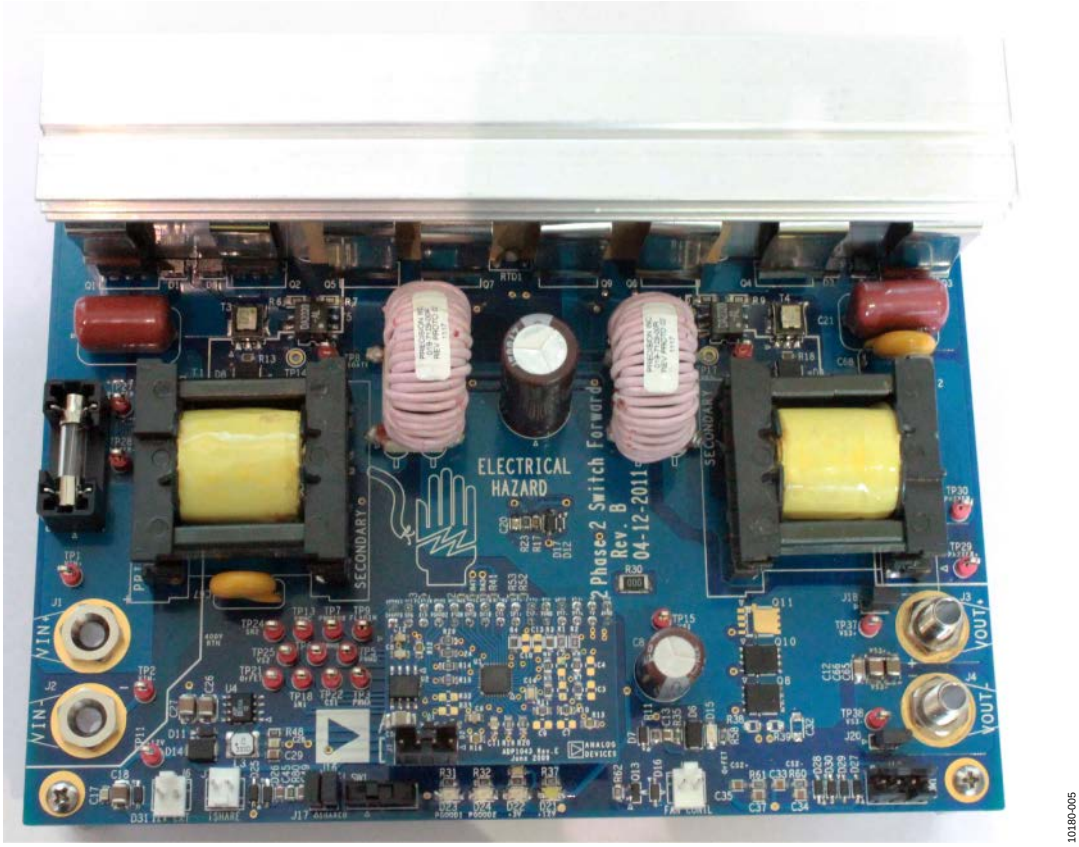

Figure 6. Printed Circuit Board with Daughter Card

5. The software should report that the ADP1046 has been located on the board. Click **Finish** to proceed to the main software interface setup window (see Figure 9). The serial number shown next to the checkbox (see Figure 7) indicates the USB dongle serial number. The windows also displays the device I²C address.

Figure 7. ADP1046 Address of 0x50 in the GUI

6. If the software does not detect the part, it enters simulation mode. Ensure that the connecter is connected to J10 (on the main board) or J7 (on the daughter card). Click the **Scan Now** icon (see Figure 8).

7. Click the **Store Board Settings to EEPROM** icon (see Figure 8), and select the **ADP1046_I2SF_B_xxx.46b** file. This file contains all the board information, including the values of the shunt and voltage dividers. Note that all board setting files have an extension of .46b.

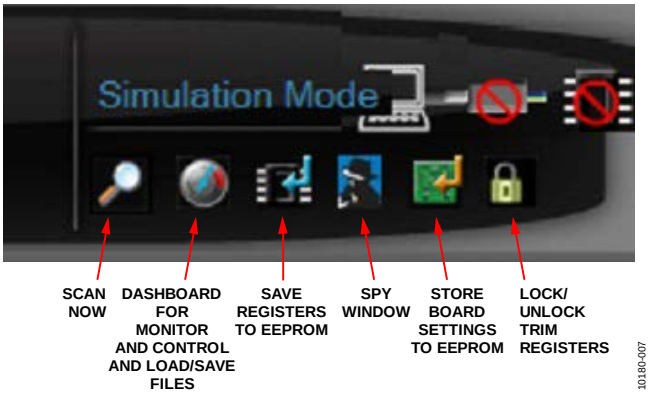

Figure 8. Scan for ADP1046 Now Icon

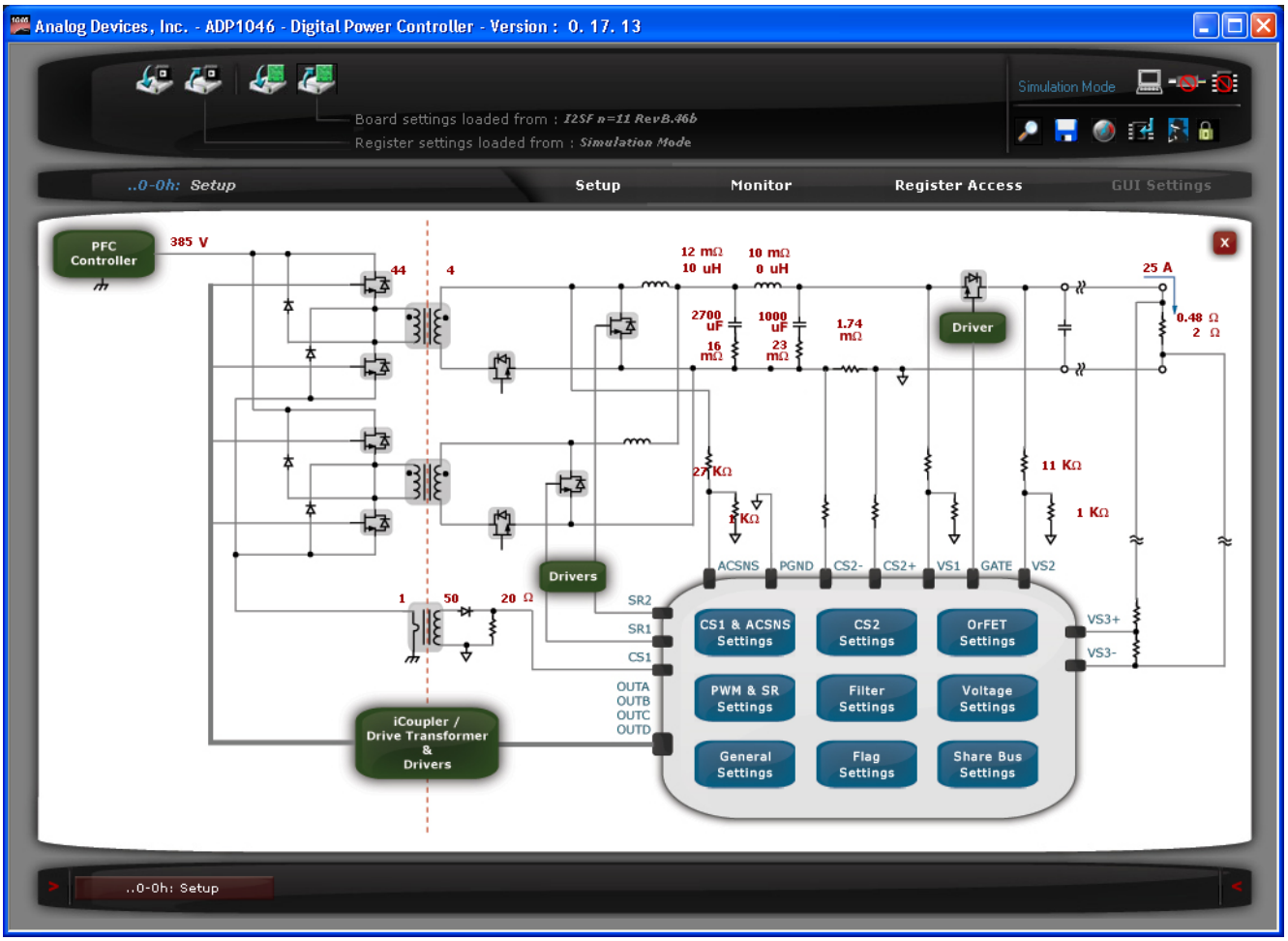

Figure 9. Main Setup Window of the ADP1046 GUI

8. The original register configuration is stored in the **ADP1046_I2SF_B_xxxx.46r** register file. (Note that all register files have an extension of .46r.) The file can be loaded using the second icon from the left in Figure 10. The IC on the board is preprogrammed, and this step is optional.
9. Connect a dc power source (385 V dc nominal, current limit to ~1 A) and an electronic load set to 1 A at the output.
10. Connect a voltmeter at the TP37 and TP38 test points. Ensure that the differential probes are used and that the ground of the probes are isolated if oscilloscope measurements are made on the primary side of the transformer.
11. Turn the PSON switch (SW1 on schematic; see Figure 76) to the on position. Then click the dashboard settings icon (2nd icon from the left in Figure 8), and turn on the software via PSON.
    The board should now be operational and ready for evaluation. The output should read 12 V dc.
12. Click the **Monitor** tab and then the **Flags and Readings** button (not shown) to load the entire state of the power supply unit (PSU) in a single user-friendly window (see Figure 11).
13. After successful startup and the board is in a steady state condition, LEDs on the board provide the status of the board. All the LEDs turn on, indicating that there are no faults detected, such as overvoltage or overcurrent. In case of a fault, the PGOOD1 or PGOOD2 LED turns off, indicating that a flag has tripped due to an out of bounds condition. The **Flags and Readings** window displays the appropriate state of the PSU.

Table 4. List of LEDs on the Evaluation Board

LED	Description
D23 (Red)	PGOOD1 signal (active low)
D24 (Red)	PGOOD2 signal (active low)
D15 (Red)	Indicates OrFET is turned on
D12 (White)	12 V from auxiliary boost

BOARD SETTINGS

The board settings can be accessed from the main setup window (see Figure 9).

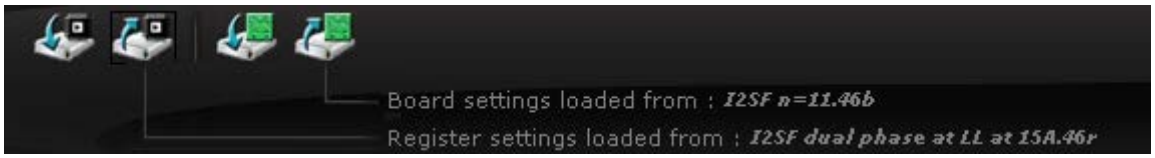

Figure 10. Different Icons on Dashboard for Loading and Saving .46r and .46b Files

Figure 11. Flags and Readings Window in GUI Showing the Entire Status of the PSU at Full Load

THEORY OF OPERATION

DURING STARTUP

The following steps briefly describe the start-up procedure of the ADP1046 and the power supply and operation of the state machine for the preprogrammed set of registers that are included in the design kit.

1. After VDD (3.3 V) is applied to the ADP1046, it takes approximately 20 µs for VCORE to reach 2.5 V. The digital core is now activated and the contents of the registers are downloaded in the EEPROM. The ADP1046 is now ready for operation.
2. PSON is applied. The power supply begins the programmed soft start ramp of 80 ms only when the logical AND of hardware and software PSON is true (programmable).
3. Because the soft start from precharge setting is active, the output voltage is sensed before the soft start ramp begins. Depending on the output voltage level of the effective soft start, the ramp is reduced by the proportional amount.
4. The OrFET power-on is dependent on the voltage difference of VS1 and VS2. If the PSU is standalone, the OrFET gate turns on at the beginning of the soft start ramp when VS1 − VS2 is less than or equal to the programmed threshold in the GUI (see the **OrFET Settings** window in the GUI, which is accessed by clicking **OrFET Settings** in Figure 9). The output regulation is from VS3, and the normal filter is in operation.
   If the PSU is starting into a live bus already at 12 V, the OrFET turns on only at the end of the soft start ramp when the internal (or local) output voltage (VS1) climbs close to the regulation point and VS1 − VS2 is greater than the programmed threshold (threshold being a negative value ranging from −384 mV to 0 mV). Prior to this, the soft start filter is active, and the regulation/feedback path is through VS1. When the OrFET turns on (GATE pin signal is toggled), the feedback path is through VS3 and the compensation filter changes to normal mode or light load filter (depending on the load and light load threshold) in a time determined by the filter transitioning speed (programmable 1 to 32 switching cycles).
5. The PSU is now running in a steady state and, depending on the load condition, one or both phases are active (second phase is on when the load current is greater than 14 A). PGOOD1 and PGOOD2 turn on after the programmed debounce.
6. If a fault is activated during the soft start or steady state, the corresponding flag is set and the programmed action is taken, such as PSU disable and reenable after 1 sec, SR power-off, OrFET disable, and OUTAUX disable.

DURING STEADY STATE

The MOSFET drivers are powered using the auxiliary boost converter from the main 12 V when the output is in regulation before PSON is applied.

The second phase is turned on only when the load current increases greater than 14 A. An asynchronous current detection on CS2 averages the load current every 75 µs, and the part exits light load mode.

If a fault such as a undervoltage protection (UVP), overvoltage protection (OVP), CS2 overcurrent protection (OCP), or CS1 OCP occurs, the programmed action such as disable OrFET or disable PWMs takes place after the debounce period. If the PSU shuts down, the soft start ramp is initiated after the programmed delay.

CONFIGURING FLAG SETTINGS

When a flag is triggered, the ADP1046 state machine waits for a programmable length of debounce time before taking any action. The response to each flag can be programmed individually. Click **Setup** and then **Flag Settings** (see Figure 9) to configure the flags. The **Flag Settings** window shows all the fault flags (if any) and the readings on one page (see Figure 12). The **Get First Flag** button (see Figure 11), which can be accessed by clicking the **Monitor** tab, determines the first flag that was set in case of a fault event.

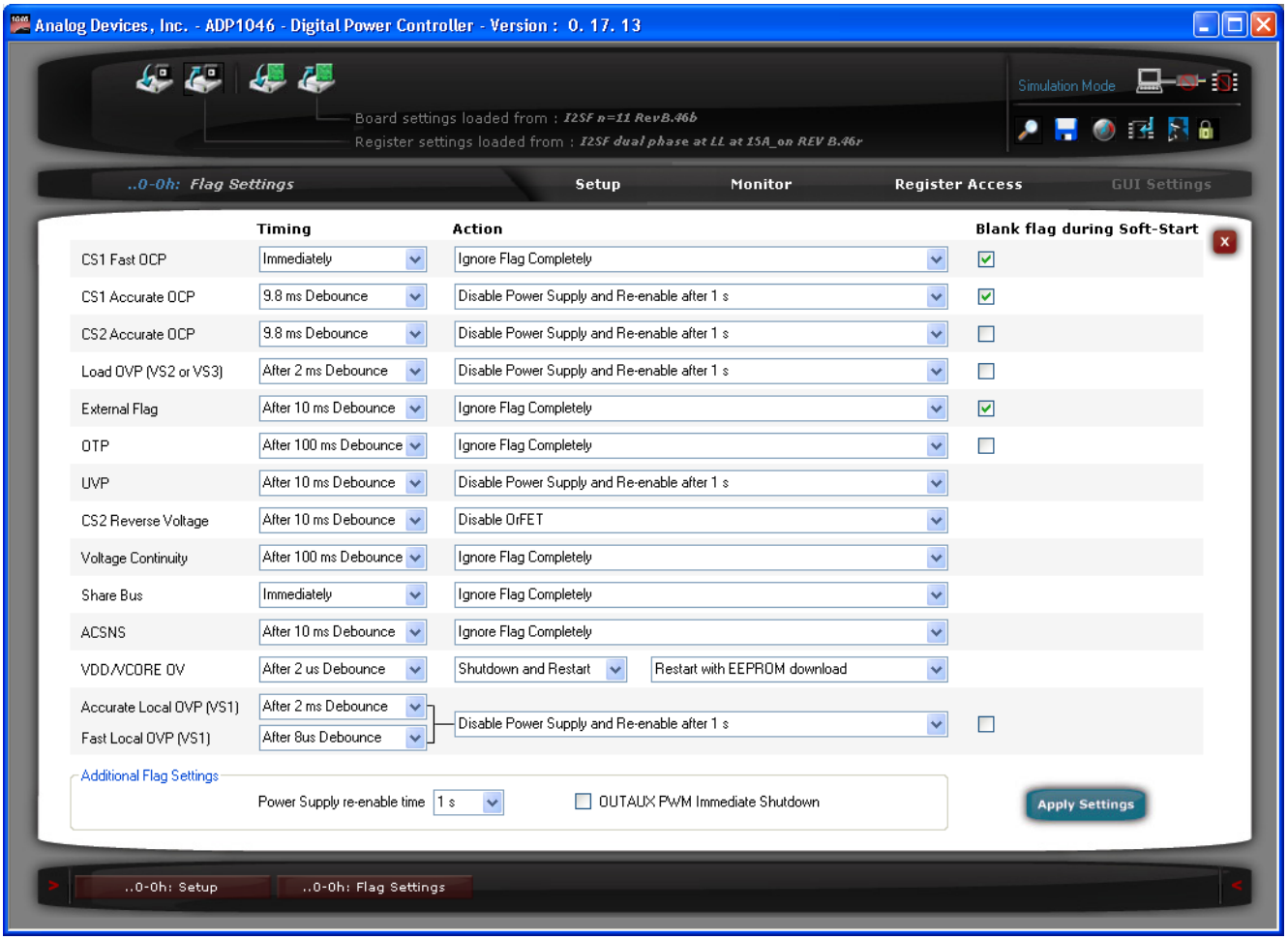

Figure 12. Flag Settings Window—Fault Configurations

PWM SETTINGS

The ADP1046 has a fully programmable PWM setup that controls seven PWMs. Due to this flexibility, the IC can function in several different topologies, such as any isolated buck derived topology, push-pull, and flyback.

The integrated volt-second balance feature is used as a current balancer of the two phases of the interleaved two-switch forward design. In other power conversion circuits such as full bridge, this feature can be used to eliminate the dc blocking capacitor.

Each PWM edge can be moved in 5 ns steps to achieve the appropriate dead time needed, and the maximum modulation limit sets the maximum duty cycle. This is displayed in Figure 13.

Click the **Monitor** tab and then **PWM & SR Settings** to access the PWM settings

Table 5. PWMs and Their Corresponding Switching Element

PWM	Switching Element Being Controlled
OUTA	Phase 1 primary switches
OUTB	Phase 1 synchronous rectifier
OUTC	Phase 1 freewheeling
OUTD	Phase 2 primary switches
SR1	Phase 2 synchronous rectifier
SR2	Phase 2 freewheeling
OUTAUX	Fan control

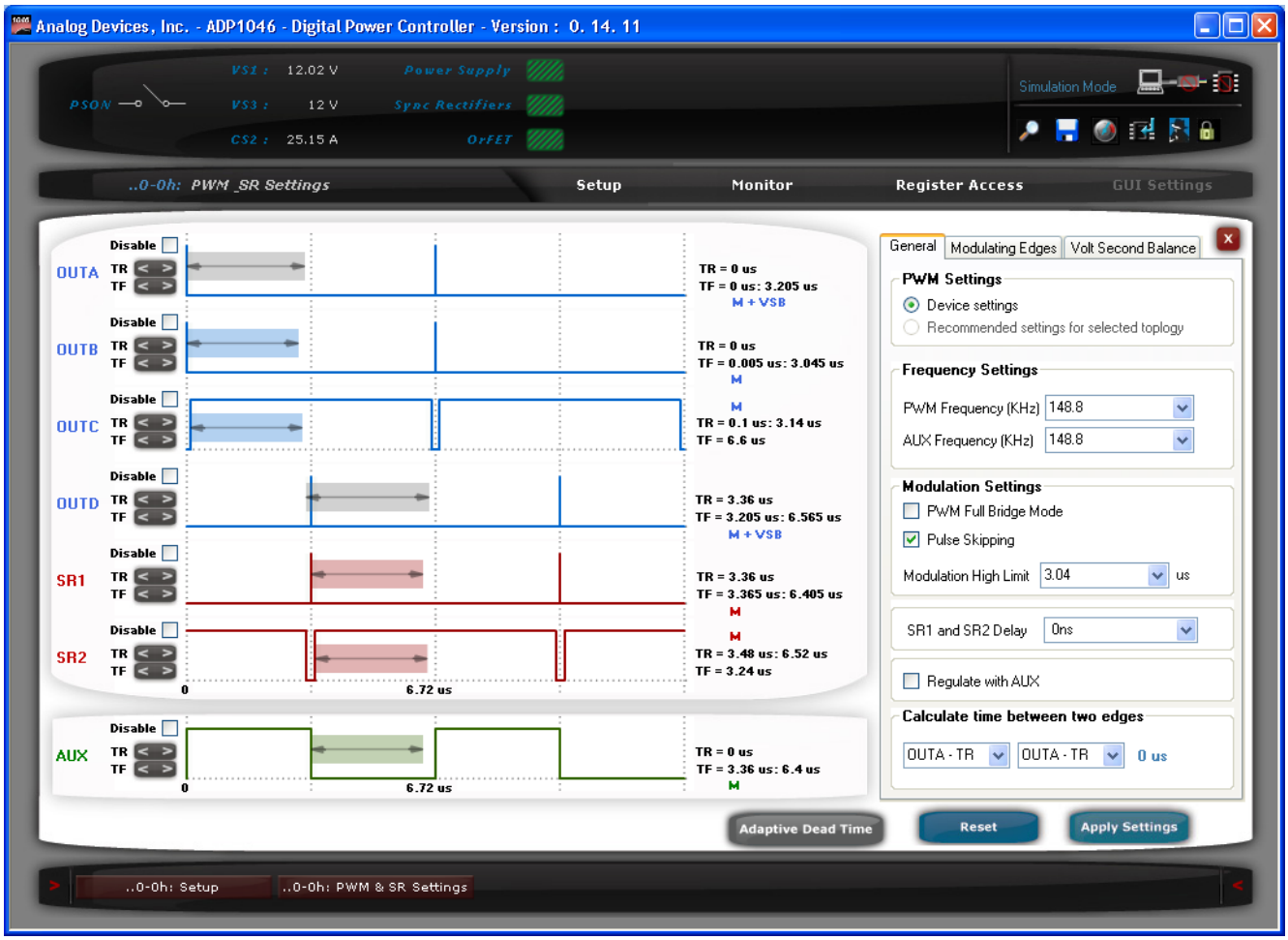

Figure 13. PWM Settings Window in the GUI

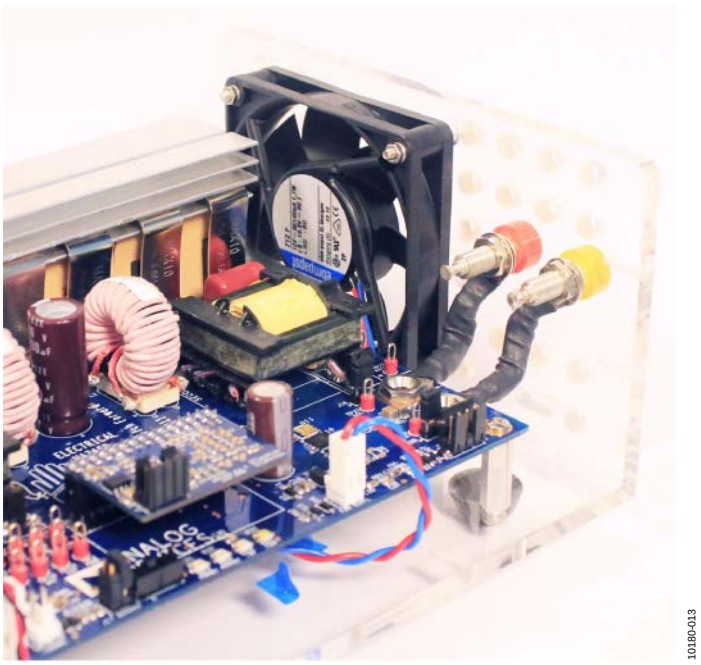

Figure 14. Fan Connection to Cool Heat Sink, Transformers, and Inductors

FAN CONTROL

The OUTAUX PWM is used to control an external fan connected to Connector J19. The average speed of the fan depends on the load. The PWM input to the fan is duty cycle modulated and is programmed with the main PWM output in a manner that provides the maximum speed at maximum load and vice versa. Note that the fan is not included in the kit.

DYNAMIC PHASE SHEDDING AND STANDBY POWER

Dynamic phase shedding is achieved using the light load feature of the ADP1046. This setting is programmed to activate within 75 µs of detecting the output current via the CS2+ and CS2− pins. The IC is programmed to enter dual phase mode at 60% of the full load current and automatically turns off the PWMs for the second phase when the load current is less than approximately 54% of the full load current.

Using an external microcontroller to communicate to the IC, the ADP1046 can also disable the synchronous rectifiers and save more power at no load by entering the pulse skipping mode, where the entire PWM pulse is skipped if the required duty cycle is less than the programmed value.

BOARD EVALUATION AND TEST DATA

STARTUP

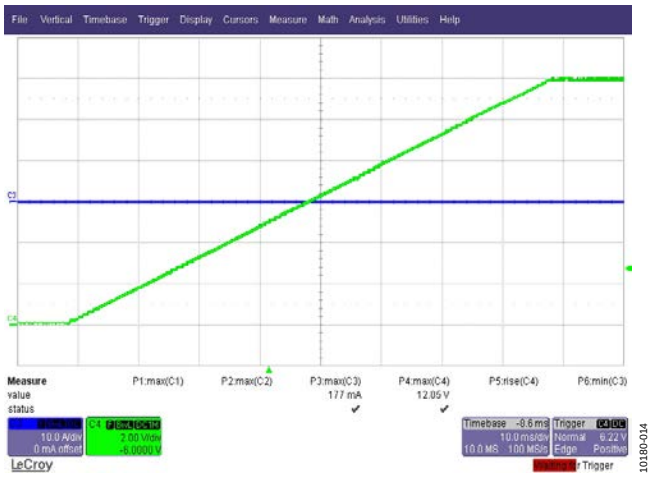

Figure 15. Startup at 350 V DC, No Load
Green Trace: Output Voltage, 2 V/div, 10 ms/div
Blue Trace: Load Current, 10 A/div, 10 ms/div

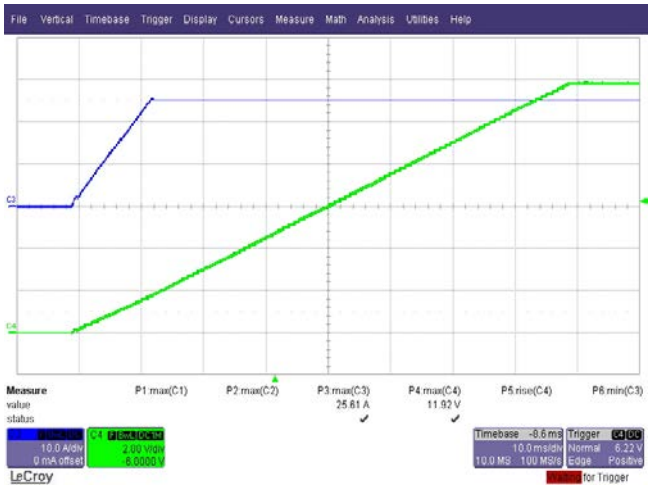

Figure 16. Startup at 350 V DC, 25 A Load (1 A/µs Slew Rate)
Green Trace: Output Voltage, 2 V/div, 10 ms/div
Blue Trace: Load Current, 10 A/div, 10 ms/div

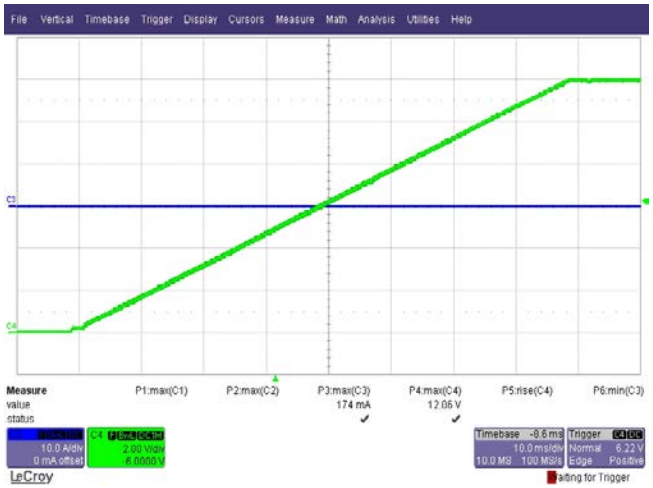

Figure 17. Startup at 385 V DC, No Load
Green Trace: Output Voltage, 2 V/div, 10 ms/div
Blue Trace: Load Current, 10 A/div, 10 ms/div

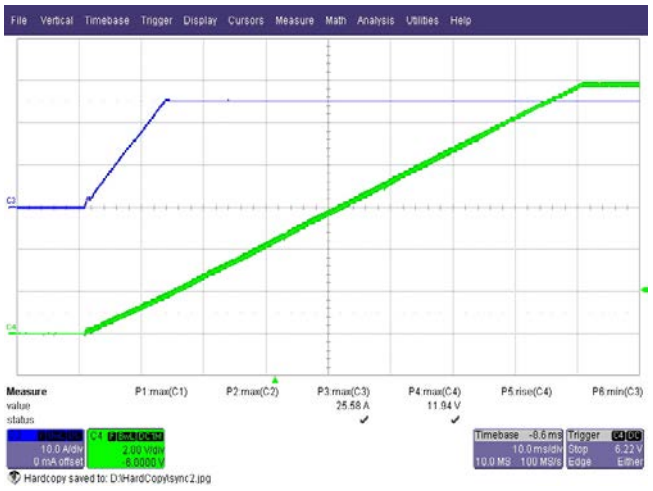

Figure 18. Startup at 385 V DC, 25 A Load (1 A/µs Slew Rate)
Green Trace: Output Voltage, 2 V/div, 10 ms/div
Blue Trace: Load Current, 10 A/div, 10 ms/div

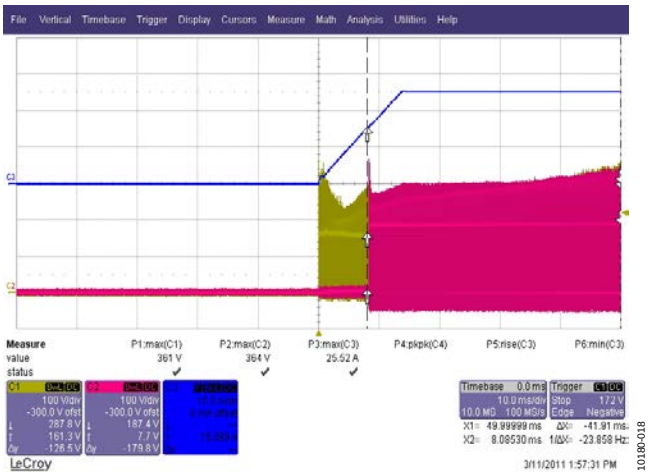

Figure 19. Startup at 350 V DC, Load (1 A/µs Slew Rate)
Yellow Trace: Phase 1 Drain Voltage on Q2, 100 V/div, 10 ms/div
Red Trace: Phase 2 Drain Voltage on Q4, 100 V/div, 10 ms/div
Blue Trace: Load Current, 10 A/div, 10 ms/div Cursor Showing Phase 2 Enabled at 15 A

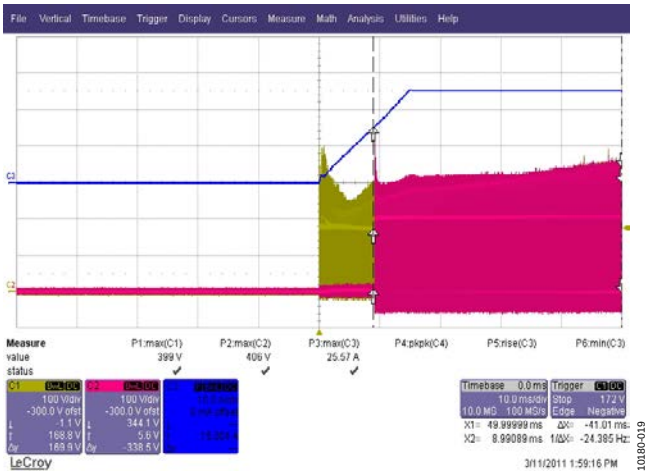

Figure 20. Startup at 385 V DC, Load (1 A/µs Slew Rate)
Yellow Trace: Phase 1 Drain Voltage on Q2, 100 V/div, 10 ms/div
Red Trace: Phase 2 Drain Voltage on Q4, 100 V/div, 10 ms/div
Blue Trace: Load Current, 10 A/div,
10 ms/div Cursor Showing Phase 2 Enabled at 15 A

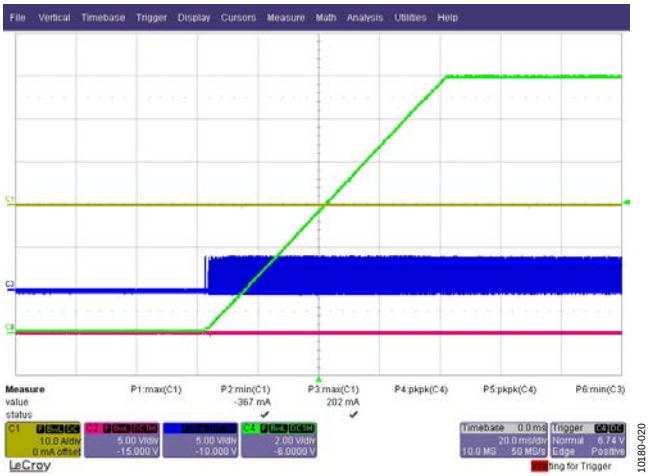

Figure 21. Synchronous Rectifier During Startup at No Load
Green Trace: Output Voltage, 2 V/div, 20 ms/div
Blue Trace: Phase 1 Synchronous Rectifier (OUTC), 5 V/div, 20 ms/div
Red Trace: Phase 2 Synchronous Rectifier (SR1), 5 V/div, 20 ms/div
Yellow Trace: Load Current, 10 A/div, 20 ms/div

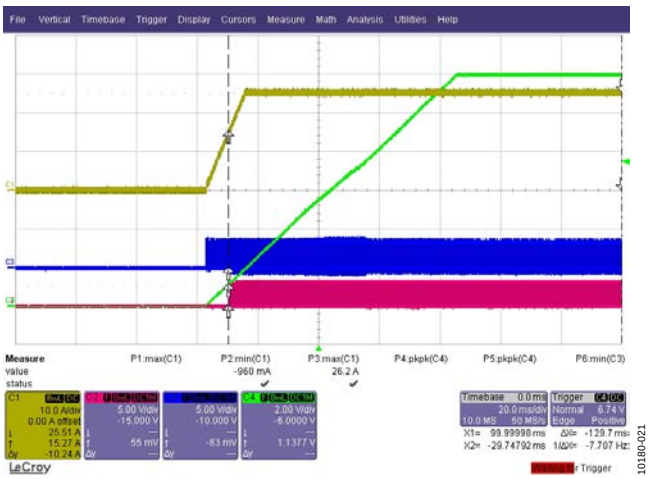

Figure 22. Synchronous Rectifier During Startup at 25 A Load
Green Trace: Output Voltage, 2 V/div, 20 ms/div
Blue Trace: Phase 1 Synchronous Rectifier (OUTC), 5 V/div, 20 ms/div
Red Trace: Phase 2 Synchronous Rectifier (SR1)
Turning On at 15 A, 5 V/div, 20 ms/div
Yellow Trace: Load Current, 10 A/div, 20 ms/div

TRANSFORMER PRIMARY WAVEFORM

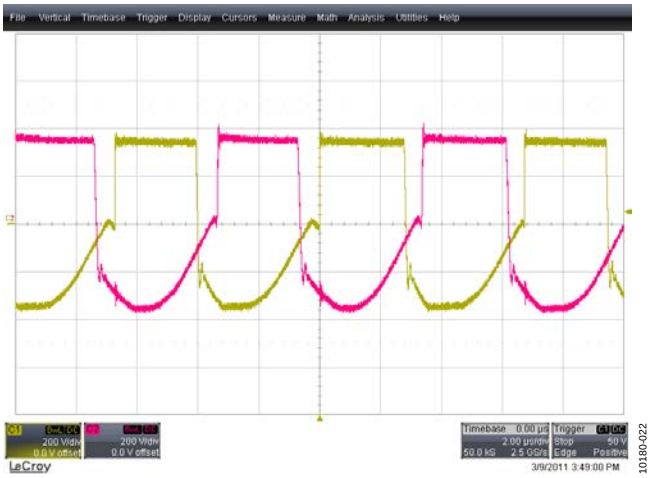

Figure 23. Transformer Primary Waveform at 25 A Load, 350 V DC
Red Trace: Voltage Across T1 Primary (Phase 1), 200 V/div, 2 µs/div
Yellow Trace: Voltage Across T2 (Phase 2), 200 V/div, 2 µs/div

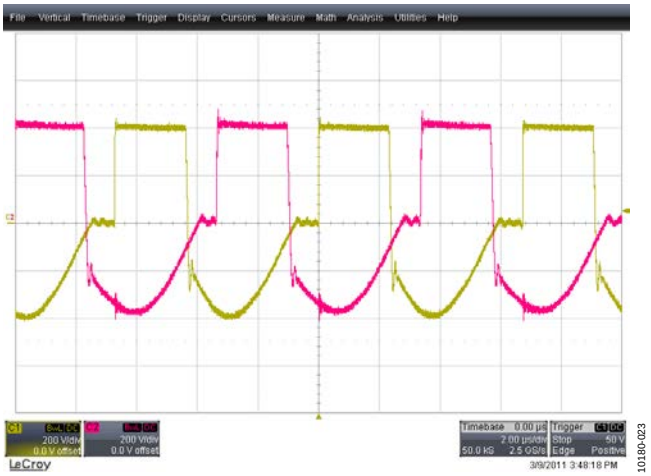

Figure 24. Transformer Primary Waveform at 25 A Load, 400 V DC
Red Trace: Voltage Across T1 Primary (Phase 1), 200 V/div, 2 µs/div
Yellow Trace: Voltage Across T2 (Phase 2), 200 V/div, 2 µs/div

PRIMARY CURRENT

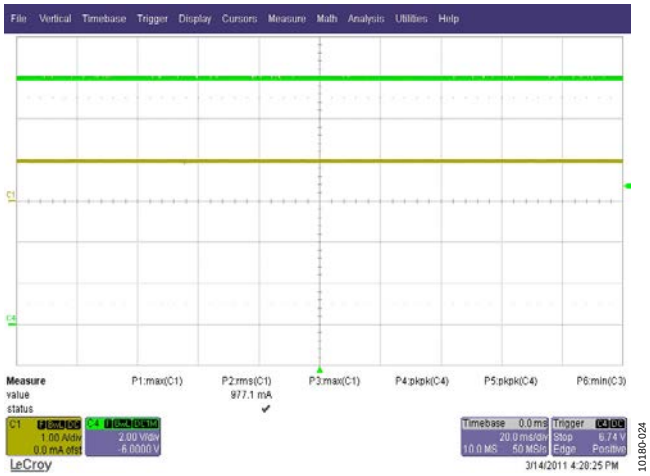

Figure 25. Input RMS Current at 25 A Load, 350 V DC
Yellow Trace: Primary Current, 1 A/div, 20 ms/div
Green Trace: Output Voltage, 2 V/div, 20 ms/div

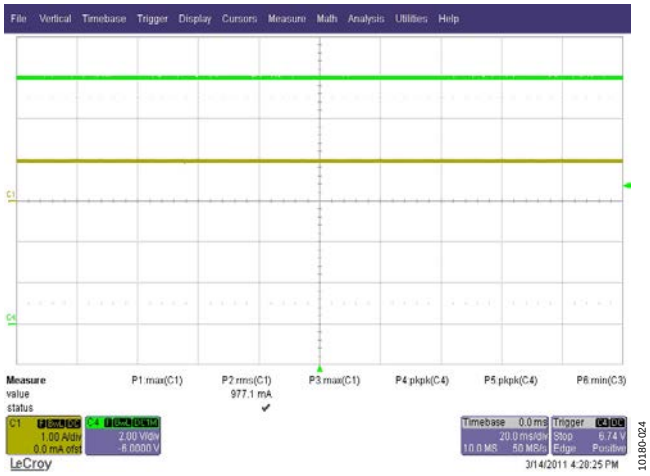

Figure 26. Input RMS Current at 25 A Load, 385 V DC
Yellow Trace: Primary Current, 1 A/div, 20 ms/div
Green Trace: Output Voltage, 2 V/div, 20 ms/div

DRAIN VOLTAGE AND CURRENT

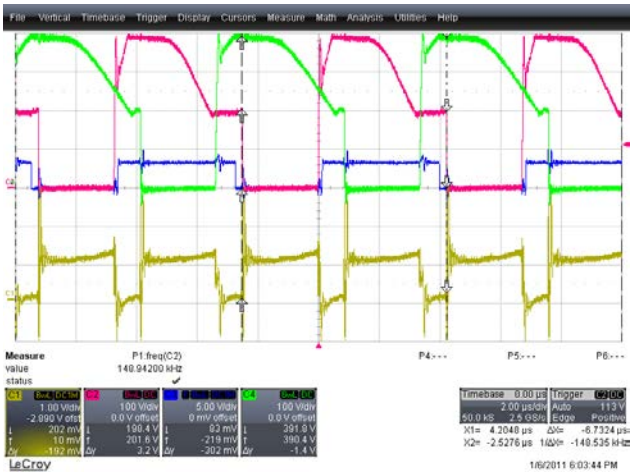

Figure 27. Drain Voltage at 25 A Load, 385 V DC
Red and Green Trace: Primary MOSFET Drain Voltage Across Q2 and Q4, 100 V/div, 2 µs/div
Yellow Trace: CS1 Pin Voltage, 1 V/div, 2 µs/div

CS1 PIN VOLTAGE AND CURRENT BALANCING OF PHASES

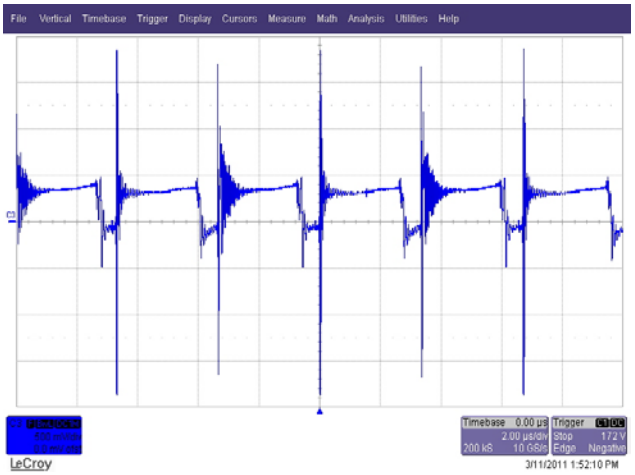

Figure 28. CS1 Pin Voltage at 25 A Load, 350 V DC, Current Balancing Enabled
Blue Trace: Voltage at CS1, 500 mV/div, 2 µs/div

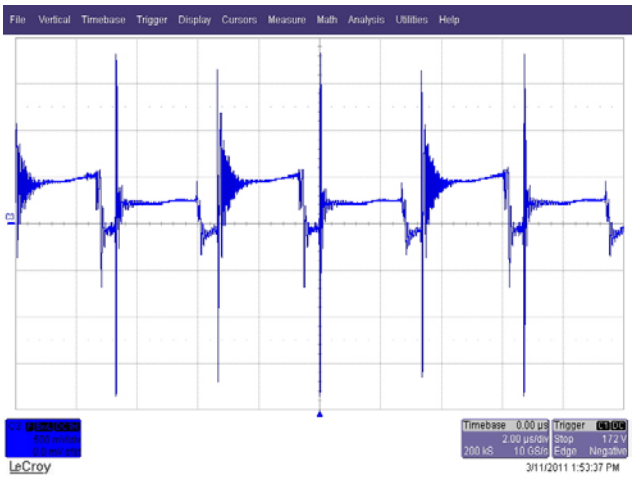

Figure 29. CS1 Pin Voltage at 25 A Load, 350 V DC, Current Balancing Disabled
Blue Trace: Voltage at CS1, 500 mV/div, 2 µs/div

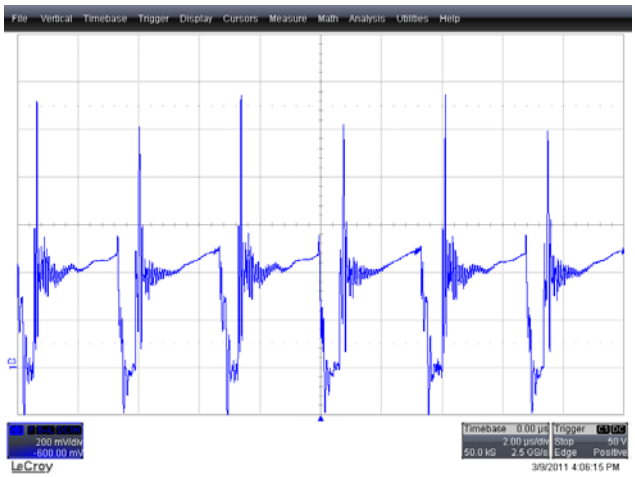

Figure 30. CS1 Pin Voltage at 25 A Load, 385 V DC, Current Balancing Enabled
Blue Trace: Voltage at CS1, 500 mV/div, 2 µs/div

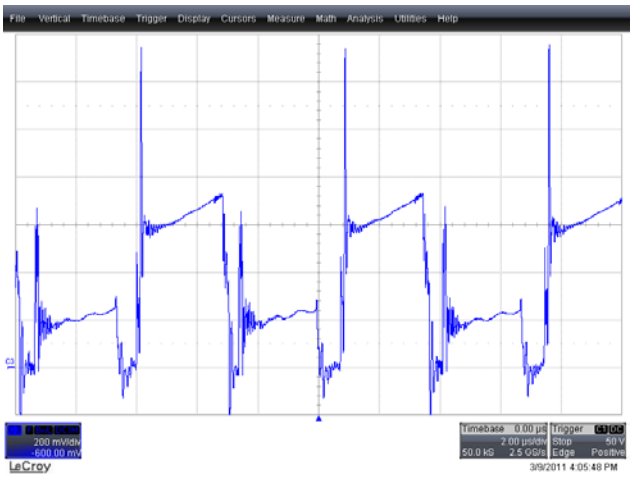

Figure 31. CS1 Pin Voltage at 25 A Load, 385 V DC, Current Balancing Disabled
Blue Trace: Voltage at CS1, 500 mV/div, 2 µs/div

SYNCHRONOUS RECTIFIER PEAK INVERSE VOLTAGE (PIV)

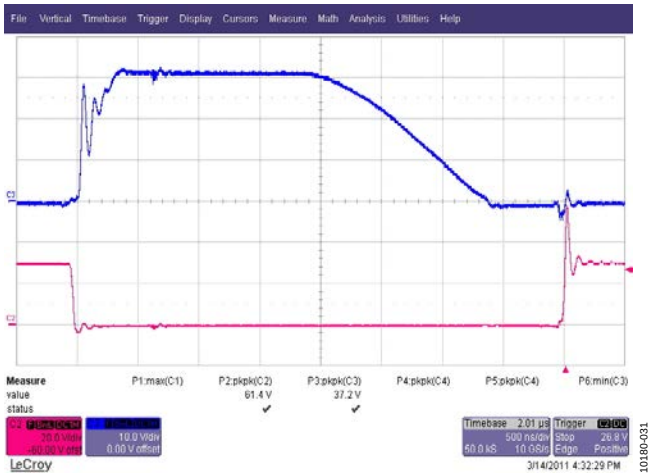

Figure 32. Synchronous Rectifier and Freewheeling MOSFET PIV at 25 A Load, 350 V DC
Blue Trace: Synchronous Rectifier, 10 V/div, 500 ns/div
Red Trace: Freewheeling FET Voltage, 20 V/div, 500 ns/div

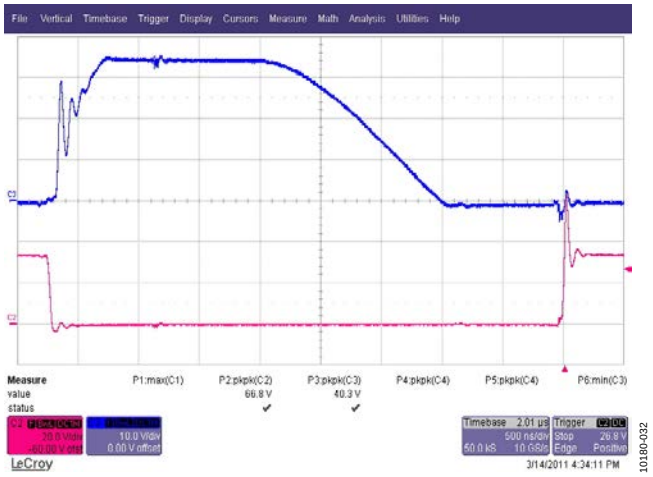

Figure 33. Synchronous Rectifier and Freewheeling MOSFET PIV at 25 A Load, 385 V DC
Blue Trace: Synchronous Rectifier, 10 V/div, 500 ns/div
Red Trace: Freewheeling FET Voltage, 20 V/div, 500 ns/div

OUTPUT RIPPLE

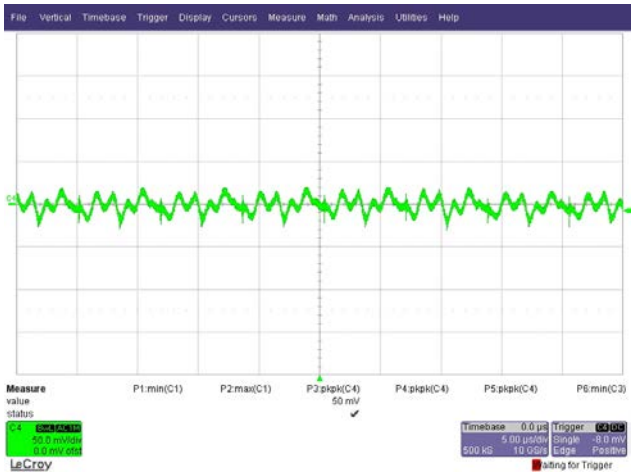

Figure 34. Output Voltage at C65 (AC-Coupled), 350 V DC, 25 A, 50 mV/div, 5 µs/div, High Frequency Component

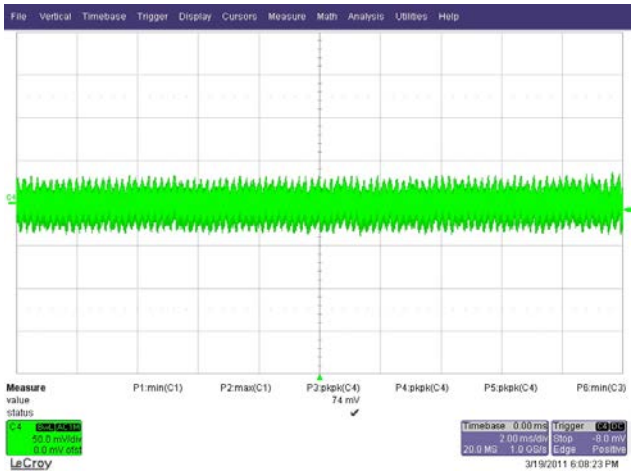

Figure 35. Output Voltage at C65 (AC-Coupled), 350 V DC, 25 A, 50 mV/div, 2 ms/div, Low Frequency Component

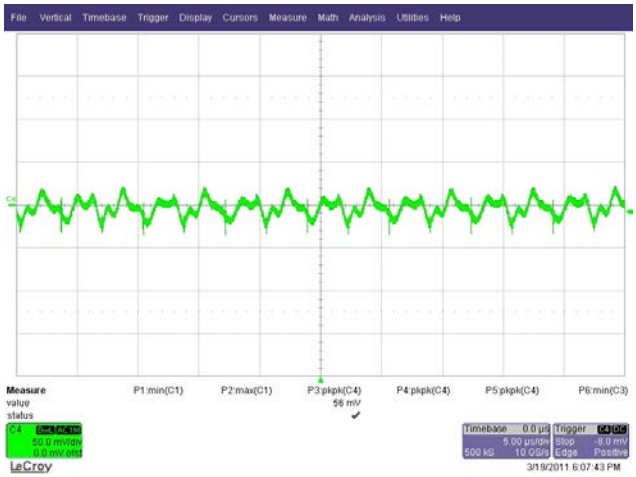

Figure 36. Output Voltage at C65 (AC-Coupled), 385 V DC, 25 A, 50 mV/div, 5 µs/div, High Frequency Component

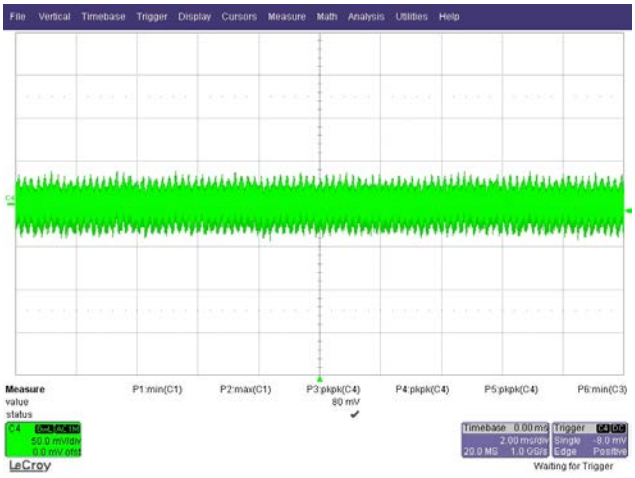

Figure 37. Output Voltage at C65 (AC-Coupled),
385 V DC, 25 A, 50 mV/div, 2 ms/div, Low Frequency Component

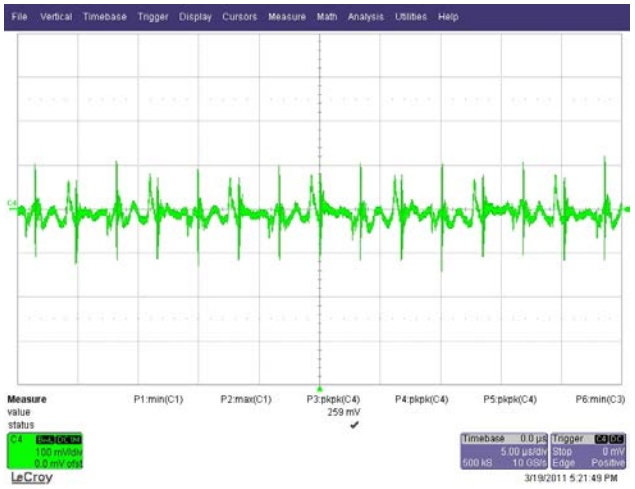

Figure 38. Output Voltage at 2700 µF Capacitor C10 (AC-Coupled),
385 V DC, 25 A, 100 mV/div, 5 µs/div, High Frequency Component

TRANSIENT VOLTAGE

Load Step of 0% to 25%

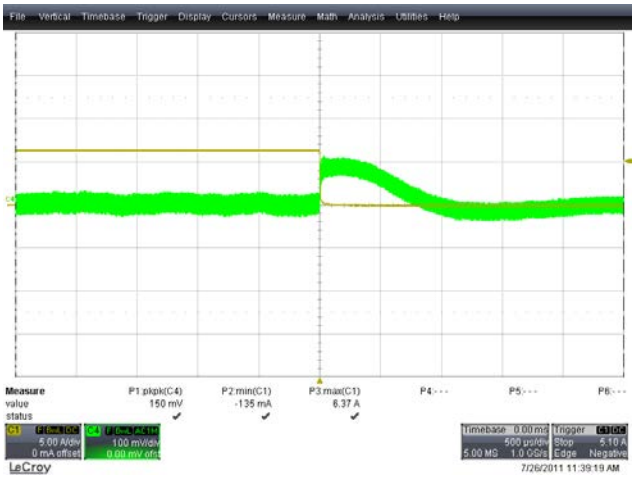

Figure 39. Output Voltage Transient, 25% to 0% Load,
385 V DC, One Phase Only
Yellow Trace: Load Current, 5 A/div, 500 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 500 µs/div

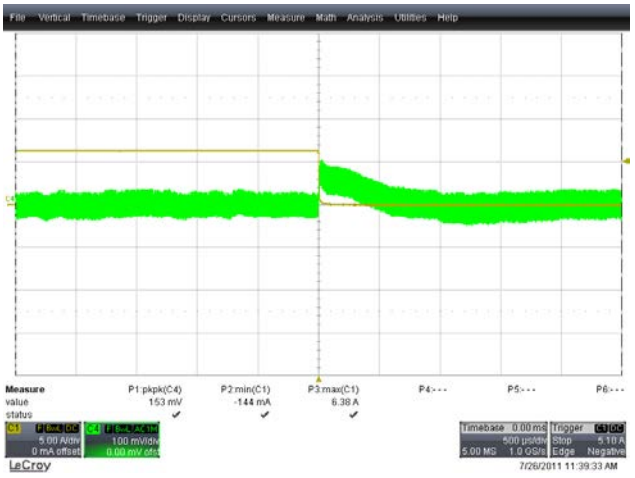

Figure 40. Output Voltage Transient, 25% to 0% Load,
385 V DC, Both Phases Active
Yellow Trace: Load Current, 5 A/div, 500 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 500 µs/div

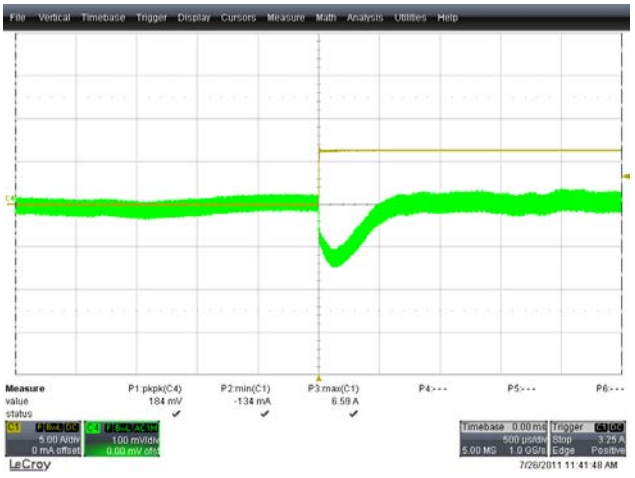

Figure 41. Output Voltage Transient, 0% to 25% Load,
385 V DC, One Phase Only
Yellow Trace: Load Current, 5 A/div, 500 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 500 µs/div

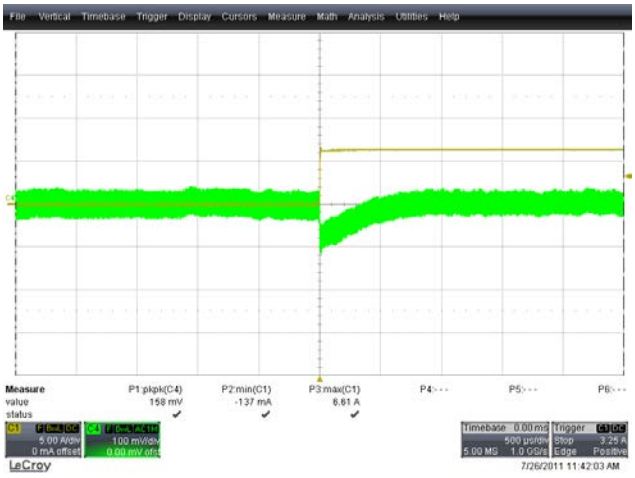

Figure 42. Output Voltage Transient, 0% to 25% Load,
385 V DC, Both Phases Active
Yellow Trace: Load Current, 5 A/div, 500 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 500 µs/div

Load Step of 25% to 50%

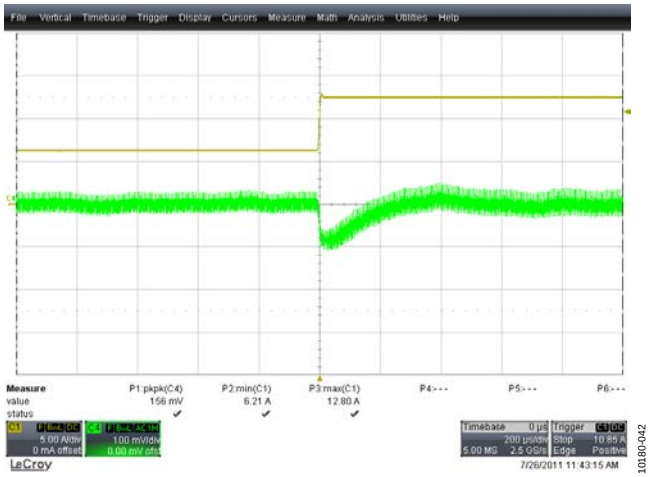

Figure 43. Output Voltage Transient, 25% to 50% Load, 385 V DC, One Phase Only
Yellow Trace: Load Current, 5 A/div, 200 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 200 µs/div

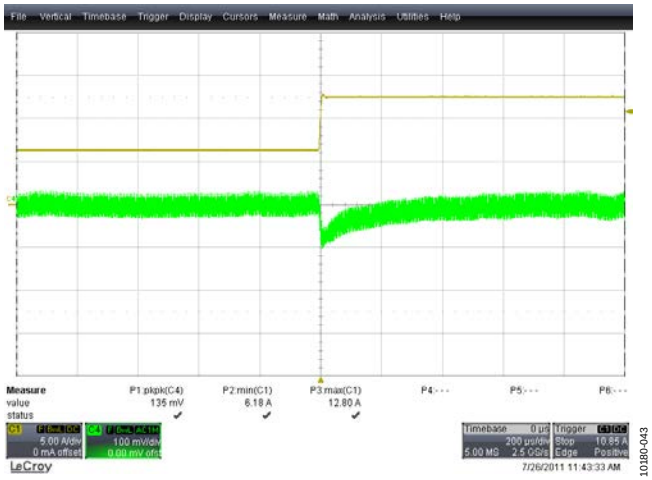

Figure 44. Output Voltage Transient, 25% to 50% Load, 385 V DC, Both Phases Active
Yellow Trace: Load Current, 5 A/div, 200 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 200 µs/div

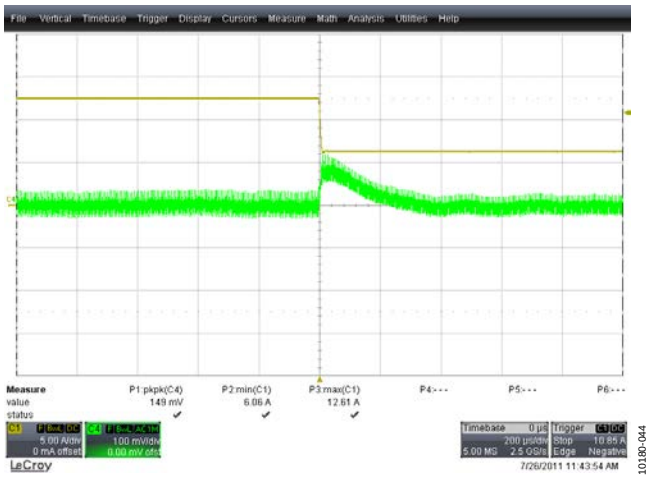

Figure 45. Output Voltage Transient, 50% to 25% Load, 385 V DC, One Phase Only
Yellow Trace: Load Current, 5 A/div, 200 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 200 µs/div

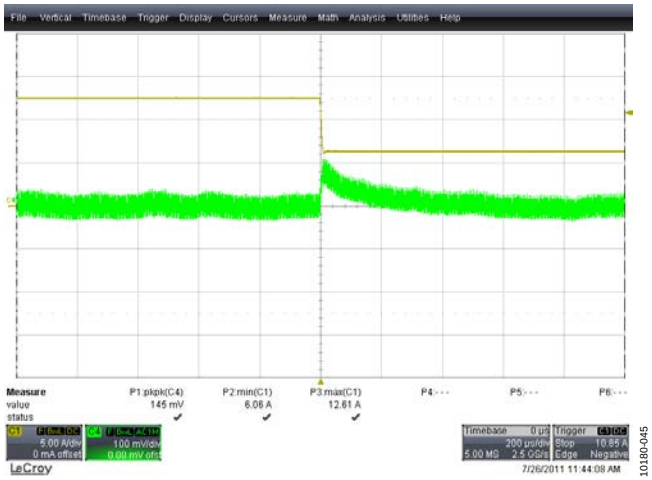

Figure 46. Output Voltage Transient, 50% to 25% Load, 385 V DC, Both Phases Active
Yellow Trace: Load Current, 5 A/div, 200 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 200 µs/div

Load Step of 50% to 75%

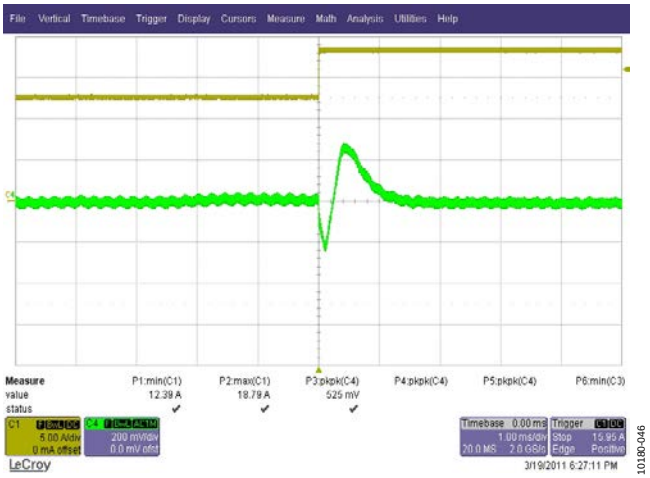

Figure 47. Output Voltage Transient, 50% to 75% Load,
385 V DC, One Phase Only
Yellow Trace: Load Current, 5 A/div, 1 ms/div
Green Trace: Output Voltage (AC-Coupled), 200 mV/div, 1 ms/div

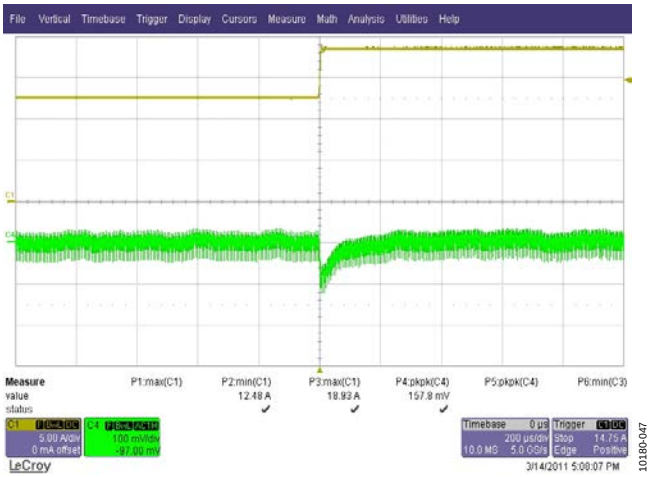

Figure 48. Output Voltage Transient, 50% to 75% Load,
385 V DC, Both Phases Active
Yellow Trace: Load Current, 5 A/div, 200 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 200 µs/div

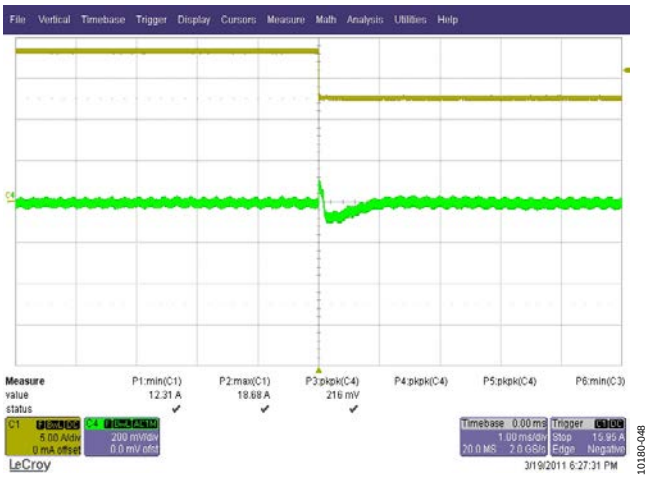

Figure 49. Output Voltage Transient, 75% to 50% Load,
385 V DC, One Phase Only
Yellow Trace: Load Current, 5 A/div, 1 ms/div
Green Trace: Output Voltage (AC-Coupled), 200 mV/div, 1 ms/div

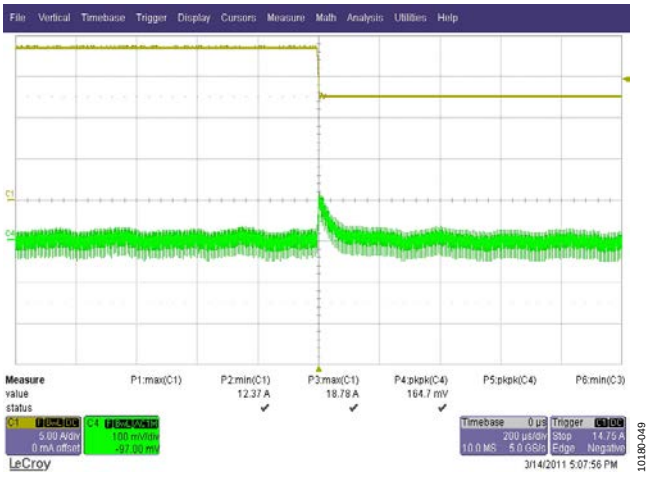

Figure 50. Output Voltage Transient, 75% to 50% Load,
385 V DC, Both Phases Active
Yellow Trace: Load Current, 5 A/div, 200 µs/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 200 µs/div

Load Step of 75% to 100%

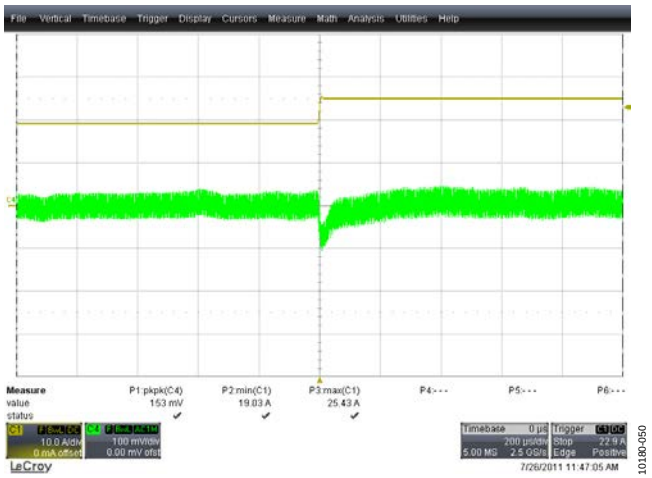

Figure 51. Output Voltage Transient, 75% to 100% Load, 385 V DC, Both Phases Active
Yellow Trace: Load Current, 10 A/div, 1 ms/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 1 ms/div

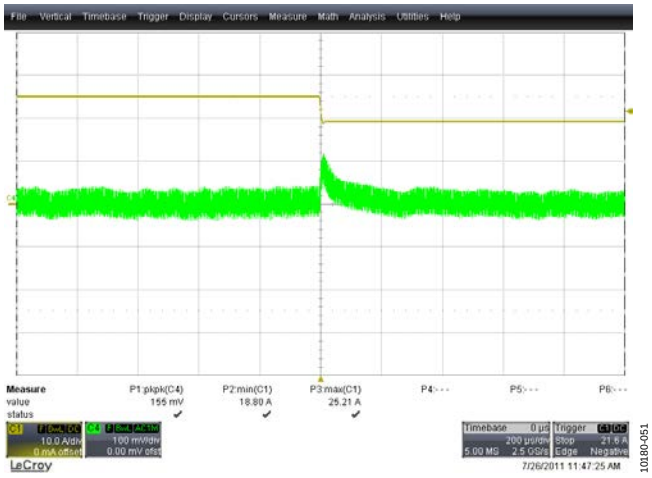

Figure 52. Output Voltage Transient, 100% to 75% Load, 385 V DC, Both Phases Active
Yellow Trace: Load Current, 10A/div, 1 ms/div
Green Trace: Output Voltage (AC-Coupled), 100 mV/div, 1 ms/div

PHASE SHEDDING TURN-ON/OFF TIME

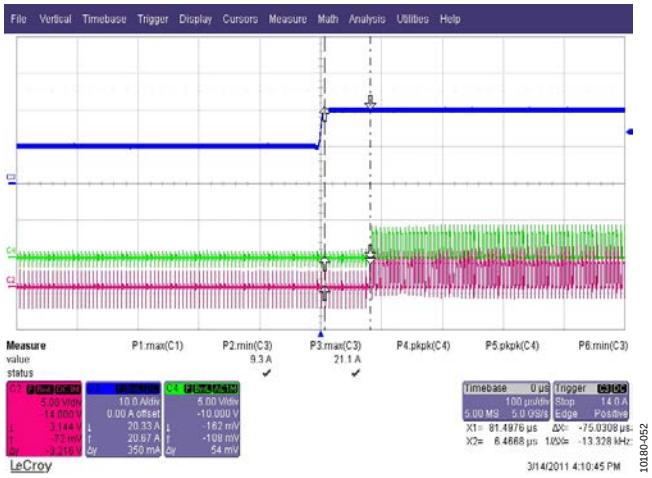

Figure 53. Synchronous Rectifier PWM Turn-On Time During Load Step 10 A to 20 A Load,
Blue Trace: Load Current, 10 A/div, 100 µs/div
Green and Red Trace: Phase 2 Synchronous Rectifier and Freewheel PWMs (SR1 and SR2), 100 µs/div

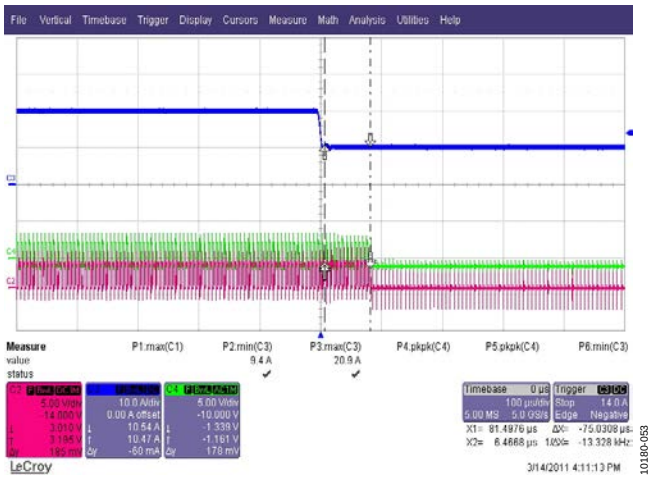

Figure 54. Synchronous Rectifier PWM Turn-On Time During Load Step 20 A to 10 A Load,
Blue Trace: Load Current, 10 A/div, 100 µs/div
Green and Red Trace: Phase 2 Synchronous Rectifier and Freewheel PWMs (SR1 and SR2), 100 µs/div

PRIMARY CURRENT DURING LOAD TRANSIENT

10 A to 20 A Load Step

Figure 55. Input Current During Load Step of 10 A to 20 A
Yellow Trace: Load Current, 5 A/div, 10 ms/div
Red Trace: Voltage at CS1 Pin, 500 mV/div (20 µs/div Zoomed In)

Figure 56. Input Current During Load Step of 10 A to 20 A Showing Steady Balancing of Both Phases; Yellow Trace: Load Current, 5 A/div, 10 ms/div
Red Trace: Voltage at CS1 Pin, 500 mV/div (20 µs/div Zoomed In)

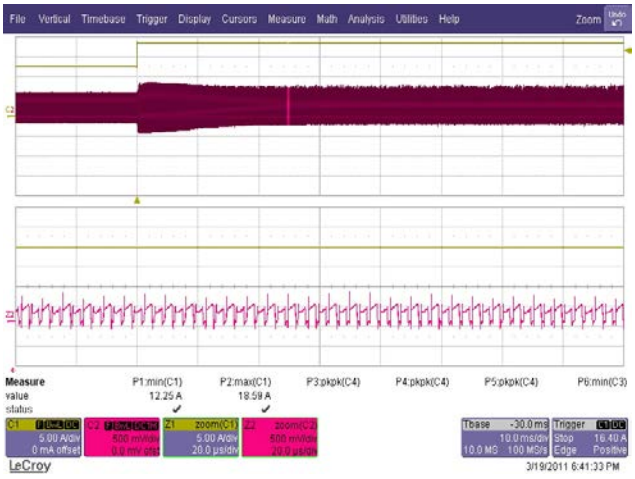

Figure 57. Input Current During Load Step of 10 A to 20 A Showing Steady Balancing of Both Phases; Yellow Trace: Load Current, 5 A/div, 10 ms/div
Red Trace: Voltage at CS1 Pin, 500 mV/div (20 µs/div Zoomed In)

20 A to 10 A Load Step

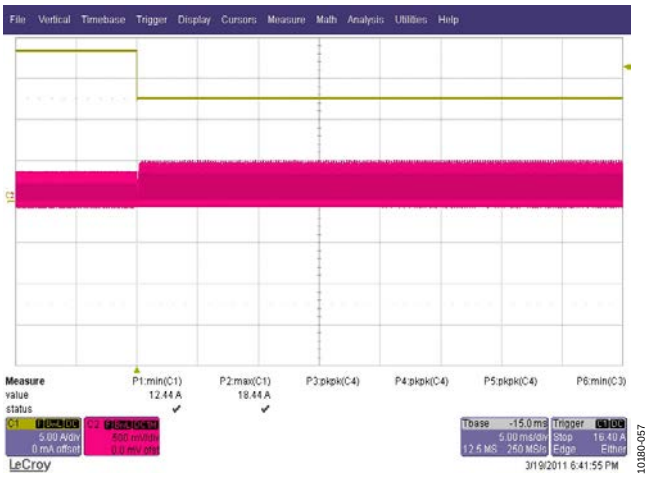

Figure 58. Input Current During Load Step of 20 A to 10 A Showing Steady Balancing of Both Phases,
Yellow Trace: Load Current, 5 A/div, 5 ms/div
Red trace: Voltage at CS1 Pin, 500 mV/div, 5 ms/div

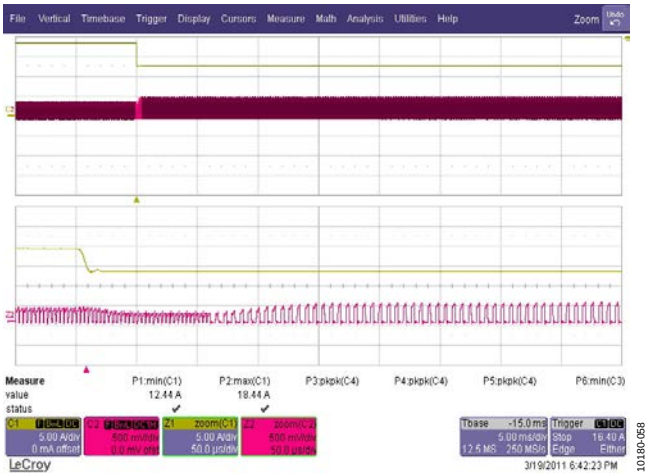

Figure 59. Input Current During Load Step of 20 A to 10 A Showing Fade-Out of Phase 2
Yellow Trace: Load Current, 5 A/div, 5 ms/div
Red Trace: Voltage at CS1 Pin, 500 mV/div (50 µs/div Zoomed In)

OUTPUT OVERCURRENT PROTECTION

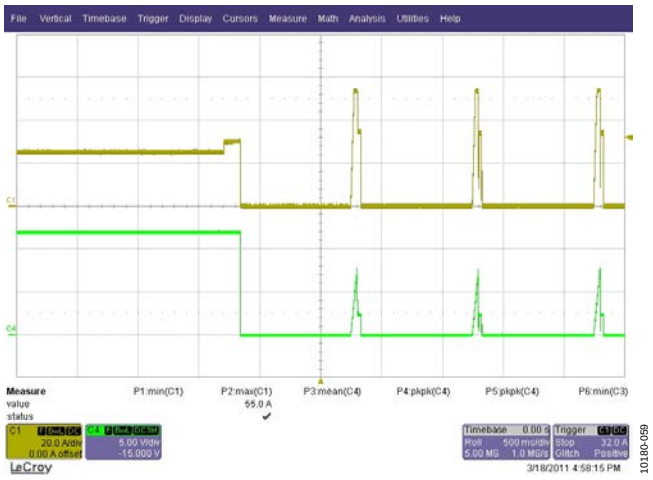

Figure 60. Output Short-Circuit Protection, 130 ms Debounce on CS2, Response Set to Disable PSU and Reenable After 1 sec, Yellow Trace: Load Current, 20 A/div, 500 ms/div Green Trace: Output Voltage, 5 V/div, 500 ms/div

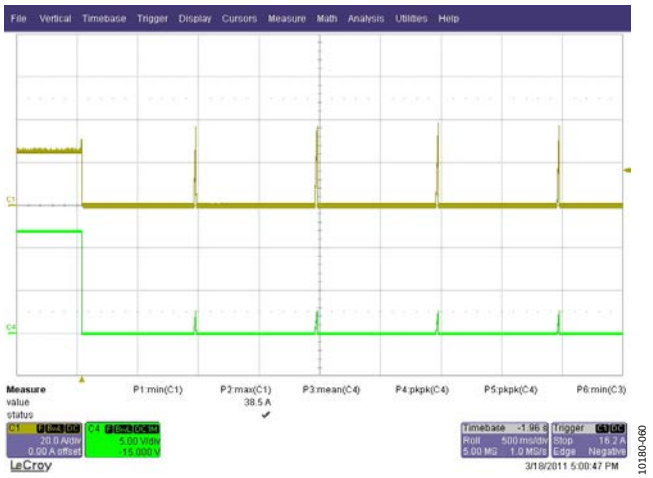

Figure 61. Output Short-Circuit Protection, 9.8 ms Debounce on CS2, Response Set to Disable PSU and Reenable After 1 sec, Yellow Trace: Load Current, 20 A/div, 500 ms/div Green Trace: Output Voltage, 5 V/div, 500 ms/div

DIGITAL CURRENT SHARING

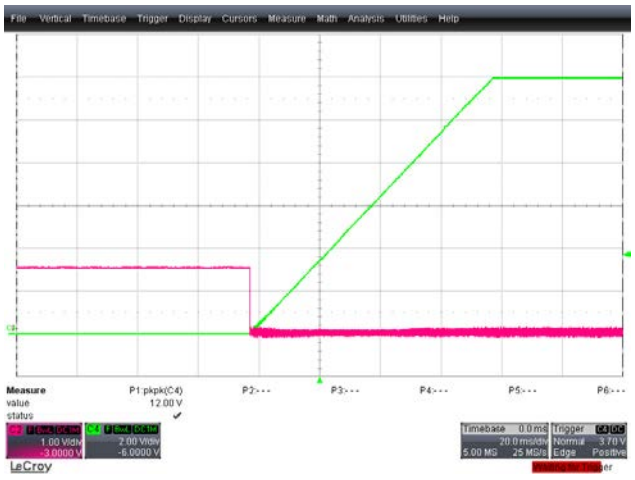

Figure 62. OrFET Turn-On Green Trace: Output Voltage, 2 V/div, 20 ms/div Red Trace: GATE Signal Voltage, 2 V/div, 20 ms/div

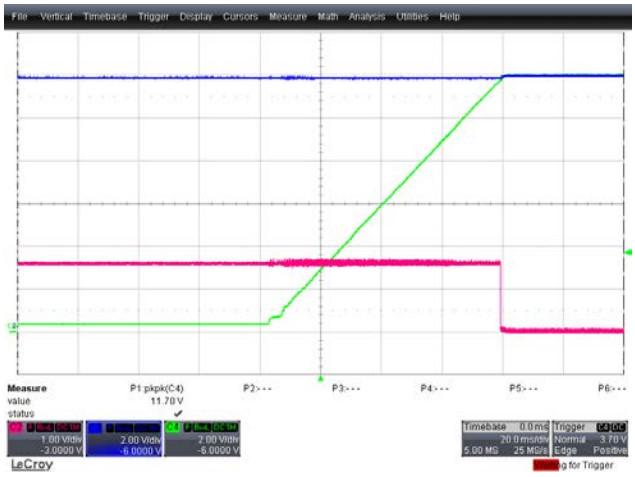

Figure 63. OrFET Turn-On in Live Bus Green Trace: Output Voltage, 2 V/div, 20 ms/div Red Trace: GATE Signal Voltage, 2 V/div, 20 ms/div

Figure 64. Digital Current Sharing with Load Step of 25 A, 42 A, 25 A Red and Yellow Traces: Output Currents of PSU1 and PSU2, 10 A/div, 500 ms/div Green and Blue Traces: SHAREo Pins of PSU1 and PSU2, 5 V/div, 20 ms/div

CLOSED-LOOP FREQUENCY RESPONSE

A network analyzer (AP200) was used to test the bode plots of the system. Jumper J18 was replaced by a 20 Ω resistor, and a continuous noise signal of 400 mV was injected into the VS3+ pin before the voltage divider (R10 and R11 on daughter card). The operating condition was 385 V dc input and a load condition of 25 A.

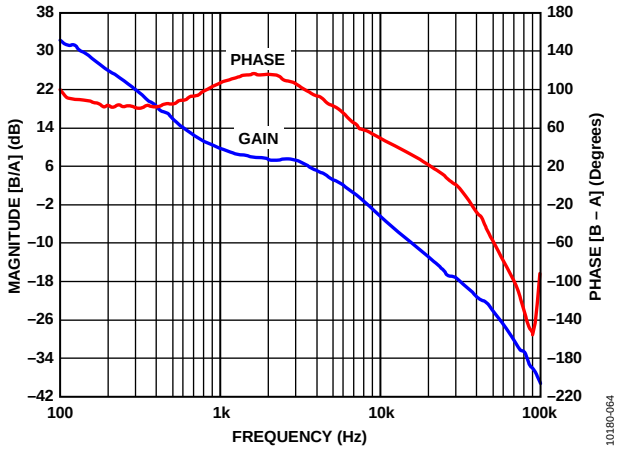

Figure 65. Bode Plots, 25 A Load, 385 V DC
Crossover Frequency = 7.36 kHz
Phase Margin = 62.8°
Gain Margin = 17 dB

EFFICIENCY

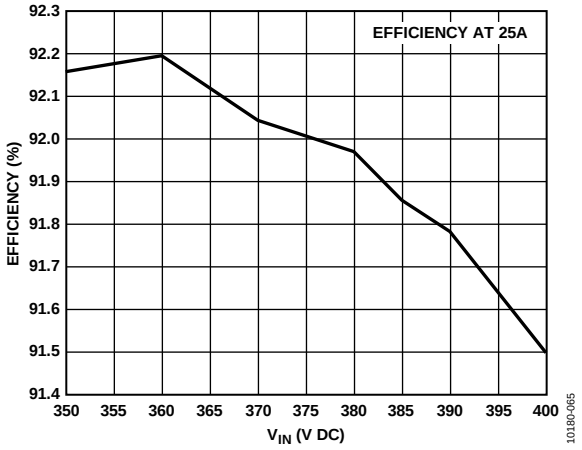

Figure 66. Efficiency vs. V_{IN}

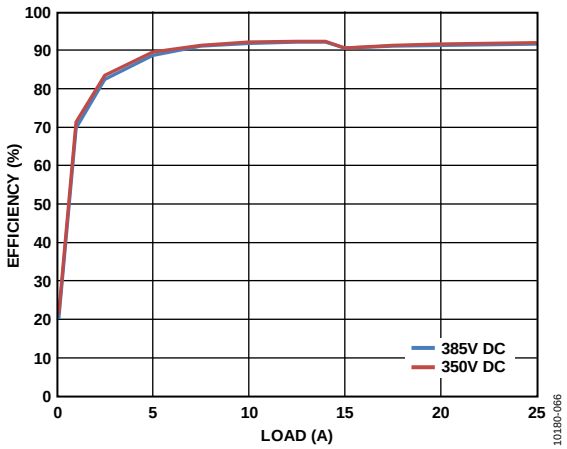

Figure 67. Efficiency vs. Load

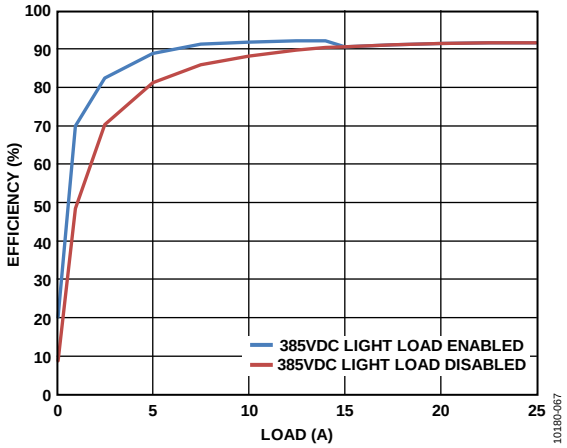

Figure 68. Efficiency vs. Load (with and Without Light Load Mode)

CS1 LINEARITY

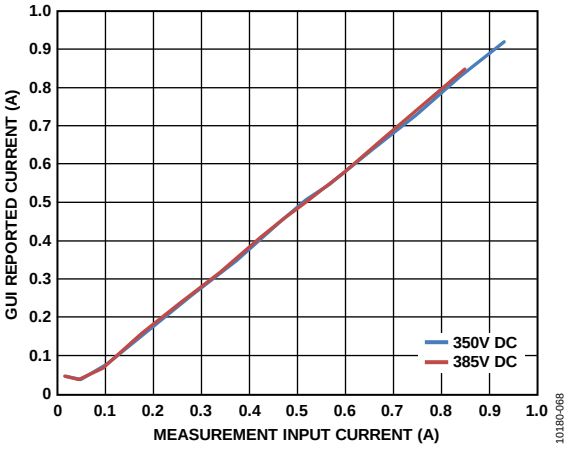

Figure 69. CS1 Linearity

ACSNS LINEARITY

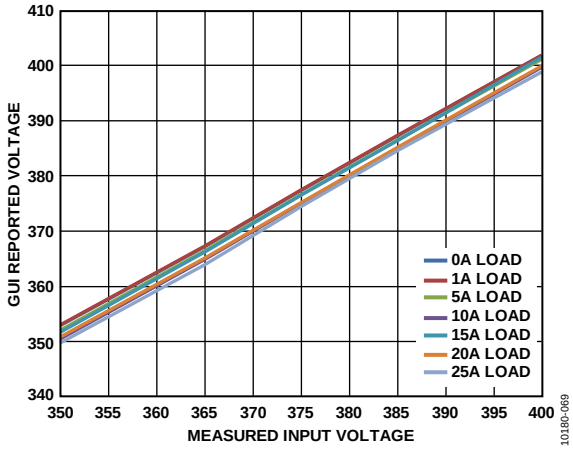

Figure 70. ACSNS Linearity vs. Load

CS2 LINEARITY

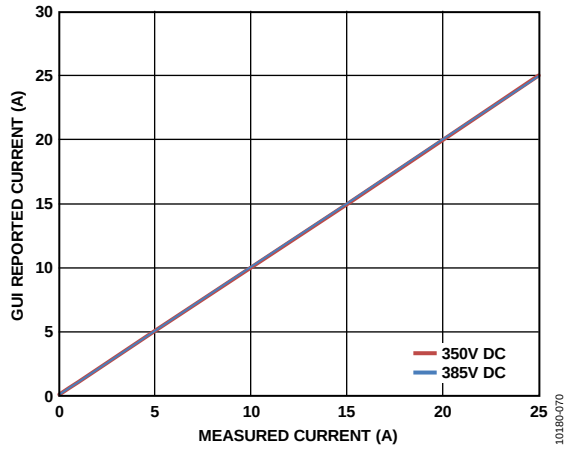

Figure 71. CS2 Linearity vs. Load

NO LOAD POWER

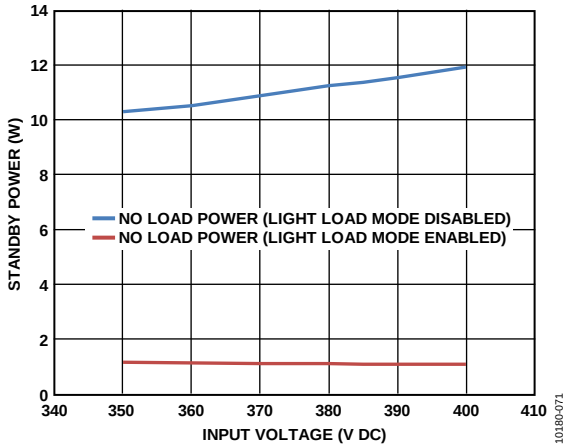

Figure 72. No Load Power

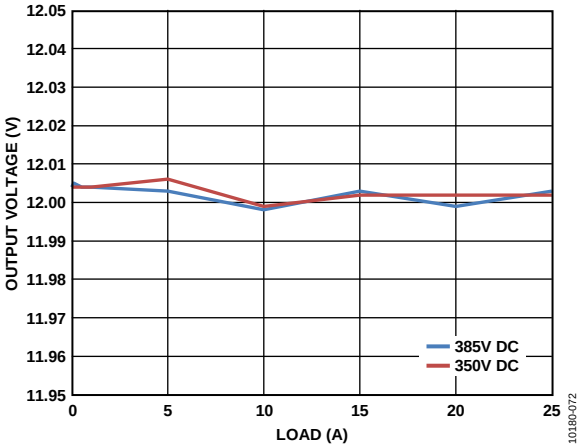

Figure 73. Output Voltage Regulation vs. Load Current

THERMAL PERFORMANCE

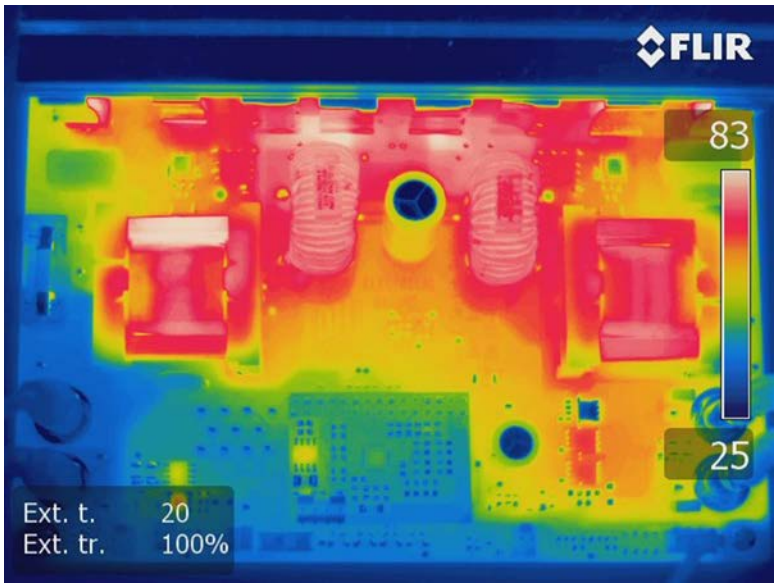

Figure 74. Thermal Performance at 385 V DC Input, 12 V, 25 A Output Load, No Airflow, Soaking Time of 60 Minutes

EVALUATION BOARD SCHEMATICS AND ARTWORK

MAIN BOARD SCHEMATIC

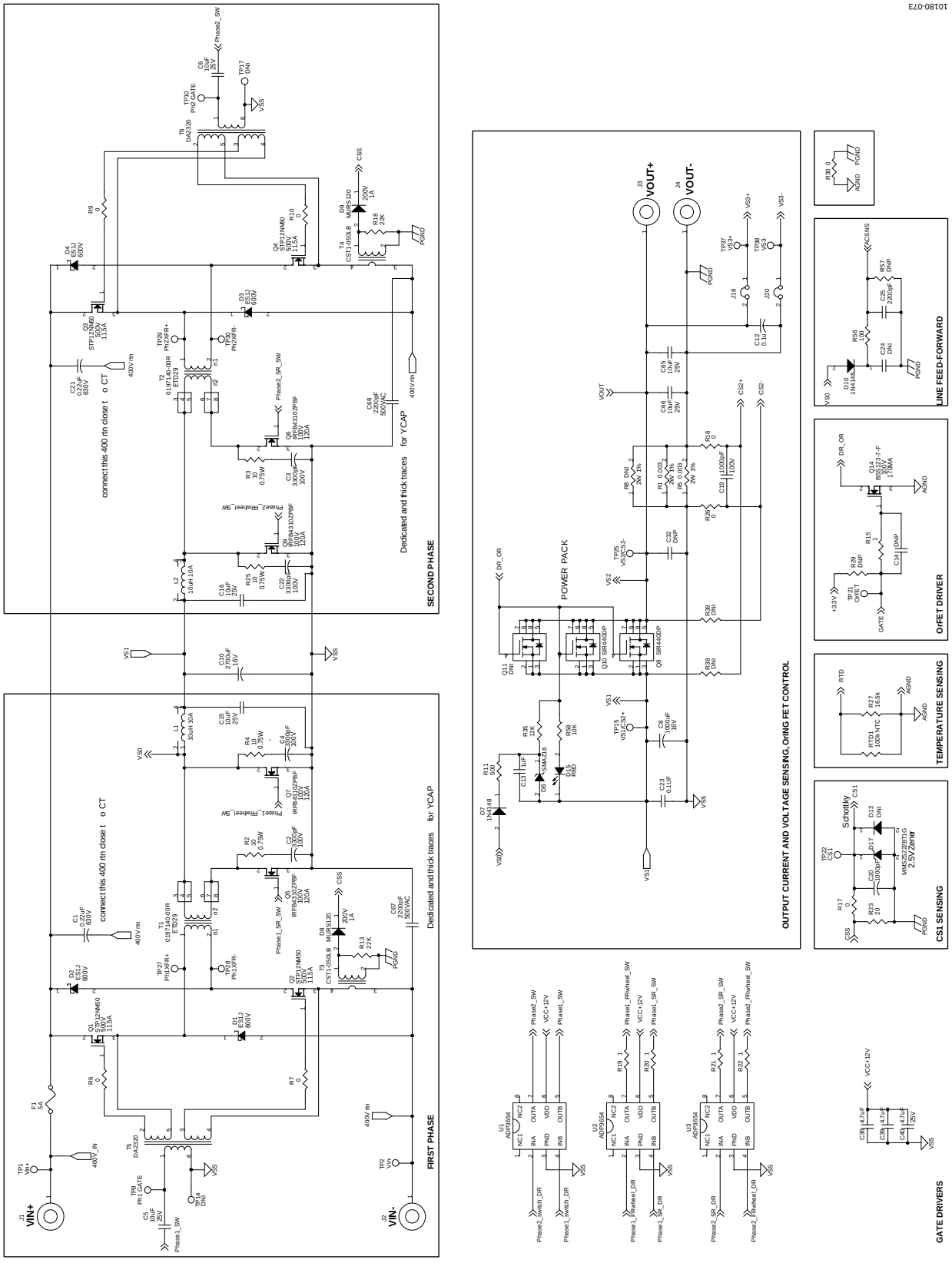

Figure 75. Schematic—Power Stage

INTERFACES SCHEMATIC

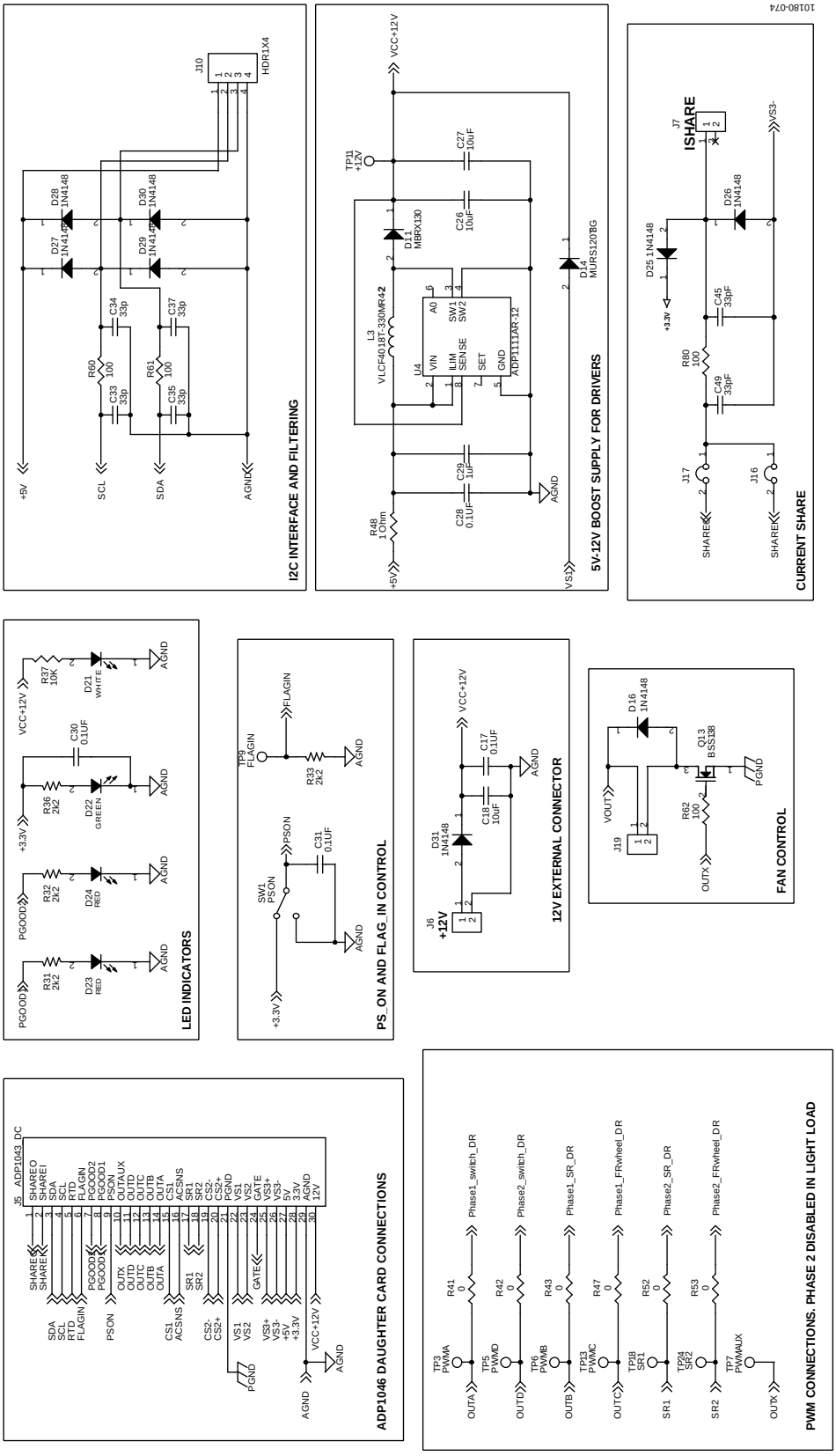

Figure 76. Schematic—Interfaces

DAUGHTER CARD SCHEMATIC

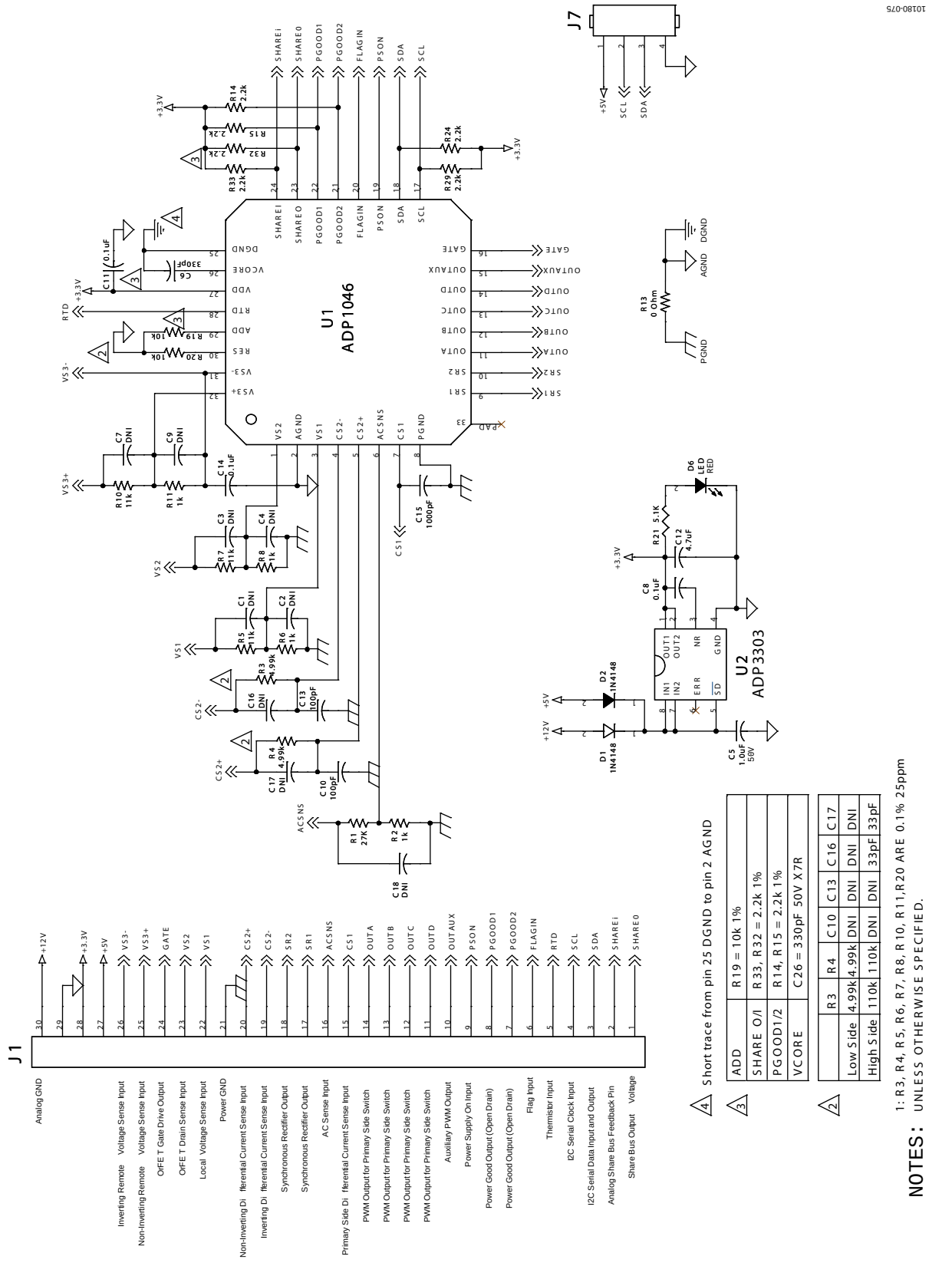

Figure 77. Daughter Card Schematic

MAIN BOARD LAYOUT

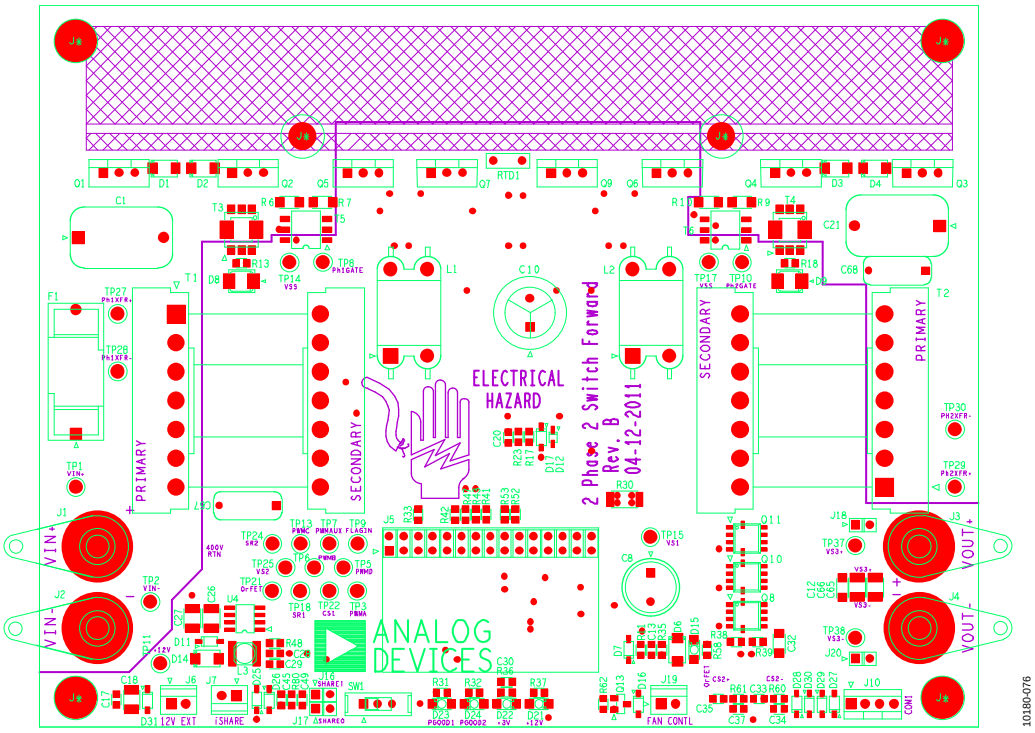

Figure 78. Layout, Top Silkscreen, 6.5 in × 5 in

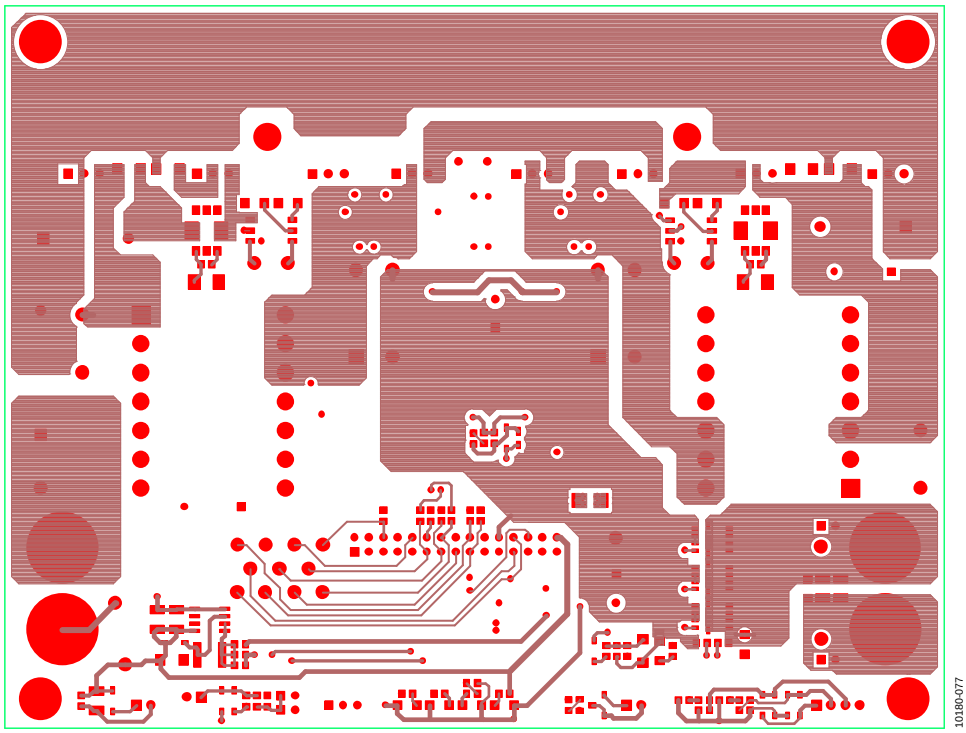

Figure 79. Layout, First Layer, 6.5 in × 5 in

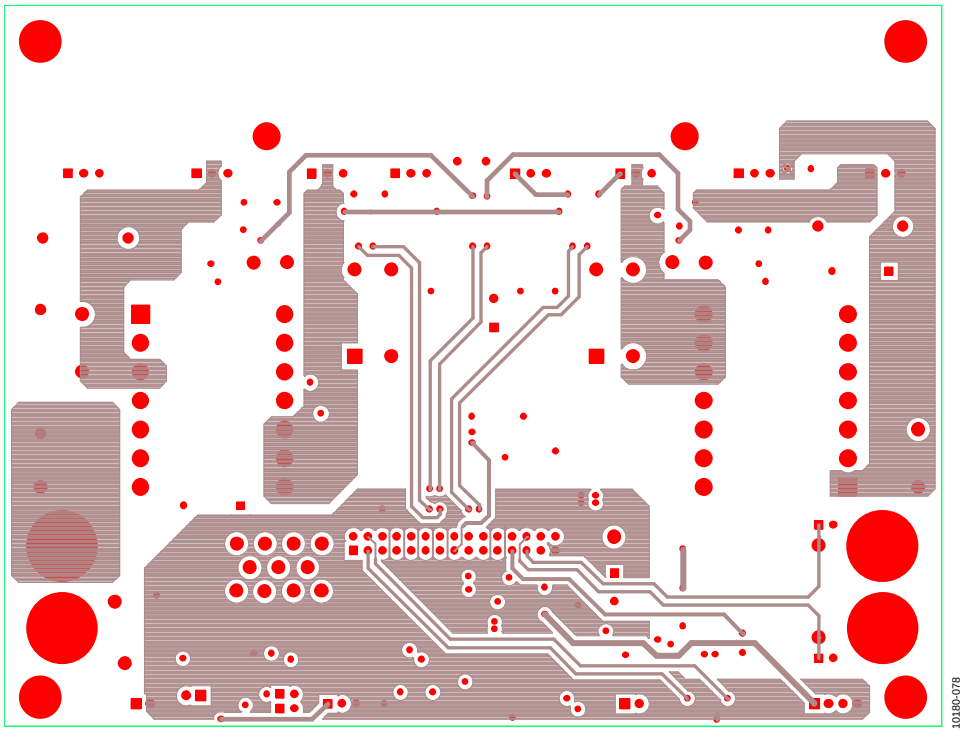

Figure 80. Layout, Second Layer, 6.5 in × 5 in

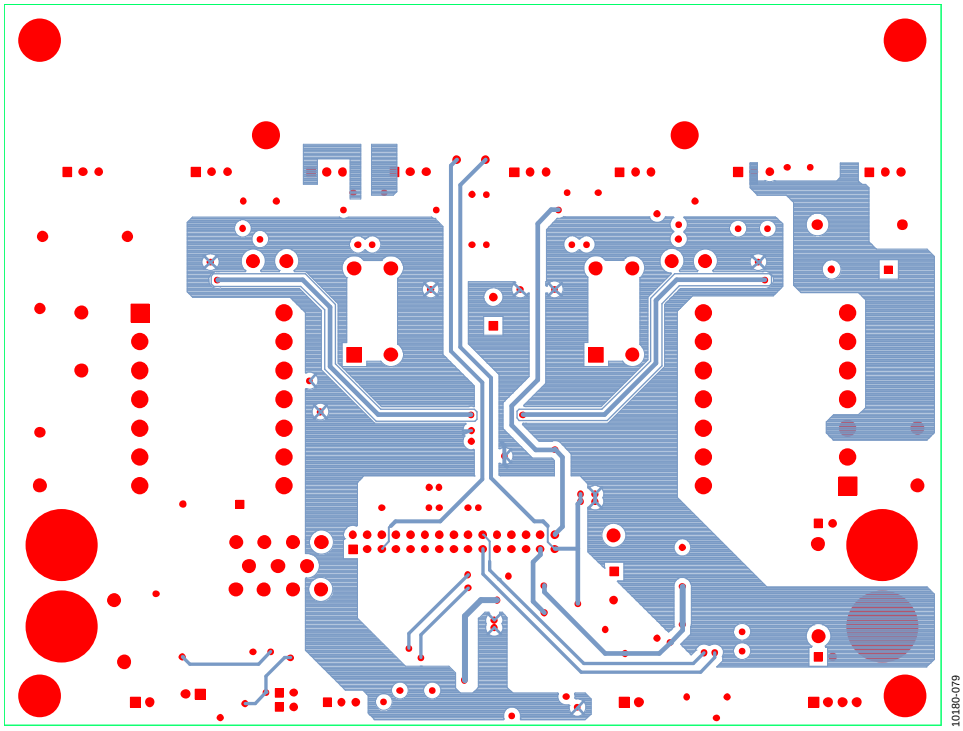

Figure 81. Layout, Third Layer, 6.5 in × 5 in

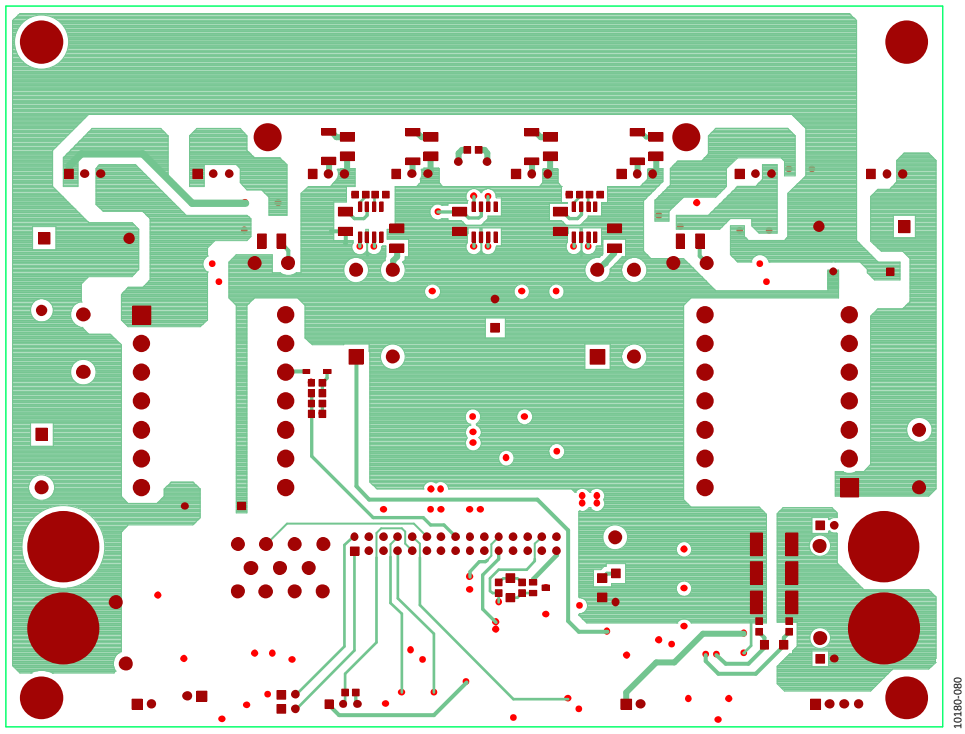

Figure 82. Layout, Bottom Layer, 6.5 in × 5 in

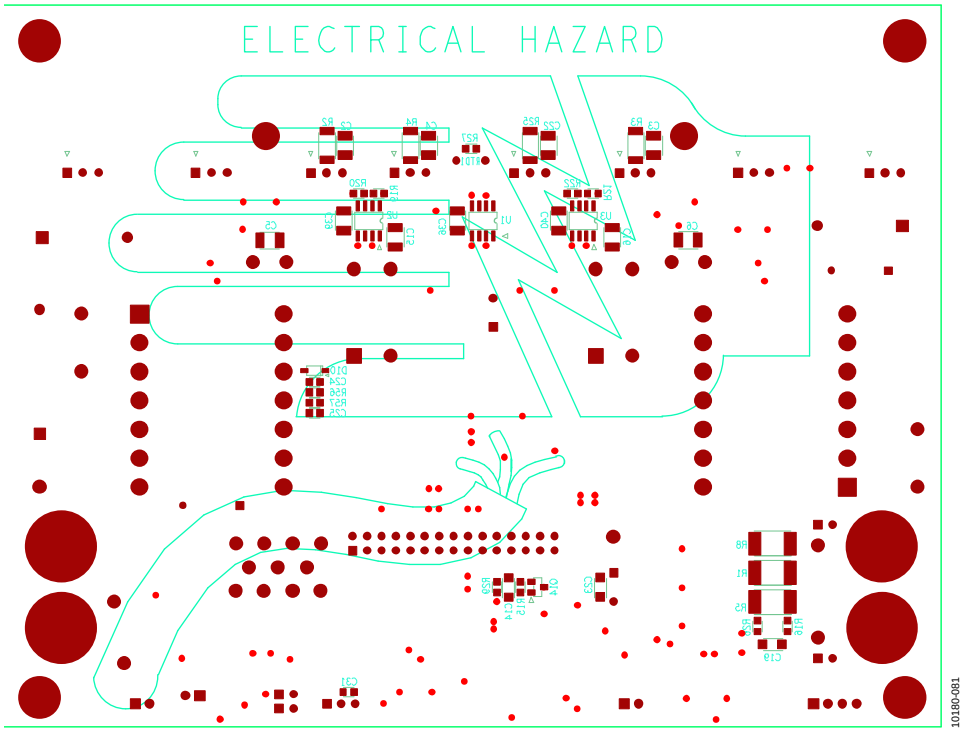

Figure 83. Layout, Bottom Layer Silkscreen, 6.5 in × 5 in

DAUGHTER CARD LAYOUT

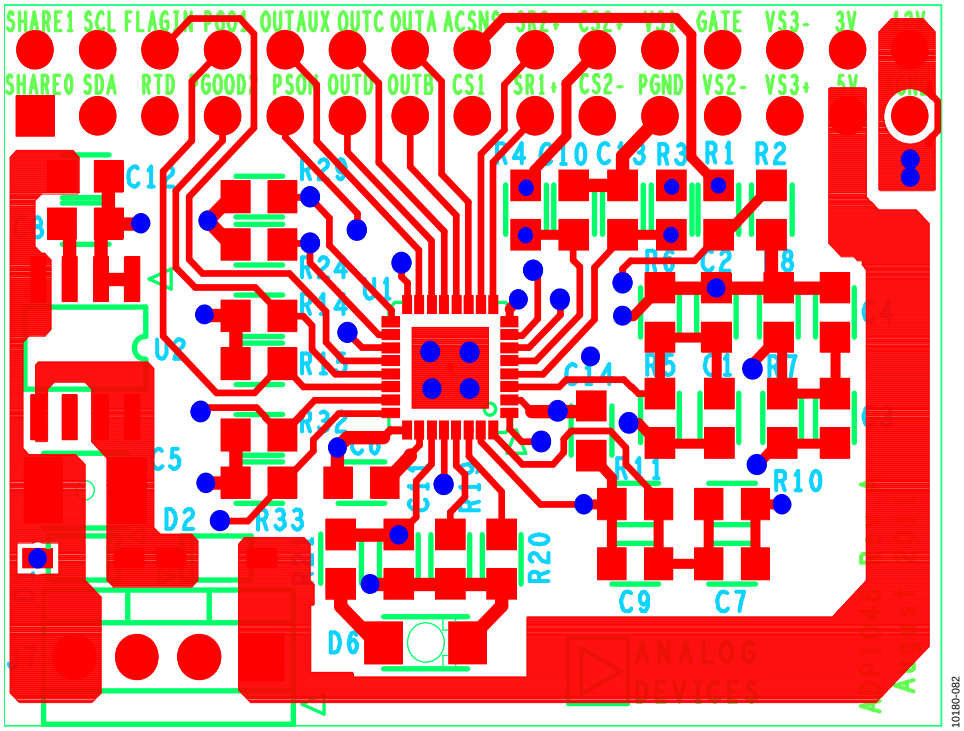

Figure 84. Top Layer, 1.5 in × 1.08 in

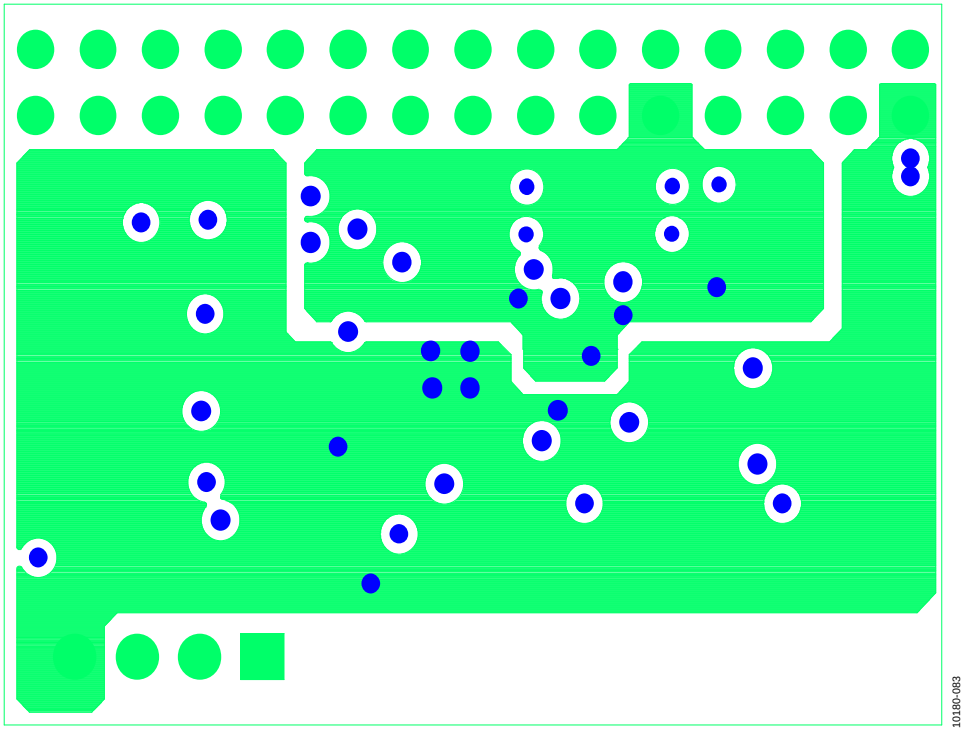

Figure 85. Ground Layer, 1.5 in × 1.08 in

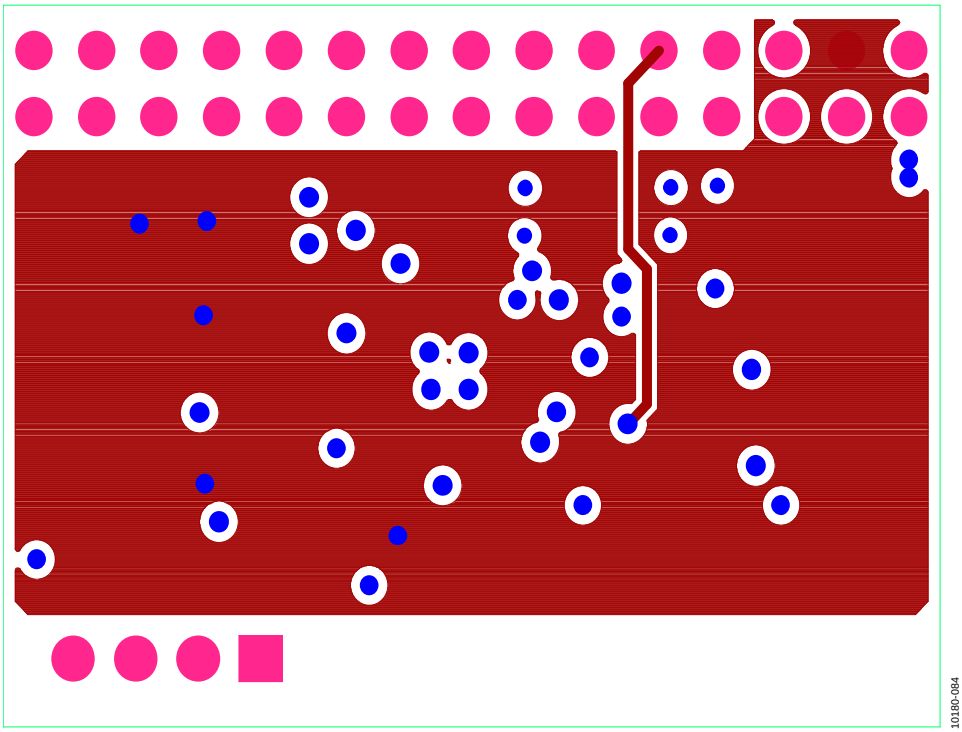

Figure 86. Power Layer, 1.5 in × 1.08 in

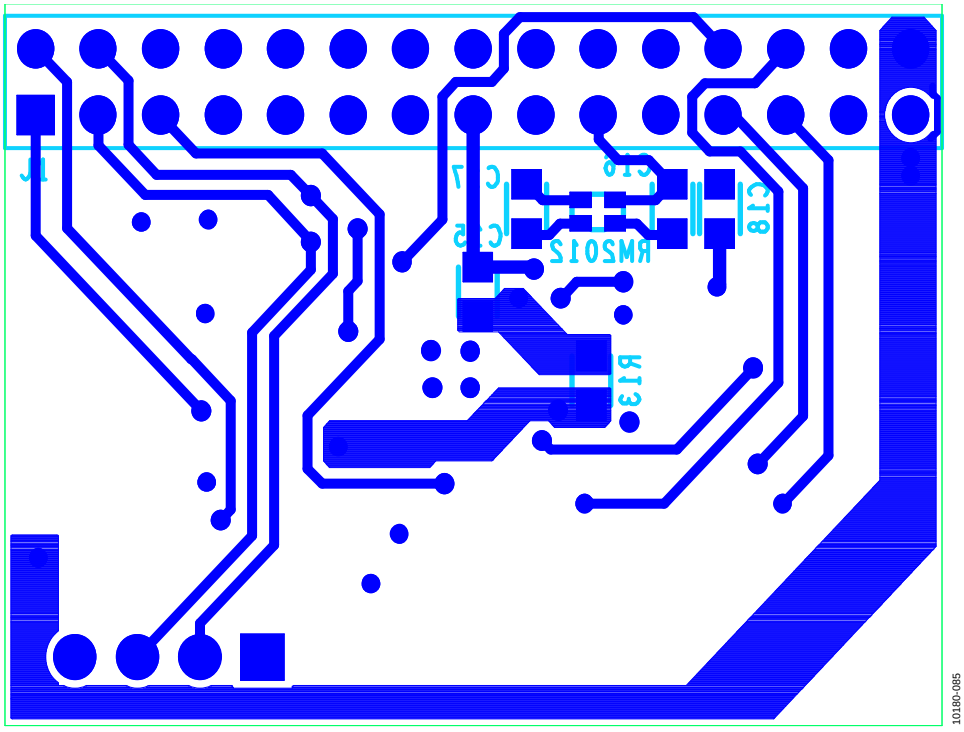

Figure 87. Bottom Layer, 1.5 in × 1.08 in

BILL OF MATERIALS

Table 6. Main Board

Qty	Reference Designator	Description	Manufacturer	Mfg Part No	Package
2	C1, 21	Capacitor metal polypro, 0.22 µF, 630 V, 3%	Panasonic	ECW-F6224HL	Polypropylene
4	C2, C3, C4, C22	SMD capacitor ceramic, 3300 pF, 100 V, 10% X7R	AVX Corp	12101C332KAT2A	1210
7	C5, C6, C15, C16, C18, C26, C27	Capacitor ceramic 10 µF, 25 V, ±20%, X5R	Panasonic	ECJ-4YB1E106M	1210
1	C8	Capacitor 1000 µF, 16 V, ±20%, elect KZE red	United Chemicon	EKZE160ELL102MJ20S	Radial Can
3	C9, C13, C29	Capacitor ceramic 1 µF, 25 V, ±10%, X7R	Murata	GCM21BR71E105KA56L	0805
1	C10	Capacitor 2700 µF, 16 V, ±20%, elect KZE radial	United Chemicon	EKZE160ELL272MK30S	Radial Can
2	C12, C17	SMD Capacitor ceramic, 0.1 µF, 50 V, 10% X7R	Murata	GRM21BR71H104KA01L	0805
1	C14	DNI			
1	C19	Capacitor ceramic 1000 pF, 100 V, ±20%, X2Y	Johnson	101X18N102MV4E	1206
1	C20	SMD capacitor 1000 pF, 10%, 100 V, X7R	AVR	08051C102KAT2A	0805
4	C23, C24, C32, C30	Capacitor ceramic 100 nF, 50 V, 10%, X7R	Murata	GRM21BR71H104KA01L	0805
1	C25	Capacitor ceramic 2200 pF, 50 V, 10%, X7R	AVX Corp	08055C222KAT2A	0805
2	C28, C31	Capacitor ceramic 0.1 µF, 50 V, 10%, X7R	Murata	GRM21BR71H104KA01L	0805
3	C33, C34, C35	Capacitor ceramic 33 pF, 50 V, ±5%, NP0	Panasonic	ECJ-2VC1H330J	0805
3	C36, C39, C40	Capacitor ceramic 4.7 µF, 25 V, 10%, X5R	TDK	C3225X7R1E475K	1210
3	C37, C45, C49	Capacitor ceramic 33 pF, 50 V, ±5%, NP0	Panasonic	ECJ-2VC1H330J	0805
1	C65	Capacitor ceramic 10 µF, 25 V, ±20%, X5R	Panasonic	ECJ-4YB1E106M	1210
1	C66	Capacitor ceramic 10 µF, 25 V, ±20%, X5R	Panasonic	ECJ-4YB1E106M	1210
2	C67, C68	Capacitor ceramic 2200 pF, 500 V ac	Vishay	VY1222M47Y5UQ63V0	VY1
4	D1 to D4	SMD diode fast REC, 1 A, 600 V	Any	ES1J-TP	DO214AC
1	D6	Diode Zener 16 V, 1 W, 5%	Diodes, Inc	SMAZ16-13-F	MSB-403
3	D7, D10, D16	SMD diode switch, 100 V, 400 mW	Diodes, Inc	1N4148W-7-F	SOD123
3	D8, D9, D14	SMD diode super fast 200 V, 1 A	Diodes, Inc	MURS120-13-F	DO-2144AA
1	D11	SMD diode Schottky 30 V, 1 A	Micro Commercial	MBRX130-TP	SOD-123
1	D12	SMD diode Schottky 10 V, 570 mW, DNI	Diodes, Inc	ZLLS410TA	SOD323
1	D17	SMD diode Zener 2.5 V, 500 mW	On Semi	MMSZ5222BT1G	MSB-403
1	D21	SMD LED white clear	Lumex Opto	SML-LX1206UWW-TR	1206
1	D22	SMD LED green clear	Chicago lighting	CMD15-21VGC/TR8	1206
3	D23, D24, D15	SMD LED super red clear	Chicago lighting	CMD15-21SRC/TR8	1206
7	D25 to D31	SMD diode switch 100 V, 400 mW	Diodes, Inc	1N4148W-7-F	SOD123
1	F1	Holder PC fuse 5 mm low profile	Keystone	4527	Fuseholder
4	J1 to J4	Connector jack banana UNINS panel MOU	Emerson	108-0740-001	BANANA JACK
1	J5	Connector RECEPT 30-position, 0.100 vertical dual	TE Connectivity	1-534206-5	F-Socket-Dual
2	J6, J7	Connector header 2-position, 3.96 mm vertical tin	Molex	09-65-2028	
1	J10	Connector header 4-position SGL PCB 30GOLD	FCI	69167-104HLF	Header male
3	J16 to J18	Connector header breakaway, 0.100, 2-position STR	TE Connectivity	4-102973-0-01	Header
1	J19	Connector header 2-position, 3.96 mm vertical tin	Molex	09-65-2028	
3	J20 to J22	Connector header breakaway, 0.100, 2-position straight	TE Connectivity	4-102973-0-01	Header
2	L1, L2	Inductor 10 µH	Precision Inc	019-7129-00R-Proto02	901
1	L3	Power inductor 33 µH, 0.42 A	Coilcraft	VLCF4018T-330MR42-2	SMT
4	Q1 to Q4	MOSFET N-channel 500 V, 12 A	ST Microelectronics	STP12NM50	TO-220

Qty	Reference Designator	Description	Manufacturer	Mfg Part No	Package
4	Q5 to Q7, Q9	MOSFET N-channel 100 V, 120 A	International Rectifier	IRFB4310ZPBF-ND	TO-220
3	Q8, Q10	SMD MOSFET N-channel 20 V, 60 A	Vishay	SIR440DP-T1-GE3	8-SOIC
1	Q11	DNI			
1	Q13	MOSFET N-channel 50 V, 220 mA	Fairchild	BSS138	SOT-23
1	Q14	SMD MOSFET N-channel 100 V, 170 mA	Diodes, Inc	BSS123-7-F	SOT23
1	RTD1	Thermistor NTC 100 kΩ, 5%, RAD	EPCOS	B57891M0104J000	B57891
2	R1, R5	SMD resistor 0.003 Ω, 2 W, 1%	Stackpole Electronics, Inc	CSNL2512FT3L00	2512
3	R2, R3, R4	SMD resistor 10.0 Ω, ¾ W, 5%	Stackpole Electronics, Inc	RMCF2010JT10R0	2010
1	R5	SMD resistor 0.003 Ω, 2 W, 1%	Stackpole Electronics, Inc	CSNL2512FT3L00	2512
2	R6, R7	Resistor 0.0 Ω,¼ W, SMD	Any	Any	1206
1	R8	DNI	DNI	DNI	2512
2	R9, R10	Resistor 0.0 Ω, ¼ W, SMD	Any	Any	1206
1	R11	SMD resistor 500.0 Ω, 5%	Any	Any	
2	R13, R18	SMD resistor 22.0 kΩ, 1/8 W, 1%	Any	Any	0805
4	R16, R17, R26, R30	SMD resistor 0.0 Ω, 1/8 W, 5%	Any	Any	0805
5	R19 to R22, R15	SMD resistor 1.00 Ω, 1/8 W, 1%	Any	Any	
2	R23, R27	SMD resistor 20.0 Ω, 1/8 W, 1%	Any	Any	0805
1	R25	SMD resistor 10.0 Ω, ¾ W, 5%	Any	Any	2010
1	R29				
4	R31, R32, R33, R36	SMD resistor 2.20 kΩ, 1/8 W, 1%	Any	Any	0805
1	R35	Resistor 12.0 k Ω, 1/8 W, 1% SMD	Any	Any	0805
2	R37, R58	SMD resistor 10.0 k Ω, 1/8 W, 1%	Any	Any	0805
13	R30, R38 to R47, R52, R53	SMD resistor 0.0 Ω, 1/8 W, 5%	Any	Any	0805
1	R48	SMD resistor 1.00 Ω, 1/8 W, 1% 0805	Any	Any	0805
2	R56, R57	SMD resistor 100 Ω, 1/8 W, 1%	Any	Any	0805
3	R60, R61, R80	Resistor 100 Ω, 1/8 W, 1% SMD	Any	Any	0805
1	R62	SMD resistor 100 Ω, 1/8 W, 1%	Any	Any	0805
1	SW1	SW slide SPDT 30 V, 0.2 A PC mount	E-Switch	EG1218	Slide-Sw
3	TP1 to TP3	Test point PC mini 0.040"D red	Keystone	5010	TP-70
7	TP5 to TP11	Test point PC mini 0.040"D red	Keystone	5010	TP-70
3	TP13 to TP15	Test point PC mini 0.040"D red	Keystone	5010	TP-70
4	TP17, TP18, TP21 to T22	Test point PC mini 0.040"D red	Keystone	5010	TP-70
6	TP24, TP25, TP27 to T30	Test point PC mini 0.040"D red	Keystone	5010	TP-70
2	TP37, TP38	Test point PC mini 0.040"D red	Keystone	5010	TP-70
2	T1, T2	Power switch mode transformers	Precision Inc	0197140-00R	ETD29
2	T3, T4	Current sensor	Coilcraft	CST1-050LB	CST1
2	T5, T6	Transformer gate drive	Coilcraft	DA2320-ALB	DA2320
3	U1, U2, U3	High speed dual 4 A MOSFET driver	Analog Devices	ADP3654A	8-lead SOIC
1	U4	IC multiconfiguration 12 V, 0.2 A	Analog Devices	ADP1111ARZ-12	8-lead SOIC

Table 7. Daughter Card

Qty	Reference	Part Description	Manufacture	Mfg Part No	Package
1	C5	Capacitor ceramic 1.0 µF, 50 V, 10%, X7R	Murata	GRM32RR71H105KA01L	1210
1	C6	Capacitor ceramic 330 pF, 10%, 100 V, X7R	AVX	08051C331KAT2A	0805
3	C8, C11, C14	Capacitor ceramic 0.1 µF, 10%, 50 V, X7R	AVX	08055C104KAT2A	0805
2	C10, C13	Capacitor ceramic 100 pF, 10%, 100 V, X7R			0805
1	C12	Capacitor ceramic 4.7 µF, ±10%, 10 V, X7R	TY	LMK212B7475KG-T	0805
1	C15	Capacitor ceramic 1000 pF, 10%, 100V, X7R	TDK	C2012X7R1A475M	0805
2	D1, D2	Diode SW 150 mA, 100 V, 1N4148	Micro Commercial	1N4448W-TP	SOD-123
1	D6	LED super red clear 75 mA, 1.7 V, SMD	Chicago Lighting	CMD15-21SRC/TR8	1206
1	J1	Connector header female 30-position 0.1" DL tin, CON30	Sullins Connector	PPTC152LFBN-RC	Fmal Socket
1	J7	Connector header 4-position SGL PCB 30 gold, HEADER4X1	FCI	69167-104HLF	Header 4POS
1	R1	Resistor 27.0 kΩ, 1/10 W, 1%, SMD	Any	Any	0805
1	R2	Resistor 1.00 kΩ, 1/8 W, 1%, SMD	Any	Any	0805
2	R3, R4	Resistor 4.99 kΩ, 1/10 W, 0.1%, ±25 ppm, SMD	Any	Any	0805
3	R5, R7, R10	Resistor 11.0 kΩ, 1/10 W, 1%, ±25 ppm, SMD	Any	Any	0805
3	R6, R8, R11	Resistor 1.00 kΩ, 1/10 W, 1%, ±25 ppm, SMD	Any	Any	0805
1	R13	Resistor 0.0 Ω, 1/8 W, 5%, SMD	Any	Any	0805
6	R14, R15, R24, R29, R32, R33	Resistor 2.20 kΩ, 1/8 W, SMD	Any	Any	0805
2	R19, R20	Resistor 10 kΩ, 1/8 W, 0.1%, SMD	Any	Any	0805
1	R21	Resistor 5.10 kΩ, 1/8 W, SMD	Any	Any	0805
1	U1	ADP1046 secondary side power supply controller	Analog Devices	ADP1046	32-lead LFCSP
1	U2	ADP3303 IC LDO linear regulator 200 mA, 3.3 V	Analog Devices	ADP3303ARZ-3.3	SOIC-8
9	C1, C2, C3, C4, C7, C9, C16, C17, C18	DNI			

APPENDIX I—TRANSFORMER SPECIFICATIONS

Table 8. Transformer Specifications

Parameter	Min	Typ	Max	Unit	Notes
Core and Bobbin					ETD 29 horizontal, 3F3 or equivalent
Primary Inductance		4.25		mH	Pin 1 and Pin 3
Leakage Inductance		7		µH	Pin 1 and Pin 3 with all other windings shorted
Resonant Frequency	850			kHz	Pin 1 and Pin 3 with all other windings open

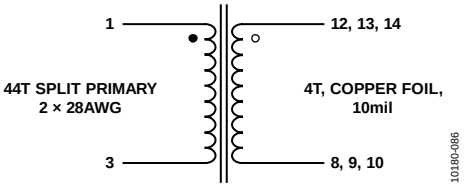

Figure 88. Transformer Electrical Diagram

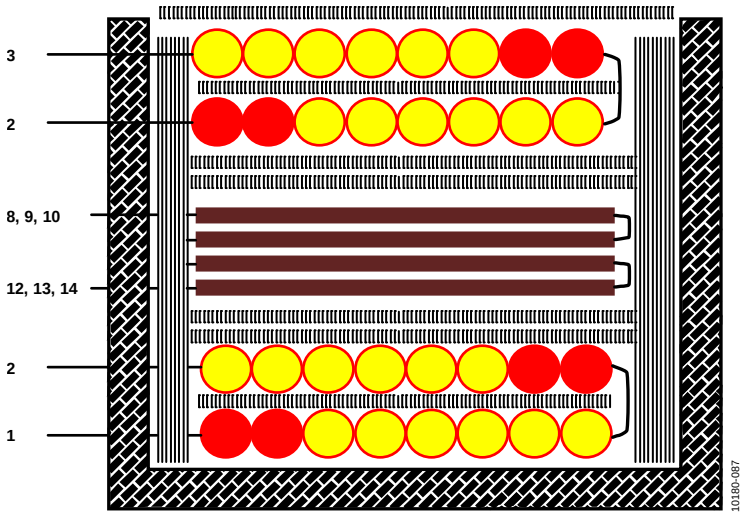

Figure 89. Transformer Construction Diagram

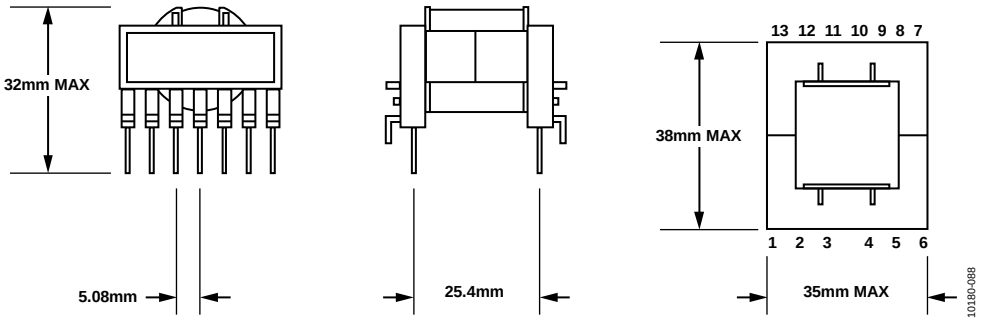

Figure 90. Transformer Bobbin Diagram

APPENDIX II—OUTPUT INDUCTOR SPECIFICATIONS

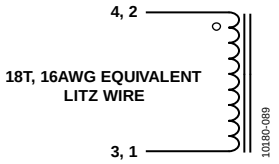

Figure 91. Output Inductor Electrical Diagram

Table 9. Output Inductor Specifications

Parameter	Min	Typ	Max	Unit	Notes
Core					77351A7, KoolMu, Magnetics, Inc.
Permeability (μ_o)	60				
Inductance	6.5	10	16	µH	Maximum at no load, typical at full load
DC Resistance		10		mΩ	

APPENDIX III—REGISTER FILE (ADP1046_I2SF_032011.46R)

Table 10.

Register Address	Programmed Setting	Name
0x0	0x00	Fault Register 1
0x1	0x00	Fault Register 2
0x2	0x00	Fault Register 3
0x3	0x01	Fault Register 4
0x4	0x00	Latched Fault Register 1
0x5	0x00	Latched Fault Register 2
0x6	0x00	Latched Fault Register 3
0x7	0x61	Latched Fault Register 4
0x8	0x03	Fault Configuration Register 1
0x9	0x33	Fault Configuration Register 2
0xA	0x30	Fault Configuration Register 3
0xB	0x03	Fault Configuration Register 4
0xC	0x20	Fault Configuration Register 5
0xD	0x80	Fault Configuration Register 6
0xE	0x45	Flag configuration
0xF	0x23	Soft start flag blank
0x10	0x00	First Flag ID
0x11	0xE6	RTD current settings
0x12	0x00	HF ADC reading
0x13	0x3AFC	CS1 value
0x14	0xC7EC	ACSNS value
0x15	0xA0BC	VS1 voltage value
0x16	0xA098	VS2 voltage value
0x17	0xA000	VS3 voltage value
0x18	0x5644	CS2 value
0x19	0x00	CS2 × VS3 value
0x1A	0x5C34	RTD temperature value
0x1B	0x00	Read temperature
0x1C	0x00	RTD offset trim MSB
0x1D	0x00	Share bus value
0x1E	0x54	Modulation value
0x1F	0x00	Line impedance value
0x20	0x07	RTD offset trim setting (LSB)
0x21	0x84	CS1 gain trim
0x22	0xAD	CS1 accurate OCP limit
0x23	0x00	CS2 gain trim
0x24	0x00	CS2 analog offset trim
0x25	0x00	CS2 digital offset trim
0x26	0x6B	CS2 accurate OCP limit
0x27	0xE3	CS1/CS2 fast OCP settings
0x28	0x46	Volt-second balance gain setting
0x29	0x04	Share bus bandwidth
0x2A	0xF1	Share bus setting
0x2B	0x82	Temperature gain trim
0x2C	0x82	PSON/soft start settings
0x2D	0x5A	PGOOD debounce and pin polarity setting
0x2E	0x26	Modulation limit
0x2F	0xA0	OTP threshold
0x30	0x1C	OrFET
0x31	0xA0	VS3 voltage setting

Register Address	Programmed Setting	Name
0x32	0x5A	VS1 overvoltage limit
0x33	0x0B	VS3 overvoltage limit
0x34	0x28	VS1 undervoltage limit
0x35	0xFF	Line impedance limit
0x36	0x07	Load line impedance
0x37	0xDD	Fast OVP comparator settings
0x38	0x00	VS1 trim
0x39	0x00	VS2 trim
0x3A	0x00	VS3 trim
0x3B	0x45	Light load disable setting
0x3C	0x00	Silicon revision ID
0x3D	0x00	Manufacturer ID
0x3E	0x00	Device ID
0x3F	0x9B	OUTAUX switching frequency setting
0x40	0x1B	PWM switching frequency setting
0x41	0x00	PWM1 positive edge timing
0x42	0x01	PWM1 positive edge setting
0x43	0x00	PWM1 negative edge timing
0x44	0x18	PWM1 negative edge setting
0x45	0x00	PWM2 positive edge timing
0x46	0x00	PWM2 positive edge setting
0x47	0x00	PWM2 negative edge timing
0x48	0x18	PWM2 negative edge setting
0x49	0x02	PWM3 positive edge timing
0x4A	0x88	PWM3 positive edge setting
0x4B	0x51	PWM3 negative edge timing
0x4C	0xC0	PWM3 negative edge setting
0x4D	0x2A	PWM4 positive edge timing
0x4E	0x10	PWM4 positive edge setting
0x4F	0x2A	PWM4 negative edge timing
0x50	0x18	PWM4 negative edge setting
0x51	0x2A	SR1 positive edge timing
0x52	0x00	SR1 positive edge setting
0x53	0x2A	SR1 negative edge timing
0x54	0x18	SR1 falling edge setting
0x55	0x2C	SR2 rising edge Timing
0x56	0x88	SR2 rising edge setting
0x57	0x27	SR2 falling edge timing
0x58	0x80	SR2 falling edge setting
0x59	0x00	PWM OUTAUX rising edge timing
0x5A	0x00	PWM OUTAUX rising edge setting
0x5B	0x0A	PWM OUTAUX falling edge timing
0x5C	0x08	PWM OUTAUX falling edge setting
0x5D	0x00	PWM and SRx pin disable setting
0x5E	0x7F	ACSNS gain trim
0x5F	0xD2	Soft start and output voltage slew rate setting
0x60	0x22	Normal mode digital filter LF gain setting
0x61	0xF2	Normal mode digital filter zero setting
0x62	0xCA	Normal mode digital filter pole setting
0x63	0x3D	Normal mode digital filter HF gain setting
0x64	0x22	Light load digital filter LF gain setting
0x65	0xF2	Light load digital filter zero setting
0x66	0xCA	Light load digital filter pole setting

Register Address	Programmed Setting	Name
0x67	0x3D	Light load digital filter HF gain setting
0x68	0x07	Adaptive dead time threshold
0x69	0x88	Dead Time 1
0x6A	0x88	Dead Time 2
0x6B	0x88	Dead Time 3
0x6C	0x88	Dead Time 4
0x6D	0x88	Dead Time 5
0x6E	0x88	Dead Time 6
0x6F	0x88	Dead Time 7
0x70	0x00	Dead time configuration
0x71	0x22	Soft start digital filter LF gain setting
0x72	0xF2	Soft start digital filter zero setting
0x73	0xCA	Soft start digital filter pole setting
0x74	0x3D	Soft start digital filter HF gain setting
0x75	0x04	Voltage line feedforward settings
0x76	0x30	Volt-second balance OUTA/OUTB settings
0x77	0x02	Volt-second balance OUTC/OUTD settings
0x78	0x00	Volt-second balance SR1/SR2 Settings
0x79	0x00	SR delay compensation
0x7A	0x0F	Filter transitions
0x7B	0x1F	PGOOD1 masking register
0x7C	0x60	PGOOD2 masking register
0x7D	0x34	Light load mode threshold settings
0x7E	0x00	Reserved
0x7F	0x00	GO byte

APPENDIX IV—BOARD FILE (ADP1046_I2SF_032011.46B)

```
Input Voltage = 385 V
N1 = 44
N2 = 4
R (CS2) = 1.75 mOhm    /* use 0.85mOhm for high side sensing with OrFET RDS_ON
I (load) = 25 A
R1 = 11 KOhm
R2 = 1 KOhm
C3 = 1 uF
C4 = 1 uF
N1 (CS1) = 1
N2 (CS1) = 50
R (CS1)  = 20 Ohm
ESR (L1) = 8 mOhm
L1 = 10 uH
C1 = 2700 uF
ESR (C1) = 16 mOhm
ESR (L2) = 10 mOhm
L2 = 0 uH
C2 = 1000 uF
ESR (C2) = 23 mOhm
R (Normal-Mode) (Load) = 0.48 Ohm
R (Light-Load-Mode) (Load) = 2 Ohm
Cap Across R1 & R2 = 0 "(1 = Yes: 0 = No)"
Topology = 3 (0 = Full Bridge: 1 = Half Bridge: 2 = Two Switch Forward: 3 = Interleaved Two
Switch Forward: 4 = Active Clamp Forward: 5 = Resonant Mode: 6 = Custom)
Switches / Diodes = 0 (0 = Switches: 1 = Diodes)
High Side / Low Side Sense (CS2) = 0 (1 = High-Side: 0 = Low-Side Sense)
Second LC Stage = 1 (1 = Yes: 0 = No)
CS1 Input Type = 0 (1 = AC: 0 = DC)
R3 = 0 KOhm
R4 = 0 KOhm
PWM Main = 0 (0 = OUTA: 1 = OUTB: 2 = OUTC: 3 = OUTD: 4 = SR1: 5 = SR2: 6 = OUTAUX)
C5 = 0 uF
C6 = 0 uF
R6 = 27 KOhm
R7 = 1 KOhm
```

RELATED LINKS

Resource	Description
ADP3654	Product Page, High Speed, Dual, 4 A MOSFET Driver
ADP1111	Product Page, Micropower, Step-Up/Step-Down SW Regulator; Adjustable and Fixed 3.3 V, 5 V, 12 V
ADP1046	Product Page, High Speed Converter Evaluation Platform (FPGA-based data capture kit)
ADP3303	Product Page, High Accuracy anyCAP® 200 mA Low Dropout Linear Regulator

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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