



ECP5™ Automotive Family

Preliminary Data Sheet

FPGA-DS-02014 Version 1.0

September 2016

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVC MOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PIO	Programmable I/O
PLL	Phase Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SCM	Serial Configuration Mode
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPCM	Slave Parallel Configuration Mode
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing

1. General Description

The ECP5 Automotive family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5 Automotive device family covers look-up-table (LUT) capacity to 44K logic elements and supports up to 203 user I/Os. The ECP5 Automotive device family also offers up to 72 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5 Automotive FPGA fabric is optimized to reach high performance with low power and low cost in mind. The ECP5 Automotive devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5 Automotive device family supports a broad range of interface standards, including DDR2/3, LPDDR2/3, XGMII and 7:1 LVDS.

The ECP5 Automotive device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE, XAUI, and SGMII), and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5 Automotive devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Semiconductor Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5 Automotive FPGA family. Synthesis library support for ECP5 Automotive devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5 Automotive device.

The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for the ECP5 Automotive family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of the design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
 - 12K to 44K LUTs
 - 197 to 203 user programmable I/Os
- Embedded SERDES
 - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
 - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
 - Up to four channels per device: PCI Express, Ethernet (1GbE, XAUI, and SGMII), and CPRI
- sysDSP™
 - Fully cascadable slice architecture
 - 12 to 160 slices for high performance multiply and accumulate
 - Powerful 54-bit ALU operations
 - Time Division Multiplexing MAC Sharing
 - Rounding and truncation
 - Each slice supports
 - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
 - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
 - Up to 1.944 Mb sysMEM™ Embedded Block RAM (EBR)
 - 194K to 351K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
 - Four DLLs and four PLLs in LAE5-45; two DLLs and two PLLs in LAE5-25 and LAE5-12
- Pre-engineered Source Synchronous I/O
 - DDR registers in I/O cells
 - Dedicated read/write levelling functionality
 - Dedicated gearing logic
 - Source synchronous standards support
 - ADC/DAC, 7:1 LVDS, XGMII
 - High Speed ADC/DAC devices

- Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
 - On-chip termination
 - LVTTTL and LVCMOS 33/25/18/15/12
 - SSTL 18/15 I, II
 - HSUL12
 - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
 - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
 - Shared bank for configuration I/Os
 - SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
 - Soft Error Detect – Embedded hard macro
 - Soft Error Correction – Without stopping user operation
 - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
 - IEEE 1149.1 and IEEE 1532 compliant
 - Reveal Logic Analyzer
 - On-chip oscillator for initialization and general use
 - 1.1 V core power supply

Table 1.1. ECP5 Automotive Family Selection Guide

Device	LAESUM-25	LAESUM-45	LAESU-12
LUTs (K)	24	44	12
sysMEM Blocks (18 Kb)	56	108	32
Embedded Memory (Kb)	1,008	1944	576
Distributed RAM Bits (Kb)	194	351	97
18 X 18 Multipliers	28	72	28
SERDES (Dual/Channels)	1/2	2/4	0
PLLs/DLLs	2/2	4/4	2/2
Packages and SERDES Channels / I/O Combinations			
381 caBGA (17 x 17 mm ²)	2/197	4/203	0/197

2. Architecture

2.1. Overview

Each ECP5 Automotive device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in [Figure 2.1](#). LAE5-45 devices have two rows. Both LAE5-25 and LAE5-12 devices have one row. In addition, the LAESUM devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM, and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5 Automotive devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5 Automotive devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 Automotive devices feature up to four embedded 3.2 Gb/s SERDES (Serializer/Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding/decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs, PIO pair, with their respective sysI/O buffers. The sysI/O buffers of the ECP5 Automotive devices are arranged in seven banks allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5 Automotive registers in PFU and sysI/O can be configured to be SET or RESET. After power up, the device is configured and then enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided PLLs, DLLs, and configuration functions. The ECP5 Automotive architecture provides up to four Delay Locked Loops (DLLs) and up to four Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates, and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5 Automotive family supports a sysCONFIG™ port located in that same corner, powered by V_{CCIO8}, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 Automotive devices use 1.1 V as their core voltage.

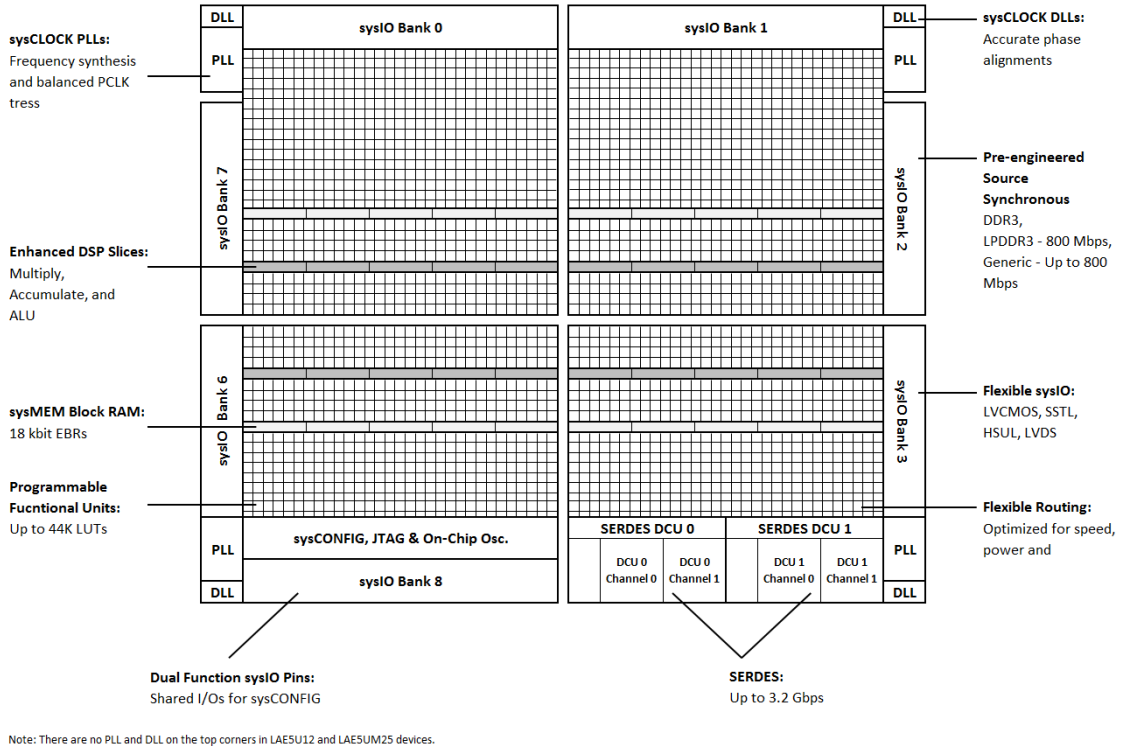


Figure 2.1. Simplified Block Diagram of LAE5UM-45 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5 Automotive device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0 – 3 as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in different modes.

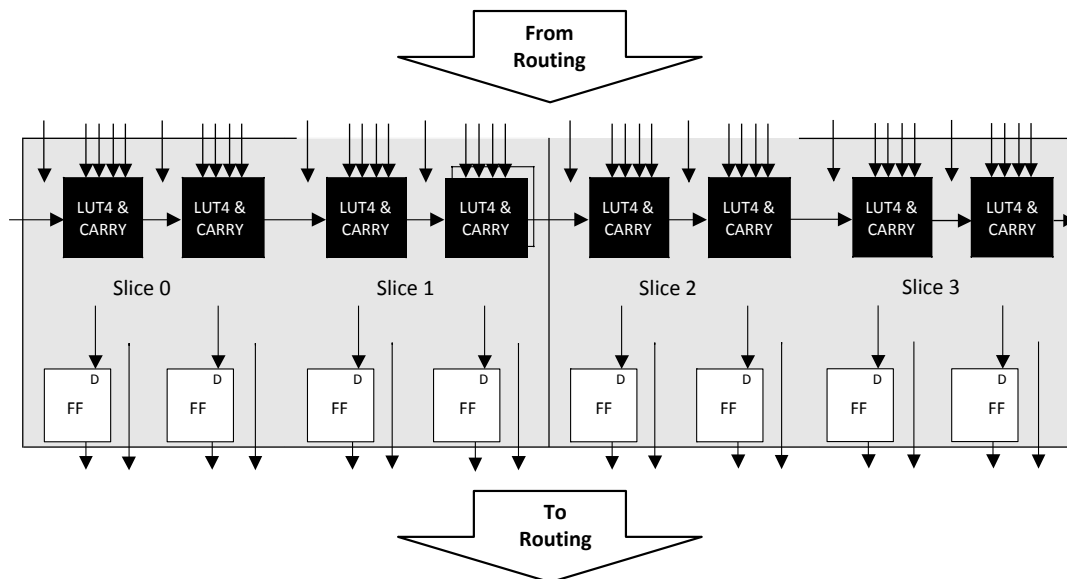


Figure 2.2. PFU Diagram

2.2.1. Slice

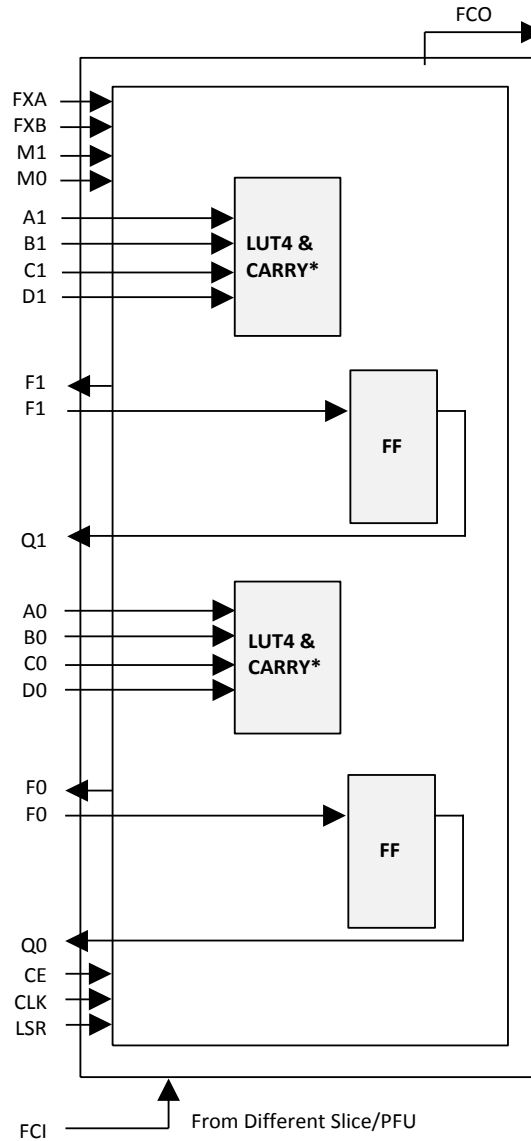
Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. [Table 2.1](#) shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions, which can be programmed as synchronous/asynchronous, clock select, chip-select, and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

[Figure 2.3](#) shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals: 13 signals from routing and 1 signal from the carry-chain routed from the adjacent slice or PFU. There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7, and LUT8. [Table 2.2](#) and [Figure 2.3](#) list the signals associated with all the slices. [Figure 2.4](#) shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7, and LUT8.



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

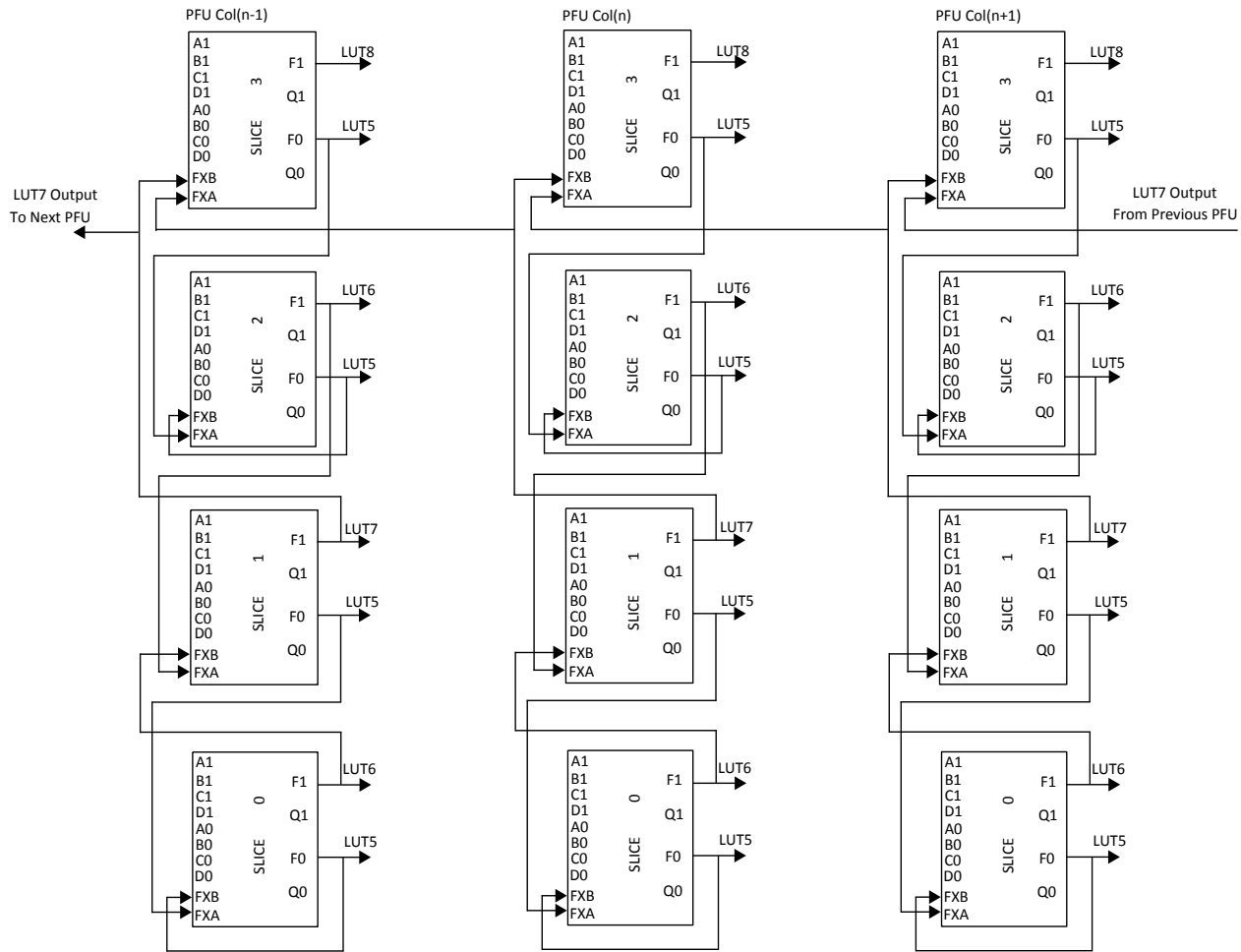


Figure 2.4. Connectivity Supporting LUT5, LUT6, LUT7, and LUT8

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8 ²
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output ¹

Notes:

1. See Figure 2.3 on page 13 for connection details.
2. Requires two adjacent PFUs.

2.2.2. Modes of Operation

Slices 0 – 2 have up to four potential modes of operation: Logic, Ripple, RAM, and ROM. Slice 3 is not needed for RAM mode, it can be used in Logic, Ripple, or ROM modes.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with synchronous preload
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration, also referred to as CCU2 mode, two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed in one PFU using each LUT block in Slice 0 and Slice 1 as a 16 x 2-bit memory in each slice. Slice 2 is used to provide memory address and control signals.

A 16 x 2-bit pseudo dual port RAM (PDPR) memory is created in one PFU by using one Slice as the read-write port and the other companion slice as the read-only port. The slice with the read-write port updates the SRAM data contents in both slices at the same write cycle.

ECP5 Automotive devices support distributed memory initialization.

The Lattice Semiconductor design tools support the creation of a variety of different size memories. Where appropriate, the software will construct memories using distributed memory primitives that represent the capabilities of the PFU. [Table 2.3](#) lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in ECP5 Automotive devices, refer to TN1264, [ECP5 and ECP5-5G Memory Usage Guide](#).

Table 2.3. Number of Slices Required to Implement Distributed RAM

	SPR 16 X 4	PDPR 16 X 4
Number of slices	3	6

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to TN1264, [ECP5 and ECP5-5G Memory Usage Guide](#).

2.3. Routing

There are many resources provided in the ECP5 Automotive devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect segments. The ECP5 Automotive family has an enhanced routing architecture that produces a compact design. The Diamond design software tool suites take the output of the synthesis tool and places and routes the design.

2.4. Clocking Structure

ECP5 Automotive clocking structure consists of:

- Clock synthesis blocks and sysCLOCK PLL;
- Balanced clock tree networks, PCLK, and ECLK trees;
- Efficient clock logic modules, CLOCK DIVIDER and Dynamic Clock Select (DCS), Dynamic Clock Control (DCC), and DLL.

Each of these functions is described as follows.

2.5. sysCLOCK PLL

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the ECP5 Automotive family support two to four full-featured General Purpose PLLs. The sysCLOCK PLLs provide the ability to synthesize clock frequencies.

The architecture of the PLL is shown in [Figure 2.5](#). Following is the description of the PLL functionality.

- CLKI is the reference frequency input to the PLL and its source can come from two different external CLK inputs or from internal routing. A non-glitchless 2-to-1 input multiplexor is provided to dynamically select between two different external reference clock sources. The CLKI input feeds into the input Clock Divider block.
- CLKFB is the feedback signal to the PLL that can come from internal feedback path, routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.
- The PLL has four clock outputs CLKOP, CLKOS, CLKOS2, and CLKOS3. Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the primary clock network. Only CLKOP and CLKOS outputs can go to the edge clock network.
- The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the PHASESEL, PHASEDIR, PHASESTEP, and PHASELOADREG ports.
- The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected.

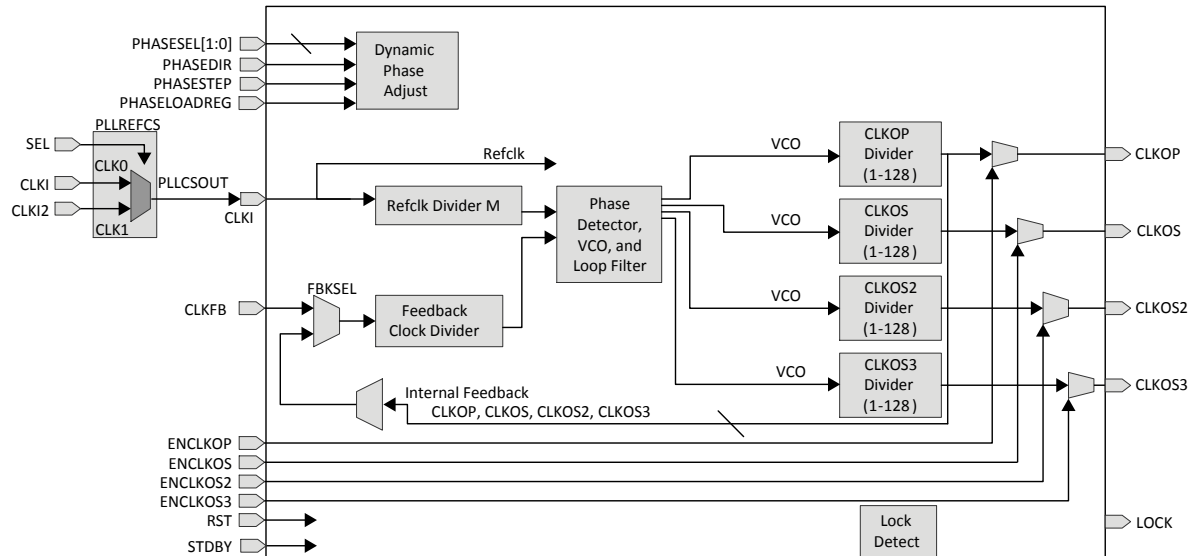


Figure 2.5. General Purpose PLL Diagram

Table 2.4 provides a description of the signals in the PLL blocks.

Table 2.4. PLL Blocks Signal Descriptions

Signal	Type	Description
CLKI	Input	Clock Input to PLL from external pin or routing
CLKI2	Input	Muxed clock input to PLL
SEL	Input	Input Clock select, selecting from CLKI and CLKI2 inputs
CLKFB	Input	PLL Feedback Clock
PHASESEL[1:0]	Input	Select which output to be adjusted on Phase by PHASEDIR, PHASESTEP, PHASELOADREG
PHASEDIR	Input	Dynamic Phase adjustment direction
PHASESTEP	Input	Dynamic Phase adjustment step
PHASELOADREG	Input	Load dynamic phase adjustment values into PLL
CLKOP	Output	Primary PLL output clock with phase shift adjustment
CLKOS	Output	Secondary PLL output clock with phase shift adjust
CLKOS2	Output	Secondary PLL output clock2 with phase shift adjust
CLKOS3	Output	Secondary PLL output clock3 with phase shift adjust
LOCK	Output	PLL LOCK to CLKI, Asynchronous signal. Active high indicates PLL lock.
STDBY	Input	Standby signal to power down the PLL
RST	Input	Resets the PLL
ENCLKOP	Input	Enable PLL output CLKOP
ENCLKOS	Input	Enable PLL output CLKOS
ENCLKOS2	Input	Enable PLL output CLKOS2
ENCLKOS3	Input	Enable PLL output CLKOS3

For more details on the PLL, you can refer to the TN1263, [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide](#).

2.6. Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5 Automotive product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLL/DEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5 Automotive also supports glitchless dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitchless selection between two clocks for the PCLK network (DCS). Overview of Clocking Network is shown in [Figure 2.6](#) on page 18, for LAE5UM-45 device.

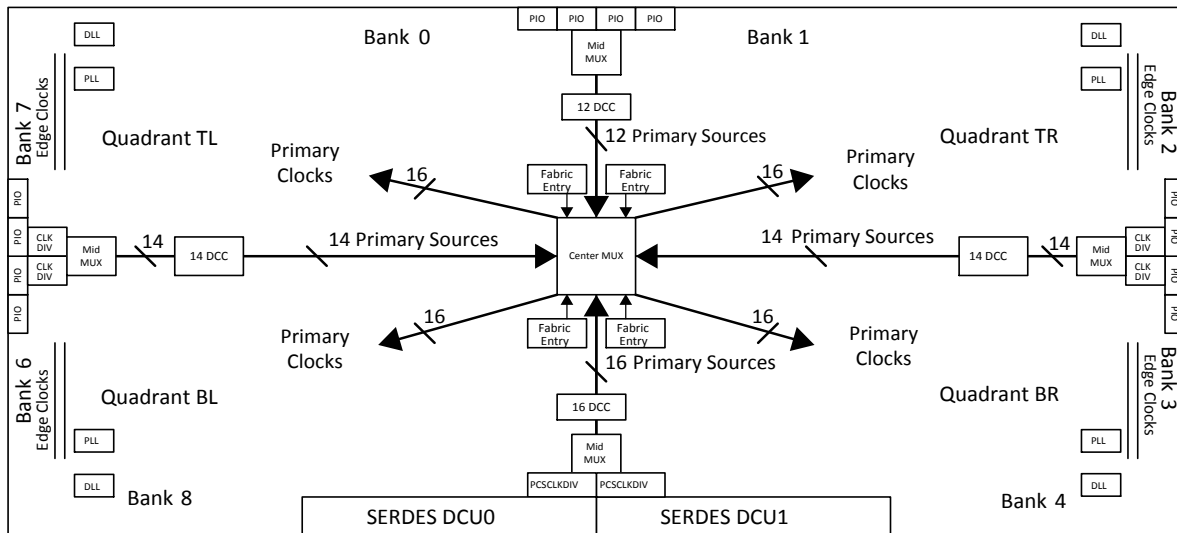


Figure 2.6. LAE5UM-45 Clocking

2.7. Primary Clocks

The ECP5 Automotive device family provides low-skew, high fanout clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Semiconductor Diamond software can automatically route each clock to one of the four quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Diamond software to locate the clock to specific quadrant. The ECP5 Automotive device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries with minimum general routing
- SERDES/PCS/PCSDIV clocks
- OSC clock

These sources are routed to one of the four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the ECP5 Automotive fabric. These routing muxes are shown in [Figure 2.6](#). Since there is a maximum of 60 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the ECP5 Automotive device. For more information about the primary clock tree and connections, refer to TN1263, [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide](#).

2.8. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to TN1263, [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide](#).

2.9. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two independent input clock sources either with or without any glitches. This is achieved regardless of when the selected signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it does not require running clocks when being used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

[Figure 2.7](#) shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to TN1263, [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide](#).

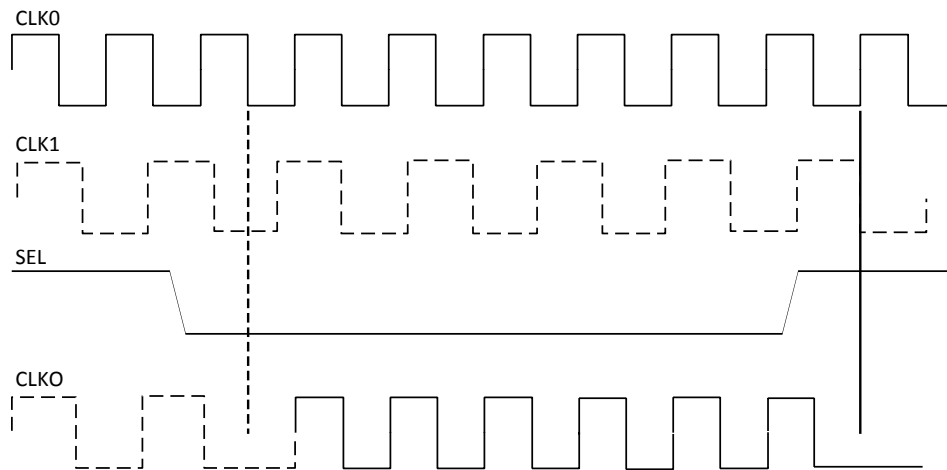


Figure 2.7. DCS Waveforms

2.10. Edge Clock

ECP5 Automotive devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90°)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

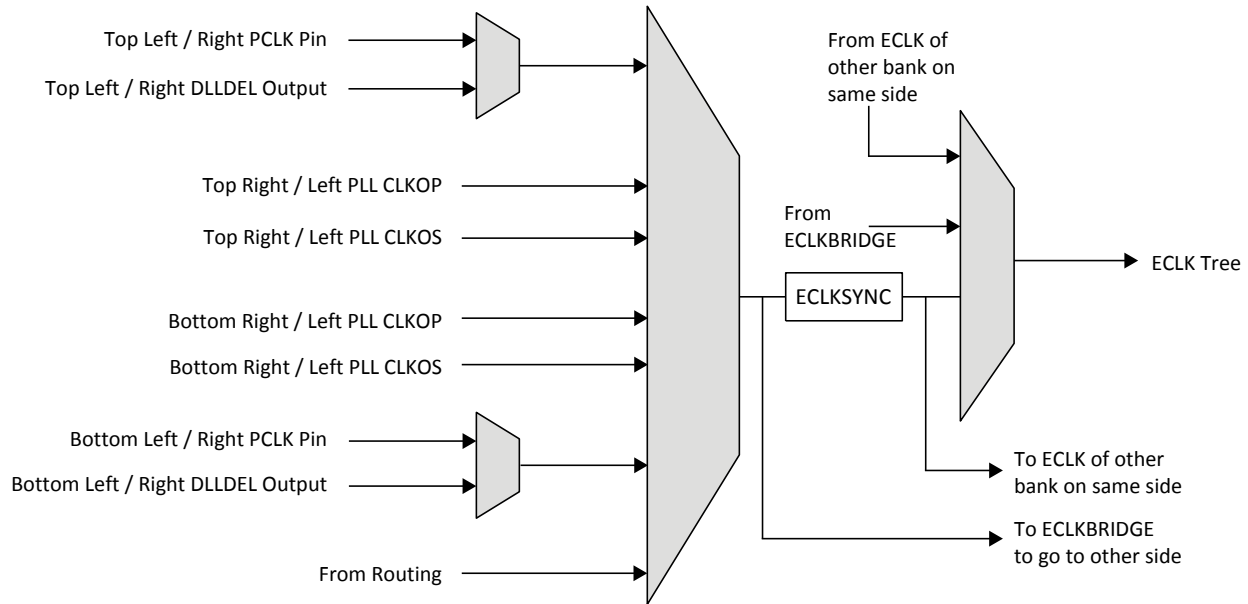


Figure 2.8. Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to TN1263, [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide](#).

2.11. Clock Dividers

ECP5 Automotive devices have two clock dividers, one on the left side and the other on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a $\div 2$, $\div 3.5$ mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal.

The clock dividers can be fed from selected PLL outputs, external primary clock pins multiplexed with the DDRDEL Slave Delay or from routing. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The SLIP signal slips the outputs one cycle relative to the input clock. For further information on clock dividers, refer to TN1263, [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide](#). Figure 2.9 shows the clock divider connections.

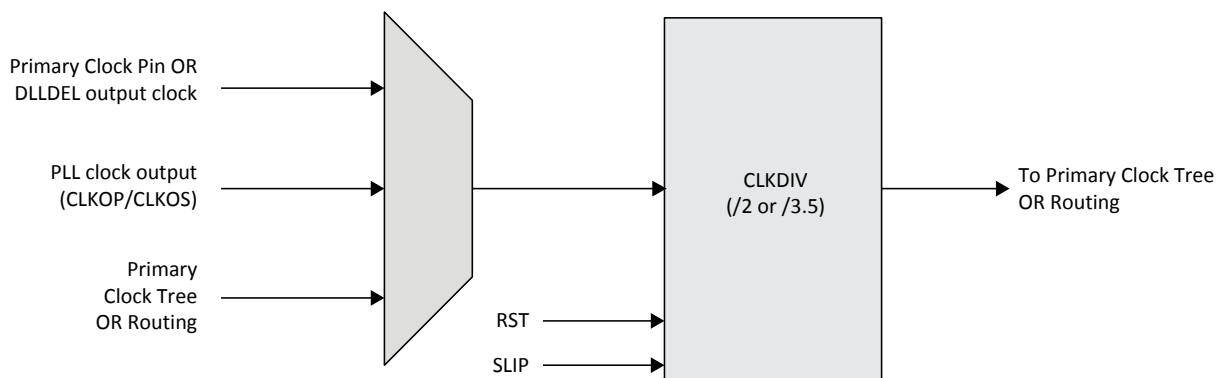


Figure 2.9. ECP5 Automotive Clock Divider Sources

2.12. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90-degree phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90-degree shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL and DLLDEL, which takes a clock input, and generates a 90-degree shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90-degree clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

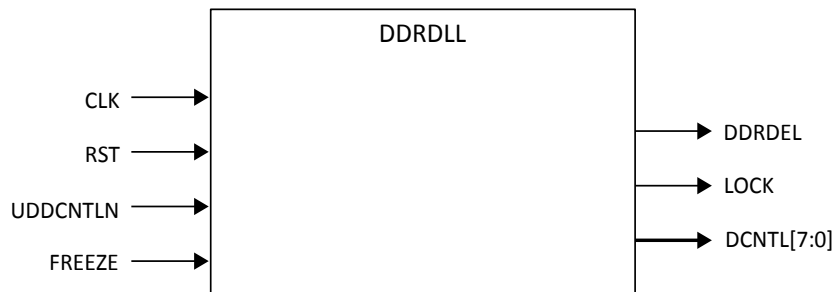


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delayed.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. When UDDCNTLN goes LOW, the delay code out the DDRDLL is updated. Should not be active during a read or a write cycle.
FREEZE	Input	FREEZE goes HIGH and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes LOW, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are identical DDRDLLs, four in each corner in LAE5-45 device and two in upper corners in both LAE5-25 and LAE5-12 devices. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL, DQSBUF, and DLLDEL use the code to delay the signal, to create the phase shifted signal used for either DDR memory, or to create 90-degree shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

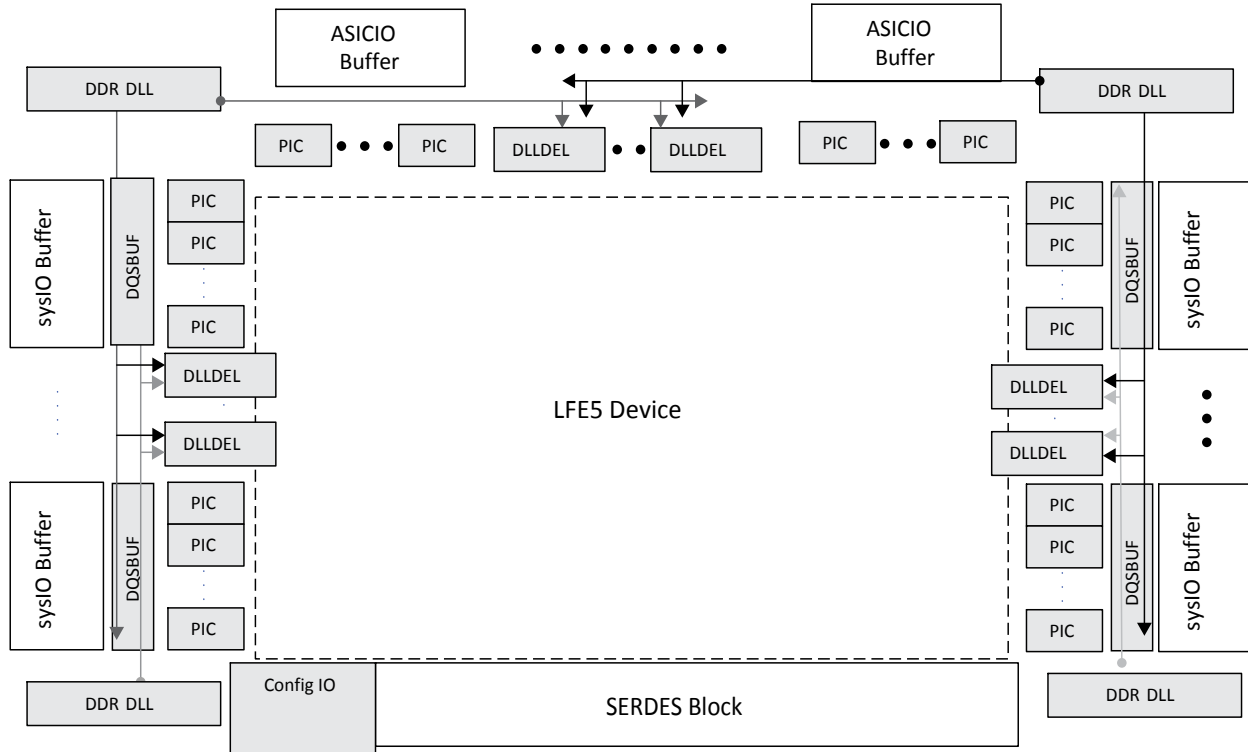


Figure 2.11. ECP5 Automotive DLL Top Level View for LFE-45

2.13. sysMEM Memory

ECP5 Automotive devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM, and FIFO buffers via external PFUs.

2.13.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.6 on page 23. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to TN1264, [ECP5 and ECP5-5G Memory Usage Guide](#).

Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36
True Dual Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36
Pseudo Dual Port	16,384 x 1
	8,192 x 2
	4,096 x 4
	2,048 x 9
	1,024 x 18
	512 x 36

2.13.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.13.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.13.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice Semiconductor design tools cascade memory transparently, based on specific design inputs.

2.13.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

- **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data at the current address does not appear on the output. This mode is supported for all data widths.
- **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
- **Read-Before-Write** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

2.13.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in [Figure 2.12](#).

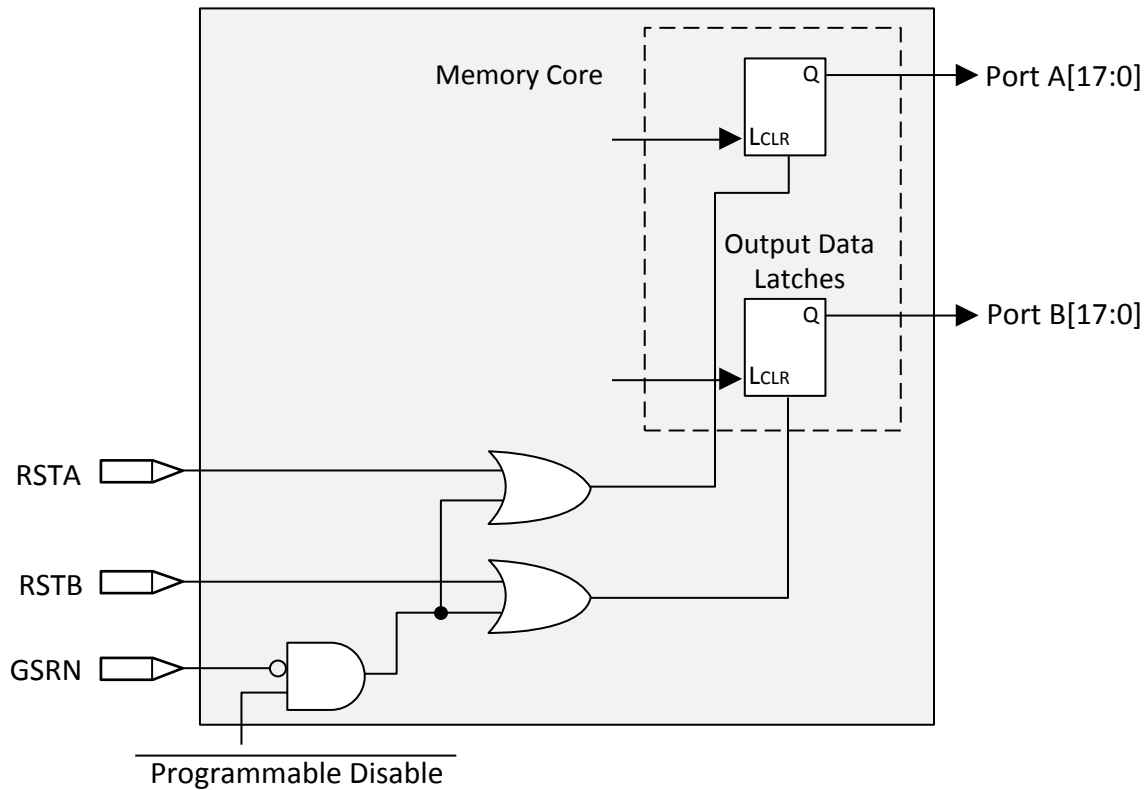


Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in [Supplemental Information](#) section on page 96.

2.14. sysDSP™ Slice

The ECP5 Automotive family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.14.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5 Automotive device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

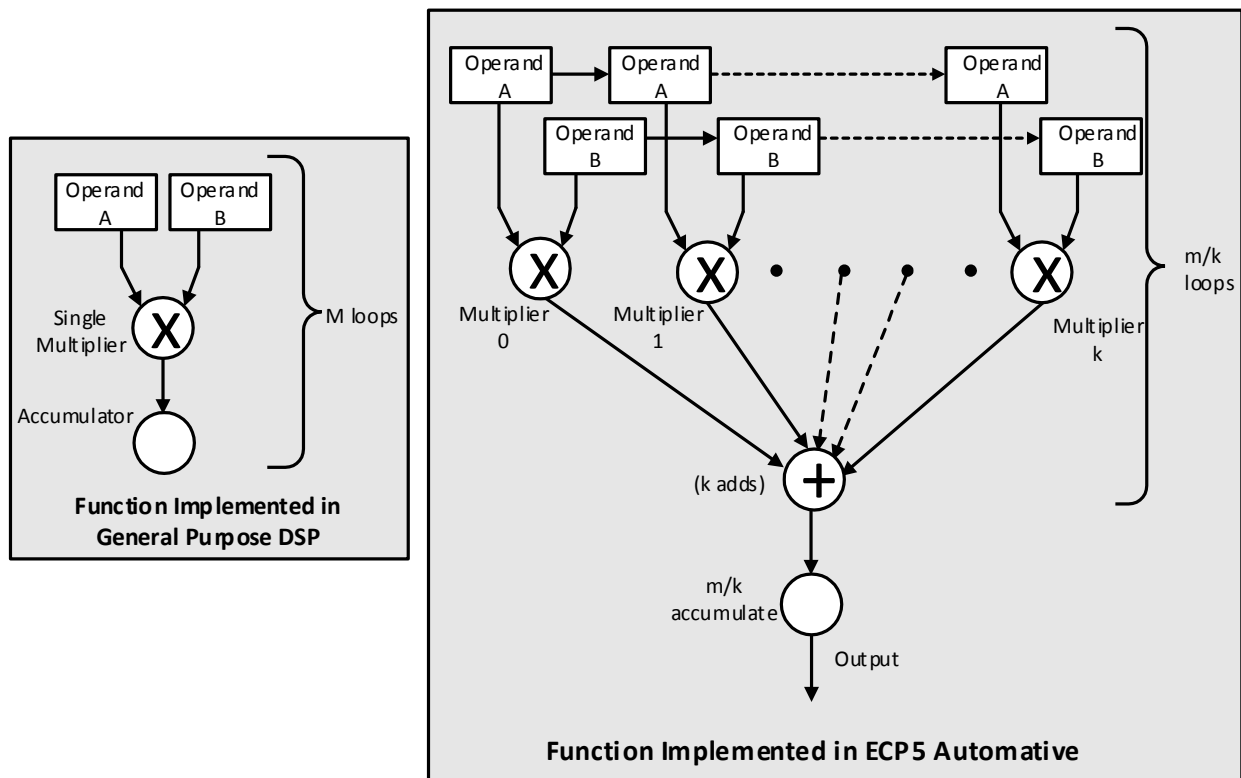


Figure 2.13. Comparison of General DSP and ECP5 Automotive Approaches

2.15. ECP5 Automotive sysDSP Slice Architecture Features

The ECP5 Automotive sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The ECP5 Automotive sysDSP Slice supports many functions that include the following:

- Fully double data rate support. Higher operation frequency (throughput of up to 370 Mb/s) is achieved by double input and output interfaces that enable twice the fabric operation throughput for most of the operation modes.
- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
 - Odd mode – Filter with Odd number of taps
 - Even mode – Filter with Even number of taps
 - Two dimensional (2D) symmetry mode – Supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture.
- Fully cascadable DSP across slices. Support for symmetric, asymmetric, and non-symmetric filters.
- Multiply function supports one 18x36, two 18x18, or four 9x9 multipliers per slice.
- Multiply function with the 36x36 multiplier uses two sysDSP slices.
- Multiply Accumulate supports one 18x36 multiplier result accumulation or two 18x18 multiplier result accumulation
- Two multipliers feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 multipliers feed into an accumulator that can accumulate up to 52 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
 - Odd mode – Filter with Odd number of taps
 - Even mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
 - 3*3 and 3*5 – Internal DSP Slice support
 - 5*5 and larger size 2D blocks – Semi-internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
 - Minimizes fabric use for common DSP and ALU functions
 - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
 - Provides matching pipeline registers
 - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) supports:
 - Dynamically selectable ALU OPCODE
 - Ternary arithmetic addition/subtraction of three inputs
 - Bit-wise two-input logic operations such as AND, OR, NAND, NOR, XOR, and XNOR
 - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as overflow, underflow and convergent rounding.
 - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in [Figure 2.14](#) on the next page, the ECP5 Automotive sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5 Automotive sysDSP slice. [Figure 2.14](#) shows the diagram of sysDSP. [Figure 2.15](#) shows the detailed diagram.

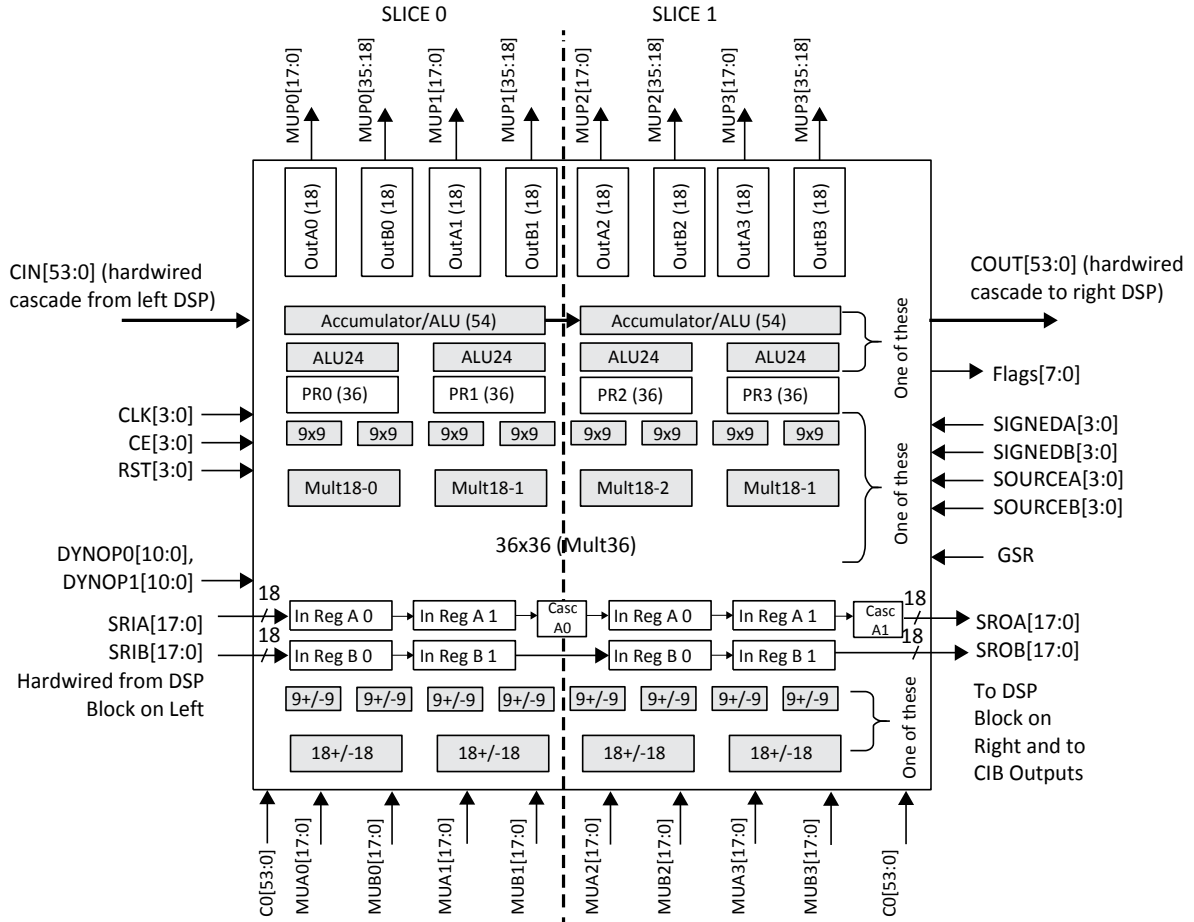


Figure 2.14. Simplified sysDSP Slice Block Diagram

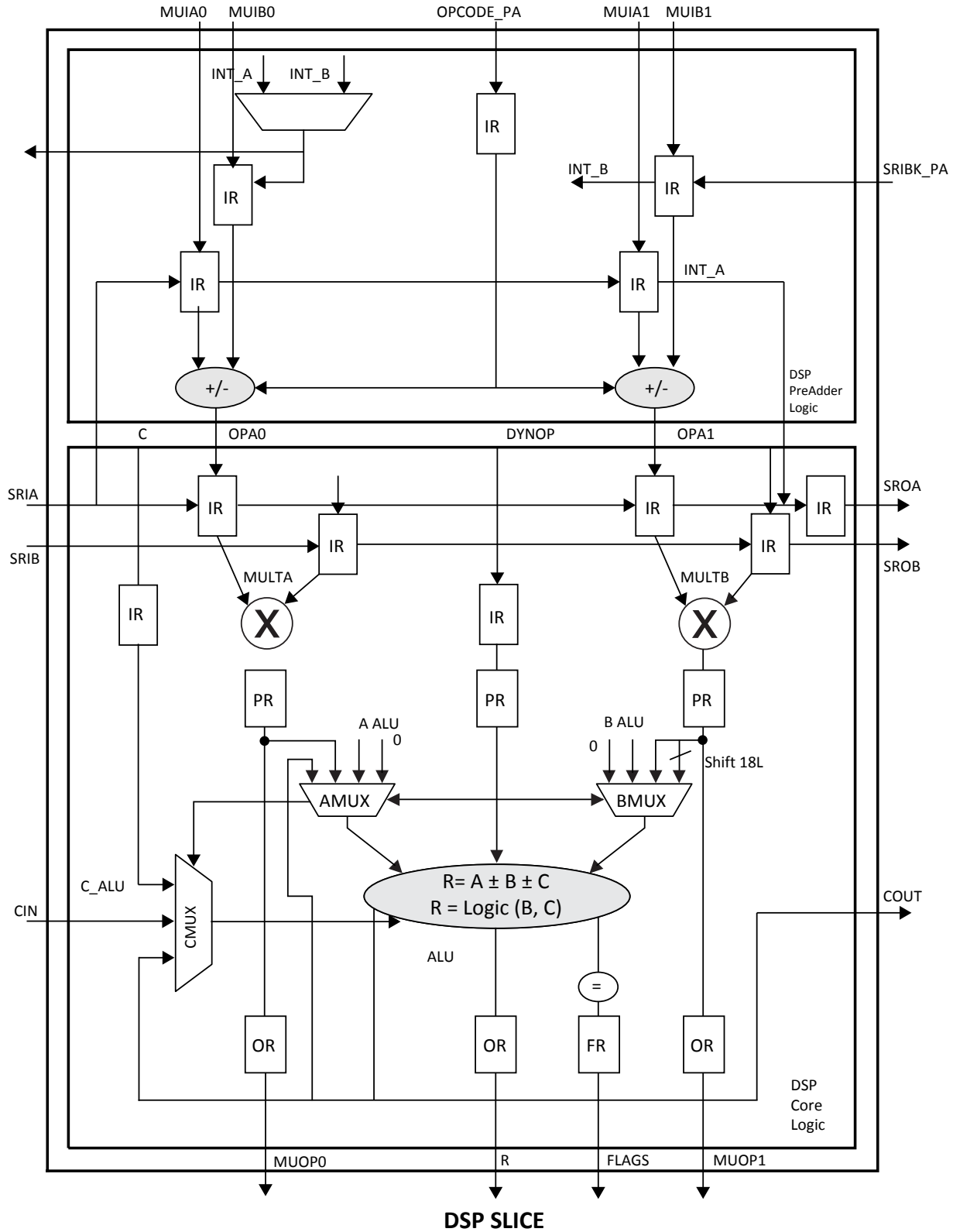


Figure 2.15. Detailed sysDSP Slice Diagram

In Figure 2.15, note that A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA, BB and C inputs. For further information, refer to TN1267, [ECP5 and ECP5-5G sysDSP Usage Guide](#).

The ECP5 Automotive sysDSP block supports the following basic elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5 Automotive slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

*Note: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the above four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation”, the following operations are possible:

- In the Add/Sub option, the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to TN1267, [ECP5 and ECP5-5G sysDSP Usage Guide](#).

2.16. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO is connected to their respective sysIO buffers and pads. On the ECP5 Automotive devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells that are called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5 Automotive devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

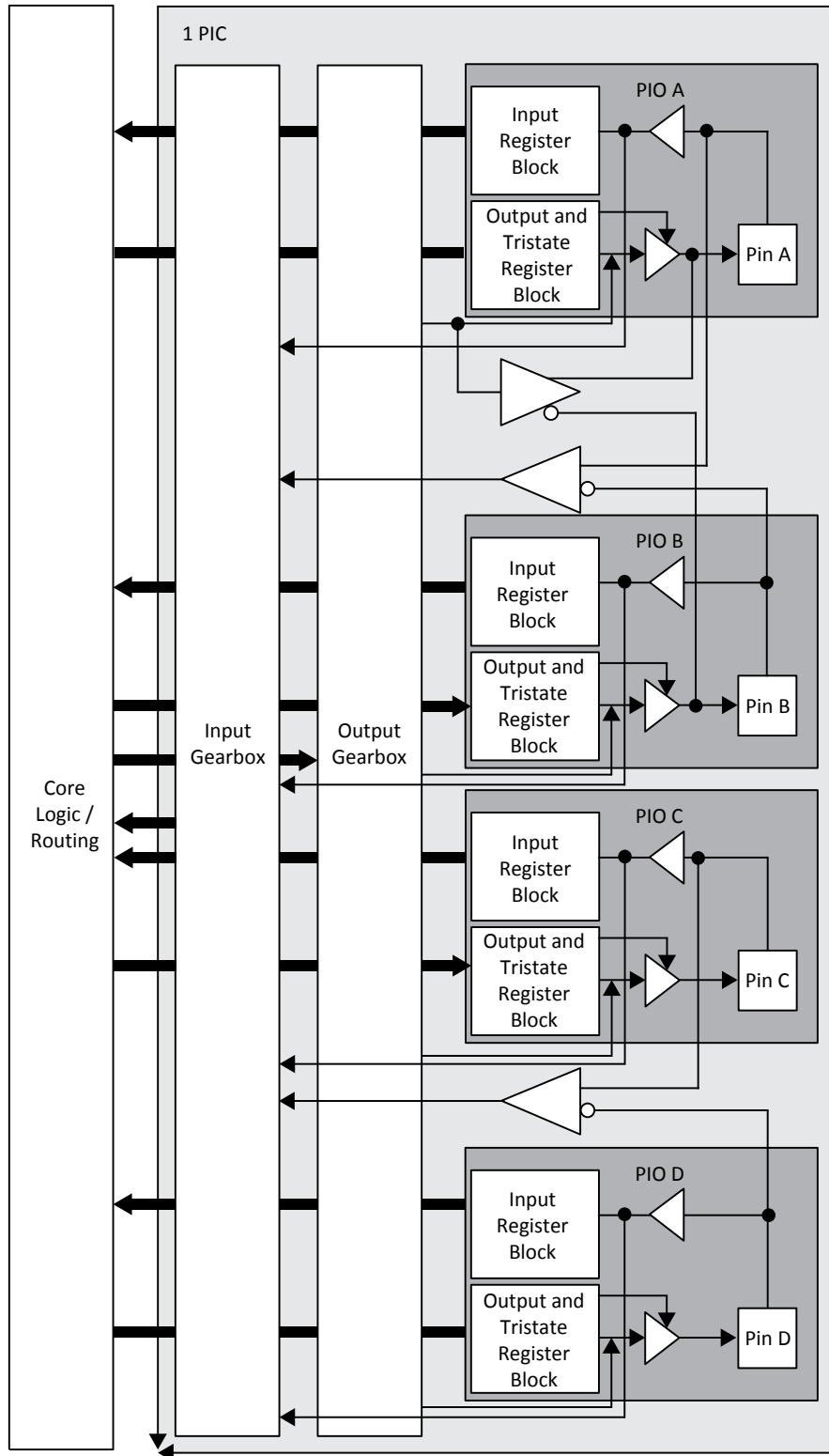


Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Side

2.17. PIO

The PIO contains three blocks: an input register block, an output register block, and a tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

2.17.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The Top side of the device will support IDDRX1 gearing function. For more information on gearing function, refer to TN1265, [ECP5 and ECP5-5G High-Speed I/O Interface](#).

Figure 2.17 shows the input register block for the PIOs on the top edge.

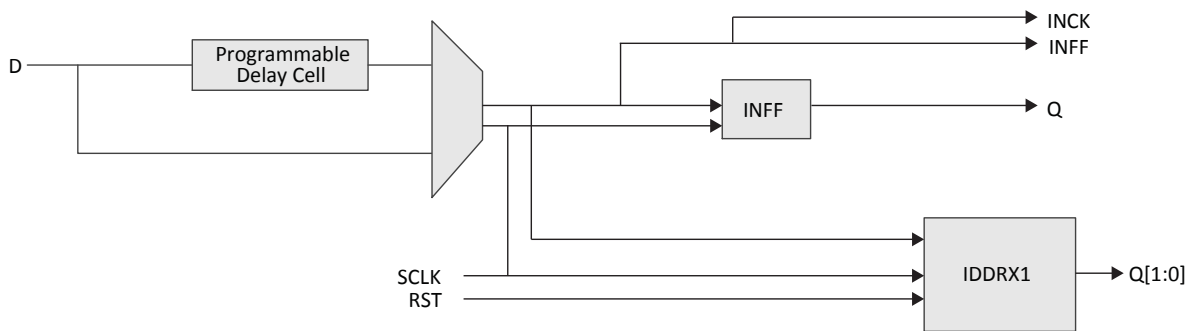
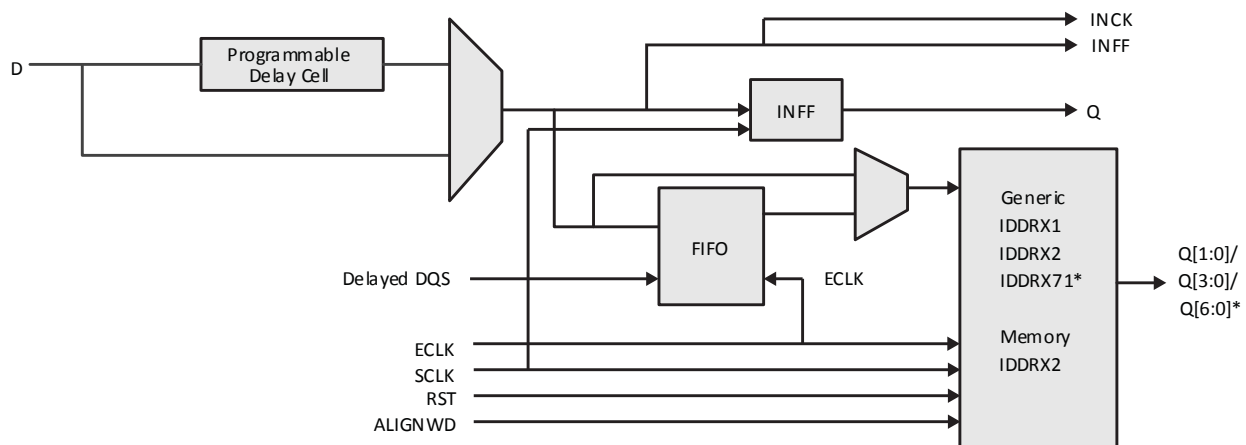


Figure 2.17. Input Register Block for PIO on Top Side of the Device

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



*Note: For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

Figure 2.18. Input Register Block for PIO on Left or Right Side of the Device

2.17.1.1. Input FIFO

The ECP5 Automotive PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in [DDR Memory Support](#) section on page 34.

Table 2.8. Input Block Port

Name	Type	Description
D	Input	High speed data input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low speed data to the device core
RST	Input	Reset to the output block
SCLK	Input	Slow speed system clock
ECLK	Input	High speed edge clock
DQS	Input	Clock from DQS control block used to clock DDR memory data
ALIGNWD	Input	Data alignment signal from device core

2.17.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers. ECP5 Automotive output data path has output programmable flip flops and output gearing logic. On the left and right sides the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks will support 1x gearing. ECP5 Automotive output data path diagram is shown in [Figure 2.19](#). The programmable delay cells are also available in the output data path. For detailed description of the output register block modes and usage, refer to TN1265, [ECP5 and ECP5-5G High-Speed I/O Interface](#).

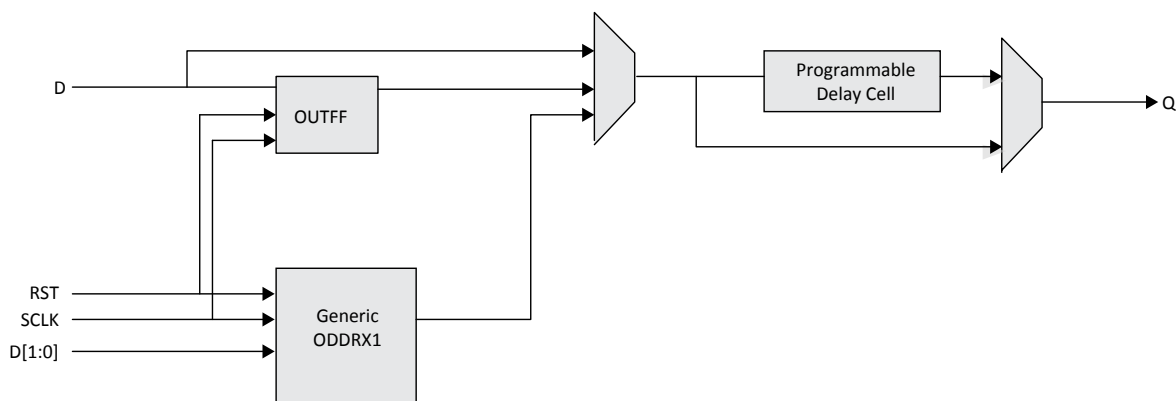
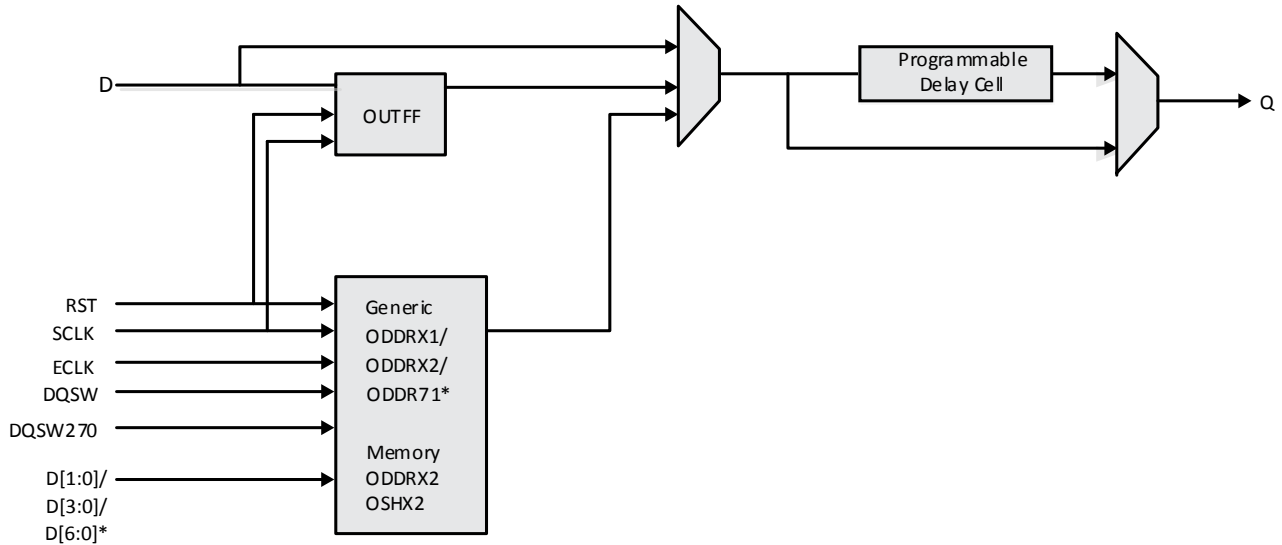


Figure 2.19. Output Register Block on Top Side



*Note: For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left or Right Side

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.18. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops, which feeds the output. DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to TN1265, [ECP5 and ECP5-5G High-Speed I/O Interface](#).

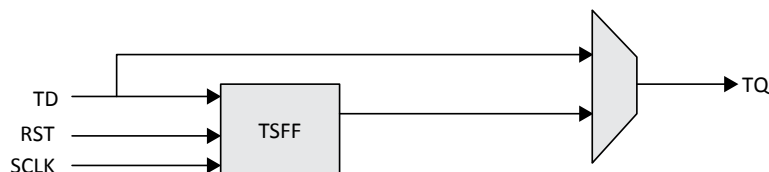


Figure 2.21. Tristate Register Block on Top Side

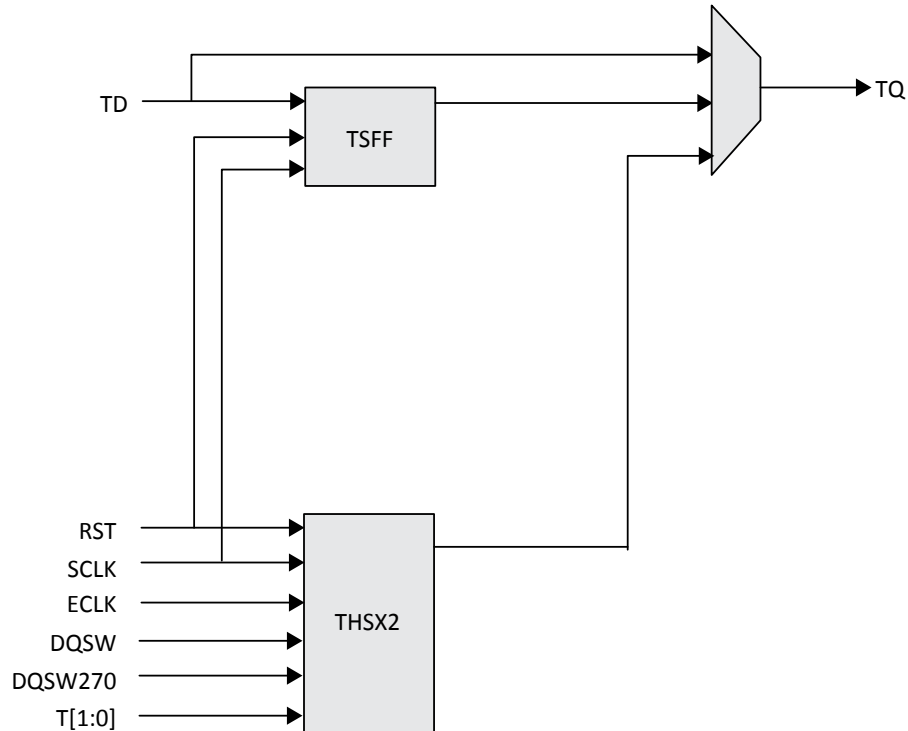


Figure 2.22. Tristate Register Block on Left or Right Side

Table 2.10. Tristate Block Port

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR register
RST	Input	Reset to the Tristate block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed system clock
ECLK	Input	High speed edge clock
DQSW	Input	Clock from DQS control block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.19. DDR Memory Support

2.19.1. DQS Grouping for DDR Memory

Some PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in Figure 2.23. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. For DQS groups with more than 11 pins bonded out, two pre-defined pins can be assigned as "virtual" V_{CCIO} by driving these pins to HIGH. These pins are required to be connected to V_{CCIO} power supply. These connections create "soft" connections to V_{CCIO} through these output pins, and make better connections on V_{CCIO} to help to reduce SSO noise. For details, refer to TN1265, [ECP5 and ECP5-5G High-Speed I/O Interface](#).

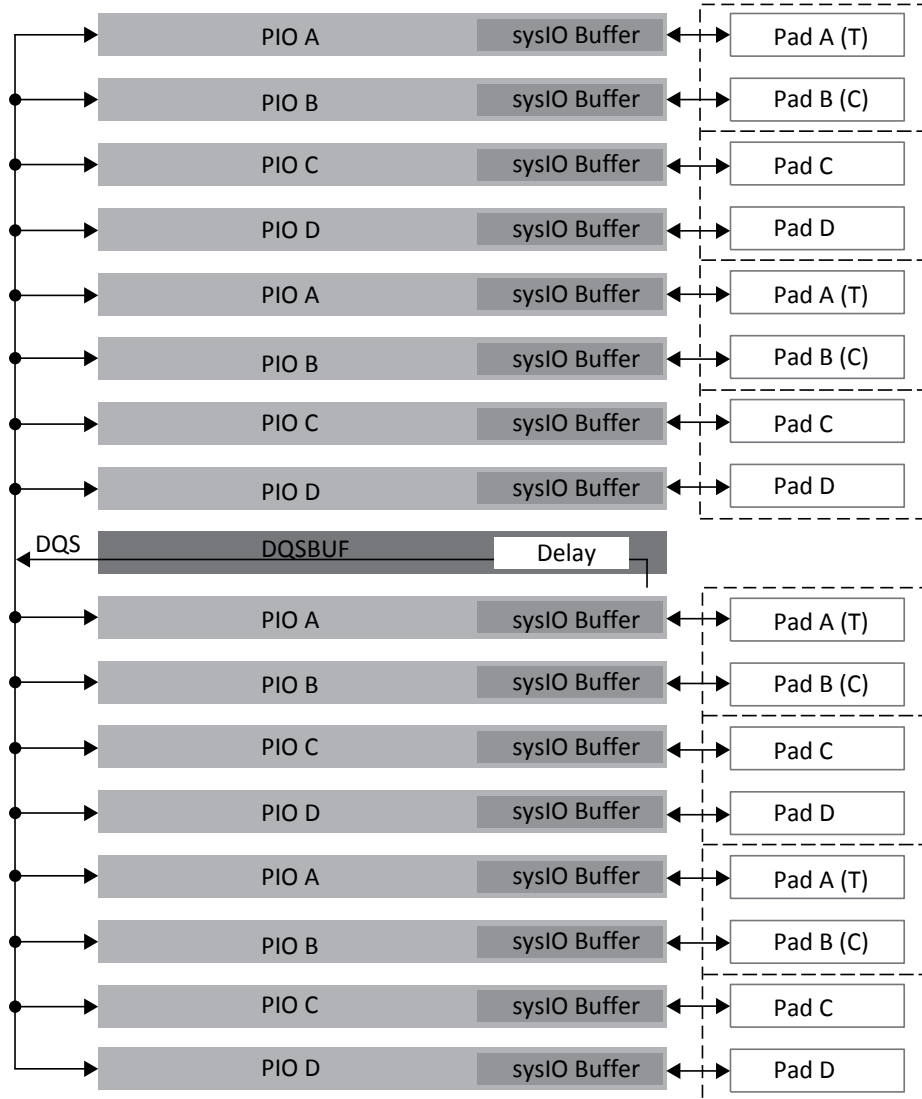


Figure 2.23. DQS Grouping on the Left and Right Edges

2.19.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces, DDR2/3, LPDDR2/3, the DQS strobe signal from the memory must be used to capture the data DQ in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifting is achieved by using DQSDEL programmable delay line in the DQS Delay Block. The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read or write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block included here generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

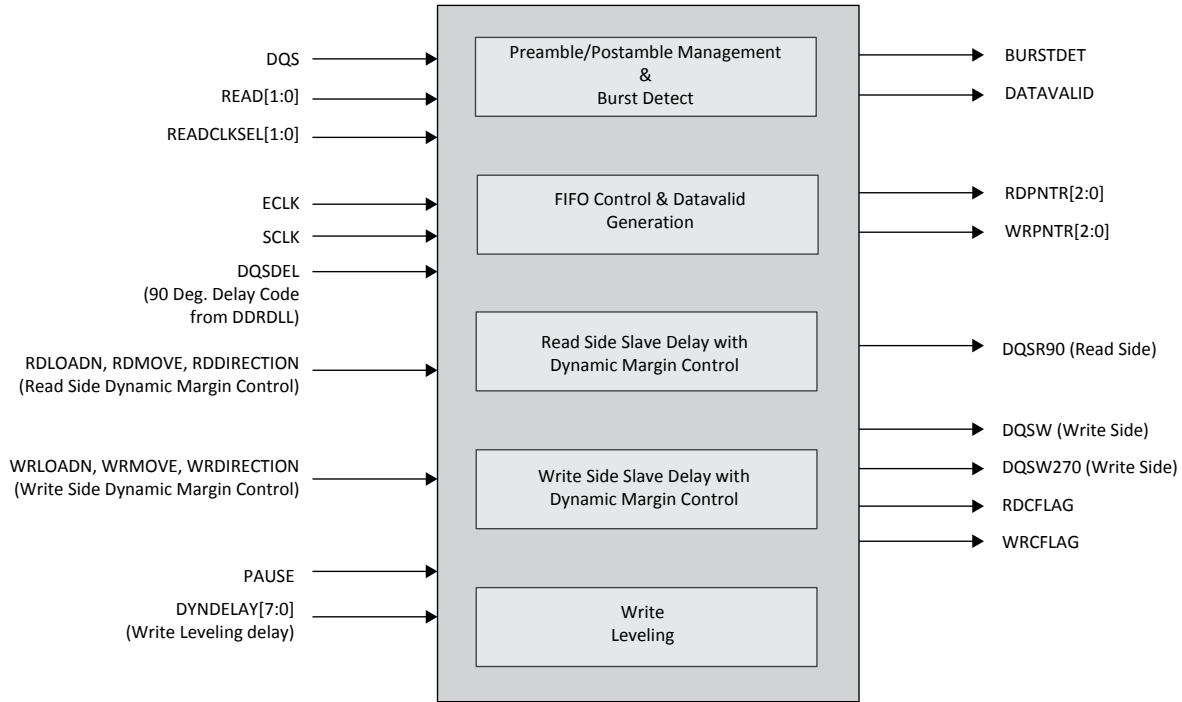


Figure 2.24. DQS Control and Delay Block (DQSBUF)

Table 2.11. DQSBUF Port list description

Name	Type	Description
DQS	Input	DDR memory DQS strobe
READ[1:0]	Input	Read Input from DDR controller
READCLKSEL[1:0]	Input	Read pulse selection
SCLK	Input	Slow system clock
ECLK	Input	High speed edge clock with the same frequency as that of the DDR memory)
DQSDEL	Input	90-degree delay code from DDRDLL
RDLOADN, RDMOVE, RDDIRECTION	Input	Dynamic margin control ports for Read delay
WRLOADN, WRMOVE, WRDIRECTION	Input	Dynamic margin control ports for Write delay
PAUSE	Input	Used by DDR controller to pause write side signals during DDRDLL code update or Write leveling
DYNDELAY[7:0]	Input	Dynamic Write leveling delay control
DQSR90	Output	90-degree delay DQS used for Read
DQSW270	Output	90-degree delay clock used for DQ Write
DQSW	Output	Clock used for DQS Write
RDPNTR[2:0]	Output	Read pointer for IFIFO module
WRPNTR[2:0]	Output	Write pointer for IFIFO module
DATAVALID	Output	Signal indicating start of valid data
BURSTDET	Output	Burst detect indicator
RDFLAG	Output	Read dynamic margin control output to indicate max value
WRFLAG	Output	Write dynamic margin control output to indicate max value

2.20. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTTL, LVPECL, and MIPI.

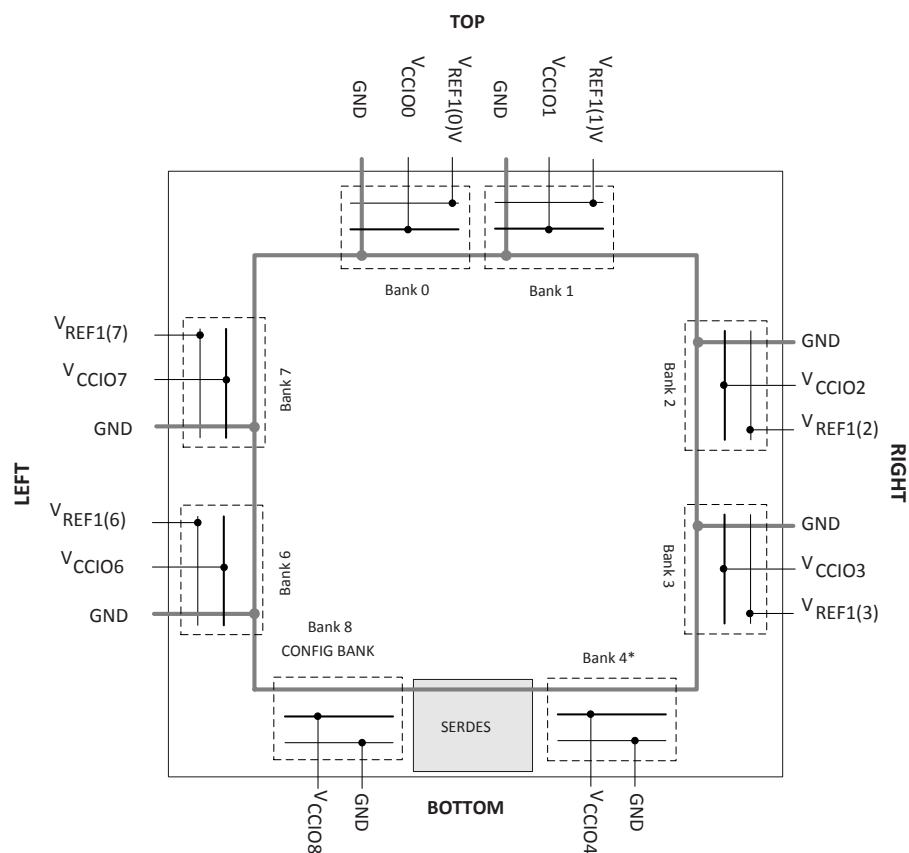
2.20.1. sysI/O Buffer Banks

ECP5 Automotive devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank, Bank 8, is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O.

In ECP5 Automotive devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage V_{CCIO} . In addition, the banks on the Left or Right side of the device, have voltage reference input, V_{REF1} per bank, which allow it to be completely independent of each other. This voltage reference input is a shared I/O pin. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5 Automotive devices, single-ended output buffers and ratioed input buffers, LVTTTL, and LVCMOS, are powered using V_{CCIO} . LVTTTL, LVCMOS33, LVCMOS25, and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .



*Note: Only 85K device has this bank.

Figure 2.25. ECP5 Automotive Device Family Banks

ECP5 Automotive devices contain two types of sysI/O buffer pairs:

- Top, Bank 0 and Bank 1, and Bottom, Bank 8 and Bank 4, single-ended sysI/O Buffer Pairs

The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and are configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

The top or bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for being used as emulated differential signaling.

Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

The top and bottom side pads can be identified by the Lattice Semiconductor Diamond tool.

- Left and right banks have 50% differential sysI/O buffer pairs and 100% single-ended outputs.

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers, both ratioed and referenced, and half of the sysI/O buffer pairs, PIOA/B pairs. Also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.20.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5 Automotive devices, see the list of technical documentation in [Supplemental Information](#) section on page 96.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.20.3. Supported sysI/O Standards

The ECP5 Automotive sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTTL and other standards. The buffers support the LVTTTL, LVCMOS 1.2V, 1.5V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to TN1262, [ECP5 and ECP5-5G sysI/O Usage Guide](#).

2.20.4. On-Chip Programmable Termination

The ECP5 Automotive devices support a variety of programmable on-chip terminations options including:

- Dynamically switchable Single-ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.

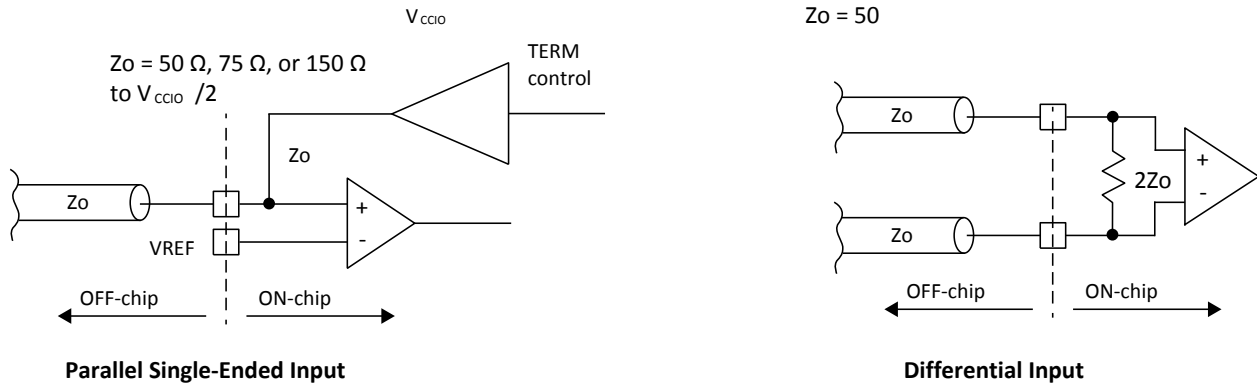


Figure 2.26. On-chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2^*$	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Note:**

TERMINATE to single-ended $V_{CCIO}/2$ and DIFFERENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFERENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance $\pm 20\%$.

Refer to TN1262, [ECP5 and ECP5-5G sysIO Usage Guide](#) for on-chip termination usage and value ranges.

2.20.5. Hot Socketing

ECP5 Automotive devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the [Hot Socketing Specifications](#) section on page 47.

2.21. SERDES and Physical Coding Sublayer

LAE5UM devices feature up to 4 channels of embedded SERDES/PCS arranged in dual-channel blocks at the bottom of the devices. Each channel supports up to 3.2 Gb/s data rate. Figure 2.27 shows the position of the dual blocks for the LAE5-45. Table 2.13 shows the location of available SERDES Duals for all devices. The LAE5UM SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express Gen1 and Gen2 (2.5 Gb/s) on ECP5UM; Gen 1, Gen2 (2.5 Gb/s)
- Ethernet (XAUI, GbE – 1000 Base CS/SX/LX and SGMII)
- SMPTE SDI (3G-SDI, HD-SDI, SD-SDI)
- CPRI (E.6.LV: 614.4 Mb/s, E.12.LV: 1228.8 Mb/s, E.24.LV: 2457.6 Mb/s, E.30.LV: 3072 Mb/s)
- JESD204A/B – ADC and DAC converter interface: 312.5 Mb/s to 3.125 Gb/s (ECP5)

Each dual contains two dedicated SERDES for high speed, full duplex serial data transfer. Each dual also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8b/10b interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in duals, multiple baud rates can be supported within a dual with the use of dedicated, per channel /1, /2 and /11 rate dividers. Additionally, two duals can be arranged together to form x4 channel link.

When a SERDES Dual in a 2-Dual device is not used, the power V_{CCA} power supply for that Dual should be connected. It is advised to connect the V_{CCA} of unused channel to core if the user knows he will not use the Dual at all. Or, it should be connected to a different regulated supply, if that Dual may be used in the future.

For an unused channel in a Dual, it is advised to connect the V_{CCHTX} to V_{CCA} . User can leave V_{CCHRX} unconnected.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well as on how to combine multiple protocols and baud rates within a device, refer to TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#).

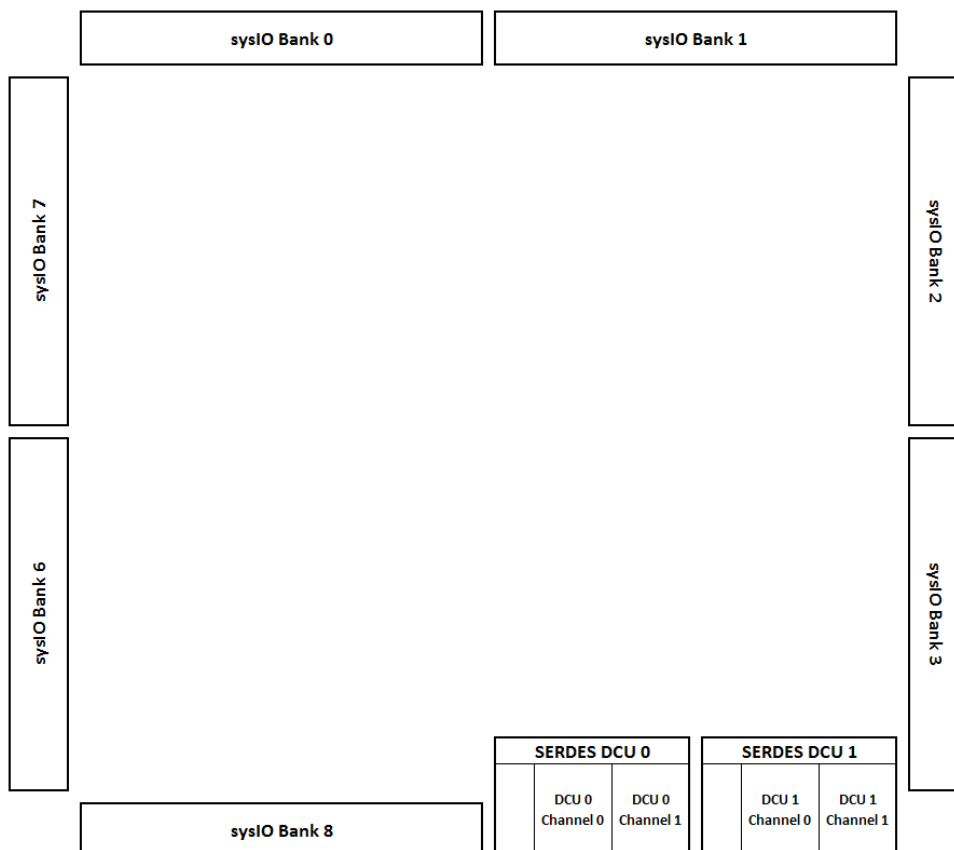


Figure 2.27. SERDES/PCS Duals (LAE5UM-45)

Table 2.13. LAE5UM SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4	614.4 1228.8 2457.6 3072.0	x1	8b10b
SD-SDI (259M, 344M)*	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
JESD204A/B	3125	x1	8b/10b

***Note:**

For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.

Table 2.14. Available SERDES Duals per LAE5UM Device

Package	LAE5UM -25	LAE5UM -45
381 caBGA	1	2

2.21.1. SERDES Block

A SERDES receiver channel may receive serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR), and de-serialize the data stream before passing the 8b/10b data to the PCS logic. The SERDES transmitter channel may receive the parallel 8b/10b data, serialize the data, and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply V_{CCA} . The output and input buffers of each channel have their own independent power supplies, V_{CCHTX} and V_{CCHRX} .

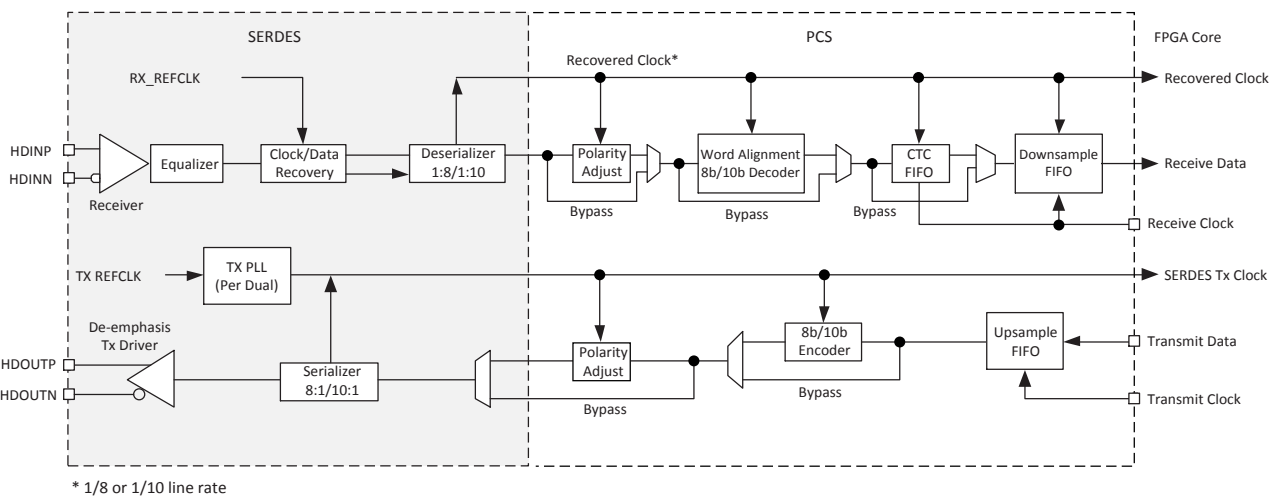


Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.21.2. PCS

As shown in [Figure 2.28](#), the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes 8b/10b, provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8b/10b data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8b/10b interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LAE5UM SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced TX de-emphasis: Programmable pre- and post-cursors improves TX output signaling.
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function.

Refer to TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#) for more information.

2.21.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration through this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express, and 4x Serial RapidIO can be implemented using IP that is available through Lattice Semiconductor), with two duals which is four SERDES channels with PCS and some additional logic from the core.

The LAE5UM devices support a wide range of protocols. Within the same dual, the LAE5UM devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. [Table 2.15](#) lists the allowable combination of primary and secondary protocol combinations.

2.22. Flexible Dual SERDES Architecture

The LAE5UM SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual, consisting of two SERDES channels, is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LAE5UM dual-channel architecture provides flexibility. More than one standard can be supported within the same dual.

[Table 2.15](#) lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LAE5UM Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LAE5UM architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#).

2.23. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5 Automotive devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses V_{CCIO8} for power supply.

For more information, refer to TN1260, [ECP5 and ECP5-5G sysCONFIG Usage Guide](#).

2.24. Device Configuration

All ECP5 Automotive devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port, support dual-byte, byte, and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are dedicated pins for TAP and sysConfig support, which are TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN, and CCLK. The remaining sysCONFIG pins are used as dual function pins. Refer to TN1260, [ECP5 and ECP5-5G sysCONFIG Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5 Automotive device:

- JTAG
- Standard Serial Peripheral Interface (SPI) to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port in Slave Parallel Configuration Mode (SPCM) mode.
- System microprocessor to drive a serial slave SPI port (SSPI mode).
- Slave Serial Configuration Mode (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5 Automotive devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.24.1. Enhanced Configuration Options

ECP5 Automotive devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O, and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice Semiconductor technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update, the ECP5 Automotive devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5 Automotive device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to TN1260, [ECP5 and ECP5-5G sysCONFIG Usage Guide](#).

2.24.2. Single Event Upset (SEU) Support

ECP5 Automotive devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5 Automotive devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5 Automotive device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode, normal operation, the device can be programmed to generate an error signal.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to TN1184, [LatticeECP3, ECP5 and ECP5-5G Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide](#).

2.24.3. On-Chip Oscillator

Every ECP5 Automotive device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. [Table 2.16](#) lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to TN1260, [ECP5 and ECP5-5G sysCONFIG Usage Guide](#).

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

2.25. Density Shifting

The ECP5 Automotive family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same package. Refer to the ECP5 Automotive Pin Migration Tables. Go to Lattice Semiconductor website. Enter ECP5 in the search field. In the Document Type navigation pane, click Pin & Package. You will get the information about the Pin Migration.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	-0.5	1.21	V
V _{CCA}	Supply Voltage	-0.5	1.32	V
V _{CCAUX} , V _{CCAUXA}	Supply Voltage	-0.5	2.75	V
V _{CCIO}	Supply Voltage	-0.5	3.63	V
—	Input or I/O Transient Voltage Applied	-0.5	3.63	V
V _{CCHR_X} , V _{CCHTX}	SERDES RX/TX Buffer Supply Voltages	-0.5	1.32	V
—	Voltage Applied on SERDES Pins	-0.5	1.80	V
T _A	Storage Temperature (Ambient)	-65	150	°C
T _J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the [Absolute Maximum Ratings](#) may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Semiconductor [Thermal Management](#) document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter	Device	Min	Max	Unit
V _{CC} ²	Core Supply Voltage	All	1.045	1.155	V
V _{CCAUX} ^{2,4}	Auxiliary Supply Voltage	All	2.375	2.625	V
V _{CCIO} ^{2,3}	I/O Driver Supply Voltage	All	1.14	3.465	V
V _{REF} ¹	Input Reference Voltage	All	0.5	1.0	V
t _{JAUTO}	Junction Temperature, Industrial Operation	All	-40	125	°C
SERDES External Power Supply⁵					
V _{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
V _{CCAUXA}	SERDES Auxiliary Supply Voltage	All	2.374	2.625	V
V _{CCHR_X} ⁶	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
V _{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in [Table 3.4](#).
4. V_{CCAUX} ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
5. Refer to TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#) for information on board considerations for SERDES power supplies.
6. V_{CCHR_X} is used for Rx termination. It can be biased to V_{cm} if external AC coupling is used. This voltage needs to meet all the HDIn input voltage level requirements specified in the [SERDES Power Supply Requirements](#) section of this Data Sheet.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies	0.01	—	10	V/ms

Note: Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On-Reset Voltage Levels

Symbol	Parameter		Min	Typ	Max	Unit	
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring V_{CC} , V_{CCAUX} , and V_{CCIO8})	V_{CC}	0.90	—	1.00	V
			V_{CCAUX}	2.00	—	2.20	V
			V_{CCIO8}	0.95	—	1.06	V
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring V_{CC} , and V_{CCAUX})	V_{CC}	0.77	—	0.87	V
			V_{CCAUX}	1.80	—	2.00	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- Only V_{CCIO8} has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
- V_{CCIO8} does not have a Power-On-Reset ramp down detection. V_{CCIO8} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Power up Sequence

Power-On-Reset (POR) puts the ECP5 Automotive device in a reset state. POR is released when V_{CC} , V_{CCAUX} , and V_{CCIO8} are ramped above the V_{PORUP} voltage, as specified above.

V_{CCIO8} controls the voltage on the configuration I/O pins. If the ECP5 Automotive device is using Master SPI mode to download configuration data from external SPI Flash, it is required to ramp V_{CCIO8} above V_{IH} of the external SPI Flash, before at least one of the other two supplies, V_{CC} and/or V_{CCAUX} , is ramped to V_{PORUP} voltage level. If the system cannot meet this power up sequence requirement, and requires the V_{CCIO8} to be ramped last, the system must keep either PROGRAMN or INITN pin LOW during power up until V_{CCIO8} reaches V_{IH} of the external SPI Flash. This ensures the signals driven out on the configuration pins to the external SPI Flash meeting the V_{IH} voltage requirement of the SPI Flash.

For LAE5UM devices, it is required to power up V_{CCA} before V_{CCAUXA} is powered up.

3.6. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDK_HS	Input or I/O Leakage Current for Top and Bottom Banks Only	$0 \leq V_{IN} \leq V_{IH} (\text{Max})$	—	—	± 1	mA
IDK	Input or I/O Leakage Current for Left and Right Banks Only	$0 \leq V_{IN} < V_{CCIO}$	—	—	± 1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5 \text{ V}$	—	18	—	mA

Notes:

1. V_{CC} , V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. I_{DK} is additive to I_{PU} , I_{PW} , or I_{BH} .
3. LVCMOS and LVTTTL only.
4. Hot socket specification defines when the hot socketed device's junction temperature is at 85 °C or below. When the hot socketed device's junction temperature is above 85 °C, the IDK current can exceed ± 1 mA.

3.7. Hot Socketing Requirements

Table 3.6. Hot Socketing Requirements

Description	Min	Typ	Max	Unit
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA
Input current per HDIN pin when device power supply is off, inputs driven ^{1, 2}	—	—	15	mA
Current per HDIN pin when device power ramps up, input driven ³	—	—	50	mA
Current per HDOUT pin when device power supply is off, outputs pulled up ⁴	—	—	30	mA

Notes:

1. Device is powered down with all supplies grounded, both HDINP and HDINN inputs driven by a CML driver with maximum allowed output V_{CCHTX} , 8b/10b data, no external AC coupling.
2. Each P and N input must have less than the specified maximum input current during hot plug. For a device with 2 DCU, the total input current would be 15 mA * 4 channels * 2 input pins per channel = 120 mA.
3. Device power supplies are ramping up to V_{CCA} and V_{CCAUX} . Both HDINP and HDINN inputs are driven by a CML driver with maximum allowed output V_{CCHTX} , 8b/10b data, internal AC coupling.
4. Device is powered down with all supplies grounded. Both HDOUTP and HDOUN outputs are pulled up to V_{CCHTX} by the far end receiver termination of 50 Ω single ended.

3.8. ESD Performance

Refer to the [ECP5 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

3.9. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{IL}, I_{IH}^{1, 4}$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	10	μA
$I_{IH}^{1, 3}$	Input or I/O High Leakage	$V_{CCIO} < V_{IN} \leq V_{IH(MAX)}$	—	—	100	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL(MAX)} \leq V_{IN} \leq V_{CCIO}$	30	—	150	μA
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V,$ $V_{CC} = 1.2 V, V_{IO} = 0 \text{ to } V_{IH(MAX)}$	—	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V,$ $V_{CC} = 1.2 V, V_{IO} = 0 \text{ to } V_{IH(MAX)}$	—	5	7	pf
V_{HYST}	Hysteresis for Single-Ended Inputs	$V_{CCIO} = 3.3 V$	—	300	—	mV
		$V_{CCIO} = 2.5 V$	—	250	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Applicable to general purpose I/Os in top and bottom banks.
4. When used as V_{REF} , maximum leakage= 25 μA .

3.10. Standby ECP5 Automotive Supply Current

Over recommended operating conditions.

Table 3.8. Standby ECP5 Automotive Supply Current

Symbol	Parameter	Device	Typical	Unit
I _{CC}	Core Power Supply Current	LAE5U-12FLAE5UM-25F	77	mA
		LAE5UM-45F	116	mA
I _{CCAUX}	Auxiliary Power Supply Current	LAE5U-12F/ LAE5UM-25F	16	mA
		LAE5UM-45F	17	mA
I _{CCIO}	Bank Power Supply Current (Per Bank)	LAE5U-12F/ LAE5UM-25F	0.5	mA
		LAE5UM-45F	0.5	mA
I _{CCA}	SERDES Power Supply Current (Per Dual)	LAE5UM-25F	11	mA
		LAE5UM-45F	9.5	mA

Notes:

- For further information on supply current, see the list of technical documentation in the [Supplemental Information](#) section on page 96.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 Hz.
- Pattern represents a “blank” configuration data file.
- T_j = 85 °C, power supplies at nominal voltage.
- To determine the ECP5 Automotive peak start-up current, use the Power Calculator tool in the Lattice Semiconductor Diamond Design Software.

3.11. SERDES Power Supply Requirements

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I _{CCA-SB}	V _{CCA} , Power Supply Current per Channel	4	—	mA
I _{CCHRX-SB} ¹	V _{CCHRX} , Input Buffer Current per Channel	—	—	mA
I _{CCHTX-SB}	V _{CCHTX} , Output Buffer Current per Channel	—	—	mA
Operating (Data Rate = 3.125 Gb/s)				
I _{CCA-OP}	V _{CCA} , Power Supply Current per Channel	43	—	mA
I _{CCHRX-OP} ²	V _{CCHRX} , Input Buffer Current per Channel	0.4	—	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current per Channel	10	—	mA
Operating (Data Rate = 2.5 Gb/s)				
I _{CCA-OP}	V _{CCA} , Power Supply Current per Channel	40	—	mA
I _{CCHRX-OP} ²	V _{CCHRX} , Input Buffer Current per Channel	0.4	—	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current per Channel	10	—	mA
Operating (Data Rate = 1.25 Gb/s)				
I _{CCA-OP}	V _{CCA} , Power Supply Current per Channel	34	—	mA
I _{CCHRX-OP} ²	V _{CCHRX} , Input Buffer Current per Channel	0.4	—	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current per Channel	10	—	mA
Operating (Data Rate = 270 Mb/s)				
I _{CCA-OP}	V _{CCA} , Power Supply Current per Channel	28	—	mA
I _{CCHRX-OP} ²	V _{CCHRX} , Input Buffer Current per Channel	0.4	—	mA
I _{CCHTX-OP}	V _{CCHTX} , Output Buffer Current per Channel	8	—	mA

Notes:

1. V_{CCAUX} ramp rate must not exceed 30 mV/μs during power-up when transitioning between 0 V and 3 V.
2. Refer to TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#) for information on board considerations for SERDES power supplies.

3.12. sysI/O Recommended Operating Conditions

Table 3.10. sysI/O Recommended Operating Conditions

Standard	V _{CCIO} (V)			V _{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVC MOS33 ¹	3.135	3.3	3.465	—	—	—
LVC MOS33D ³ Output	3.135	3.3	3.465	—	—	—
LVC MOS25 ¹	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 ¹	1.14	1.2	1.26	—	—	—
LVTTL33 ¹	3.135	3.3	3.465	—	—	—
SSTL15_I, _II ²	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II ²	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12 ²	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input ³	1.425	1.5	1.575	—	—	—
LVDS25 ^{1,3} Output	2.375	2.5	2.625	—	—	—
subLVDS ³ (Input only)	—	—	—	—	—	—
SLVS ³ (Input only)	—	—	—	—	—	—
LVDS25E ³ Output	2.375	2.5	2.625	—	—	—
MLVDS ³ Output	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1,3} Output	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1,3} Output	2.375	2.5	2.625	—	—	—
HSULD12D ^{2,3}	1.14	1.2	1.26	—	—	—
SSTL135D_I, II ^{2,3}	1.28	1.35	1.42	—	—	—
SSTL15D_I, II ^{2,3}	1.43	1.5	1.57	—	—	—
SSTL18D_I ^{1,2,3} , II ^{1,2,3}	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to TN1262, [ECP5 and ECP5-5G sysIO Usage Guide](#).
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power.
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to TN1262, [ECP5 and ECP5-5G sysIO Usage Guide](#) for details.

3.13. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max (V)	V _{OH} Min (V)	I _{OL} ¹ (mA)	I _{OH} ¹ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVC MOS33	-0.3	0.8	2.0	3.465	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
LVC MOS25	-0.3	0.7	1.7	3.465	0.4	V _{CCIO} - 0.4	12, 8, 4	-12, -8, -4
LVC MOS18	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} - 0.4	12, 8, 4	-12, -8, -4
LVC MOS15	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} - 0.4	8, 4	-8, -4
LVC MOS12	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.465	0.4	V _{CCIO} - 0.4	8, 4	-8, -4
LVTTL33	-0.3	0.8	2.0	3.465	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
SSTL18_I (DDR2 Memory)	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	3.465	0.4	V _{CCIO} - 0.4	6.7	-6.7
SSTL18_II	-0.3	V _{REF} -	V _{REF} + 0.125	3.465	0.28	V _{CCIO} - 0.28	13.4	-13.4
SSTL15_I (DDR3 Memory)	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} - 0.31	7.5	-7.5
SSTL15_II (DDR3 Memory)	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.465	0.31	V _{CCIO} - 0.31	8.8	-8.8
SSTL135_I (DDR3L Memory)	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} - 0.27	7	-7
SSTL135_II (DDR3L Memory)	-0.3	V _{REF} - 0.09	V _{REF} + 0.09	3.465	0.27	V _{CCIO} - 0.27	8	-8
MIPI D-PHY (LP)	-0.3	0.55	0.88	3.465	—	—	—	—
HSUL12 (LPDDR2/3 Memory)	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.465	0.3	V _{CCIO} - 0.3	4	-4

Notes:

- For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O. All I/Os are used in the same V_{CCIO}.
- Not all IO types are supported in all banks. Refer to TN1262, [ECP5 and ECP5-5G sysIO Usage Guide](#) for details.

3.14. sysI/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.11. LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two	± 100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	± 10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100 \Omega$	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100 \Omega$	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM}), R_T = 100 \Omega$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2, R_T = 100 \Omega$	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0 V$ Driver outputs shorted to each other	—	—	12	mA

Note: On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5 V$ or $3.3 V$.

3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes, class I and class II, are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with $3.3 V V_{CCIO}$. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

3.14.4. LVDS25E

The top and bottom sides of ECP5 Automotive devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3.1 is one possible solution for point-to-point signals.

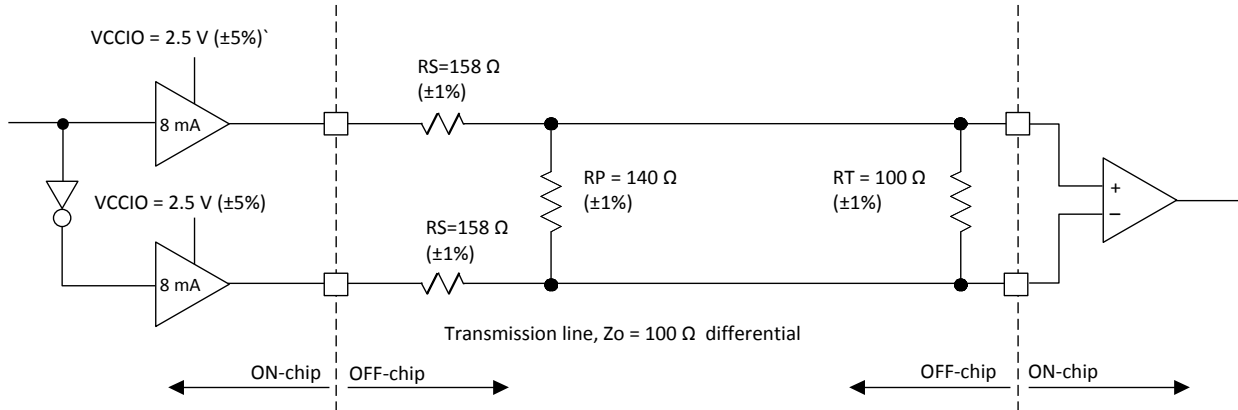


Figure 3.1. LVDS25E Output Termination Example

Table 3.12. LVDS25E DC Conditions

Parameter	Description	Typical	Unit
V _{CCIO}	Output Driver Supply (±5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (±1%)	158	Ω
R _P	Driver Parallel Resistor (±1%)	140	Ω
R _T	Receiver Termination (±1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

3.14.5. BLVDS25

The ECP5 Automotive devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

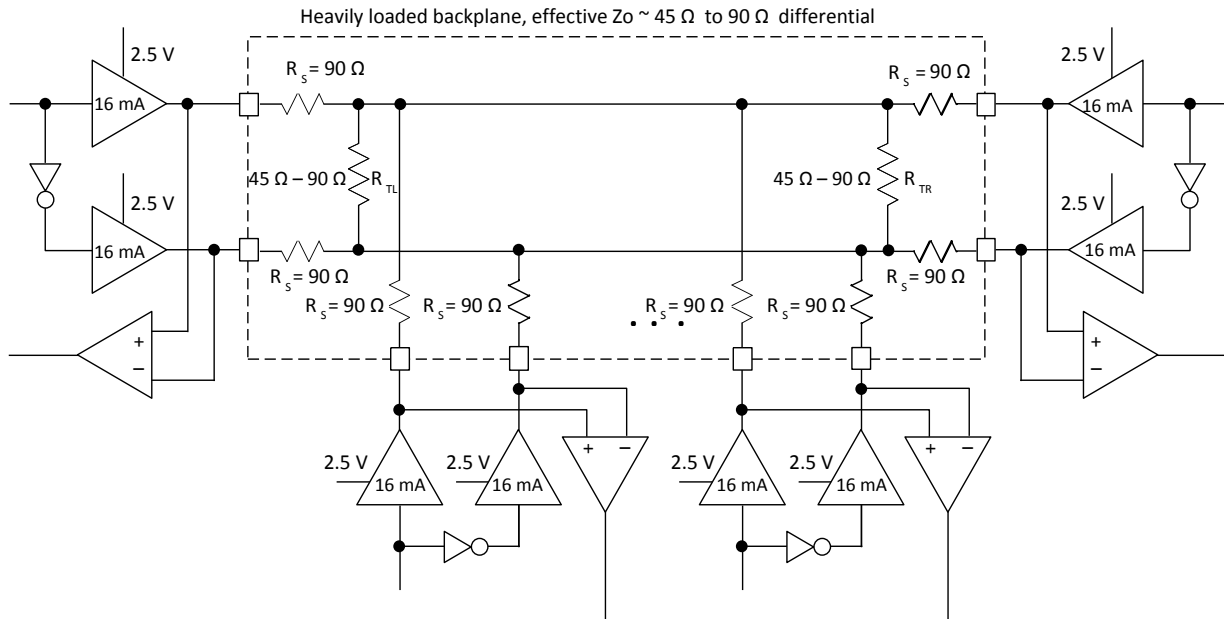


Figure 3.2. BLVDS25 Multi-point Output Example

Over recommended operating conditions.

Table 3.13. BLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo = 45 Ω	Zo = 90 Ω	
V _{CCIO}	Output Driver Supply (±5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (±1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (±1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (±1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage	1.38	1.48	V
V _{OL}	Output Low Voltage	1.12	1.02	V
V _{OD}	Output Differential Voltage	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

Note: For input buffer, see LVDS Table 3.11 on page 53.

3.14.6. LVPECL33

The ECP5 Automotive devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.3 is one possible solution for point-to-point signals.

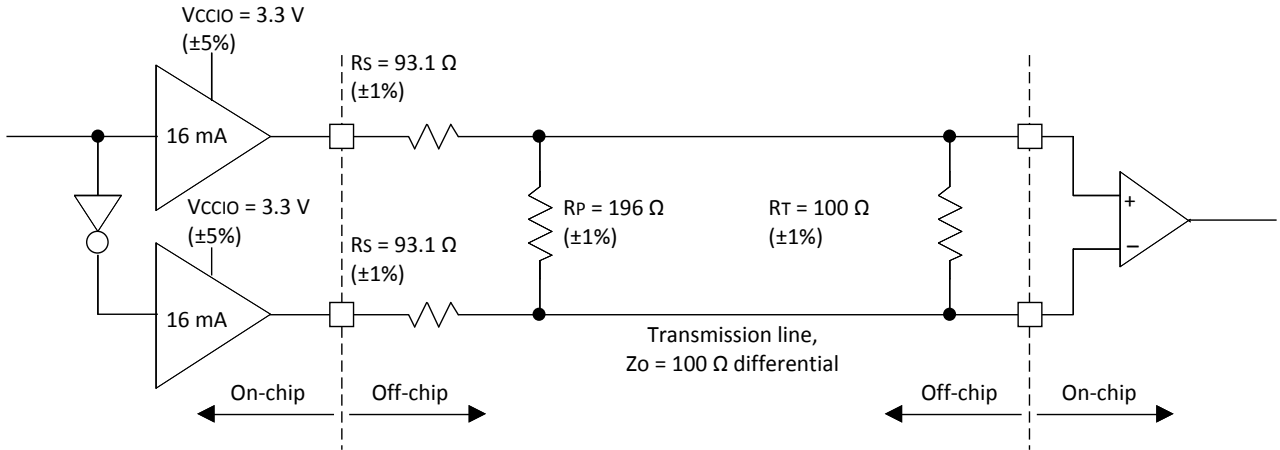


Figure 3.3. Differential LVPECL33

Over recommended operating conditions.

Table 3.14. LVPECL33 DC Conditions

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (±1%)	93	Ω
R_P	Driver Parallel Resistor (±1%)	196	Ω
R_T	Receiver Termination (±1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

Note: For input buffer, see LVDS Table 3.11 on page 53.

3.14.7. MLVDS25

The ECP5 Automotive devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.4 is one possible solution for MLVDS standard implementation. Resistor values in the figure are industry standard values for 1% resistors.

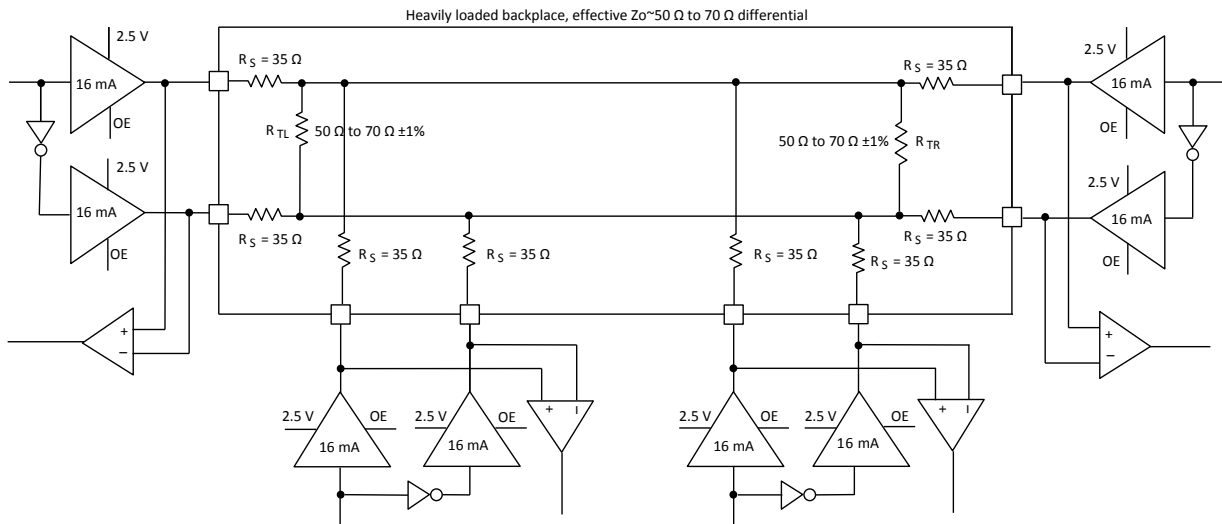


Figure 3.4. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Table 3.15. MLVDS25 DC Conditions

Parameter	Description	Typical		Unit
		Zo=50 Ω	Zo=70 Ω	
VCCIO	Output Driver Supply (±5%)	2.50	2.50	V
ZOUT	Driver Impedance	10.00	10.00	Ω
RS	Driver Series Resistor (±1%)	35.00	35.00	Ω
RTL	Driver Parallel Resistor (±1%)	50.00	70.00	Ω
RTR	Receiver Termination (±1%)	50.00	70.00	Ω
VOH	Output High Voltage	1.52	1.60	V
VOL	Output Low Voltage	0.98	0.90	V
VOD	Output Differential Voltage	0.54	0.70	V
VCM	Output Common Mode Voltage	1.25	1.25	V
IDC	DC Output Current	21.74	20.00	mA

Note: For input buffer, see LVDS Table 3.11 on page 53.

3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 for SLVS-400 standard. This standard evolved from the traditional LVDS standard relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV, or 400 mV p-p, SLVS swing contributes to a reduction in power.

The ECP5 Automotive devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5 Automotive LVDS input parameters, as listed in [Table 3.16](#).

Table 3.16. Input to SLVS

Parameter	ECP5 Automotive LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5 Automotive does not support SLVS output. However, SLVS output can be created using ECP5 Automotive LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. [Figure 3.5](#) shows how the LVDS output can be shifted externally to meet SLVS levels.

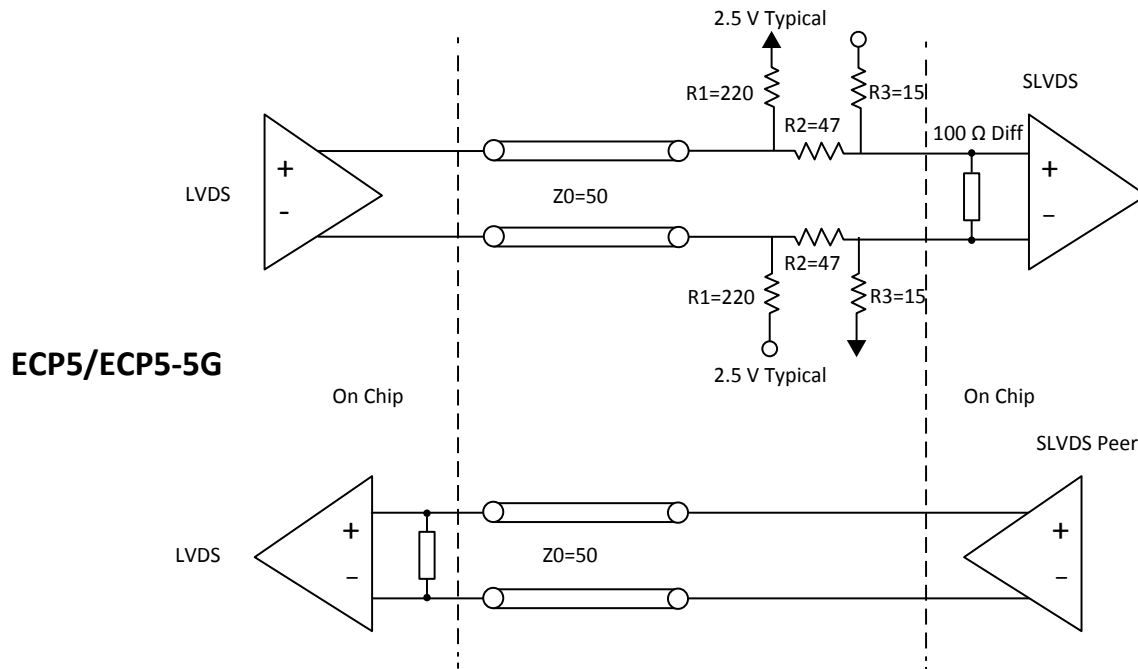


Figure 3.5. SLVS Interface

3.15. Typical Building Block Function Performance

Table 3.17. Pin-to-Pin Performance

Function	-6 Timing	Unit
Basic Functions		
16-Bit Decoder	—	ns
32-Bit Decoder	—	ns
64-Bit Decoder	—	ns
4:1 Mux	—	ns
8:1 Mux	—	ns
16:1 Mux	—	ns
32:1 Mux	—	ns

Notes:

1. I/Os are configured with LVCMOS25 with $V_{CCIO}=2.5$, 12 mA drive.
2. These functions were generated using Lattice Semiconductor Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
3. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Semiconductor Diamond design software tool.

Table 3.18. Register-to-Register Performance

Function	-6 Timing	Unit
Basic Functions		
16-Bit Decoder	—	MHz
32-Bit Decoder	—	MHz
64-Bit Decoder	—	MHz
4:1 Mux	—	MHz
8:1 Mux	—	MHz
16:1 Mux	—	MHz
32:1 Mux	—	MHz
8-Bit Adder	—	MHz
16-Bit Adder	—	MHz
64-Bit Adder	—	MHz
16-Bit Counter	—	MHz
32-Bit Counter	—	MHz
64-Bit Counter	—	MHz
64-Bit Accumulator	—	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	—	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	—	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	—	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	—	MHz
DSP Functions (DDR/SDR)		
9 x 9 Multiplier (All Registers)	—	MHz
18 x 18 Multiplier (All Registers)	—	MHz
36 x 36 Multiplier (All Registers)	—	MHz
18 x 18 Multiply-Add/Sub (All Registers)	—	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	—	MHz

Notes:

1. These functions were generated using Lattice Semiconductor Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Semiconductor Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

3.17. ECP5 Automotive Maximum I/O Buffer Speed

Over recommended operating conditions.

Table 3.19. ECP5 Automotive Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MIPI D-PHY (HS Mode)	MIPI Video	400	MHz
SLVS	SLVS similar to MIPI	400	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, $V_{CCIO} = 1.5\text{ V}$	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, $V_{CCIO} = 1.35\text{ V}$	400	MHz
HSUL12 (all supported classes)	HSUL_12 class I, II, $V_{CCIO} = 1.2\text{ V}$	400	MHz
LVTTTL33	LVTTTL, $V_{CCIO} = 3.3\text{ V}$	200	MHz
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	200	MHz
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	200	MHz
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	200	MHz
LVC MOS15	LVC MOS 1.5, $V_{CCIO} = 1.5\text{ V}$	200	MHz
LVC MOS12	LVC MOS 1.2, $V_{CCIO} = 1.2\text{ V}$	200	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	400	MHz
MLVDS25	MLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
BLVDS25	BLVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	300	MHz
LVPECL33	LVPECL, Emulated, $V_{CCIO} = 3.3\text{ V}$	300	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, $V_{CCIO} = 1.8\text{ V}$	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, $V_{CCIO} = 1.5\text{ V}$	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, $V_{CCIO} = 1.35\text{ V}$	400	MHz
HSUL12 (all supported classes)	HSUL12 class I, II, $V_{CCIO} = 1.2\text{ V}$	400	MHz
LVTTTL33	LVTTTL, $V_{CCIO} = 3.3\text{ V}$	150	MHz
LVC MOS33 (For all drives)	LVC MOS, 3.3 V	150	MHz
LVC MOS25 (For all drives)	LVC MOS, 2.5 V	150	MHz
LVC MOS18 (For all drives)	LVC MOS, 1.8 V	150	MHz
LVC MOS15 (For all drives)	LVC MOS, 1.5 V	150	MHz
LVC MOS12 (For all drives)	LVC MOS, 1.2 V	150	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVC MOS timing is measured with the load specified in Switching Test Conditions, [Table 3.41](#) on page 87.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

3.18. ECP5 Automotive External Switching Characteristics

Over recommended commercial operating conditions.

Table 3.20. ECP5 Automotive External Switching Characteristics

Parameter	Description	Device	-6		Unit
			Min	Max	
Clocks					
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	257	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	1.0	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	—	—	505	ps
Edge Clock					
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	312	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	1.50	—	ns
t_{SKEW_EDGE}	Edge Clock Skew Within a Bank	—	—	200	ps
Generic SDR Input					
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL					
t_{CO}	Clock to Output - PIO Output Register	All Devices	—	6.8	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All Devices	0	—	ns
t_H	Clock to Data Hold - PIO Input Register	All Devices	3.3	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.46	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All Devices	—	312	MHz
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL					
t_{COPLL}	Clock to Output - PIO Output Register	All Devices	—	4.1	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	0.85	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	0.98	—	ns
t_{SU_DELP}	Clock to Data Setup - PIO Input Register with Data Input Delay	All Devices	1.95	—	ns
t_{H_DELP}	Clock to Data Hold - PIO Input Register with Data Input Delay	All Devices	0	—	Ns

Table 3.20. ECP5 Automotive External Switching Characteristics (Continued)

Parameter	Description	Device	-6		Unit
			Min	Max	
Generic DDR Input					
Generic DDRX1 Inputs with Clock and Data Centered at Pin (GDDR1_RX.SCLK.Centered) Using PCLK Clock Input - Figure 3.6					
$t_{SU_GDDR1_centered}$	Data Setup Before CLK Input	All Devices	0.52	—	ns
$t_{HD_GDDR1_centered}$	Data Hold After CLK Input	All Devices	0.52	—	ns
$f_{DATA_GDDR1_centered}$	GDDR1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX_GDDR1_centered}$	GDDR1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX1 Inputs with Clock and Data Aligned at Pin (GDDR1_RX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.7					
$t_{SU_GDDR1_aligned}$	Data Setup from CLK Input	All Devices	—	-0.55	ns + 1/2 UI
$t_{HD_GDDR1_aligned}$	Data Hold from CLK Input	All Devices	0.55	—	ns + 1/2 UI
$f_{DATA_GDDR1_aligned}$	GDDR1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX_GDDR1_aligned}$	GDDR1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin (GDDR2_RX.ECLK.Centered) Using PCLK Clock Input, Left and Right Sides Only - Figure 3.6					
$t_{SU_GDDR2_centered}$	Data Setup before CLK Input	All Devices	0.471	—	ns
$t_{HD_GDDR2_centered}$	Data Hold after CLK Input	All Devices	0.471	—	ns
$f_{DATA_GDDR2_centered}$	GDDR2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX_GDDR2_centered}$	GDDR2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin (GDDR2_RX.ECLK.Aligned) Using PCLK Clock Input, Left and Right Sides Only - Figure 3.7					
$t_{SU_GDDR2_aligned}$	Data Setup from CLK Input	All Devices	—	-0.495	ns + 1/2 UI
$t_{HD_GDDR2_aligned}$	Data Hold from CLK Input	All Devices	0.495	—	ns + 1/2 UI
$f_{DATA_GDDR2_aligned}$	GDDR2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX_GDDR2_aligned}$	GDDR2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Video DDRX1 Inputs With Clock and Data Aligned at Pin (GDDR71_RX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.11					
$t_{SU_LVDS71_i}$	Data Setup from CLK Input (bit i)	All Devices	—	-0.41	ns+(1/2+i) UI
$t_{HD_LVDS71_i}$	Data Hold from CLK Input (bit i)	All Devices	0.41	—	ns+(1/2+i) UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	262.5	MHz

Table 3.20. ECP5 Automotive External Switching Characteristics (Continued)

Parameter	Description	Device	-6		Unit
			Min	Max	
Generic DDR Output					
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDR1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.8					
t _{DVB_GDDR1_centered}	Data Output Valid before CLK Output	All Devices	-0.67	—	ns + 1/2 UI
t _{DVA_GDDR1_centered}	Data Output Valid after CLK Output	All Devices	-0.67	—	ns + 1/2 UI
f _{DATA_GDDR1_centered}	GDDR1 Data Rate	All Devices	—	500	Mb/s
f _{MAX_GDDR1_centered}	GDDR1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDR1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9					
t _{DIB_GDDR1_aligned}	Data Output Invalid before CLK Output	All Devices	-0.3	—	ns
t _{DIA_GDDR1_aligned}	Data Output Invalid after CLK Output	All Devices	—	0.3	ns
f _{DATA_GDDR1_aligned}	GDDR1 Data Rate	All Devices	—	500	Mb/s
f _{MAX_GDDR1_aligned}	GDDR1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDR2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8					
t _{DVB_GDDR2_centered}	Data Output Valid Before CLK Output	All Devices	-0.676	—	ns + 1/2 UI
t _{DVA_GDDR2_centered}	Data Output Valid After CLK Output	All Devices	—	0.676	ns + 1/2 UI
f _{DATA_GDDR2_centered}	GDDR2 Data Rate	All Devices	—	624	Mb/s
f _{MAX_GDDR2_centered}	GDDR2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDR2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9					
t _{DIB_GDDR2_aligned}	Data Output Invalid before CLK Output	All Devices	-0.2	—	ns
t _{DIA_GDDR2_aligned}	Data Output Invalid after CLK Output	All Devices	—	0.2	ns
f _{DATA_GDDR2_aligned}	GDDR2 Data Rate	All Devices	—	624	Mb/s
f _{MAX_GDDR2_aligned}	GDDR2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDR71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12					
t _{DIB_LVDS71_i}	Data Output Invalid before CLK Output	All Devices	-0.2	—	ns + (i) UI
t _{DIA_LVDS71_i}	Data Output Invalid after CLK Output	All Devices	—	0.2	ns + (i) UI
f _{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	525	Mb/s
f _{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	262.5	MHz
Memory Interface					
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)					
t _{DVBDQ_DDR2} t _{DVBDQ_DDR3} t _{DVBDQ_DDR3L} t _{DVBDQ_LPDDR2} t _{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	-0.374	ns + 1/2 UI
t _{DVADQ_DDR2} t _{DVADQ_DDR3} t _{DVADQ_DDR3L} t _{DVADQ_LPDDR2} t _{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.374	—	ns + 1/2 UI

Table 3.20. ECP5 Automotive External Switching Characteristics (Continued)

Parameter	Description	Device	-6		Unit
			Min	Max	
f_{DATA_DDR2} f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	624	Mb/s
f_{MAX_DDR2} f_{MAX_DDR3} f_{MAX_DDR3L} f_{MAX_LPDDR2} f_{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	312	MHz
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS)					
t_{DQVBS_DDR2} t_{DQVBS_DDR3} t_{DQVBS_DDR3L} t_{DQVBS_LPDDR2} t_{DQVBS_LPDDR3}	Data Output Valid before DQS Output	All Devices	—	-0.25	UI
t_{DQVAS_DDR2} t_{DQVAS_DDR3} t_{DQVAS_DDR3L} t_{DQVAS_LPDDR2} t_{DQVAS_LPDDR3}	Data Output Valid after DQS Output	All Devices	0.25	—	UI
f_{DATA_DDR2} f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	624	Mb/s
f_{MAX_DDR2} f_{MAX_DDR3} f_{MAX_DDR3L} f_{MAX_LPDDR2} f_{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	312	MHz

Notes:

- Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.
- General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load.
 Generic DDR timing are numbers based on LVDS I/O.
 DDR2 timing numbers are based on SSTL18.
 DDR3 timing numbers are based on SSTL15.
 LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
- Uses LVDS I/O standard for measurements.
- Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
- All numbers are generated with the Diamond software.

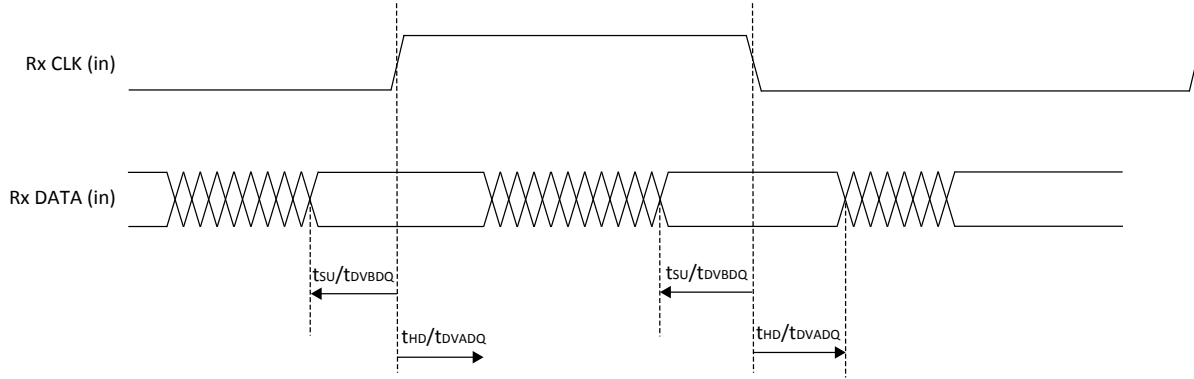


Figure 3.6. Receiver RX.CLK. Centered Waveforms

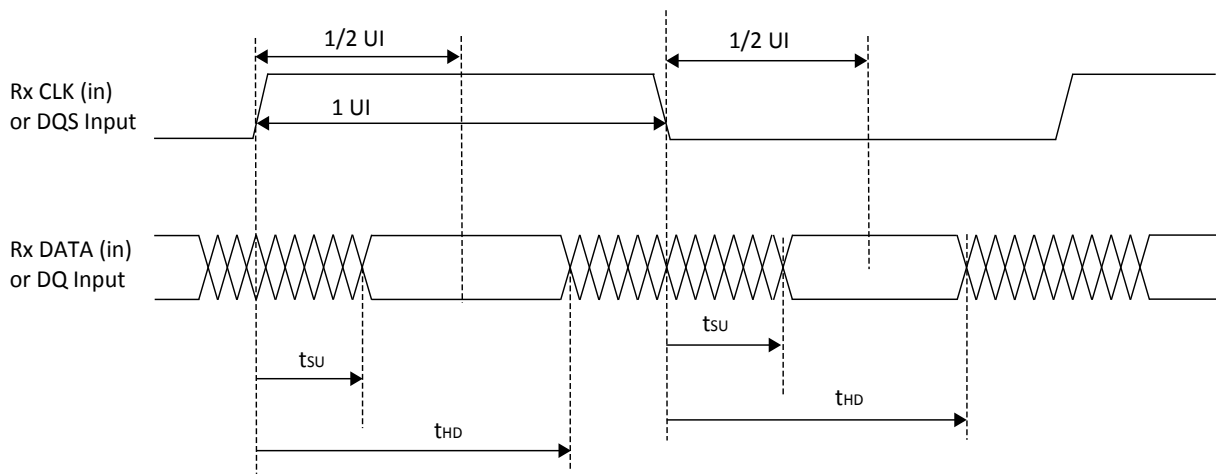


Figure 3.7. Receiver RX.CLK. Aligned and DDR Memory Input Waveforms

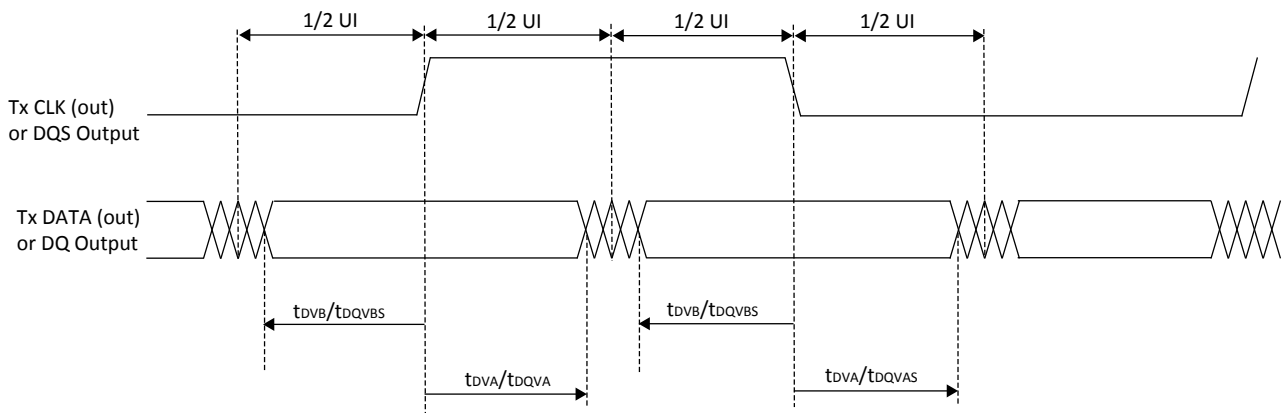


Figure 3.8. Transmit TX.CLK. Centered and DDR Memory Output Waveforms

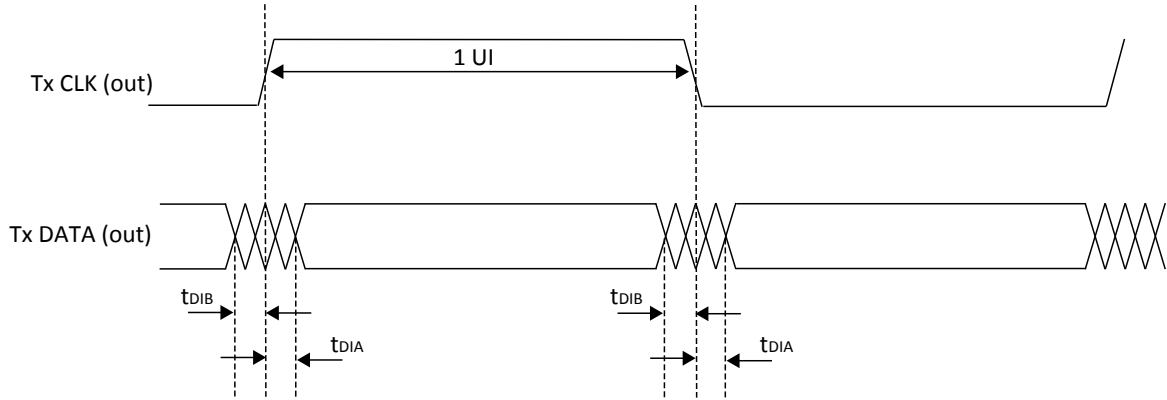
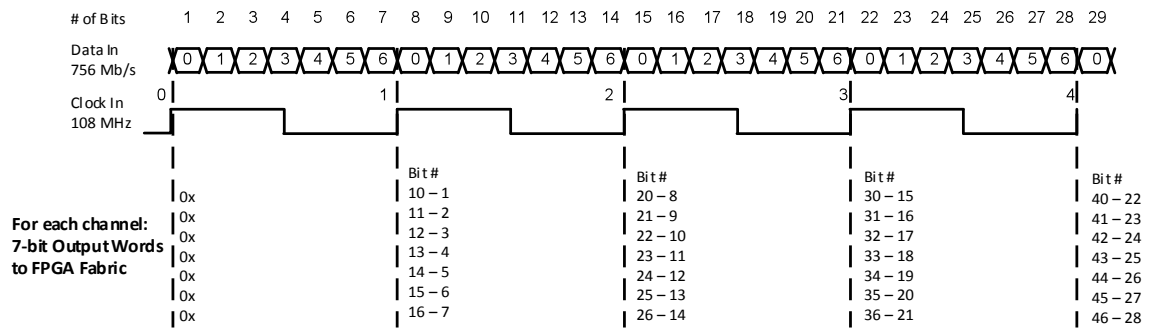


Figure 3.9. Transmit TX.CLK. Aligned Waveforms

Receiver – Shown for one LVDS channel



Transmitter – Shown for one LVDS channel

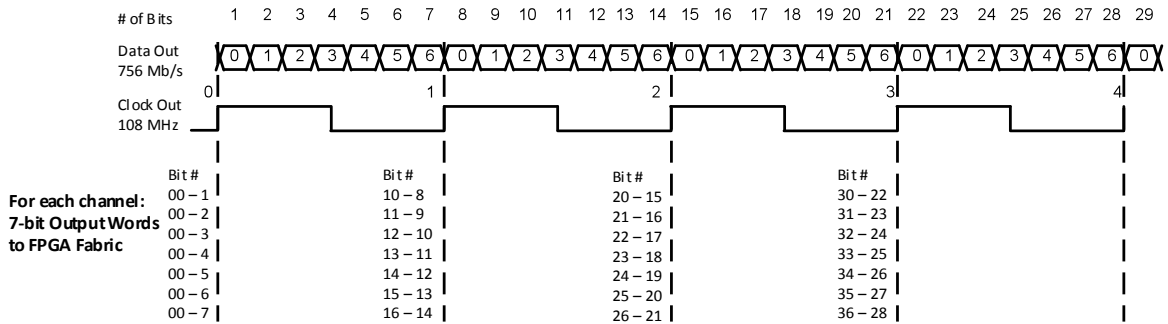


Figure 3.10. DDRX71 Video Timing Waveforms

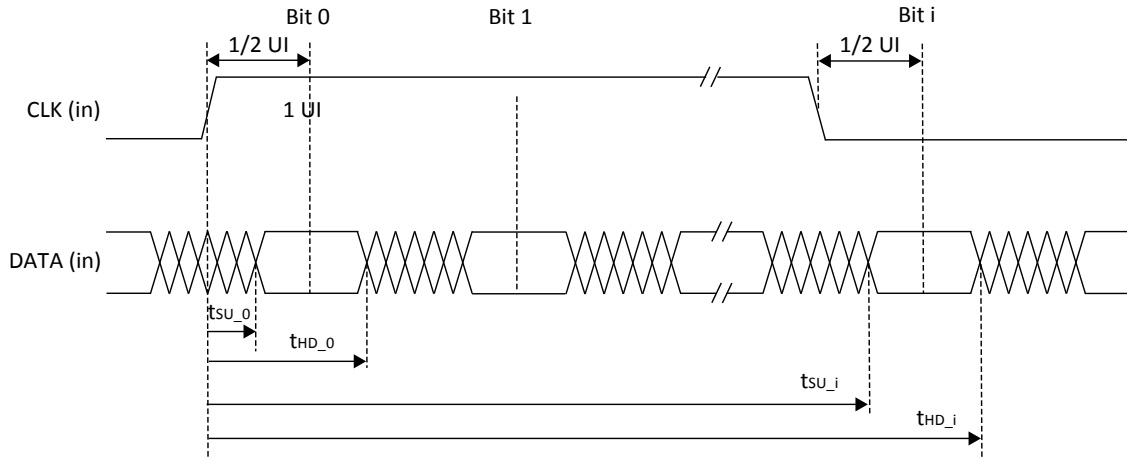


Figure 3.11. Receiver DDRX71_RX Waveforms

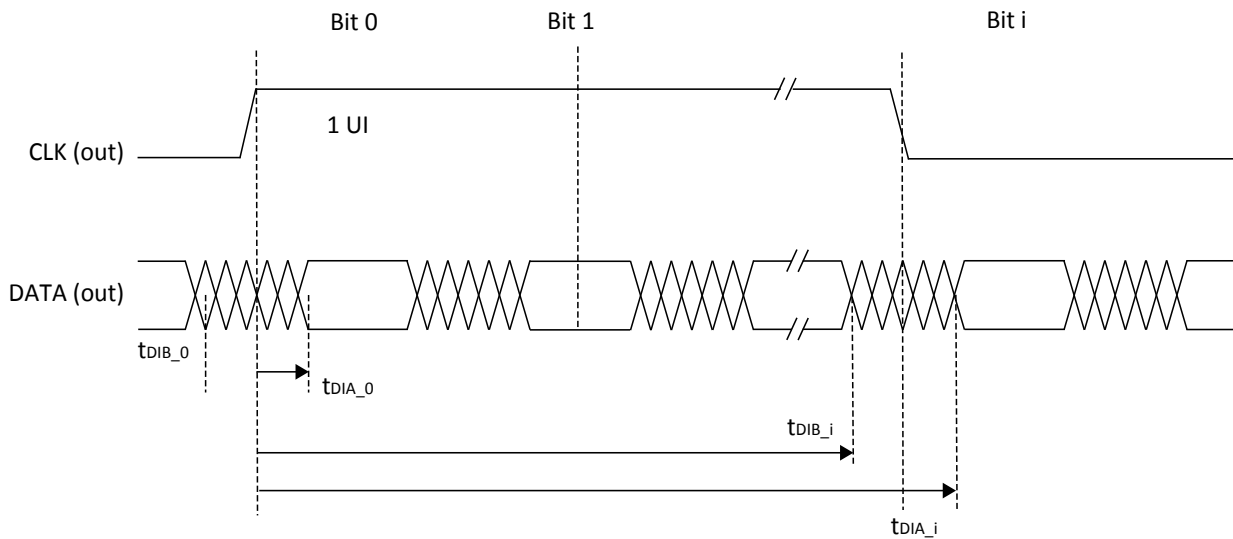


Figure 3.12. Transmitter DDRX71_TX Waveforms

3.19. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 3.21. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	8	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	3.125	400	MHz
f_{VCO}	PLL VCO Frequency	—	400	800	MHz
f_{PFD}^3	Phase Detector Input Frequency	—	10	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	-5	5	%
t_{OPJIT}^1	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.050	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	UIPP
t_{SPO}	Static Phase Offset	Divider ratio =	—	400	ps p-p
t_W	Output Clock Pulse Width	At 90% or 10%	0.9	—	ns
t_{LOCK}^2	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST/ Pulse Width	—	1	—	ms
t_{RSTREC}	RST Recovery Time	—	1	—	ns
t_{LOAD_REG}	Min Pulse for CIB_LOAD_REG	—	10	—	ns
$t_{ROTATE-SETUP}$	Min time for CIB dynamic phase controls to be stable fore CIB_ROTATE	—	5	—	ns
$t_{ROTATE-WD}$	Min pulse width for CIB_ROTATE to maintain "0" or	—	4	—	VCO cycles

Notes:

- Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
- Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
- Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

3.20. SERDES High-Speed Data Transmitter

Table 3.22. Serial Output Timing and Levels

Symbol	Description	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Peak-Peak Differential voltage on selected amplitude ^{1, 2}	-25%	—	25%	mV, p-p
$V_{TX-CM-DC}$	Output common mode voltage	—	$V_{CCHTX} / 2$	—	mV, p-p
T_{TX-R}	Rise time (20% to 80%)	50	—	—	ps
T_{TX-F}	Fall time (80% to 20%)	50	—	—	ps
$T_{TX-CM-AC-P}$	RMS AC peak common-mode output voltage	—	—	20	mV
Z_{TX-SE}	Single ended output impedance for 50/75 Ω	-20%	50/75	20%	Ω
	Single ended output impedance for 6K Ω	-25%	6K	25%	Ω
$RL_{TX-DIFF}$	Differential return loss with package included ³	—	—	-10	dB
RL_{TX-COM}	Common mode return loss with package included ³	—	—	-6	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at $V_{CCHTX} \pm 5\%$.
2. Refer to TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#) for settings of Tx amplitude.
3. Return los = -10 dB (differential), -6 dB (common mode) for $100 \text{ MHz} \leq f \leq 1.6 \text{ GHz}$ with 50 Ω output impedance configuration. This includes degradation due to package effects.

Table 3.23. Channel Output Jitter

Description	Frequency	Min	Typ	Max	Unit
Deterministic	3.125 Gb/s	—	—	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	—	—	0.24	UI, p-p

Note:

Values are measured with PRBS 2⁷-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

3.21. SERDES/PCS Block Latency

Table 3.24 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.24. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit ³
Transmit Data Latency¹							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency²							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = -245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

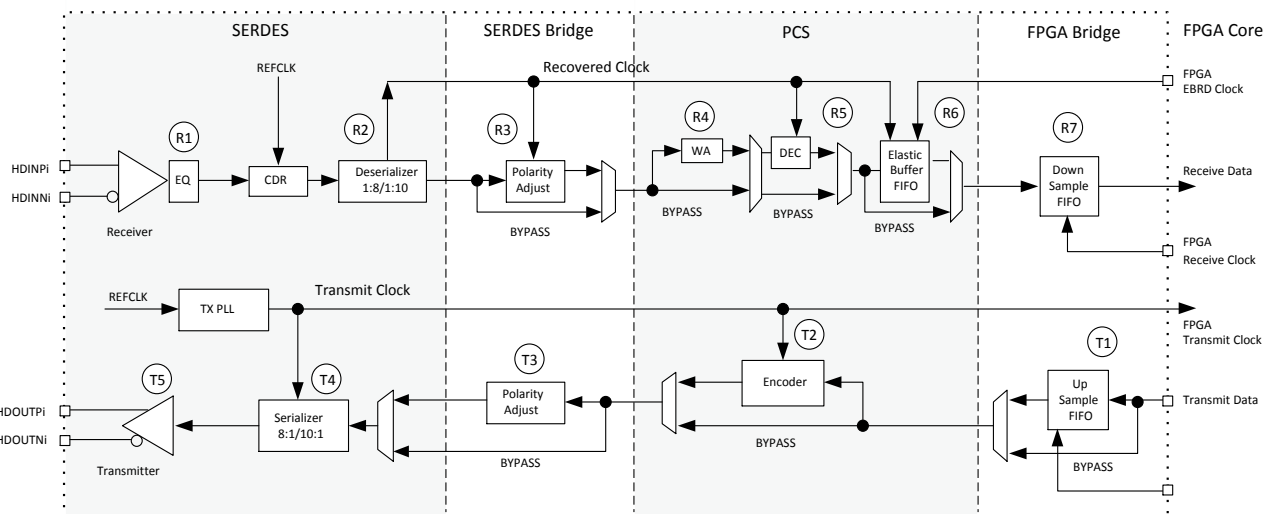


Figure 3.13. Transmitter and Receiver Latency Block Diagram

3.22. SERDES High-Speed Data Receiver

Table 3.25. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
V _{RX-DIFF-S}	Differential input sensitivity	150	—	1760	mV, p-p
V _{RX-IN}	Input levels	0	—	V _{CCA} +0.5 ²	V
V _{RX-CM-DCCM}	Input common mode range (internal DC coupled mode)	0.6	—	V _{CCA}	V
V _{RX-CM-ACCM}	Input common mode range (internal AC coupled mode) ²	0.1	—	V _{CCA} +0.2	V
T _{RX-RELOCK}	SCDR re-lock time ¹	—	1000	—	Bits
Z _{RX-TERM}	Input termination 50/75 Ω /High Z	-20%	50/75/5 K	+20%	Ω
RL _{RX-RL}	Return loss without package	—	—	-10	dB

Notes:

1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.26. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Note:

Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.

3.24. SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. [Table 3.27](#) specifies reference clock requirements over the full range of operating conditions.

Table 3.27. External Reference Clock Specification (refclkp/refclkn)⁵

Symbol	Description	Min	Typ	Max	Unit
F _{REF}	Frequency range	50	—	320	MHz
F _{REF-PPM}	Frequency tolerance ¹	-1000	—	1000	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ^{2,4}	200	—	V _{CCAUXA}	mV, p-p
V _{REF-IN-DIFF}	Input swing, differential clock	200	—	2*V _{CCAUXA}	mV, p-p differential
V _{REF-IN}	Input levels	0	—	V _{CCAUXA} + 0.4	V
D _{REF}	Duty cycle ³	40	—	60	%
T _{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T _{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
Z _{REF-IN-TERM-DIFF}	Differential input termination	-30%	100/HiZ	+30%	Ω
C _{REF-IN-CAP}	Input capacitance	—	—	7	pF

Notes:

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#).
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
3. Measured at 50% amplitude.
4. Single-ended clocking is achieved by applying a reference voltage V_{REF} on REFCLKN input, with the clock applied to REFCLKP input pin. V_{REF} should be set to mid-point of the REFCLKP voltage swing.
5. refclkp and refclkn are standard external reference clock inputs.

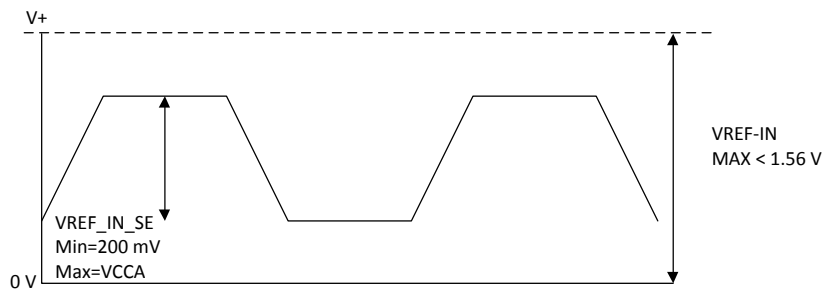
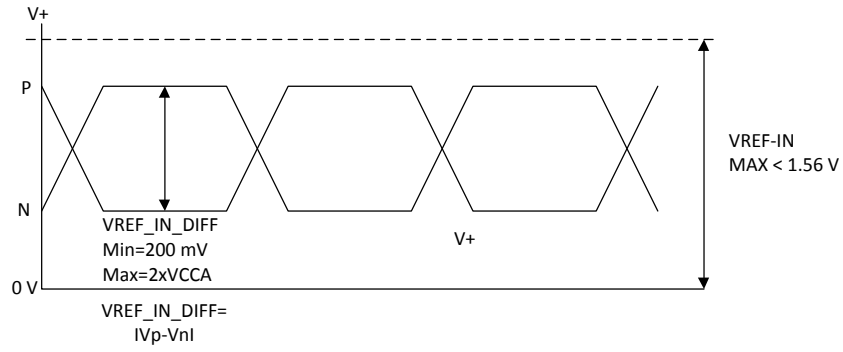


Figure 3.14. SERDES External Reference Clock Waveforms

3.25. PCI Express Electrical and Timing Characteristics

3.25.1. 2.5 Gb/s PCIe AC and DC Characteristics

Over recommended operating conditions.

Table 3.28. 2.5 Gb/s PCIe

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit¹						
UI	Unit Interval	—	399.8	400	400.12	ps
V _{TX-DIFF_P-P}	Differential Peak-to-peak Output	—	0.8	1.0	1.2	V
V _{TX-DE-RATIO}	De-emphasis Differential Output voltage ratio	—	-3	-3.5	-4	dB
V _{TX-CM-AC_P}	RMS AC Peak Common-mode Output Voltage	—	—	—	20	mV
V _{TX-RCV-DETECT}	Amount of Voltage Change Allowed during Receiver Detection	—	—	—	600	mV
V _{TX-CM-DC}	Tx DC Common Mode Voltage	—	0	—	V _{CCHTX}	V
I _{TX-SHORT}	Output Short Circuit Current	V _{TX-D+=0.0 V} V _{TX-D-=0.0 V}	—	—	90	mA
Z _{TX-DIFF-DC}	Differential Output Impedance	—	80	100	120	Ω
RL _{TX-DIFF}	Differential Return Loss	—	10	—	—	dB
RL _{TX-CM}	Common Mode Return Loss	—	6.0	—	—	dB
T _{TX-RISE}	Tx Output Rise Time	20% to 80%	0.125	—	—	UI
T _{TX-FALL}	Tx Output Fall Time	20% to 80%	0.125	—	—	UI
L _{TX-SKEW}	Lane-to-lane Static Output Skew for All Lanes in Port/Link	—	—	—	1.3	ns
T _{TX-EYE}	Transmitter Eye Width	—	0.75	—	—	UI
T _{TX-EYE-MEDIAN-TO-MAX-JITTER}	Maximum Time between Jitter Median and Maximum Deviation from	—	—	—	0.125	UI
Receive^{1,2}						
UI	Unit Interval	—	399.88	400	400.12	ps
V _{RX-DIFF_P-P}	Differential Peak-to-peak Input	—	0.34 ³	—	1.2	V
V _{RX-IDLE-DET-DIFF_P-P}	Idle Detect Threshold Voltage	—	65	—	340 ³	mV
V _{RX-CM-AC_P}	RMS AC Peak Common-mode Input Voltage	—	—	—	150	mV
Z _{RX-DIFF-DC}	DC Differential Input Impedance	—	80	100	120	Ω
Z _{RX-DC}	DC Input Impedance	—	40	50	60	Ω
Z _{RX-HIGH-IMP-DC}	Power-down DC Input Impedance	—	200K	—	—	Ω
RL _{RX-DIFF}	Differential Return Loss	—	10	—	—	dB
RL _{RX-CM}	Common Mode Return Loss	—	6.0	—	—	dB

Notes:

1. Values are measured at 2.5 Gb/s.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express 1.1 standard.

3.26. CPRI LV2 E.48 Electrical and Timing Characteristics – Preliminary

Table 3.29. CPRI LV2 E.48 Electrical and Timing Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmit						
UI	Unit Interval	—	203.43	203.45	203.47	ps
T _{DCD}	Duty Cycle Distortion	—	—	—	0.05	UI
J _{UBHPJ}	Uncorrelated Bounded High Probability Jitter	—	—	—	0.15	UI
J _{TOTAL}	Total Jitter	—	—	—	0.3	UI
Z _{RX-DIFF-DC}	DC Differential Impedance	—	80	—	120	Ω
T _{SKEW}	Skew between Differential Signals	—	—	—	9	ps
R _{LTX-DIFF}	Tx Differential Return Loss (S22), including package and silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R _{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	100 MHz < freq < 3.6864 GHz	6	—	—	dB
I _{TX-SHORT}	Transmitter Short-circuit Current	—	—	—	100	mA
T _{RISE_FALL-DIFF}	Differential Rise and Fall Time	—	—	—	—	ps
L _{TX-SKEW}	Lane-to-lane output skew	—	—	—	—	ps
Receive						
UI	Unit Interval	—	203.43	203.45	203.47	ps
V _{RX-DIFF-PP}	Differential Rx Peak-peak Voltage	—	—	—	1.2	V, p-
V _{RX-EYE_Y1_Y2}	Receiver Eye Opening Mask, Y1 and Y2	—	62.5	—	375	mV, diff
V _{RX-EYE_X1}	Receiver Eye Opening Mask, X1	—	—	—	0.3	UI
T _{RX-TJ}	Receiver Total Jitter Tolerance (not including sinusoidal)	—	—	—	0.6	UI
R _{LRX-DIFF}	Receiver Differential Return Loss, Package plus Silicon	100 MHz < freq < 3.6864 GHz	—	—	–8	dB
		3.6864 GHz < freq < 4.9152 GHz	—	—	–8 + 16.6 *log (freq/3.6864)	dB
R _{LRX-CM}	Receiver Common Mode Return Loss, Package plus Silicon	—	6	—	—	dB
Z _{RX-DIFF-DC}	Receiver DC Differential	—	80	100	120	Ω

Note: Data is measured with PRBS7 data pattern, not with PRBS-31 pattern.

3.27. XAUI/CPRI LV E.30 Electrical and Timing Characteristics

3.27.1. AC and DC Characteristics

Over recommended operating conditions.

Table 3.30. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}	Differential Rise/Fall Time	20% to 80%	—	80	—	ps
$Z_{TX_DIFF_DC}$	Differential Impedance	—	80	100	120	Ω
$J_{TX_DDJ}^{2,3}$	Output Data Deterministic Jitter	—	—	—	0.17	UI
$J_{TX_TJ}^{1,2,3}$	Total Output Data Jitter	—	—	—	0.35	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Over recommended operating conditions.

Table 3.31. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential Return Loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common Mode Return Loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential Termination Resistance	—	80	100	120	Ω
$J_{RX_DJ}^{1,2,3}$	Deterministic Jitter Tolerance Peak-to-peak	—	—	—	0.37	UI
$J_{RX_RJ}^{1,2,3}$	Random Jitter Tolerance Peak-to-peak	—	—	—	0.18	UI
$J_{RX_SJ}^{1,2,3}$	Sinusoidal Jitter Tolerance Peak-to-peak	—	—	—	0.10	UI
$J_{RX_TJ}^{1,2,3}$	Total Jitter Tolerance Peak-to-peak	—	—	—	0.65	UI
T_{RX_EYE}	Receiver Eye Opening	—	0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

3.28. CPRI LV E.24 Electrical and Timing Characteristics

3.28.1. AC and DC Characteristics

Table 3.32. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}^1	Differential Rise/Fall time	20% to 80%	—	80	—	ps
$Z_{TX_DIFF_DC}$	Differential Impedance	—	80	100	120	Ω
$J_{TX_DDJ}^{3,4}$	Output Data Deterministic Jitter	—	—	—	0.17	UI
$J_{TX_TJ}^{2,3,4}$	Total Output Data Jitter	—	—	—	0.35	UI

Notes:

1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance or 100 Ω differential impedance.
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.33. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL _{RX_DIFF}	Differential Return Loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL _{RX_CM}	Common Mode Return Loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential Termination Resistance	—	80	100	120	Ω
J _{RX_DJ} ^{2, 3, 4}	Deterministic Jitter Tolerance Peak-to-peak	—	—	—	0.37	UI
J _{RX_RJ} ^{2, 3, 4}	Random Jitter Tolerance Peak-to-peak	—	—	—	0.18	UI
J _{RX_SJ} ^{2, 3, 4}	Sinusoidal Jitter Tolerance Peak-to-peak	—	—	—	0.10	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total Jitter Tolerance Peak-to-peak	—	—	—	0.65	UI
T _{RX_EYE}	Receiver Eye Opening	—	0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity, and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.29. Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

3.29.1. AC and DC Characteristics

Table 3.34. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T _{RF}	Differential Rise/Fall Time	20% to 80%	—	80	—	ps
Z _{TX_DIFF_DC}	Differential Impedance	—	80	100	120	Ω
J _{TX_DDJ} ^{2, 3}	Output Data Deterministic Jitter	—	—	—	0.10	UI
J _{TX_TJ} ^{1, 2, 3}	Total Output Data Jitter	—	—	—	0.24	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.35. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL _{RX_DIFF}	Differential Return Loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL _{RX_CM}	Common Mode Return Loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z _{RX_DIFF}	Differential Termination Resistance	—	80	100	120	Ω
J _{RX_DJ} ^{1, 2, 3, 4}	Deterministic Jitter Tolerance Peak-to-peak	—	—	—	0.34	UI
J _{RX_RJ} ^{1, 2, 3, 4}	Random Jitter Tolerance Peak-to-peak	—	—	—	0.26	UI
J _{RX_SJ} ^{1, 2, 3, 4}	Sinusoidal Jitter Tolerance Peak-to-peak	—	—	—	0.11	UI
J _{RX_TJ} ^{1, 2, 3, 4}	Total Jitter Tolerance Peak-to-peak	—	—	—	0.71	UI
T _{RX_EYE}	Receiver Eye Opening	—	0.29	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter, and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.36. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR _{SDO}	Serial Data Rate	—	270	—	2975	Mb/s
T _{JALIGNMENT} ²	Serial Output Jitter, Alignment	270 Mb/s ³	—	—	0.2	UI
T _{JALIGNMENT} ²	Serial Output Jitter, Alignment	1485 Mb/s	—	—	0.2	UI
T _{JALIGNMENT} ^{1,2}	Serial Output Jitter, Alignment	2970 Mb/s	—	—	0.3	UI
T _{JTIMING}	Serial Output Jitter, Timing	270 Mb/s ³	—	—	0.2	UI
T _{JTIMING}	Serial Output Jitter, Timing	1485 Mb/s	—	—	1	UI
T _{JTIMING}	Serial Output Jitter, Timing	2970 Mb/s	—	—	2	UI

Notes:

1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. 270 Mb/s is supported with Rate Divider only.
4. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice Semiconductor SERDES device configured to 50 Ω output impedance connecting to the external cable driver with differential signaling.
5. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mb/s.
6. All LAE5UM devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.

Table 3.37. Receive

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR _{SDI}	Serial Input Data Rate	—	270	—	2970	Mb/s

Table 3.38. Reference Clock

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F _{VCLK}	Video Output Clock Frequency	—	54	—	148.5	MHz
DC _V	Duty Cycle, Video Clock	—	45	50	55	%

Note: 270 Mb/s SD-SDI (is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.

3.31. ECP5 Automotive sysCONFIG Port Timing Specifications

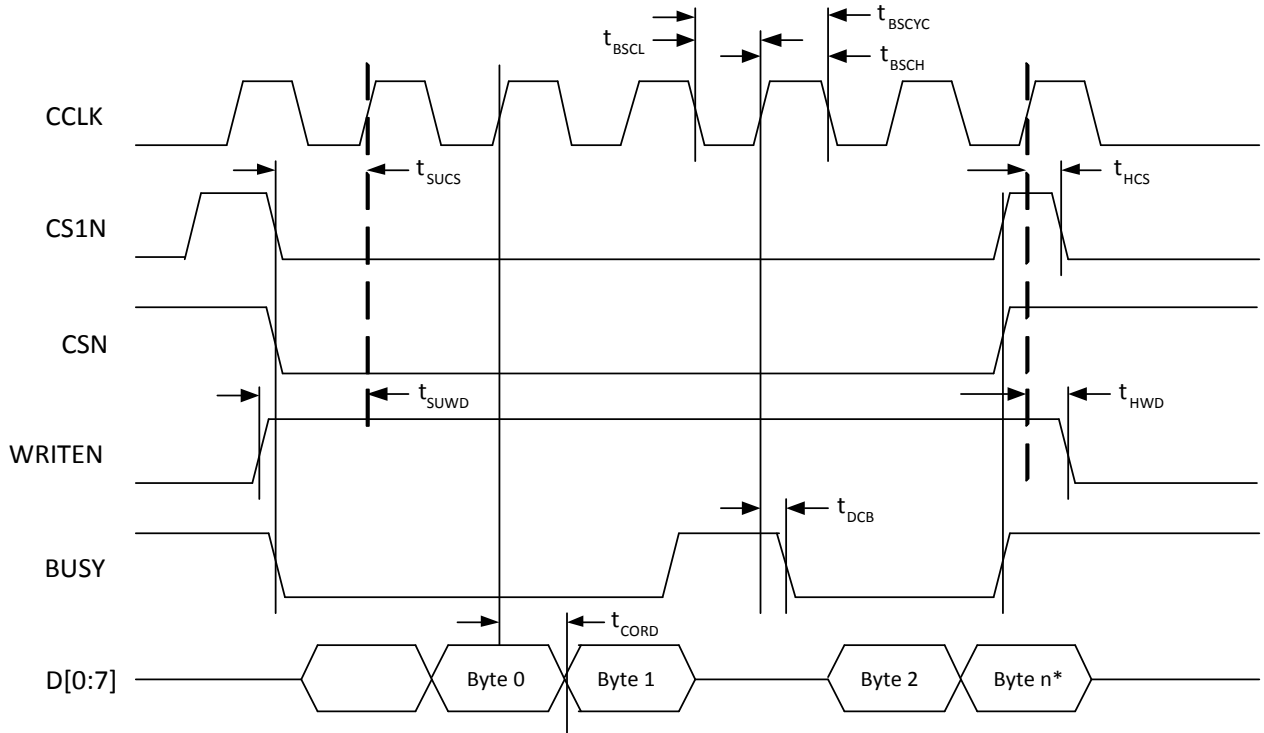
Over recommended operating conditions.

Table 3.39. ECP5 Automotive sysCONFIG Port Timing Specifications

Symbol	Parameter	Frequency	Min	Max	Unit
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC} , V_{CCAUX} or V_{CCI08} (whichever is the last) to the rising edge of INITN	—	—	33	ms
t_{VMC}	Time from t_{ICFG} to the valid Master CCLK	—	—	5	us
t_{CZ}	CCLK from Active to High-Z	—	—	300	ns
Master CCLK					
—	Frequency	All selected frequencies	-20	20	%
—	Duty Cycle	All selected frequencies	40	60	%
All Configuration Modes					
t_{PRGM}	PROGRAMN LOW Pulse Accepted	—	110	—	ns
t_{PRGMRJ}	PROGRAMN LOW Pulse Rejected	—	—	50	ns
t_{INITL}	INITN LOW Time	—	—	55	ns
t_{DPPINT}	PROGRAMN LOW to INITN LOW	—	—	70	ns
$t_{DPPDONE}$	PROGRAMN LOW to DONE LOW	—	—	80	ns
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	150	ns
Slave SPI					
f_{CCLK}	CCLK Input Clock Frequency	—	—	60	MHz
t_{CCLKH}	CCLK Input Clock Pulswidth HIGH	—	6	—	ns
t_{CCLKL}	CCLK Input Clock Pulswidth LOW	—	6	—	ns
t_{STSU}	CCLK Setup Time	—	1	—	ns
t_{STH}	CCLK Hold Time	—	1	—	ns
t_{STCO}	CCLK Falling Edge to Valid Output	—	—	10	ns
t_{STOZ}	CCLK Falling Edge to Valid Disable	—	—	10	ns
t_{STOV}	CCLK Falling Edge to Valid Enable	—	—	10	ns
t_{SCS}	Chip Select HIGH Time	—	25	—	ns
t_{SCSS}	Chip Select Setup Time	—	3	—	ns
t_{SCSH}	Chip Select Hold Time	—	3	—	ns
Master SPI					
f_{CCLK}	Max Selected CCLK Output Frequency	—	—	62	MHz
t_{CCLKH}	CCLK Output Clock Pulse Width HIGH	—	3.5	—	ns
t_{CCLKL}	CCLK Output Clock Pulse Width LOW	—	3.5	—	ns
t_{STSU}	CCLK Setup Time	—	5	—	ns
t_{STH}	CCLK Hold Time	—	1	—	ns
t_{CSSPI}	INITN HIGH to Chip Select LOW	—	100	200	ns
t_{CFGX}	INITN HIGH to First CCLK Edge	—	—	150	ns
Slave Serial					
f_{CCLK}	CCLK Input Clock Frequency	—	—	66	MHz
t_{SSCH}	CCLK Input Clock Pulse Width HIGH	—	5	—	ns
t_{SSCL}	CCLK Input Clock Pulse Width LOW	—	5	—	ns
t_{SUSCDI}	CCLK Setup Time	—	0.5	—	ns

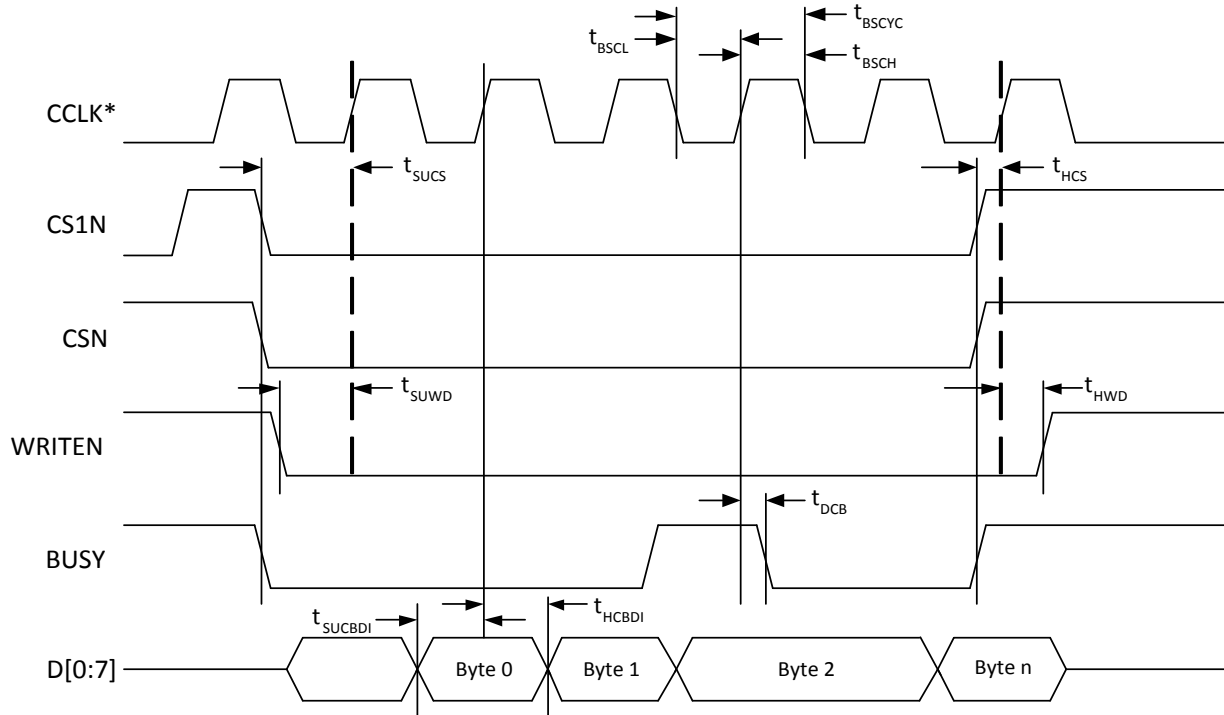
Table 3.39. ECP5 Automotive sysCONFIG Port Timing Specifications (Continued)

Symbol	Parameter	Frequency	Min	Max	Unit
Slave Parallel					
t_{HSCDI}	CCLK Hold Time	—	1.5	—	ns
f_{CCLK}	CCLK Input Clock Frequency	—	—	50	MHz
t_{BSCH}	CCLK Input Clock Pulsewidth HIGH	—	6	—	ns
t_{BSCL}	CCLK Input Clock Pulsewidth LOW	—	6	—	ns
t_{CORD}	CCLK to DOUT for Read Data	—	—	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	—	1.5	—	ns
t_{HCBDI}	Data Hold Time to CCLK	—	1.5	—	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK	—	45	—	ns
t_{HCWD}	WRITEN Hold Time to CCLK	—	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	—	12	ns



*n = last byte of read cycle.

Figure 3.15. sysCONFIG Parallel Port Read Cycle



*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3.16. sysCONFIG Parallel Port Write Cycle

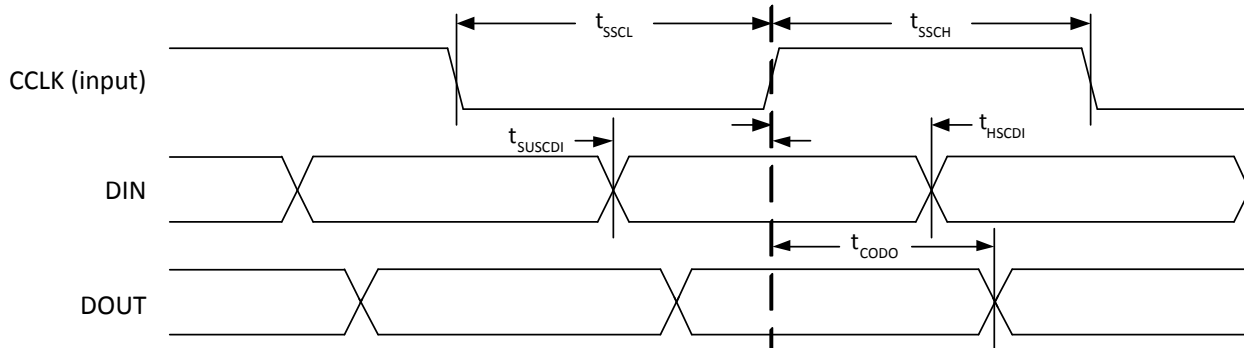
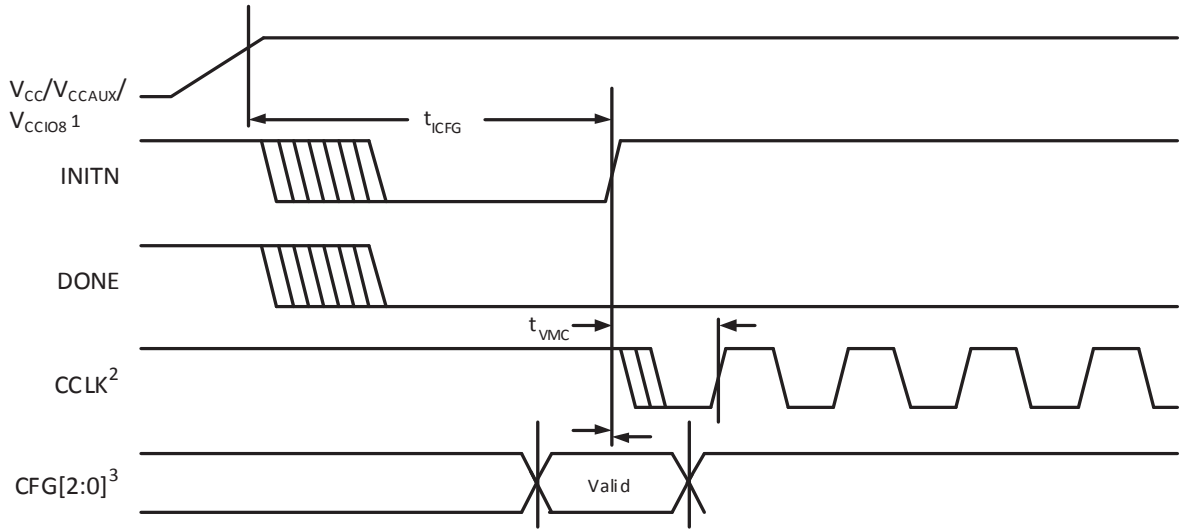


Figure 3.17. sysCONFIG Slave Serial Port Timing



Notes:

1. Time taken from V_{CC} , V_{CCAUX} or V_{CCIO8} , whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPI_M).
3. The CFG pins are normally static (hardwired).

Figure 3.18. Power-On-Reset (POR) Timing

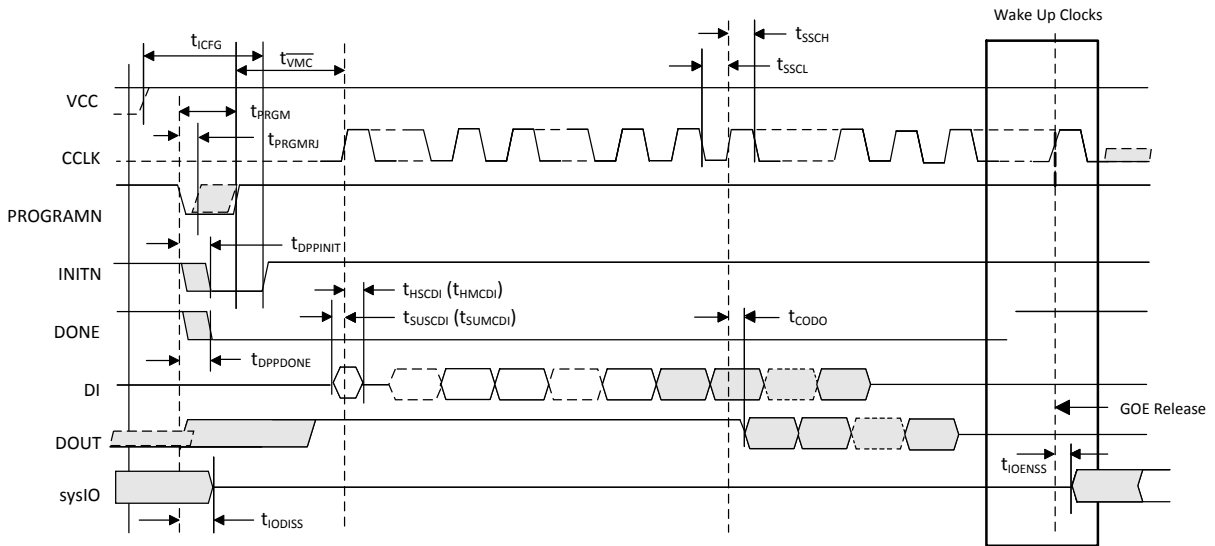
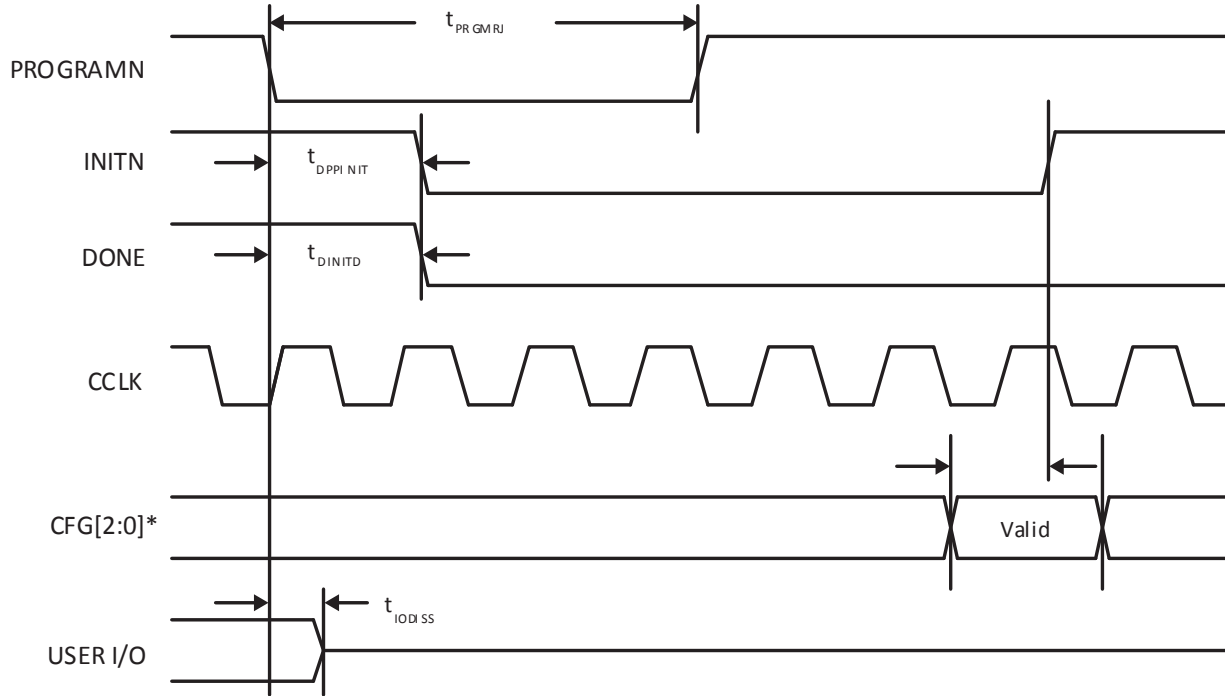


Figure 3.19. sysCONFIG Port Timing



*Note: The CFG pins are normally static (hardwired).

Figure 3.20. Configuration from PROGRAMN Timing

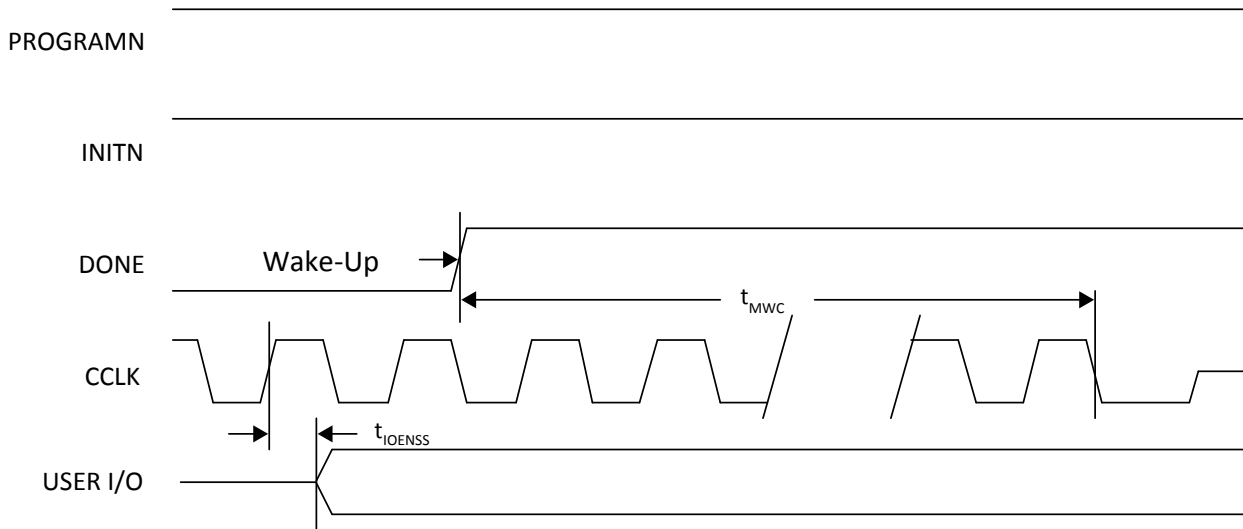


Figure 3.21. Wake-Up Timing

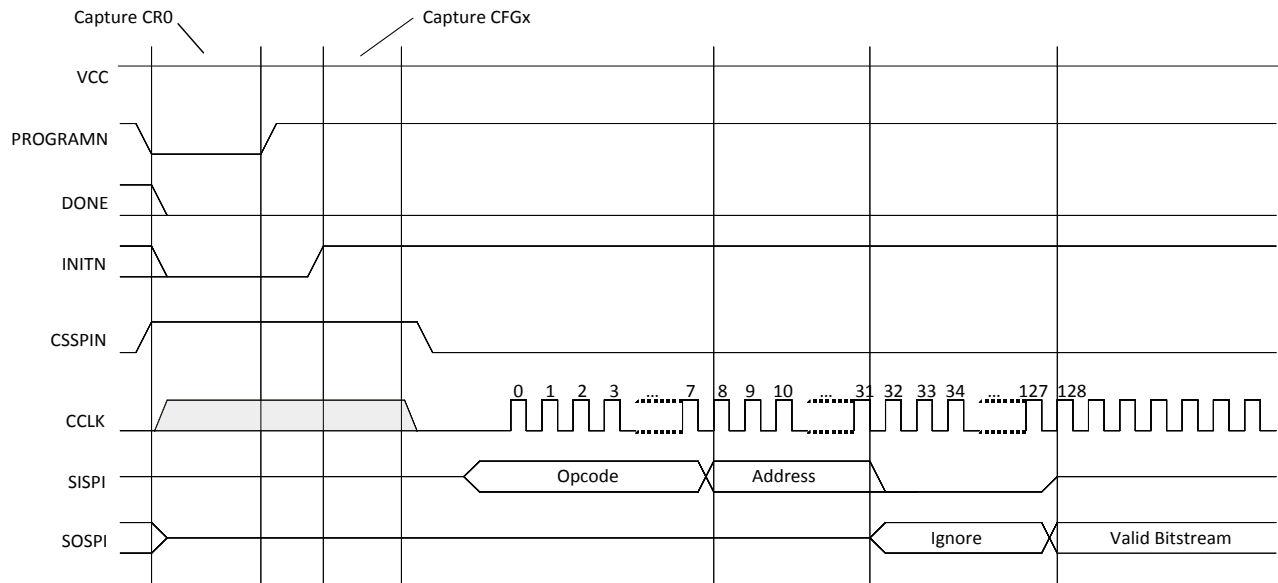


Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.40. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	10	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	8	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTco}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTcoEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	25	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BUODIS}	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
t_{BUPOEN}	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

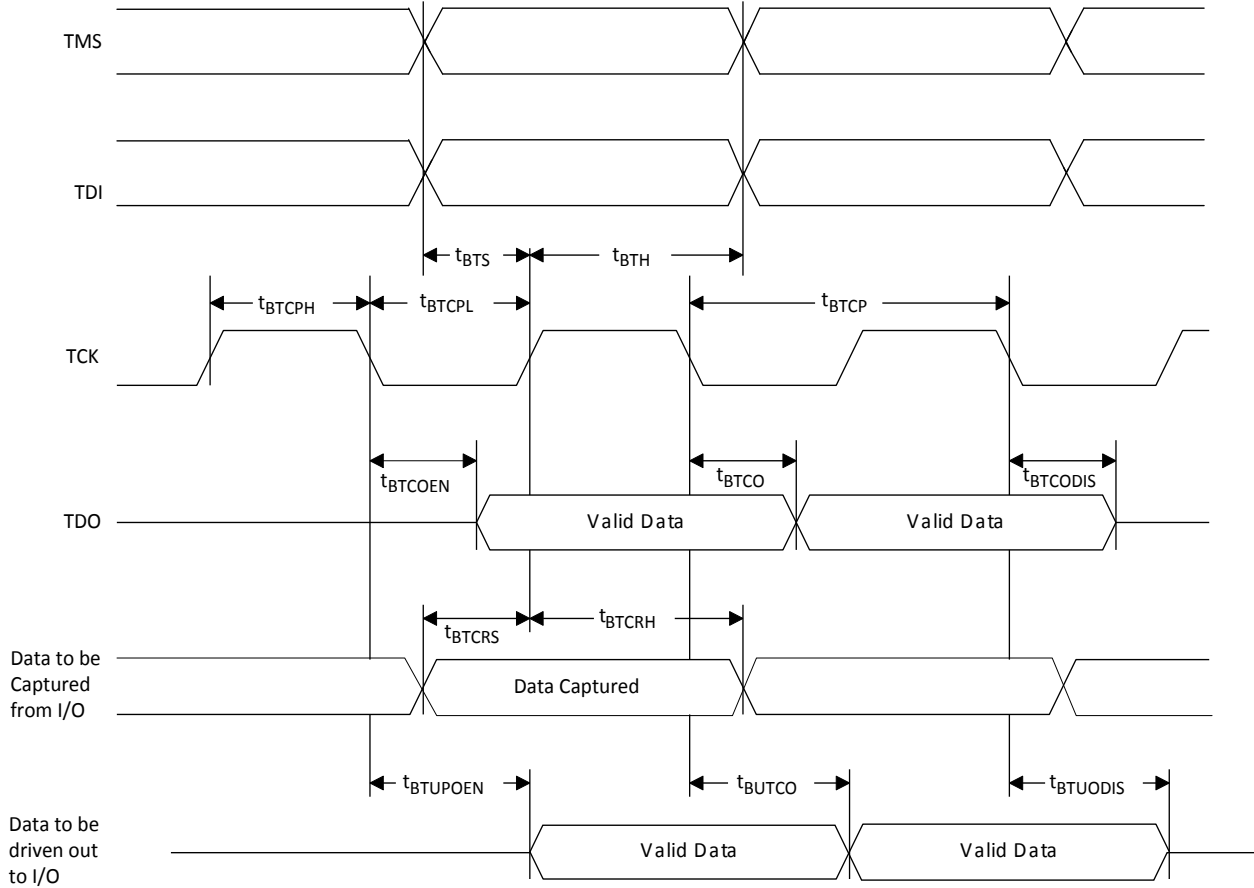
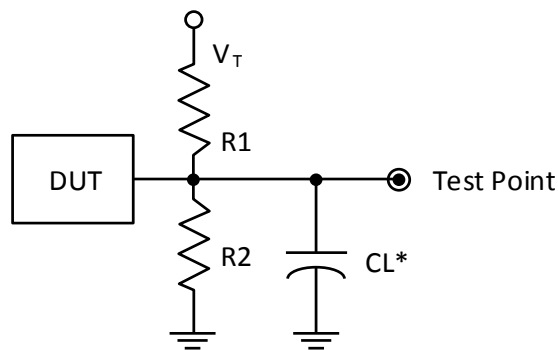


Figure 3.23. JTAG Port Timing Waveforms

3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.41.



*Note: CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards

Table 3.41. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V _{OH} - 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. Pinout Information

4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[L/R] [Group Number]_[A/B/C/D]	I/O	<p>[L/R] indicates the L (Left), or R (Right) edge of the device. [Group Number] indicates the PIO [A/B/C/D] group.</p> <p>[A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tristated with an internal pull-down resistor enabled. If any pin is not used, or not bonded to a package pin, it is tristated and default to have pull-down enabled after configuration.</p> <p>PIO A and B are grouped as a pair. PIO C and D are grouped as a pair. Each pair supports true LVDS differential input buffer. Only PIO A and B pair supports true LVDS differential output buffer.</p> <p>Each A/B and C/D pair supports programmable on/off differential input termination of 100 Ω.</p>
P[T/B][Group Number]_[A/B]	I/O	<p>[T/B] indicates the T (top) or B (bottom) edge of the device. [Group Number] indicates the PIO [A/B] group.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with sysConfig pins. These pins, when not being used as configuration pins, can be programmed as I/Os for user logic. During configuration, the pins not used in configuration are tristated with an internal pull-down resistor enabled. If any pin is not used, or not bonded to a package pin, it is tristated and default to have pull-down enabled after configuration.</p> <p>PIOs on top and bottom do not support differential input signaling or true LVDS output signaling, but it can support emulated differential output buffer.</p>
GSRN	I	Active LOW Global RESET signal. Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins. V _{CC} = 1.1 V
V _{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. V _{CCAUX} = 2.5 V.
V _{CCIOx}	—	Dedicated power supply pins for I/O bank x. V _{CCIO8} is used for configuration and JTAG.
V _{REF1_x}	—	Reference supply pins for I/O bank x. Pre-determined shared pin in each bank are assigned as V _{REF1} input. When not being used, they may be used as I/O pins.
PLL, DLL and Clock Functions		
[LOC]_[GPLL][T, C]_IN	I	General Purpose PLL (GPLL) input pads: [LOC] = ULC, LLC, URC and LRC, T = true and C = complement. These pins are shared I/O pins. When not being configured as GPLL input pads, they can be used as general purpose I/O pins.
GR_PCLK[Bank][num]	I	General Routing Signals in Banks 0, 1, 2, 3, 4, 6 and 7. There are two in each bank ([num] = 0, 1). Refer to TN1263, ECP5 sysClock PLL/DLL Design and Usage Guide . These pins are shared I/O pins. When not being configured as GR pins, they can be used as general purpose I/O pins.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1, 2, 3, 6 and 7). There are two in each bank ([num] = 0, 1). These are shared I/O pins. When not being configured as PCLK pins, they can be used as general purpose I/O pins.

Signal Name	I/O	Description
PLL, DLL and Clock Functions (Continued)		
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
[T/R]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_num = ball number associated with DQS[T] pin.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. This is a dedicated input pin.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. Note: once a configuration port is selected, it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.
Configuration Pads (Used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on the rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes – Master SPI or Master Serial. This is a dedicated pin.
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPI _m mode data output. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DOUT/CSON	O	Serial data output. Chip select output. SPI/SPI _m mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DO/MOSI/IOO	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.

Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) (Continued)		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
SERDES Function		
V _{CCA} x	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All V _{CCA} supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect V _{CCA} to V _{CC} . V _{CCA} x = 1.1 V for ECP5
V _{CCAUX} x	—	SERDES Aux Power Supply pin for SERDES Dual x. V _{CCAUX} x = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5.

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. num defines the associated channel in the quad.

4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device Only		
P[L/R] [n-6]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n-3]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n]	A	DQS (P)
	B	DQS (N)
	C	DQ
	D	DQ
P[L/R] [n+3]	A	DQ
	B	DQ
	C	DQ
	D	DQ

Note: "n" is a row PIC number.

4.3. Pin Information Summary

4.3.1. LAE5UM

Pin Information Summary		LAE5UM -25	LAE5UM-45
Pin Type		381 caBGA	381 caBGA
General Purpose Inputs/Outputs per Bank	Bank 0	24	27
	Bank 1	32	33
	Bank 2	32	32
	Bank 3	32	33
	Bank 4	0	0
	Bank 6	32	33
	Bank 7	32	32
	Bank 8	13	13
Total Single-Ended User I/O		197	203
V _{CC}		20	20
V _{CCAUX} (Core)		4	4
V _{CCIO}	Bank 0	2	2
	Bank 1	2	2
	Bank 2	3	3
	Bank 3	3	3
	Bank 4	0	0
	Bank 6	3	3
	Bank 7	3	3
	Bank 8	2	2
TAP		4	4
Miscellaneous Dedicated Pins		7	7
GND		59	59
NC		8	2
Reserved		2	2
SERDES		28	28
V _{CCA} (SERDES)	V _{CCA0}	2	2
	V _{CCA1}	2	2
V _{CCAUX} (SERDES)	V _{CCAUXA0}	2	2
	V _{CCAUXA1}	2	2
GNDA (SERDES)		—	26
Total Balls		—	381
High Speed Differential Input / Output Pairs	Bank 0	0	0
	Bank 1	0	0
	Bank 2	16/8	16/8
	Bank 3	16/8	16/8
	Bank 4	0	0
	Bank 6	16/8	16/8
	Bank 7	16/8	16/8
	Bank 8	0	0

LAESUM (Continued)

Pin Information Summary		LAESUM -25	LAESUM-45
Pin Type		381 caBGA	381 caBGA
Total High Speed Differential I/O Pairs		64/32	64/32
DQS Groups (> 11 pins in group)	Bank 0	0	0
	Bank 1	0	0
	Bank 2	2	2
	Bank 3	2	2
	Bank 4	0	0
	Bank 6	2	2
	Bank 7	2	2
	Bank 8	0	0
Total DQS Groups		8	8

4.3.2. LAESU

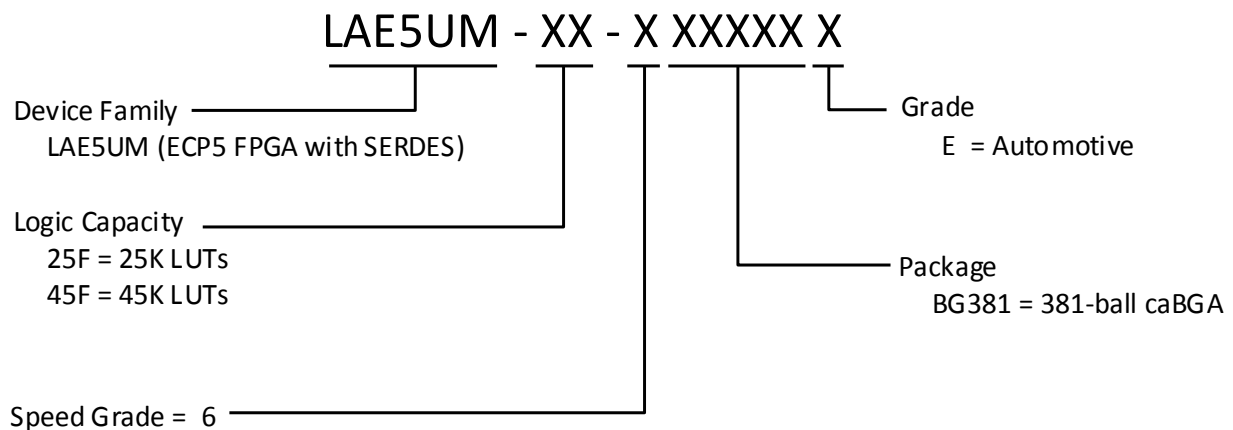
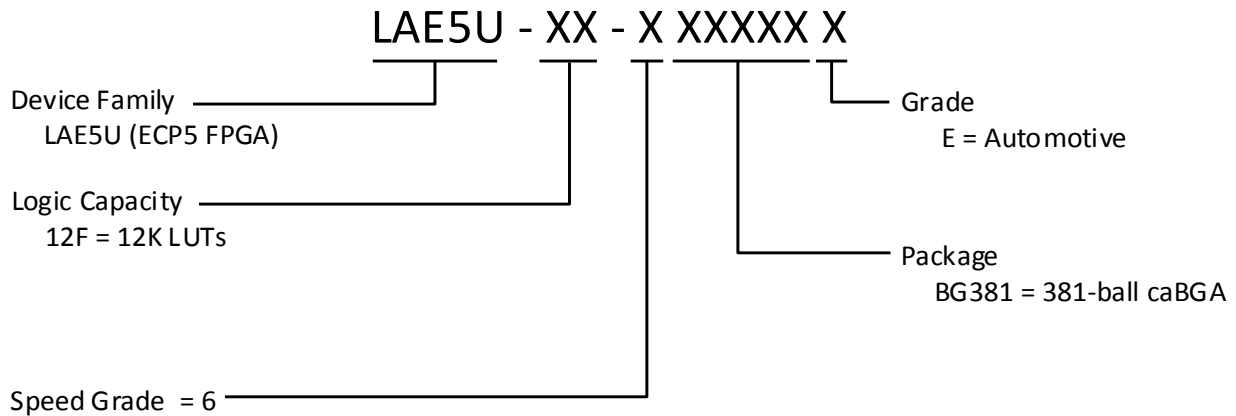
Pin Information Summary		LAESU-12
Pin Type		381 caBGA
General Purpose Inputs/Outputs per Bank	Bank 0	24
	Bank 1	32
	Bank 2	32
	Bank 3	32
	Bank 4	0
	Bank 6	32
	Bank 7	32
	Bank 8	13
Total Single-Ended User I/O		197
V _{CC}		20
V _{CCAUX} (Core)		4
V _{CCIO}	Bank 0	2
	Bank 1	2
	Bank 2	3
	Bank 3	3
	Bank 4	0
	Bank 6	3
	Bank 7	3
	Bank 8	2
TAP		4
Miscellaneous Dedicated Pins		7
GND		99
NC		26
Reserved		6
Total Balls		381

LAESU (Continued)

Pin Information Summary		LAESU-12
Pin Type		381 caBGA
High Speed Differential Input / Output Pairs	Bank 0	0
	Bank 1	0
	Bank 2	16/8
	Bank 3	16/8
	Bank 4	0
	Bank 6	16/8
	Bank 7	16/8
	Bank 8	0
Total High Speed Differential I/O Pairs		64/32
DQS Groups (> 11 pins in group)	Bank 0	0
	Bank 1	0
	Bank 2	2
	Bank 3	2
	Bank 4	0
	Bank 6	2
	Bank 7	2
	Bank 8	0
Total DQS Groups		8

5. Ordering Information

5.1. ECP5 Automotive Part Number Description



5.2. Ordering Part Numbers

5.2.1. Automotive

Part number	Grade	Package	Pins	Temp.	LUTs (K)	SERDES
LAE5U-12F-6BG381E	-6	Lead free caBGA	381	Automotive	12	No
LAE5UM-25F-6BG381E	-6	Lead free caBGA	381	Automotive	24	Yes
LAE5UM-45F-6BG381E	-6	Lead free caBGA	381	Automotive	44	Yes

Supplemental Information

For Further Information

A variety of technical notes for the ECP5 Automotive family are available.

- TN1184, [LatticeECP3, ECP-5 and ECP5-5G Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide](#)
- TN1260, [ECP5 and ECP5-5G sysCONFIG Usage Guide](#)
- TN1261, [ECP5 and ECP5-5G SERDES/PCS Usage Guide](#)
- TN1262, [ECP5 and ECP5-5G sysIO Usage Guide](#)
- TN1263, [ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide](#)
- TN1264, [ECP5 and ECP5-5G Memory Usage Guide](#)
- TN1265, [ECP5 and ECP5-5G High-Speed I/O Interface](#)
- TN1266, [Power Consumption and Management for ECP5 and ECP5-5G Devices](#)
- TN1267, [ECP5 and ECP5-5G sysDSP Usage Guide](#)

For further information on interface standards, refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL): www.jedec.org
- PCI: www.pcisig.com

Revision History

Date	Version	Section	Change Summary
September 2016	1.0	All	Initial preliminary release.



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