Freescale Semiconductor
Technical Data

Document Number: MRF7S19210H
Rev. 1, 3/2011

√RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7S19210HR3
MRF7S19210HSR3

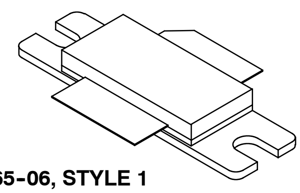
1930-1990 MHz, 63 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

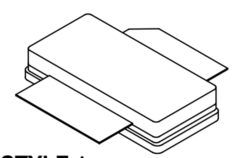
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1400 mA, P_{out} = 63 Watts Avg., f = 1987.5 MHz, IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  - Power Gain — 20 dB
  - Drain Efficiency — 29%
  - Device Output Signal PAR — 5.9 dB @ 0.01% Probability on CCDF
  - ACPR @ 5 MHz Offset — -33 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 1960 MHz, 190 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 1 dB Compression Point ≃ 190 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel.



CASE 465-06, STYLE 1
NI-780
MRF7S19210HR3



CASE 465A-06, STYLE 1
NI-780S
MRF7S19210HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 85°C, 190 W CW Case Temperature 79°C, 63 W CW	$R_{\theta JC}$	 0.34 0.38	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

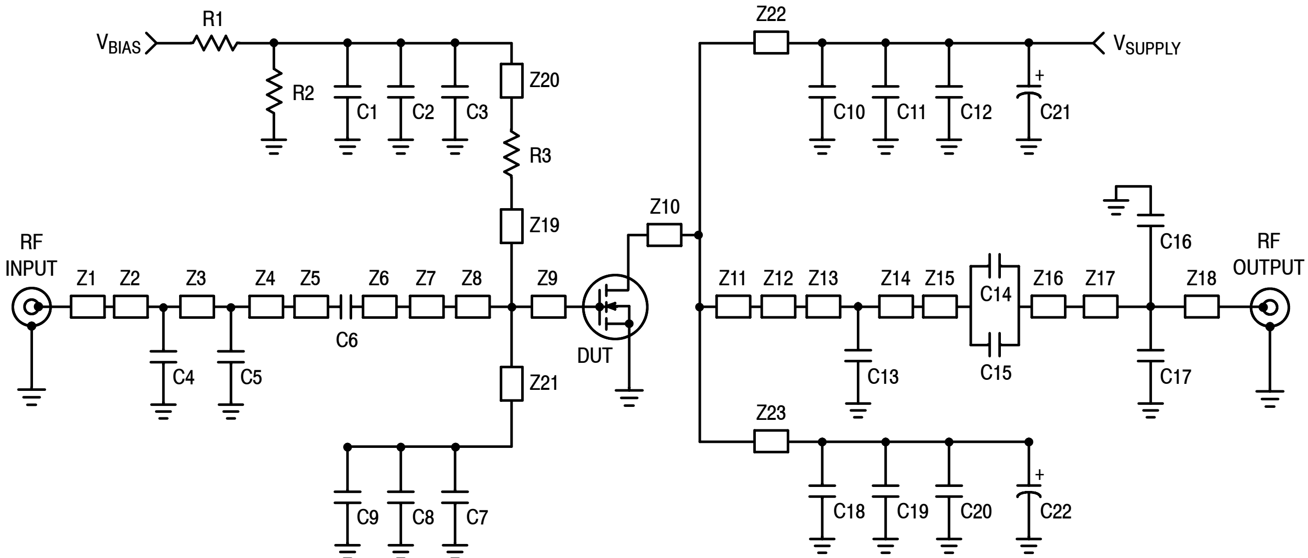
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 513 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 1400 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 1400 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4	5.4	7	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 5.13 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.17	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	257	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	508	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 63 W Avg., f = 1987.5 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18	20	21.5	dB
Drain Efficiency	η_D	26	29	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.5	5.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33	-31	dBc
Input Return Loss	IRL	—	-9.5	-6	dB

1. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 1930-1990 MHz Bandwidth					
IMD Symmetry @ 160 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	15	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	50	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 63 W Avg.	G_F	—	0.9	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 190 W CW	Φ	—	0.95	—	°
Average Group Delay @ P_{out} = 190 W CW, f = 1960 MHz	Delay	—	2.82	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 190 W CW, f = 1960 MHz, Six Sigma Window	ΔΦ	—	28.9	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.019	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.008	—	dB/°C



Z1	0.126″ x 0.066″ Microstrip	Z13	0.078″ x 0.102″ Microstrip
Z2	0.584″ x 0.079″ Microstrip	Z14	0.319″ x 0.102″ Microstrip
Z3	0.110″ x 0.079″ Microstrip	Z15	0.709″ x 0.220″ Microstrip
Z4	0.133″ x 0.079″ Microstrip	Z16	0.709″ x 0.220″ Microstrip
Z5	0.059″ x 0.118″ Microstrip	Z17	0.747″ x 0.066″ Microstrip
Z6	0.059″ x 0.118″ Microstrip	Z18	0.227″ x 0.066″ Microstrip
Z7	0.197″ x 0.102″ Microstrip	Z19	0.145″ x 0.090″ Microstrip
Z8	0.860″ x 0.551″ Microstrip	Z20	0.548″ x 0.090″ Microstrip
Z9	0.114″ x 0.551″ Microstrip	Z21	0.734″ x 0.090″ Microstrip
Z10	0.129″ x 1.102″ Microstrip	Z22, Z23	1.044″ x 0.100″ Microstrip
Z11	0.304″ x 1.102″ Microstrip	PCB	Taconic RF35, 0.030″, ε_r = 3.5
Z12	0.295″ x 0.276″ Microstrip		

Figure 1. MRF7S19210HR3(HSR3) Test Circuit Schematic

Table 5. MRF7S19210HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C11, C12, C19, C20	10 μF, 50 V Chip Capacitors	C5750X5R1H106M	TDK
C2, C8	100 nF Chip Capacitors	12065C104KAT2A	AVX
C3, C6, C7, C10, C14, C15, C18	8.2 pF Chip Capacitors	ATC100B8R2BT500XT	ATC
C4	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C5	1.8 pF Chip Capacitor	ATC100B1R8BT500XT	ATC
C13	0.4 pF Chip Capacitor	ATC100B0R4BT500XT	ATC
C16, C17	0.5 pF Chip Capacitors	ATC100B0R5BT500XT	ATC
C21, C22	470 μF Electrolytic Capacitors	222212018471	Vishay BC Components
R1, R2	10 kΩ, 1/4 W Chip Resistors	WCR120610KFI	Welwyn
R3	10 Ω, 1/4 W Chip Resistor	WCR120610RFI	Welwyn

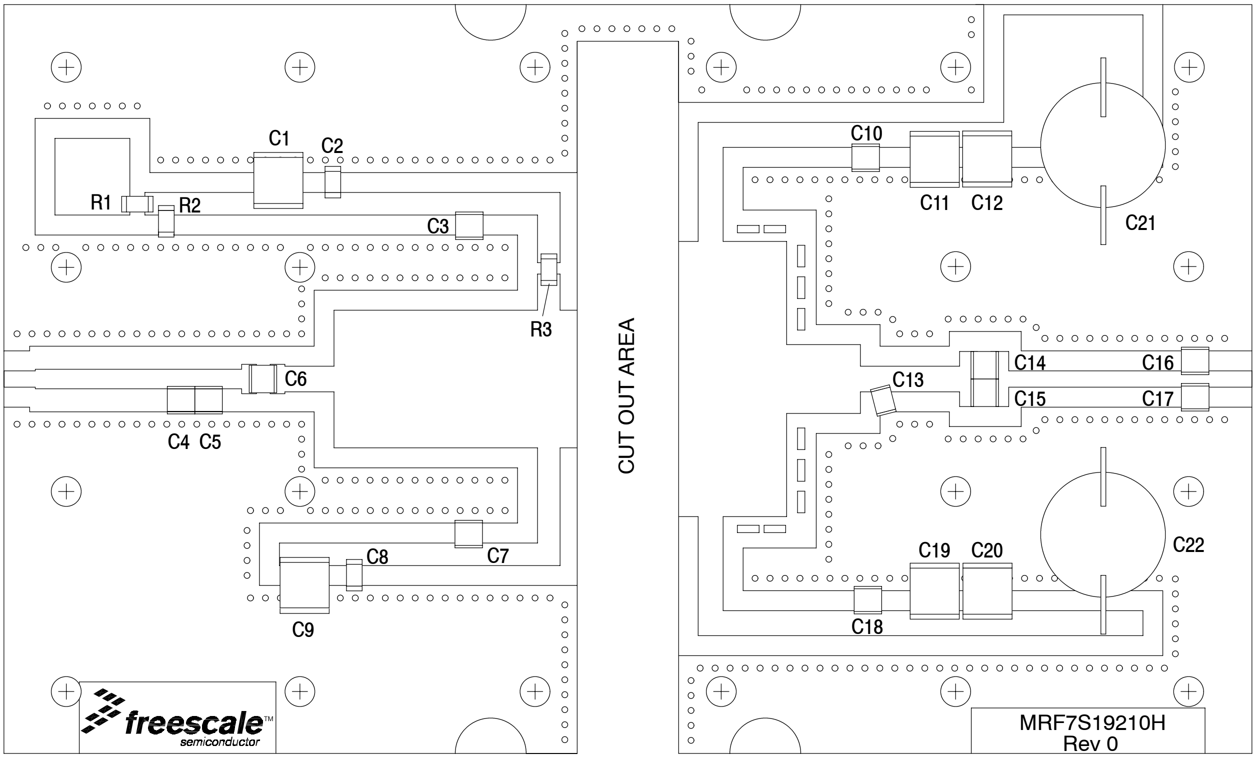


Figure 2. MRF7S19210HR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

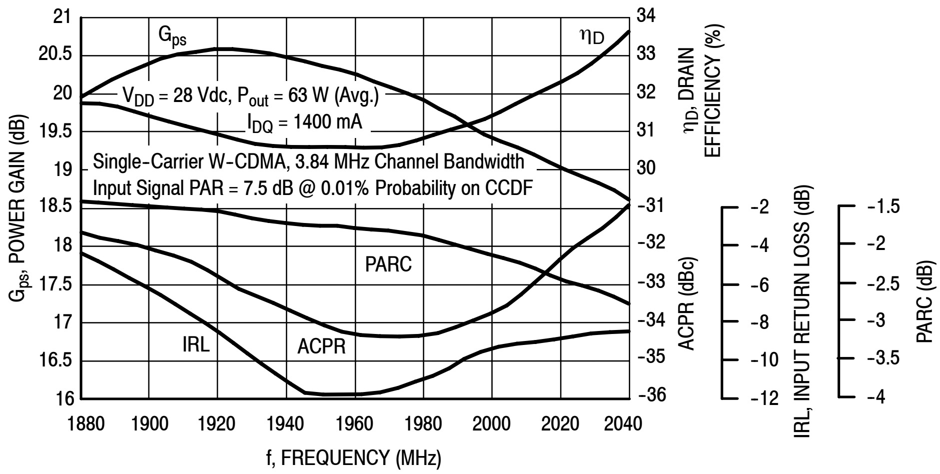


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

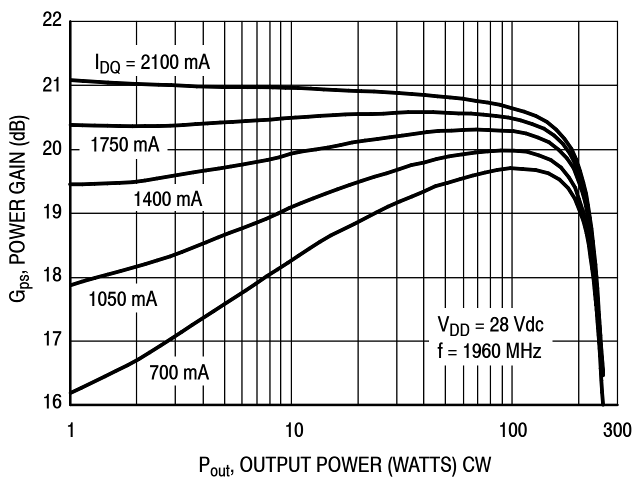


Figure 4. Power Gain versus Output Power

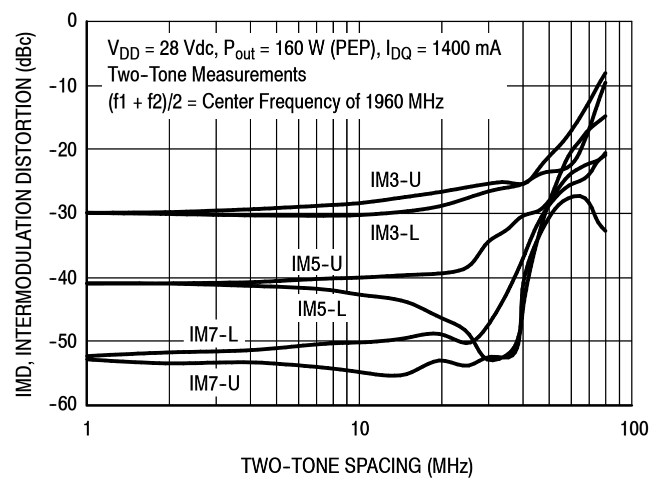


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

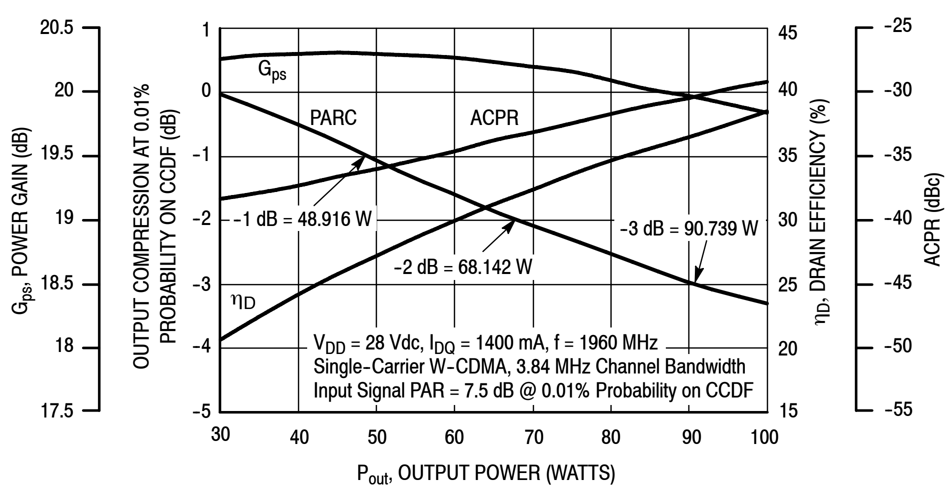


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

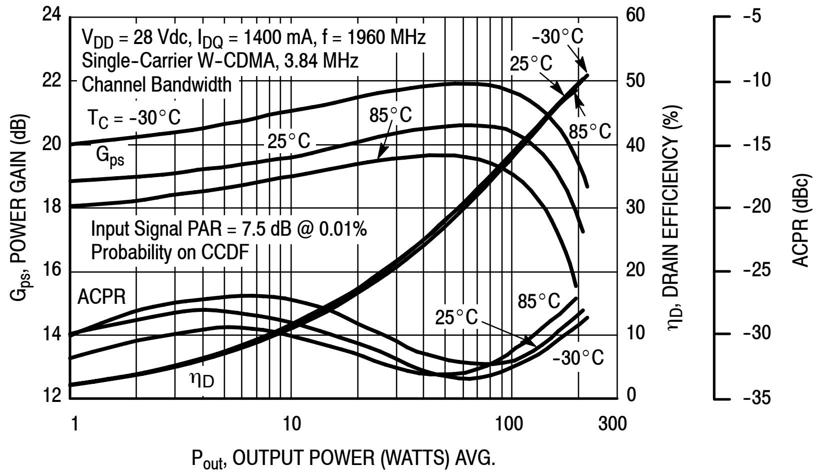


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

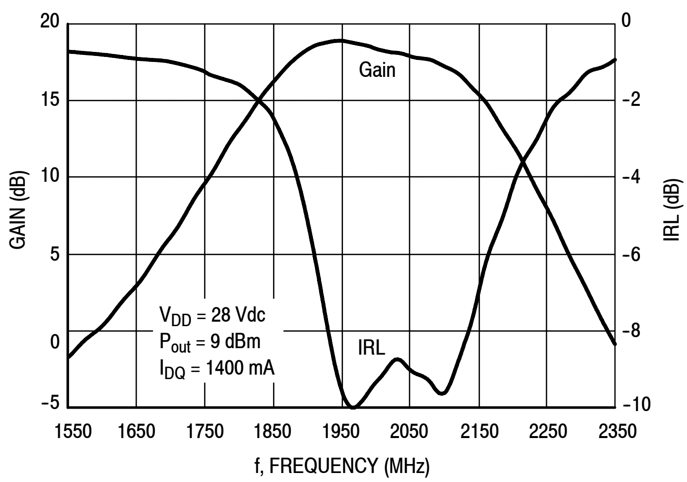


Figure 8. Broadband Frequency Response

W-CDMA TEST SIGNAL

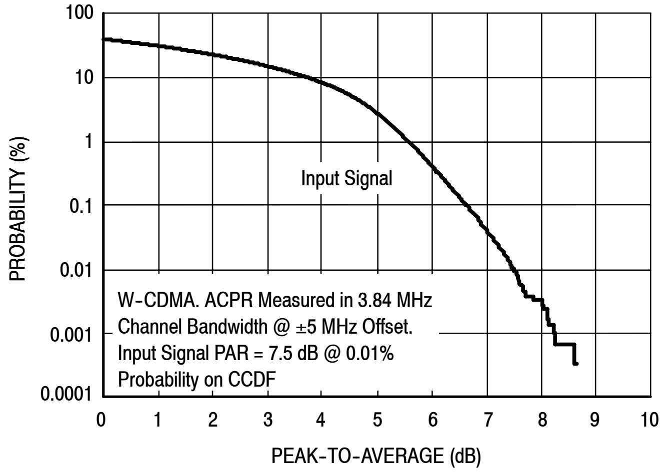


Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

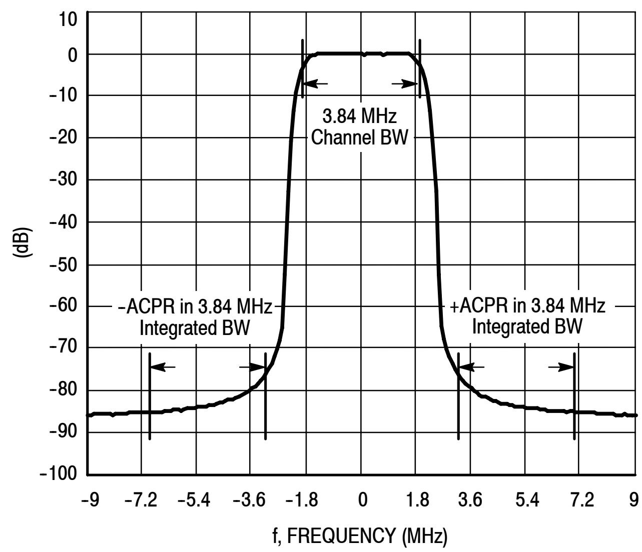
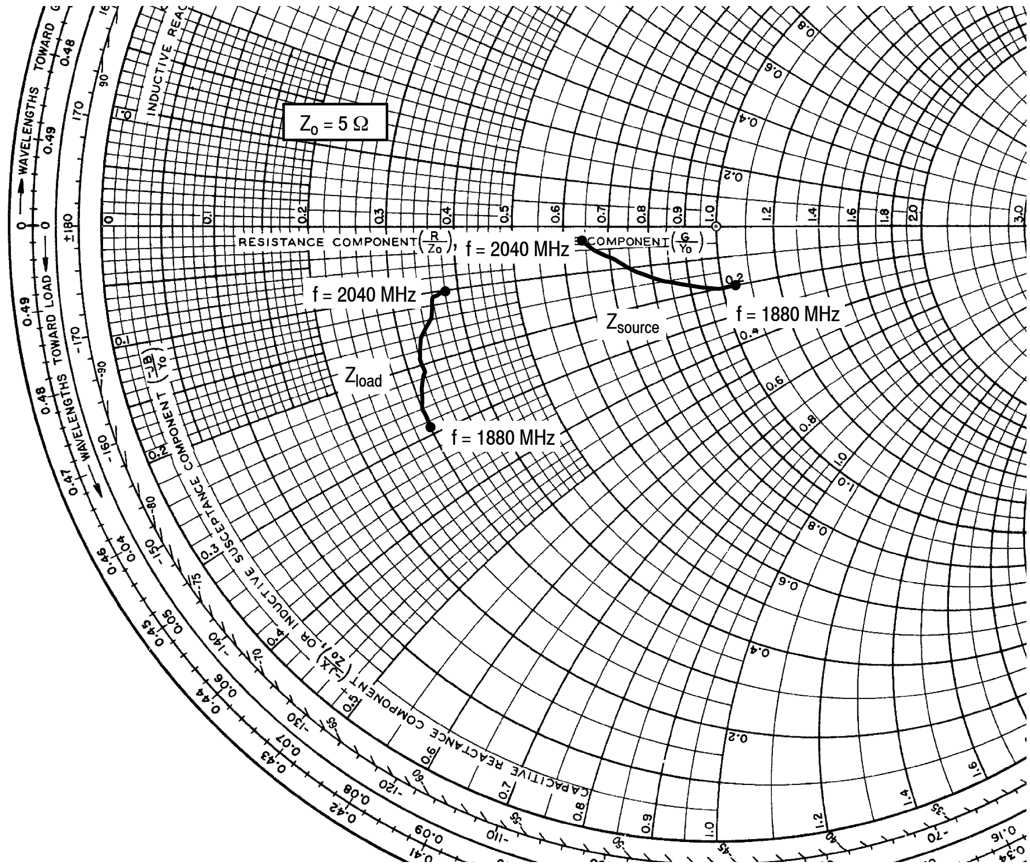


Figure 10. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 63 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1880	5.20 - j1.02	1.49 - j1.45
1900	4.90 - j1.00	1.52 - j1.30
1920	4.60 - j0.92	1.55 - j1.16
1940	4.31 - j0.82	1.58 - j1.04
1960	4.04 - j0.71	1.61 - j0.93
1980	3.80 - j0.56	1.66 - j0.82
2000	3.58 - j0.42	1.73 - j0.70
2020	3.38 - j0.30	1.81 - j0.57
2040	3.19 - j0.16	1.88 - j0.49

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

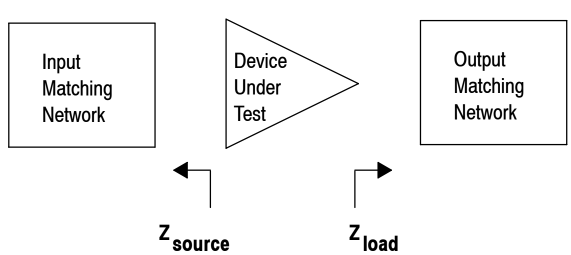
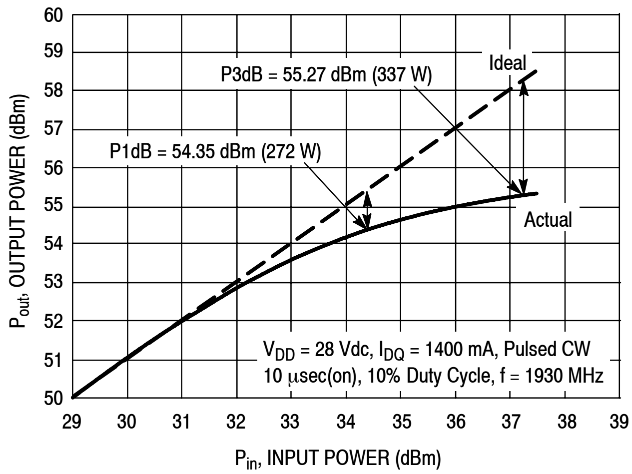


Figure 11. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

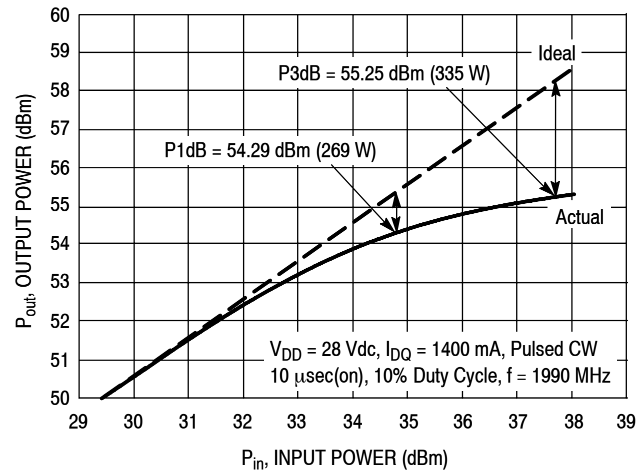


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	5.72 – j5.51	1.30 – j0.69

Figure 12. Pulsed CW Output Power versus Input Power @ 28 V @ 1930 MHz



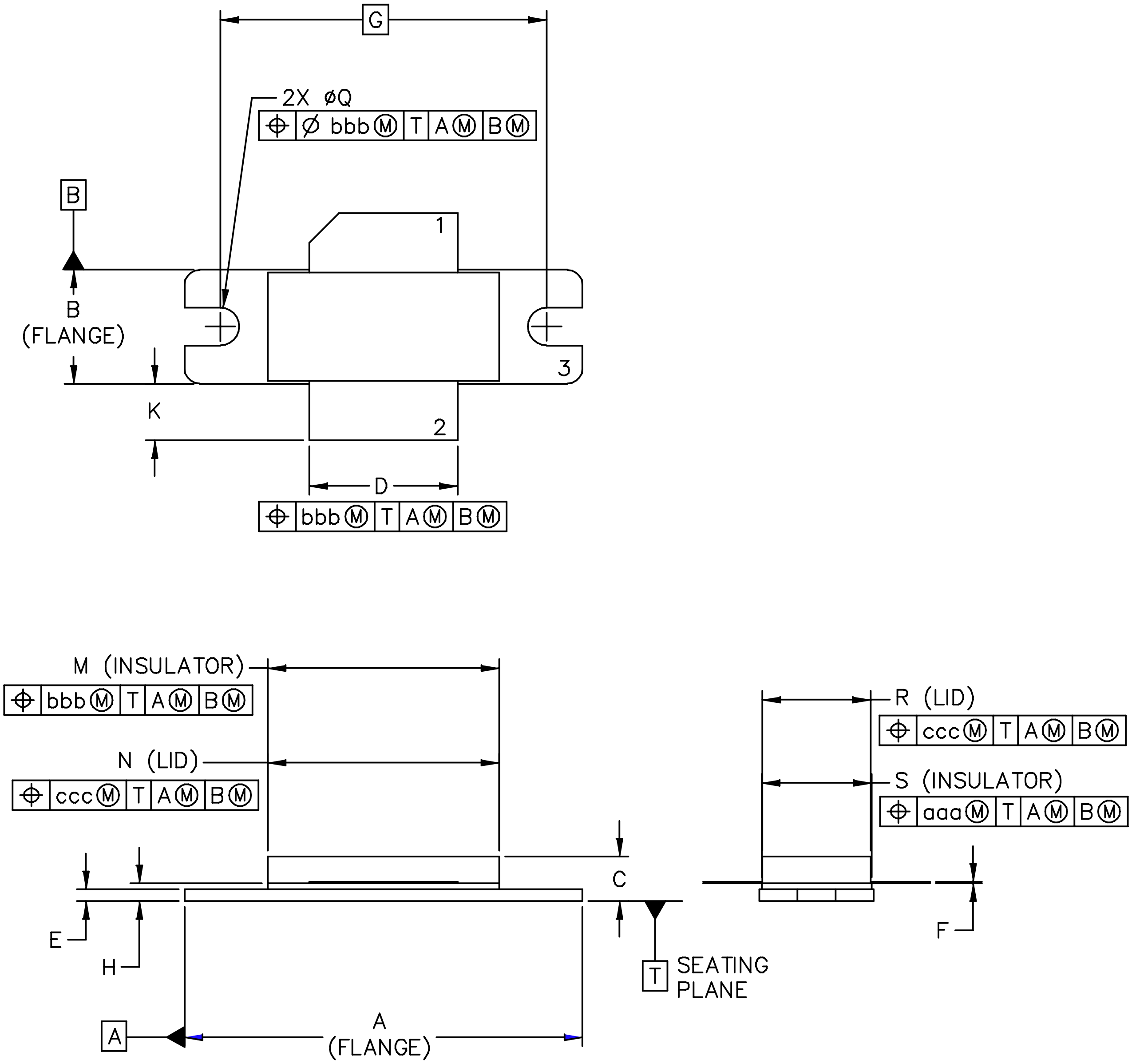
NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	6.20 + j1.19	1.09 – j046

Figure 13. Pulsed CW Output Power versus Input Power @ 28 V @ 1990 MHz

PACKAGE DIMENSIONS



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	CASE NUMBER: 465–06	31 MAR 2005
	STANDARD: NON–JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M—1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX	DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX
A	1.335	–	1.345	33.91	–	34.16	R	.365	–	.375	9.27	–	9.53
B	.380	–	.390	9.65	–	9.91	S	.365	–	.375	9.27	–	9.52
C	.125	–	.170	3.18	–	4.32	aaa	–	.005	–	–	0.127	–
D	.495	–	.505	12.57	–	12.83	bbb	–	.010	–	–	0.254	–
E	.035	–	.045	0.89	–	1.14	ccc	–	.015	–	–	0.381	–
F	.003	–	.006	0.08	–	0.15	–	–	–	–	–	–	–
G	1.100 BSC			27.94 BSC			–	–	–	–	–	–	–
H	.057	–	.067	1.45	–	1.7	–	–	–	–	–	–	–
K	.170	–	.210	4.32	–	5.33	–	–	–	–	–	–	–
M	.774	–	.786	19.66	–	19.96	–	–	–	–	–	–	–
N	.772	–	.788	19.6	–	20	–	–	–	–	–	–	–
Q	ø.118	–	ø.138	ø3	–	ø3.51	–	–	–	–	–	–	–

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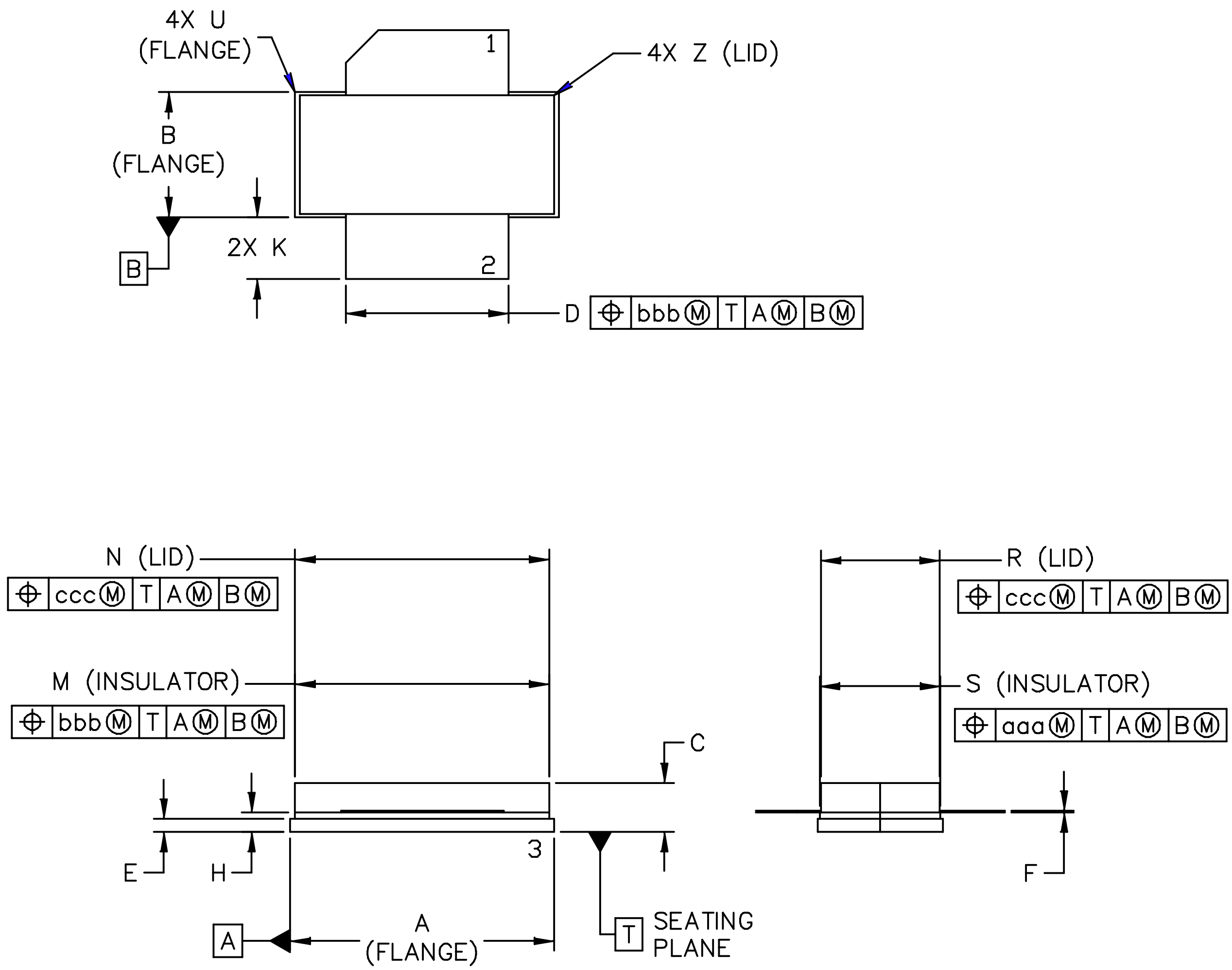

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STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX	DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX
A	.805	–	.815	20.45	–	20.7	U	–	–	.040	–	–	1.02
B	.380	–	.390	9.65	–	9.91	Z	–	–	.030	–	–	0.76
C	.125	–	.170	3.18	–	4.32	aaa	–	.005	–	–	0.127	–
D	.495	–	.505	12.57	–	12.83	bbb	–	.010	–	–	0.254	–
E	.035	–	.045	0.89	–	1.14	ccc	–	.015	–	–	0.381	–
F	.003	–	.006	0.08	–	0.15	–	–	–	–	–	–	–
H	.057	–	.067	1.45	–	1.7	–	–	–	–	–	–	–
K	.170	–	.210	4.32	–	5.33	–	–	–	–	–	–	–
M	.774	–	.786	19.61	–	20.02	–	–	–	–	–	–	–
N	.772	–	.788	19.61	–	20.02	–	–	–	–	–	–	–
R	.365	–	.375	9.27	–	9.53	–	–	–	–	–	–	–
S	.365	–	.375	9.27	–	9.52	–	–	–	–	–	–	–

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PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2008	• Initial Release of Data Sheet
1	Mar. 2011	• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13628, p. 1, 2 • Fig. 9, MTTF versus Junction Temperature removed, p. 7. Refer to the device’s MTTF Calculator available at freescale.com/RFpower. Go to Design Resources > Software and Tools. • Fig. 10, CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal and Fig. 11, Single-Carrier W-CDMA Spectrum updated to show the undistorted input test signal, p. 8 (renumbered as Figs. 9 and 10 respectively after Fig. 9 removed) • Added Electromigration MTTF Calculator and RF High Power Model availability to Product Software, p. 15

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