Monolithic 4A High Voltage 2-Cell Li-Ion Battery Charger

FEATURES

- **Wide Input Voltage Range: 9V to 32V (40V Absolute Maximum)**
- **Programmable Charge Current Up to 4A**
- **Selectable C/10 or Onboard Timer Termination**
- **Dynamic Charge Rate Programming/Soft-Start**
- **Programmable Input Current Limit**
- ±0.5% Float Voltage Accuracy
- ±7.5% Charge Current Accuracy
- ±4% C/10 Detection Accuracy
- NTC Resistor Temperature Monitor
- Auto-Recharge at 97.5% Float Voltage
- Auto-Precondition at <70% Float Voltage
- Bad Battery Detection with Auto-Reset
- Average Current Mode, Synchronous Switcher
- User Programmable Frequency
- Low Profile (0.75mm) 5mm × 6mm 36-Lead QFN Package

APPLICATIONS

- Industrial Handheld Instruments
- 12V to 24V Automotive and Heavy Equipment
- Desktop Cradle Chargers
- Notebook Computers

DESCRIPTION

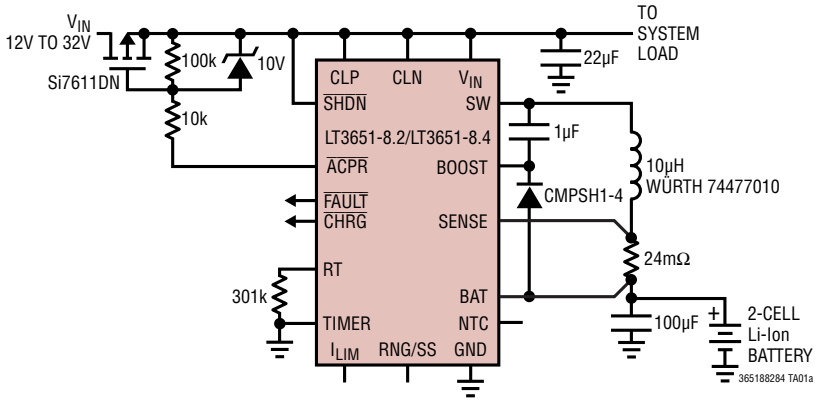
The LT®3651-8.2/LT3651-8.4 are 2-cell, 4A Li-Ion/Polymer battery chargers that operate over a 9V to 32V input voltage range. An efficient monolithic average current mode synchronous switching regulator provides constant current, constant voltage charging with programmable maximum charge current. A charging cycle starts with battery insertion or when the battery voltage drops 2.5% below the float voltage. Charger termination is selectable as either charge current or internal safety timer timeout. Charge current termination occurs when the charge current falls to one-tenth the programmed maximum current (C/10). Timer based termination is typically set to three hours and is user programmable (charging continues below C/10 until timeout). Once charging is terminated, the LT3651-8.2/LT3651-8.4 supply current drops to 85µA into a standby mode.

The LT3651-8.2/LT3651-8.4 offer several safety features. A discharged battery is preconditioned with a small trickle charge and generates a signal if unresponsive. A thermistor monitors battery temperature, halting charging if out of range. Excessive die temperature reduces charge current. Charge current is also reduced to maintain constant input current to prevent excessive input loading.

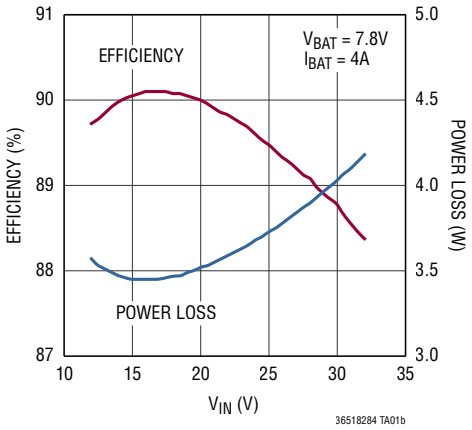
The LT3651-8.2/LT3651-8.4 are available in a 5mm × 6mm 36-lead QFN package.

TYPICAL APPLICATION

12V to 32V 2-Cell 4A Charger



Efficiency, Power Loss vs V_{IN}

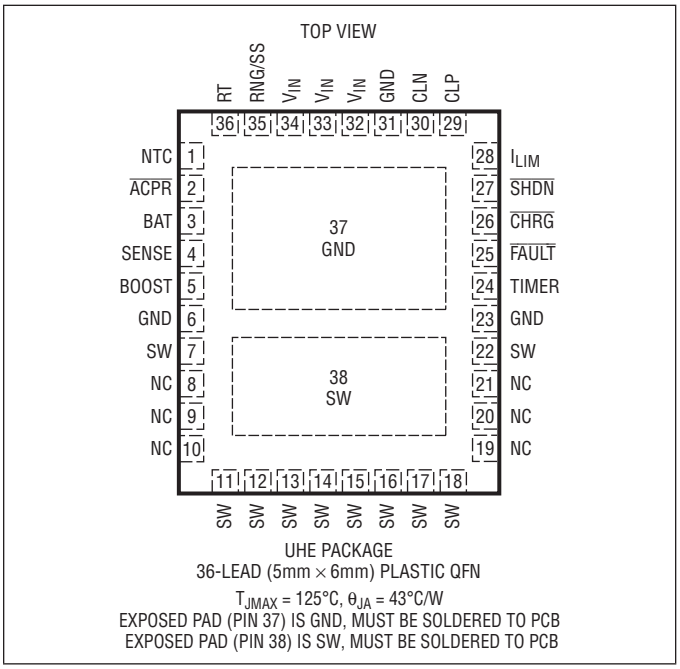


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 40V
CLN, CLP, $\overline{SHDN}$, $\overline{CHRG}$,
$\overline{FAULT}$, $\overline{ACPR}$ ..... V_{IN} + 0.5V Up to 40V
CLP – CLN .....±0.5V
SW 40V
SW – V_{IN}.....4.5V
BOOST ..... SW + 10V Up to 50V
SENSE, BAT 10V
SENSE-BAT ..... –0.5V to 0.5V
TIMER, RNG/SS, I_{LIM}, NTC, RT 2.5V
Operating Junction Temperature Range
(Notes 2, 3).....–40 to 125°C
Storage Temperature Range .....–65 to 150°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 37) IS GND, MUST BE SOLDERED TO PCB
EXPOSED PAD (PIN 38) IS SW, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3651EUHE-8.2#PBF	LT3651EUHE-8.2#TRPBF	365182	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3651IUHE-8.2#PBF	LT3651IUHE-8.2#TRPBF	365182	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3651EUHE-8.4#PBF	LT3651EUHE-8.4#TRPBF	365184	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LT3651IUHE-8.4#PBF	LT3651IUHE-8.4#TRPBF	365184	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 20V, $\overline{SHDN}$ = 2V, SENSE = BAT = $V_{BAT(FLT)}$, C_{TIMER} = 0.68µF, R_T = 50k, CLP = CLN = V_{IN}, BOOST – SW = 4V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Range		●	9.0		32	V
V_{IN} OVLO Threshold	V_{IN} Rising		32	35	40	V
V_{IN} OVLO Hysteresis				1.1		V
V_{IN} UVLO Threshold	V_{IN} Rising	●		8.7	9.0	V
V_{IN} UVLO Hysteresis				0.2		V
Battery Float Voltage, $V_{BAT(FLT)}$	LT3651-8.2	 ●	8.16 8.12	8.2	8.24 8.28	V V
	LT3651-8.4	 ●	8.36 8.32	8.4	8.44 8.48	V V
Battery Recharge Voltage Hysteresis	Threshold Voltage Relative to $V_{BAT(FLT)}$			–200		mV
Battery Precondition Threshold Voltage, $V_{BAT(PRE)}$	LT3651-8.2, V_{BAT} Rising LT3651-8.4, V_{BAT} Rising			5.65 5.80		V V
Battery Precondition Threshold Hysteresis	Threshold Voltage Relative to $V_{BAT(PRE)}$			90		mV
Operating V_{IN} Supply Current	CC/CV Mode, Top Switch On, I_{SW} = 0 Standby Mode Shutdown ($\overline{SHDN}$ = 0)			8.6 80 17		mA µA µA
Top Switch On Voltage	$V_{IN} – V_{SW}$, I_{SW} = 4A			480		mV
Bottom Switch On Voltage	V_{SW}, I_{SW} = 4A			–140		mV
BOOST Supply Current	Switch High, I_{SW} = 0, 2.5V < ($V_{BOOST} – V_{SW}$) < 8.5V			17		mA
BOOST Switch Drive	I_{BOOST}/I_{SW}, I_{SW} = 4A			22		mA/A
Precondition Current Sense Voltage	$V_{SENSE} – V_{BAT}$, V_{BAT} = 5.0V			14		mV
Input Current Limit Voltage	$V_{CLP} – V_{CLN}$, I_{LIM} Open	●	70	95	115	mV
CLP Input Bias Current				120		nA
CLN Input Bias Current				36		µA
I_{LIM} Bias Current		●	43	50	57	µA
System Current Limit Programming Gain	$V_{ILIM}/(V_{CLP} – V_{CLN})$, V_{ILIM} = 0.5V			11.5		V/V
Maximum Charge Current Sense Voltage	$V_{SENSE} – V_{BAT}$, V_{BAT} = 7.5V, $V_{RNG/SS}$ > 1.1V	●	88	95	103	mV
C/10 Trigger Sense Voltage	$V_{SENSE} – V_{BAT}$	●	4.5	8.6	12.3	mV
BAT Input Bias Current	Charging Terminated			0.1	1	µA
SENSE Input Bias Current	Charging Terminated			0.1	1	µA
RNG/SS Bias Current		●	44	50	56	µA
Charge Current Limit Programming Gain	$V_{RNG/SS}/(V_{SENSE} – V_{BAT})$, $V_{RNG/SS}$ = 0.5V	●	8.5	10.8	12.5	V/V
NTC Range Limit (High)	V_{NTC} Rising	●	1.25	1.36	1.45	V
NTC Range Limit (Low)	V_{NTC} Falling	●	0.27	0.29	0.31	V
NTC Threshold Hysteresis	% of Threshold			10		%
NTC Disable Impedance	Minimum External Impedance to GND	●	150	470		kΩ
NTC Bias Current	V_{NTC} = 0.75V	●	46.5	50	53.5	µA
Shutdown Threshold	$V_{\overline{SHDN}}$ Rising	●	1.15	1.20	1.23	V
Shutdown Hysteresis				95		mV
$\overline{SHDN}$ Input Bias Current				–10		nA
Status Low Voltage	$V_{\overline{CHRG}}$, $V_{\overline{FAULT}}$, $V_{\overline{ACPR}}$, Load = 10mA	●			0.45	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 20V, $\overline{SHDN}$ = 2V, SENSE = BAT = $V_{BAT(FLT)}$, C_{TIMER} = 0.68µF, R_T = 50k, CLP = CLN = V_{IN}, BOOST – SW = 4V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TIMER Charge/Discharge Current				25		µA
TIMER Disable Threshold		●	0.1	0.25		V
Full Charge Cycle Time-Out				3		Hour
Precondition Timeout				22.5		Minute
Timer Accuracy		●	–13		13	%
Switcher Operating Frequency, f_O	R_T = 50kΩ R_T = 250kΩ			1.1 250		MHz kHz
Minimum SW On-Time, $t_{ON(MIN)}$				150		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3651-8.2/LT3651-8.4 are tested under pulse loaded conditions such that $T_J = T_A$. The LT3651-8.2E/LT3651-8.4E are guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3651-8.2I/LT3651-8.4I are guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

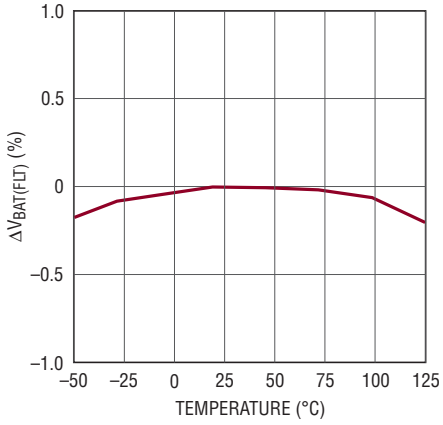
$$T_J = T_A + P_D \bullet \theta_{JA}$$

where θ_{JA} (in °C/W) is the package thermal impedance.

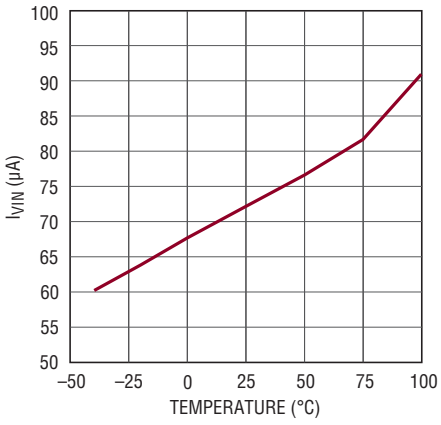
Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

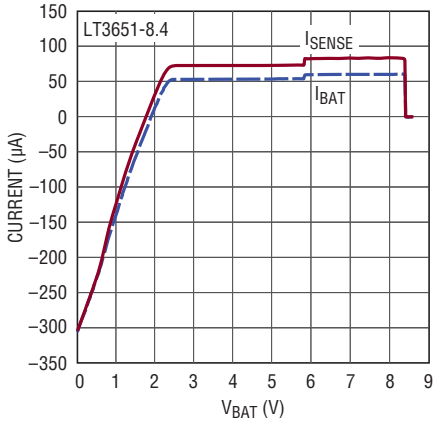
Battery Float Voltage vs Temperature



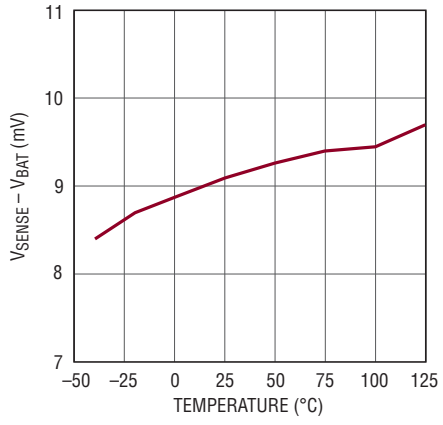
V_{IN} Standby Mode Current vs Temperature



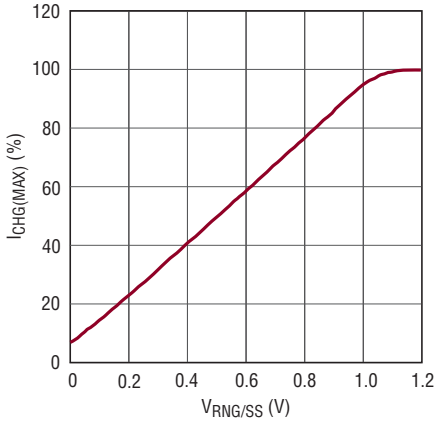
SENSE and BAT Pin Currents vs BAT Voltage (V_{SENSE} = V_{BAT})



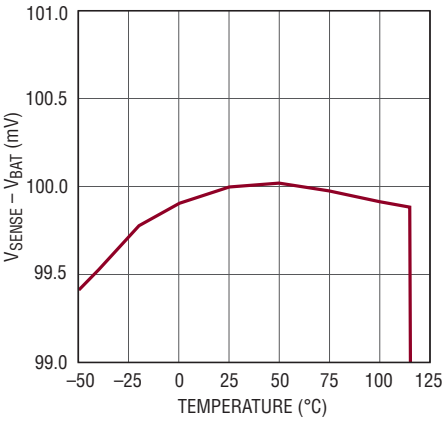
C/10 Threshold (V_{SENSE} – V_{BAT}) vs Temperature



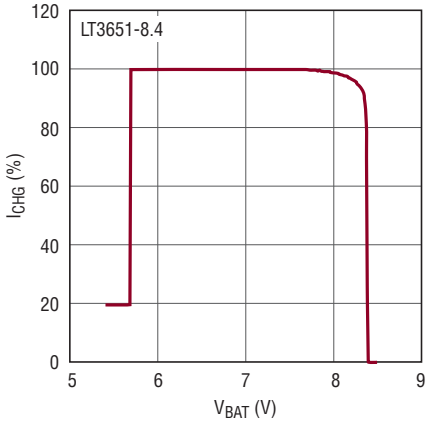
Maximum Charge Current vs $V_{RNG/SS}$ as a Percentage of Programmed $I_{IN(MAX)}$



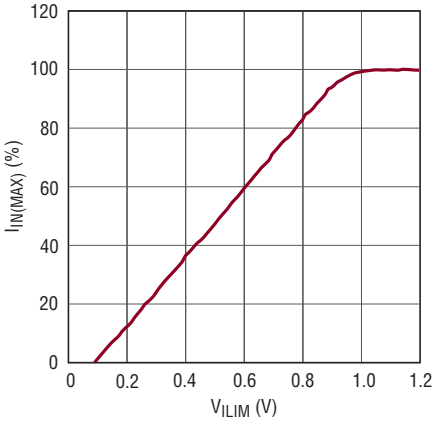
I_{CHG} Current Limit (V_{SENSE} – V_{BAT}) vs Temperature



Charge Current vs V_{BAT} as a Percentage of Programmed $I_{CHG(MAX)}$

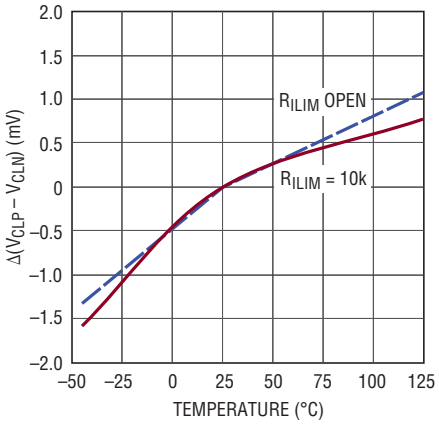


Maximum Input Current vs V_{ILIM} as a Percentage of Programmed $I_{IN(MAX)}$

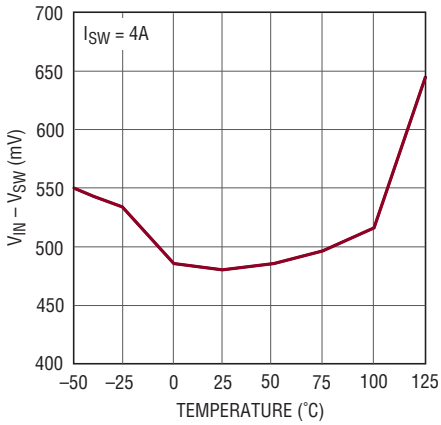


TYPICAL PERFORMANCE CHARACTERISTICS

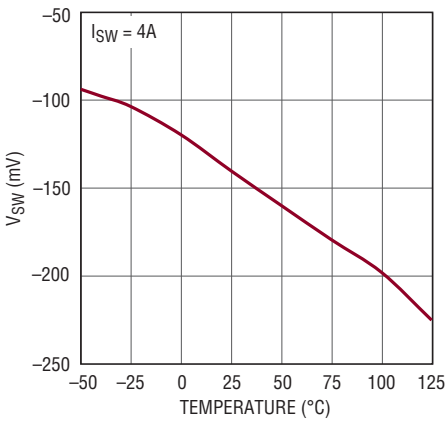
Input Current Limit Voltage Threshold vs Temperature



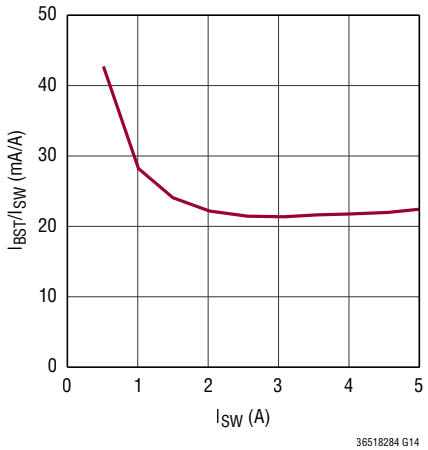
Topside Switch V_{ON} vs Temperature



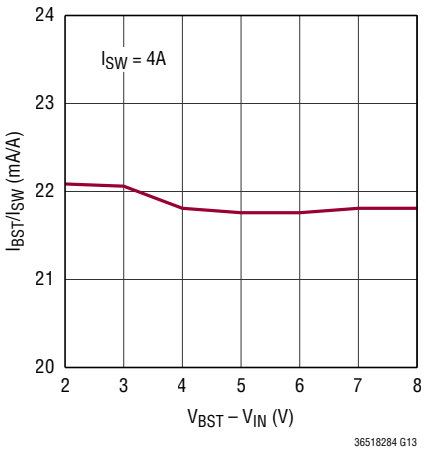
Bottom Side Switch V_{ON} vs Temperature



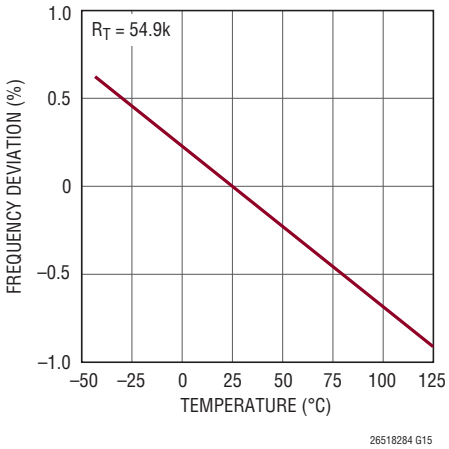
Boost Drive vs Switch Current



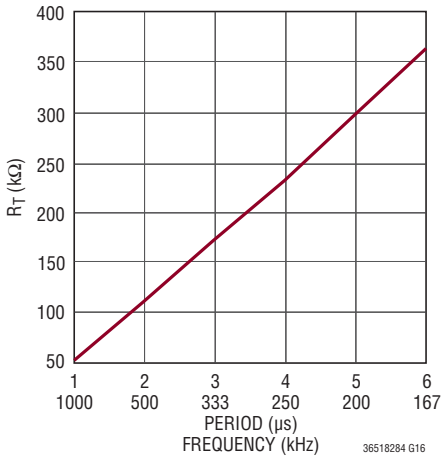
Boost Drive vs Boost Voltage



Oscillator Frequency vs Temperature



Timer Resistor (R_T) vs Period and Frequency



PIN FUNCTIONS

NTC (Pin 1): Battery Temperature Monitor Pin. This pin is used to monitor battery temperature. Typically a 10kΩ NTC (negative temperature coefficient) thermistor (B = 3380) is embedded with the battery and connected from the NTC pin to ground. The pin sources 50µA into the resistor and monitors the voltage across the thermistor, regulating charging based on the voltage. If this function is not desired, leave the NTC pin unconnected.

$\overline{\text{ACPR}}$ (Pin 2): Open-Collector AC Present Status Pin. This pin sinks current to indicate that V_{IN} is valid and the charger is on. Typically a resistor pull-up is used on this pin. This pin can be pulled up to voltages as high as V_{IN} when disabled, and can sink currents up to 10mA when enabled.

BAT (Pin 3): Battery Voltage Monitor Pin. This pin monitors battery voltage. A Kelvin connection is made to the battery from this pin and a decoupling capacitor (C_{BAT}) is placed from this pin to ground.

The charge function operates to achieve the final float voltage at this pin. The auto-restart feature initiates a new charging cycle when the voltage at the BAT pin falls 2.5% below this float voltage. Once the charge cycle is terminated, the input bias current of the BAT pin is reduced to <0.1µA to minimize battery discharge while the charger remains connected.

SENSE (Pin 4): Charge Current Sense Pin. The charge current is monitored with a sense resistor (R_{SENSE}) connected between this pin and the BAT pin. The inductor current flows through R_{SENSE} to the battery. The voltage across this resistor sets the average charge current. The maximum average charge current (I_{MAX}) corresponds to 95mV across the sense resistor.

BOOST (Pin 5): Bootstrapped Supply Rail for Switch Drive. This pin facilitates saturation of the high side switch transistor. Connect a 1µF or greater capacitor from the BOOST pin to the SW pin. The operating range of this pin is 0V to 8.5V, referenced to the SW pin when the switch is high. The voltage on the decoupling capacitor is refreshed through a rectifying diode, with the anode connected to either the battery output voltage or an external source, and the cathode connected to the BOOST pin.

GND (Pins 6, 23, 31, 37): Ground. These pins are the ground pins for the part. Pins 31 and 37 must be connected together. Pins 6 and 23 are connected via the leadframe to the exposed backside Pin 37. Solder the exposed backside to the PCB for good thermal and electrical connection.

SW (Pins 7, 11-18, 22, 38): Switch Output Pin. These pins are the output of the charger switches. An inductor is connected between these pins and the SENSE pin. When the switcher is active, the inductor is charged by the high side switch from V_{IN} and discharged by the bottom side switch to GND. Solder the exposed backside, Pin 38, to the PCB for good thermal connection.

NC (Pins 8-10,19-21): No Connect. These pins can be left floating (not connected).

TIMER (Pin 24): End-Of-Cycle Timer Programming Pin. A capacitor on this pin to ground determines the full charge end-of-cycle time. Full charge end-of-cycle time is programmed with this capacitor. A 3 hour charge cycle is obtained with a 0.68µF capacitor. This timer also controls the bad battery fault that is generated if the battery does not reach the precondition threshold voltage within one-eighth of a full cycle (22.5 minutes for a 3 hour charge cycle).

The timer based termination is disabled by connecting the TIMER pin to ground. With the timer function disabled, charging terminates when the charge current drops below a C/10 rate, or approximately 10% of maximum charge rate.

$\overline{\text{FAULT}}$ (Pin 25): Open-Collector Fault Status Output. This pin indicates charge cycle fault conditions during a battery charging cycle. Typically a resistor pull-up is used on this pin. This status pin can be pulled up to voltages as high as V_{IN} when disabled, and can sink currents up to 10mA when enabled. A temperature fault causes this pin to be pulled low. If the internal timer is used for termination, a bad battery fault also causes this pin to be pulled low. If no fault conditions exist, the $\overline{\text{FAULT}}$ pin remains high impedance.

$\overline{\text{CHRG}}$ (Pin 26): Open-Collector Charger Status Output. This pin indicates the battery charging status. Typically a resistor pull-up is used on this pin. This status pin can be pulled up to voltages as high as V_{IN} when disabled,

PIN FUNCTIONS

and can sink currents up to 10mA when enabled. $\overline{CHRG}$ is pulled low during a battery charging cycle. When the charge cycle is terminated, the $\overline{CHRG}$ pin becomes high impedance. If the internal timer is used for termination, the pin stays low during the charging cycle until the charge current drops below a C/10 rate, or approximately 10% of the maximum charge current. A temperature fault also causes this pin to be pulled low.

$\overline{SHDN}$ (Pin 27): Shutdown Pin. This pin can be used for precision UVLO functions. When this pin rises above the 1.20V threshold, the part is enabled. The pin has 95mV of voltage hysteresis. When in shutdown mode, all charging functions are disabled. When the $\overline{SHDN}$ pin is pulled below 0.4V, the IC enters a low current shutdown mode where the V_{IN} pin current is reduced to 17µA. Typical $\overline{SHDN}$ pin input bias current is 10nA. Connect the pin to V_{IN} if the shutdown function is not desired.

I_{LIM} (Pin 28): Input Current Limit Programming. This pin allows for setting and dynamic adjustment of the system input current limit, and can be used to employ a soft-start function. The voltage on this pin sets the maximum input current by setting the maximum voltage across the input current sense resistor, placed between CLP and CLN.

The effective range on the pin is 0V to 1V. 50µA is sourced from this pin usually to a resistor (R_{ILIM}) to ground. V_{IILIM} represents approximately 11 times the maximum voltage across the input current sense resistor. If no R_{ILIM} is used the part will default to maximum input current.

Soft-start functionality for input current can be implemented with a capacitor (C_{ILIM}) from I_{LIM} to ground. The soft-start capacitor and the programming resistor can be implemented in parallel.

CLP/CLN (Pin 29/Pin 30): System Current Limit Positive and Negative Input. System current levels are monitored by connecting a sense resistor from the input power supply to the CLP pin, connecting a sense resistor from the CLP pin to the CLN pin and then connecting CLN to V_{IN}. The system load is then delivered from the CLN pin. The LT3651-8.2/LT3651-8.4 servo the maximum charge current required to maintain programmed maximum system current. The system current limit is set as a function of the voltage on the I_{LIM} pin and the input current sense resistor. This function is disabled by shorting CLP, CLN and V_{IN} together.

V_{IN} (Pins 32, 33, 34): Charger Input Supply. These pins provide power for the LT3651-8.2/LT3651-8.4. Charge current for the battery flows into these pins. I_{VIN} is less than 100µA after charge termination. Connect the pins together.

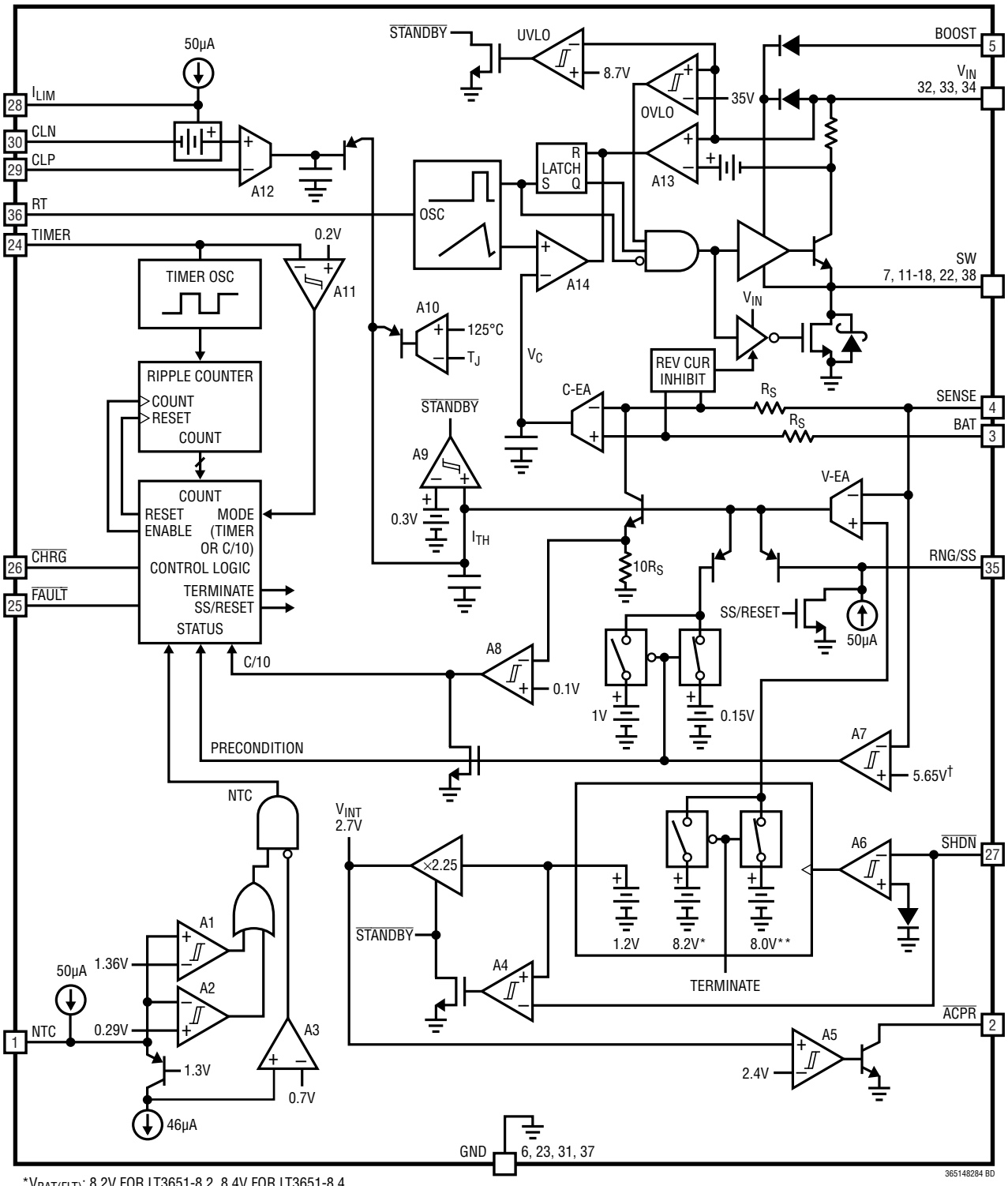
RNG/SS (Pin 35): Charge Current Range and Soft-Start Pin. This pin allows for setting and dynamic adjustment of the maximum charge current, and can be used to employ a soft-start function. The voltage on this pin sets the maximum charge current by setting the maximum voltage across the charge current sense resistor, R_{SENSE}, placed between SENSE and BAT.

The effective range on the pin is 0V to 1V. 50µA is sourced from this pin usually to a resistor ($R_{RNG/SS}$) to ground. $V_{RNG/SS}$ represents approximately 10 times the maximum voltage across the charge current sense resistor. If no $R_{RNG/SS}$ is used the part will default to maximum charge current.

Soft-start functionality for charge current can be implemented by connecting a capacitor ($C_{RNG/SS}$) from RNG/SS to ground. The soft-start capacitor and the programming resistor can be implemented in parallel. The RNG/SS pin is pulled low during fault conditions, allowing graceful recovery from faults if $C_{RNG/SS}$ is used.

RT (Pin 36): Switcher Oscillator Timer Set Pin. A resistor from this pin to ground sets the switcher oscillator frequency. Typically this is 54.9k for f_{OSC} = 1MHz.

BLOCK DIAGRAM



*$V_{BAT(FLT)}$: 8.2V FOR LT3651-8.2, 8.4V FOR LT3651-8.4
**$V_{BAT(FLT)} - \Delta V_{RECHRG}$: 8V FOR LT3651-8.2, 8.2V FOR LT3651-8.4
†$V_{BAT(PRE)}$: 5.65V FOR LT3651-8.2, 5.8V FOR LT3651-8.4

OPERATION

Overview

The LT3651-8.2/LT3651-8.4 are complete Li-Ion battery chargers, addressing wide input voltage and high currents (up to 4A). High charging efficiency is produced with a constant frequency, average current mode synchronous step-down switcher architecture.

The charger includes the necessary circuitry to allow for programming and control of constant current, constant voltage (CC/CV) charging with both current only and timer termination. High charging efficiency is achieved by the switcher by using a bootstrapped supply for low switch drop for the high side driver and a MOSFET for the low side (synchronous) switch.

Maximum charge current is set with an external sense resistor in series with the inductor and is adjustable through the RNG/SS pin. Total system input current is monitored with an input sense resistor and is used to maintain constant input current by regulating battery charge current. It is adjustable through the I_{LIM} pin.

If the battery voltage is low, charge current is automatically reduced to 15% of the programmed current to provide safe battery preconditioning. Once the battery voltage climbs above the battery precondition threshold, the IC automatically increases the maximum charge current to the full programmed value.

Charge termination can occur when charge current decreases to one-tenth the programmed maximum charge current (C/10 termination). Alternately, termination can be time based through the use of an internal programmable charge cycle control timer. When using the timer termination, charging continues beyond the C/10 level to "top-off" a battery. Charging typically terminates three hours after initiation. When the timer-based scheme is used, bad battery detection is also supported. A system fault is triggered if a battery stays in precondition mode for more than one-eighth of the total charge cycle time.

Once charging is terminated and the LT3651-8.2/LT3651-8.4 are not actively charging, the IC automatically enters a low current standby mode in which supply bias currents are reduced to <85µA. If the battery voltage drops 2.5% from the full charge float voltage, the LT3651-8.2/LT3651-8.4 engage an automatic charge cycle restart. The IC also automatically restarts a new charge cycle after a bad battery fault once the failed battery is removed and replaced with another battery.

After charging is completed the input bias currents on the pins connecting to the battery are reduced to minimize battery discharge.

The LT3651-8.2/LT3651-8.4 contain provisions for a battery temperature monitoring circuit. Battery temperature is monitored by using a NTC thermistor located with the battery. If the battery temperature moves outside a safe charging range of 0°C to 40°C the charging cycle suspends and signals a fault condition.

The LT3651-8.2/LT3651-8.4 contain two digital open-collector outputs, which provide charger status and signal fault conditions. These binary coded pins signal battery charging, standby or shutdown modes, battery temperature faults and bad battery faults.

A precision undervoltage lockout is possible by using a resistor divider on the shutdown pin ($\overline{SHDN}$). The input supply current is 17µA when the IC is in shutdown.

General Operation (See Block Diagram)

The LT3651-8.2/LT3651-8.4 use an average current mode control loop architecture to control average charge current. The LT3651-8.2/LT3651-8.4 sense charger output voltage via the BAT pin. The difference between this voltage and the internal float voltage reference is integrated by the voltage error amplifier (V-EA). The amplifier output voltage (I_{TH}) corresponds to the desired average voltage across the inductor sense resistor, R_{SENSE}, connected between the SENSE and BAT pins. The I_{TH} voltage is divided down by a factor of 10, and provides a voltage offset on the input of the current error amplifier (C-EA). The difference between this imposed voltage and the current sense resistor voltage is integrated by C-EA. The resulting voltage (V_C) provides a voltage that is compared against an internally generated ramp and generates the switch duty cycle that controls the charger's switches.

OPERATION

The I_{TH} error voltage corresponds linearly to average current sensed across the inductor current sense resistor. Maximum charge current is controlled by clamping the maximum voltage of I_{TH} to 1V. This limits the maximum current sense voltage (voltage across R_{SENSE}) to 95mV setting the maximum charge current. Manipulation of maximum charge current is possible through the RNG/SS and I_{LIM} pins (see the RNG/SS: Dynamic Charge Current Adjust, RNG/SS: Soft-Start and I_{LIM} Control sections).

If the voltage on the BAT pin (V_{BAT}) is below $V_{BAT(PRE)}$, A7 initiates the precondition mode. During the precondition interval, the charger continues to operate in constant current mode, but the I_{TH} clamp is reduced to 0.15V reducing charge current to 15% of the maximum programmed value.

As V_{BAT} approaches the float voltage (V_{FLOAT}) the voltage error amp V-EA takes control of I_{TH} and the charger transitions into constant voltage (CV) mode. As this occurs, the I_{TH} voltage falls from the limit clamp and charge current is reduced from the maximum value. When the I_{TH} voltage falls below 0.1V, A8 signals C/10. If the charger is configured for C/10 termination the charge cycle is terminated. Once the charge cycle is terminated, the $\overline{CHRG}$ status pin becomes high impedance and the charger enters low current standby mode.

The LT3651-8.2/LT3651-8.4 contain an internal charge cycle timer that terminates a successful charge cycle after a programmed amount of time. This timer is typically programmed to achieve end-of-cycle in three hours, but can be configured for any amount of time by setting an appropriate timing capacitor value (C_{TIMER}). When timer termination is used, the charge cycle does not terminate after C/10 is achieved. Because the $\overline{CHRG}$ status pin responds to the C/10 current level, the IC will indicate a fully charged battery status, but the charger will continue to source low currents. At the programmed end of the cycle time the charge cycle stops and the part enters standby mode. If the battery did not achieve at least 97.5% of the full float voltage at the end-of-cycle, charging is deemed unsuccessful and another full-timer cycle is initiated.

Use of the timer function also enables bad battery detection. This fault condition is achieved if the battery does not respond to preconditioning and the charger remains in (or enters) precondition mode after one-eighth of the programmed charge cycle time. A bad battery fault halts the charging cycle, the $\overline{CHRG}$ status pin goes high impedance and the $\overline{FAULT}$ pin is pulled low.

When the LT3651-8.2/LT3651-8.4 terminate a charging cycle, whether through C/10 detection or by reaching timer end-of-cycle, the average current mode analog loop remains active but the internal float voltage reference is reduced by 2.5%. Because the voltage on a successfully charged battery is at the full float voltage, the voltage error amp detects an overvoltage condition and rails low. When the voltage error amp output drops below 0.3V, the IC enters standby mode, where most of the internal circuitry is disabled and the V_{IN} bias current is reduced to <100µA. When the voltage on the BAT pin drops below the reduced float reference level, the output of the voltage error amp will climb, at which point the IC comes out of standby mode and a new charging cycle is initiated.

The system current limit allows charge current to be reduced in order to maintain a constant input current. Input current is measured via a resistor (R_{CL}) that is placed between the CLP and CLN pins. Power is applied through this resistor and is used to supply both V_{IN} of the chip and other system loads. An offset produced on the inputs of A12 sets the threshold. When that threshold is achieved, I_{TH} is reduced, lowering the charge current thus maintaining the maximum input current.

50µA of current is sourced from I_{LIM} to a resistor (R_{ILIM}) that is placed from that pin to ground. The voltage on I_{LIM} determines the regulating voltage across R_{CL}. 1V on I_{LIM} corresponds to 95mV across R_{CL}. The I_{LIM} pin clamps internally to 1V maximum.

If the junction temperature of the die becomes excessive, A10 activates decreasing I_{TH} and reduces charge current. This reduces on-chip power dissipation to safe levels but continues charging.

APPLICATIONS INFORMATION

OSC Frequency

A precision resistor to ground sets the LT3651-8.2/LT3651-8.4 switcher oscillator frequency, f_{OSC}, permitting user adjustability of the frequency value. Typically this frequency is in the 200kHz to 1MHz range. Power consideration may necessitate lower frequency operation especially if the charger is operated with very high voltages. Adjustability also allows the user to position switching harmonics if their system requires.

The timing resistor, R_T, value is set by the following:

$$R_T = \frac{54.9}{f_{OSC}(MHz)}(k\Omega)$$

Set R_T to 54.9k for 1MHz operation.

V_{IN} Input Supply

The LT3651-8.2/LT3651-8.4 are biased directly from the charger input supply through the V_{IN} pin. This supply provides large switched currents, so a high quality, low ESR decoupling capacitor is required to minimize voltage glitches on V_{IN}. The V_{IN} decoupling capacitor (C_{VIN}) absorbs all input switching ripple current in the charger. Size is determined by input ripple voltage with the following equation:

$$C_{IN(BULK)} \frac{I_{CHG(MAX)} \bullet V_{BAT}}{f_{OSC}(MHz) \bullet \Delta V_{IN} \bullet V_{IN}}(\mu F)$$

where ΔV_{IN} is the input ripple, $I_{CHG(MAX)}$ is the maximum charge current and f is the oscillator frequency. A good starting point for ΔV_{IN} is 0.1V. Worst-case conditions are with V_{BAT} high and V_{IN} at minimum. So for a 15V $V_{IN(MIN)}$, I_{MAX} = 4A and a 1MHz oscillator frequency:

$$C_{IN(BULK)} = \frac{4 \bullet 8.2}{1 \bullet 0.1 \bullet 15} = 22\mu F$$

The capacitor must have an adequate ripple current rating. RMS ripple current, $I_{CVIN(RMS)}$ is approximated by:

$$I_{CVIN(RMS)} \approx I_{CHG(MAX)} \bullet \left(\frac{V_{BAT}}{V_{IN}}\right) \bullet \sqrt{\frac{V_{IN}}{V_{BAT}} - 1}$$

which has a maximum at $V_{IN} = 2 \bullet V_{BAT}$, where $I_{CVIN(RMS)} = I_{CHG(MAX)}/2$. In the example above that requires a capacitor RMS rating of 2A.

Boost Supply

The BOOST bootstrapped supply rail drives the internal switch and facilitates saturation of the high side switch transistor. The BOOST voltage is normally created by connecting a 1µF capacitor from the BOOST pin to the SW pin. Operating range of the BOOST pin is 2V to 8.5V, as referenced to the SW pin.

The boost capacitor is normally charged via a diode connected from the battery or an external source through the low side switch. Rate the diode average current greater than 0.1A and its reverse voltages greater than $V_{IN(MAX)}$.

If an external supply that is greater than the input is available ($V_{BOOST} - V_{IN} > 2V$), it may be used in place of the bootstrap capacitor and diode.

V_{IN} ,V_{BOOST} Start-Up Requirement

The LT3651-8.2/LT3651-8.4 operate with a V_{IN} range of 9V to 32V. The charger begins a charging cycle when the detected battery voltage is below the auto-restart float voltage and the part is enabled.

When V_{IN} is below 10.5V and the BOOST capacitor is uncharged, the high side switch would normally not have sufficient head room to start switching. During normal operation the low side switch is deactivated when charge current is very low to prevent reverse current in the inductor. However in order to facilitate start-up, the LT3651-8.2/LT3651-8.4 enable the switch if V_{BOOST} voltage is low. This allows initial charging of the BOOST capacitor which then permits the high side switch to saturate and efficiently operate. The boost capacitor charges to full potential after a few cycles.

The design should consider that as the switcher turns on and input current increases, input voltage drops due to source input impedance and input capacitance. This potentially allows the input voltage to drop below the internal V_{IN} UVLO turn-on and thus disrupt normal behavior and potentially stall start-up. If an input current sense resis-

APPLICATIONS INFORMATION

tor is used, its drop must be considered as well. These problems are worsened because input current is largest at low input voltage. Pay careful attention to drops in the power path. Adding a soft-start capacitor to the RNG/SS pin and setting UVLO to 9V with the $\overline{SHDN}$ pin is required at low V_{IN}.

BAT Output Decoupling

It is recommended that the LT3651-8.2/LT3651-8.4 charger output have a decoupling capacitor. If the battery can be disconnected from the charger output this capacitor is required. The value of this capacitor (C_{BAT}) is related to the minimum operational V_{IN} voltage such that:

$$C_{BAT} \approx 20\mu F + \left(\frac{350\mu F}{V_{IN(MIN)}}\right)$$

The voltage rating on C_{BAT} must meet or exceed the battery float voltage.

R_{SENSE}: Charge Current Programming

The LT3651-8.2/LT3651-8.4 charger is configurable to charge at average currents as high as 4A (see Figure 1). If RNG/SS maximum voltage is not limited, the inductor sense resistor, R_{SENSE}, has 95mV across it at maximum charge current so:

$$R_{SENSE} = \frac{0.095V}{I_{CHG(MAX)}}$$

where $I_{CHG(MAX)}$ is the maximum average charge current. R_{SENSE} is 24mΩ for a 4A charger.

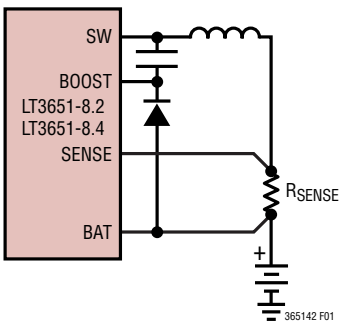


Figure 1. Programming Maximum Charge Current Using R_{SENSE}

Inductor Selection

The primary criteria for inductor value selection in the LT3651-8.2/LT3651-8.4 charger is the ripple current created during switching. Ripple current, ΔI_{MAX}, is typically set within a range of 25% to 35% of the maximum charge current, I_{MAX}. This percentage typically gives a good compromise between losses due to ripple and inductor size. An approximate formula for inductance is:

$$L = \frac{V_{BAT} + V_F}{\Delta I_{MAX} \bullet f_{OSC}(MHz)} \bullet \left(1 - \frac{V_{BAT} + V_F}{V_{IN} + V_F}\right)(\mu H)$$

Worse-case ripple is at high V_{IN} and high V_{BAT}. V_F is the forward voltage of the synchronous switch (approximately 0.14V at 4A). Figure 2 shows inductance for the case of a 4A charger. The inductor must have a saturation current equal to or exceeding the maximum peak current in the inductor. Peak current is $I_{CHG(MAX)} + \Delta I_{CHG(MAX)}/2$.

Magnetics vendors typically specify inductors with maximum RMS and saturation current ratings. Select an inductor that has a saturation current rating at or above peak current, and an RMS rating above $I_{CHG(MAX)}$. Inductors must also meet a maximum volt-second product requirement. If this specification is not in the data sheet of an inductor, consult the vendor to make sure the maximum volt-second product is not being exceeded by your design. The minimum required volt-second product is approximately:

$$\frac{V_{BAT}}{f_{OSC(MHz)}} \bullet \left(1 - \frac{V_{BAT}}{V_{IN(MAX)}}\right)(V \bullet \mu s)$$

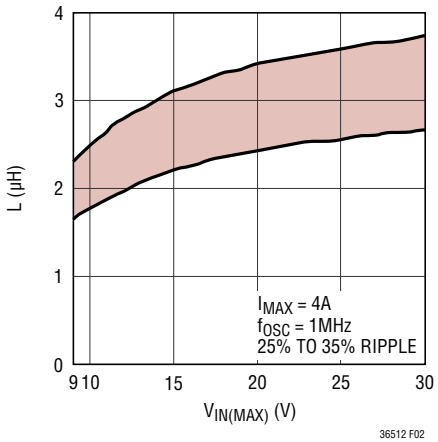


Figure 2. Inductance (L) vs Maximum V_{IN}

APPLICATIONS INFORMATION

Acceptable power inductors are available from several manufacturers such a Würth Elektronik, Vishay, Coilcraft and TDK.

System Input Current Limit

The LT3651-8.2/LT3651-8.4 contain a PowerPath™ control feature to help manage supply load currents. The charger adjusts charger output current in response to a system load so as to maintain a constant input supply load. If overall input supply current exceeds the programmed maximum value the charge current is diminished in an attempt to keep supply current constant. One application where this is helpful is if you have a current limited input supply. Setting the maximum input current limit below the supply limit prevents supply collapse.

A resistor, R_{CL}, is placed between the input supply and the system and charger loads as shown in Figure 3.

The LT3651-8.2/LT3651-8.4 source 50µA from the I_{LIM} pin, so a voltage is developed by simply connecting a resistor to ground. The voltage on the I_{LIM} pin corresponds to 11.5 times the maximum voltage across the input sense resistor (R_{CL}). Input current limit is defined by:

$$I_{INPUT(MAX)} = \frac{V_{ILIM}}{11.5 \bullet R_{CL}} = \frac{50\mu A \bullet R_{ILIM}}{11.5 \bullet R_{CL}}$$

The programming range for I_{LIM} is 0V to 1V. Voltages higher than 1V have no effect on the maximum input current. The default maximum sense voltage is 95mV and is obtained if R_{ILIM} is greater than 20k or if the pin is left open.

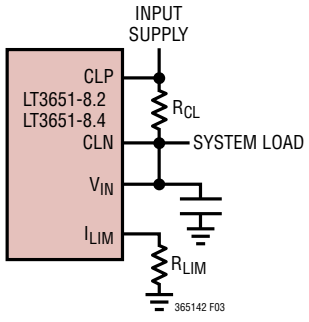


Figure 3. Input Current Limit Configuration

For example, say you want a maximum input current of 2A and the charger is designed for 4A maximum average charge current, which is 1A V_{IN} referred (4A times duty cycle). Using the full I_{LIM} range, the maximum voltage across R_{CL} is 95mV. So R_{CL} is set at 95mV/2A = 48mΩ. When the system load exceeds 1A (= 2A – 1A) charge current is reduced such that the total input current stays at 2A. When the system load is 2A the charge current is 0. This feature only controls charge current so if the system load exceeds the maximum limit and no other limitation is designed, the input current exceeds the maximum desired, though the charge current reduces to 0A. When the input limiter reduces charge current it does not impact the internal system timer if used. See Figure 4.

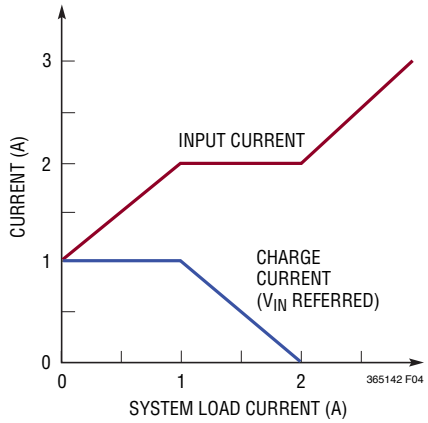


Figure 4. Input Current Limit for 4A Maximum Charger and 6A System Current Limit

If reduced voltage overhead or better efficiency is required then reduce the maximum voltage across R_{CL}. So for instance, a 10k R_{ILIM} sets the maximum R_{CL} voltage to 43mV. This reduction comes at the expense of slightly increased limit variation.

Note the LT3651-8.2/LT3651-8.4 internally integrate the input limit signals. This should normally provide sufficient filtering and reduce the sensitivity to current spikes. For the best accuracy take care to provide good Kelvin connections from R_{CL} to CLP, CLN.

APPLICATIONS INFORMATION

Further flexibility is possible by dynamically altering the I_{LIM} pin. Different resistor values could be switched in to create unique input limit conditions. The I_{LIM} pin can also be tied to a servo amplifier for other options. See the information in the following section concerning $I_{RNG/SS}$ programming for examples.

RNG/SS: Dynamic Current Adjust

The RNG/SS pin gives the user the capability to adjust maximum charge current dynamically. The part sources 50µA from the pin, so connecting a resistor to ground develops a voltage. The voltage on the RNG/SS pin corresponds to ten times the maximum voltage across the charge current sense resistor, R_{SENSE}. The defining equations for charge current are:

$$I_{MAX(RNG/SS)} = \frac{V_{RNG/SS}}{10.8 \bullet R_{SENSE}} = \frac{50\mu A \bullet R_{RNG/SS}}{10.8 \bullet R_{SENSE}}$$

$I_{MAX(RNG/SS)}$ is the maximum charge current.

The programming range for RNG/SS is 0V to 1V. Voltages higher than 1V have no effect on the maximum charge current. The default maximum sense voltage is 95mV and is obtained if $R_{RNG/SS}$ is greater than 20k or if the pin is left open.

For example, say you want to reduce the maximum charge current to 50% of the maximum value. Set RNG/SS to 0.5V (50% of 1V), imposing a 46mV maximum sense voltage. Per the above equation, 0.5V on RNG/SS requires a 10k resistor. If the charge current needs to be dynamically adjustable then Figure 5 shows one method.

Active servos can also be used to impose voltages on the RNG/SS pin, provided they can only sink current. Active circuits that source current cannot be used to drive the RNG/SS pin. An example is shown in Figure 6.

RNG/SS: Soft-Start

Soft-start functionality is also supported by the RNG/SS pin. The 50µA sourced from the RNG/SS pin can linearly charge a capacitor, $C_{RNG/SS}$, connected from the RNG/SS pin to ground (see Figure 7). The maximum charge current follows this voltage. Thus, the charge current increases from zero to the fully programmed value as the

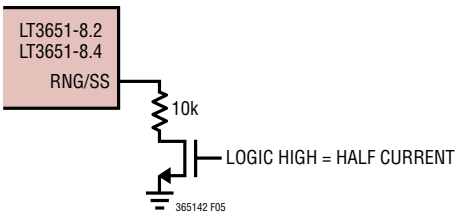


Figure 5. Using the RNG/SS Pin for Digital Control of Maximum Charge Current

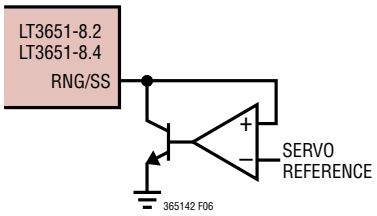


Figure 6. Driving the RNG/SS Pin with a Current-Sink Active Servo Amplifier

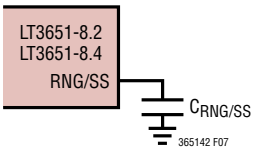


Figure 7. Using the RNG/SS Pin for Soft-Start

APPLICATIONS INFORMATION

capacitor charges from 0V to 1V. The value of $C_{RNG/SS}$ is calculated based on the desired time to full current (t_{SS}) following the relation:

$$C_{RNG/SS} = 50\mu A \bullet t_{SS}$$

The RNG/SS pin is pulled to ground internally when charging is terminated so each new charging cycle begins with a soft-start cycle. RNG/SS is also pulled to ground during bad battery and NTC fault conditions, so a graceful recovery from these faults is possible.

Status Pins

The LT3651-8.2/LT3651-8.4 report charger status through two open-collector outputs, the $\overline{CHRG}$ and $\overline{FAULT}$ pins. These pins can accept voltages as high as V_{IN}, and can sink up to 10mA when enabled.

The $\overline{CHRG}$ pin indicates that the charger is delivering current at greater than a C/10 rate, or one-tenth of the programmed maximum charge current. The $\overline{FAULT}$ pin signals bad battery and NTC faults. These pins are binary coded, and signal state following the table below. On indicates the pin pulled low, and Off indicates pin high impedance.

Table 1. Status Pins State Table

STATUS PINS STATE		CHARGER STATUS
$\overline{CHRG}$	$\overline{FAULT}$	
Off	Off	Not Charging—Standby or Shutdown Mode
Off	On	Bad Battery Fault (Precondition Timeout/EOC Failure)
On	Off	Normal Charging at C/10 or Greater
On	On	NTC Fault (Pause)

C/10 Termination

The LT3651-8.2/LT3651-8.4 support a low current based termination scheme, where a battery charge cycle terminates when the current output from the charger falls to below one-tenth the maximum current, as programmed with R_{SENSE}. The C/10 threshold current corresponds to 9mV across R_{SENSE}. This termination mode is engaged by shorting the TIMER pin to ground.

When C/10 termination is used, a LT3651-8.2/LT3651-8.4 charger sources battery charge current as long as the average current level remains above the C/10 threshold. As the full-charge float voltage is achieved, the charge current falls until the C/10 threshold is reached, at which time the charger terminates and the LT3651-8.2/LT3651-8.4 enter standby mode. The $\overline{CHRG}$ status pin follows the charge cycle and is high impedance when the charger is not actively charging.

When V_{BAT} drops below 97.5% of the full-charged float voltage, whether by battery loading or replacement of the battery, the charger automatically re-engages and starts charging.

There is no provision for bad battery detection if C/10 termination is used.

Timer Termination

The LT3651-8.2/LT3651-8.4 support a timer-based termination scheme, in which a battery charge cycle is terminated after a specific amount of time elapses. Timer termination is engaged when a capacitor (C_{TIMER}) is connected from the TIMER pin to ground. The timer cycle end-of-cycle (t_{EOC}) occurs based on C_{TIMER} following the relation:

$$C_{TIMER} = \frac{t_{EOC}(Hrs)}{3} \bullet 0.68(\mu F)$$

so a typical 3 hour timer end-of-cycle would use a 0.68µF capacitor.

The $\overline{CHRG}$ status pin continues to signal charging at a C/10 rate, regardless of which termination scheme is used. When timer termination is used, the $\overline{CHRG}$ status pin is pulled low during a charge cycle until the charger output current falls below the C/10 threshold. The charger continues to "top off" the battery until timer end-of-cycle, when the LT3651-8.2/LT3651-8.4 terminate the charge cycle and enters standby mode.

APPLICATIONS INFORMATION

Termination at the end of the timer cycle only occurs if the charge cycle was successful. A successful charge cycle occurs when the battery is charged to within 2.5% of the full-charge float voltage. If a charge cycle is not successful at end-of-cycle, the timer cycle resets and charging continues for another full-timer cycle.

When V_{BAT} drops below 97.5% of the full-charge float voltage, whether by battery loading or replacement of the battery, the charger automatically re-engages and starts charging.

Precondition and Bad Battery Fault

A LT3651-8.2/LT3651-8.4 charger has a precondition mode, in which charge current is limited to 15% of the programmed I_{MAX}, as set by R_{SENSE}. The precondition current corresponds to 14mV across R_{SENSE}.

Precondition mode is engaged while the voltage on the BAT pin is below the precondition threshold ($V_{BAT(PRE)}$). Once the BAT voltage rises above the precondition threshold, normal full-current charging can commence. The LT3651-8.2/LT3651-8.4 incorporate 2.5% of threshold for hysteresis to prevent mode glitching.

When the internal timer is used for termination, bad battery detection is engaged. This fault detection feature is designed to identify failed cells. A bad battery fault is triggered when the voltage on BAT remains below the precondition threshold for greater than one-eighth of a full timer cycle (one-eighth end-of-cycle). A bad battery fault is also triggered if a normally charging battery re-enters precondition mode after one-eighth end-of-cycle.

When a bad battery fault is triggered, the charge cycle is suspended, so the $\overline{CHRG}$ status pin becomes high impedance. The $\overline{FAULT}$ pin is pulled low to signal a fault detection. The RNG/SS pin is also pulled low during this fault, to accommodate a graceful restart, in the event that a soft-start function is incorporated (see the RNG/SS: Soft-Start section).

Cycling the charger's power or $\overline{SHDN}$ function initiates a new charge cycle, but a LT3651-8.2/LT3651-8.4 charger does not require a reset. Once a bad battery fault is detected, a new timer charge cycle initiates when the BAT pin exceeds the precondition threshold voltage. During a bad battery fault, 1mA is sourced from the charger. Removing the failed battery allows the charger output voltage to rise and initiate a charge cycle reset. In that way removing a bad battery resets the LT3651-8.2/LT3651-8.4. A new charge cycle is started by connecting another battery to the charger output.

Battery Temperature Fault: NTC

The LT3651-8.2/LT3651-8.4 can accommodate battery temperature monitoring by using an NTC (negative temperature coefficient) thermistor close to the battery pack. The temperature monitoring function is enabled by connecting a 10kΩ, B = 3380 NTC thermistor from the NTC pin to ground. If the NTC function is not desired, leave the pin unconnected.

The NTC pin sources 50µA and monitors the voltage dropped across the 10kΩ thermistor. When the voltage on this pin is above 1.36V (0°C) or below 0.29V (40°C), the battery temperature is out of range, and the LT3651-8.2/LT3651-8.4 trigger an NTC fault. The NTC fault condition remains until the voltage on the NTC pin corresponds to a temperature within the 0°C to 40°C range. Both hot and cold thresholds incorporate hysteresis that corresponds to 2.5°C.

During an NTC fault, charging is halted and both status pins are pulled low. If timer termination is enabled, the timer count is suspended and held until the fault condition is relieved. The RNG/SS pin is also pulled low during this fault, to accommodate a graceful restart in the event that a soft-start function is being incorporated (see the RNG/SS: Soft-Start section).

APPLICATIONS INFORMATION

If higher operational charging temperatures are desired, the temperature range can be expanded by adding series resistance to the 10k NTC resistor. Adding a 0.91k (0TC) resistor will increase the effective temperature threshold to 45°C.

Thermal Foldback

The LT3651-8.2/LT3651-8.4 contain a thermal foldback protection feature that reduces maximum charger output current if the internal IC junction temperature approaches 125°C. In most cases, on-chip temperature servos such that any overtemperature conditions are relieved with only slight reductions in maximum charge current.

In some cases, the thermal foldback protection feature can reduce charge currents below the C/10 threshold. In applications that use C/10 termination (TIMER = 0V), the LT3651-8.2/LT3651-8.4 suspend charging and enters standby mode until the overtemperature condition is relieved.

Layout Considerations

The LT3651-8.2/LT3651-8.4 switch node has rise and fall times that are typically less than 10ns to maximize conversion efficiency. These fast switch times require care in the board layout to minimize noise problems. The philosophy is to keep the physical area of high current loops small (the inductor charge/discharge paths) to minimize magnetic radiation. Keep traces wide and short to minimize parasitic inductance and resistance and shield fast switching voltage nodes (SW, BOOST) to reduce capacitive coupling.

The switched node (SW pin) trace should be kept as short as possible to minimize high frequency noise. The V_{IN} capacitor (C_{IN}) should be placed close to the IC to minimize this switching noise. Short, wide traces on these nodes minimize stray inductance and resistance. Keep the BOOST decoupling capacitor in close proximity to the IC to minimize ringing from trace inductance. Route the SENSE and BAT traces together and keep the traces as short as possible. Shielding these signals from switching noise with ground is recommended. Make Kelvin connections to the battery and sense resistor.

Keep high current paths and transients isolated from battery ground, to assure an accurate output voltage reference. Effective grounding is achieved by considering switched current in the ground plane, and careful component placement and orientation can effectively steer these high currents such that the battery reference does not get corrupted. Figure 8 illustrates the high current, high speed current loops. When the top switch is enabled (charge loop), current flows from the input bypass capacitor (C_{IN}) through the switch and inductor to the battery positive terminal. When the top switch is disabled (discharge loop), current to the battery positive terminal is provided from ground through the synchronous switch. In both cases, these switched currents return to ground via the output bypass capacitor (C_{BAT}).

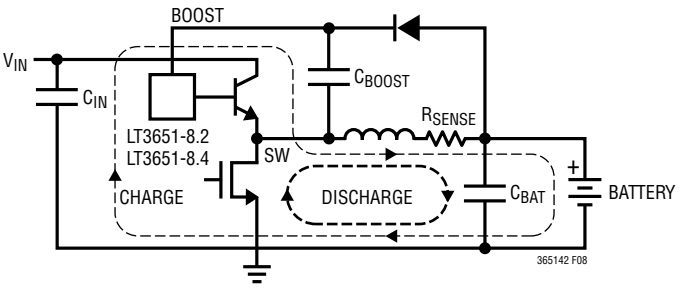


Figure 8

Power Considerations

The LT3651-8.2/LT3651-8.4 packaging is designed to efficiently remove heat from the IC via the exposed pad on the backside of the package, which is soldered to a copper footprint on the PCB. This footprint should be made as large as possible to reduce the thermal resistance of the IC case to ambient air.

APPLICATIONS INFORMATION

Consideration should be given for power dissipation and overall efficiency in a LT3651-8.2/LT3651-8.4 charger. A detailed analysis is beyond the scope of the data sheet, however following are general guidelines.

The major components of power loss are: conduction and transition losses of the LT3651-8.2/LT3651-8.4 switches; losses in the inductor and sense resistors; and AC losses in the decoupling capacitors. Switch conduction loss is fixed. Transition losses are adjustable by changing switcher frequency. Higher input voltages cause an increase in transition losses, decreasing overall efficiency. However transition losses are inversely proportional to switcher oscillator frequency so lowering operating frequency reduces these losses. But lower operating frequency usually requires higher inductance to maintain inductor ripple current (inversely proportional). Inductors with larger values typically have more turns, increasing ESR unless you increase wire diameter making them physically larger. So there is an efficiency and board size trade-off. Secondarily, inductor AC losses increase with frequency and lower ripple reduces AC capacitor losses.

The following simple rules of thumb assume a charge current of 4A and battery voltage of 7.5V, with 1MHz oscillator, 24mΩ sense resistor and 3.3µH/20mΩ inductor.

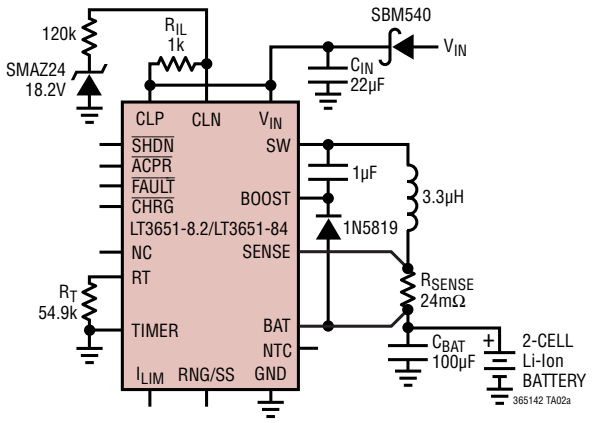
A 1% increase in efficiency represents a 0.35W reduction in power loss at 85% overall efficiency. One way to do this is to decrease resistance in the high current path. A reduction of 0.2W at 4A requires a 22mΩ reduction in resistance. This can be done by reducing inductor ESR. It is also possible to lower the sense resistance (with a reduction in $R_{RNG/SS}$ as well), with a trade-off of slightly less accurate current accuracy. All high current board traces should have the lowest resistance possible. Addition of input current limit sense resistance reduces efficiency.

Charger efficiency drops approximately linearly with increasing frequency all other things constant. At 15V V_{IN} there is a 1% improvement in efficiency for every 200kHz reduction in frequency (100kHz to 1MHz); At 28V V_{IN}, 1% for every 100kHz.

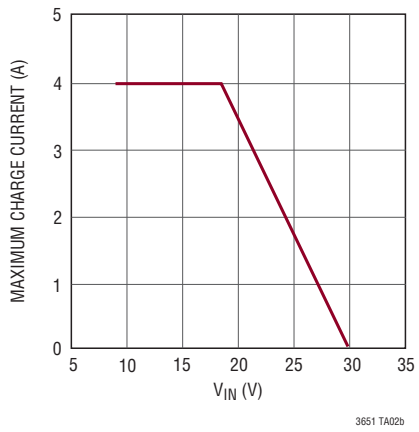
Of course all of these must be experimentally confirmed in the actual charger.

TYPICAL APPLICATIONS

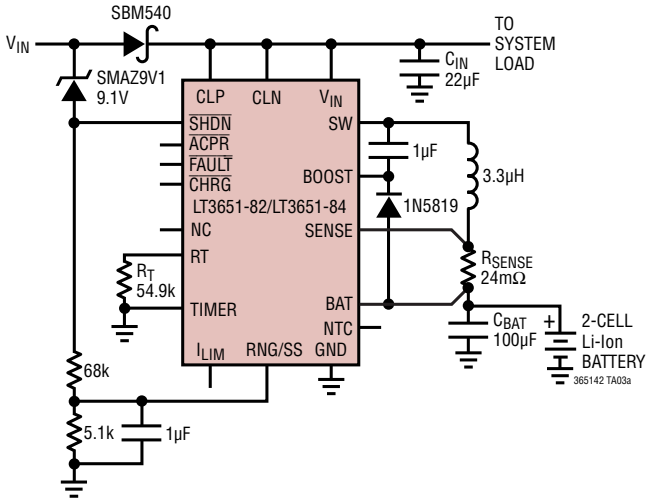
9V to 32V 4A Charger with High Voltage Current Foldback



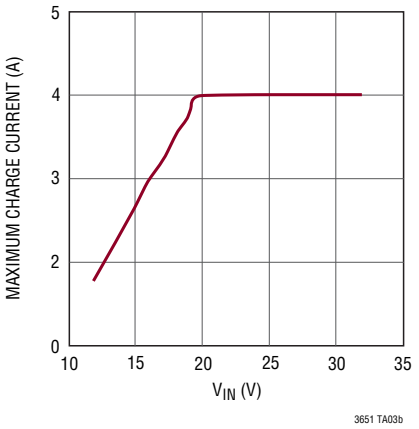
Maximum Charge Current vs V_{IN}



12V to 32V 4A Charger with Low Voltage Current Foldback Using the RNG/SS Pin

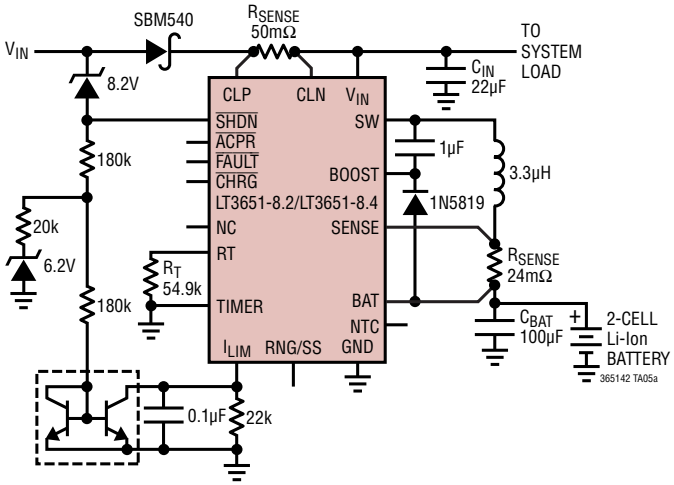


Maximum Charge Current vs V_{IN}

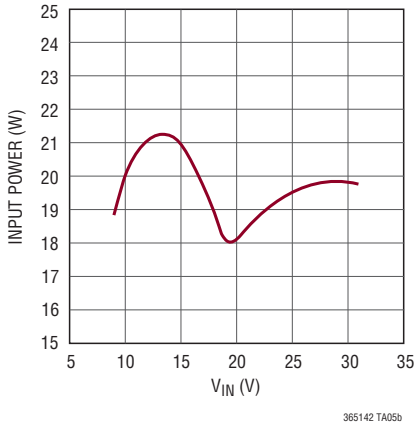


TYPICAL APPLICATIONS

9V to 32V 4A Charger with Approximately Constant Input Power



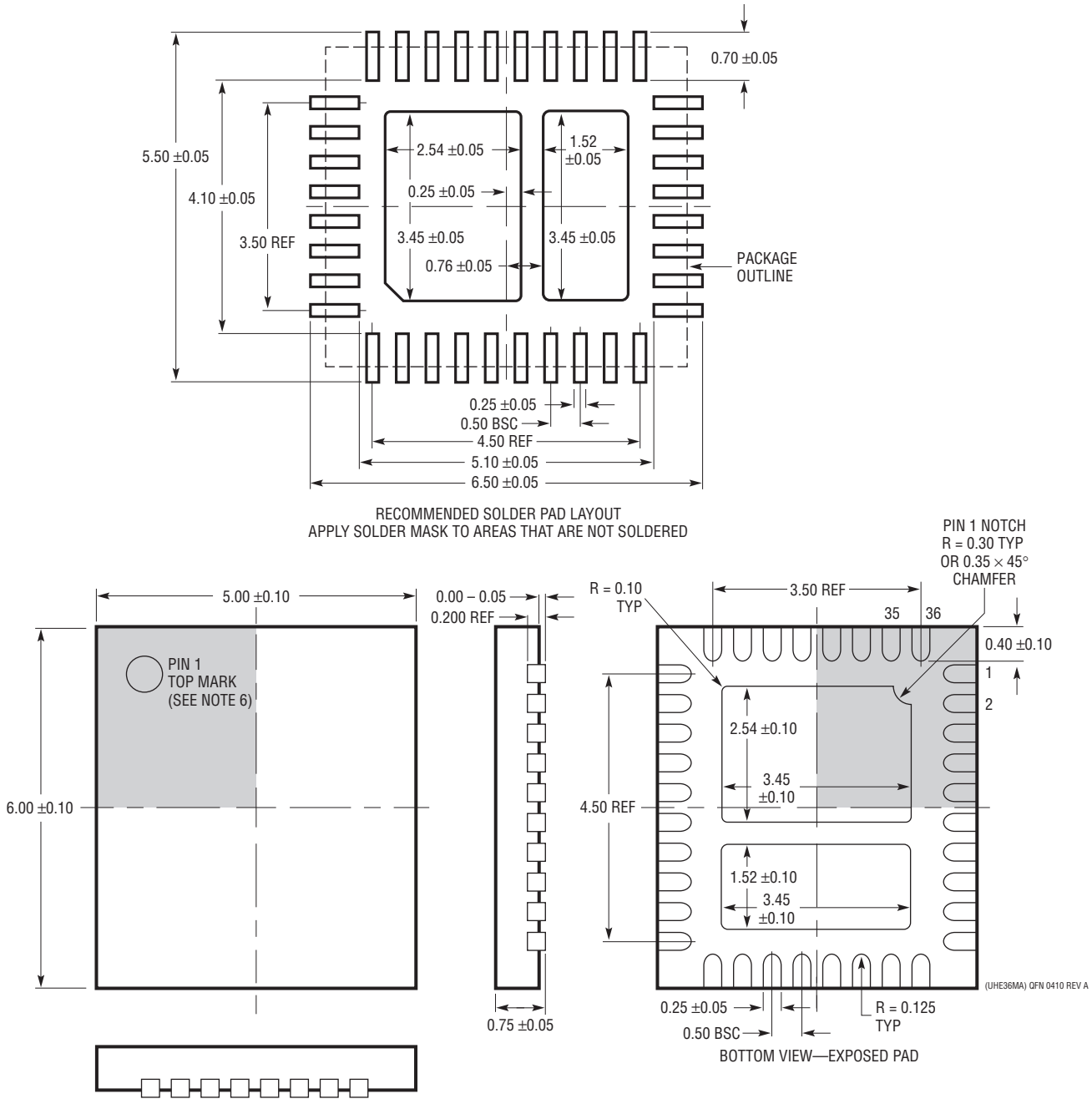
Input Power vs V_{IN}



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHE Package
Variation: UHE36MA
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1753 Rev A)



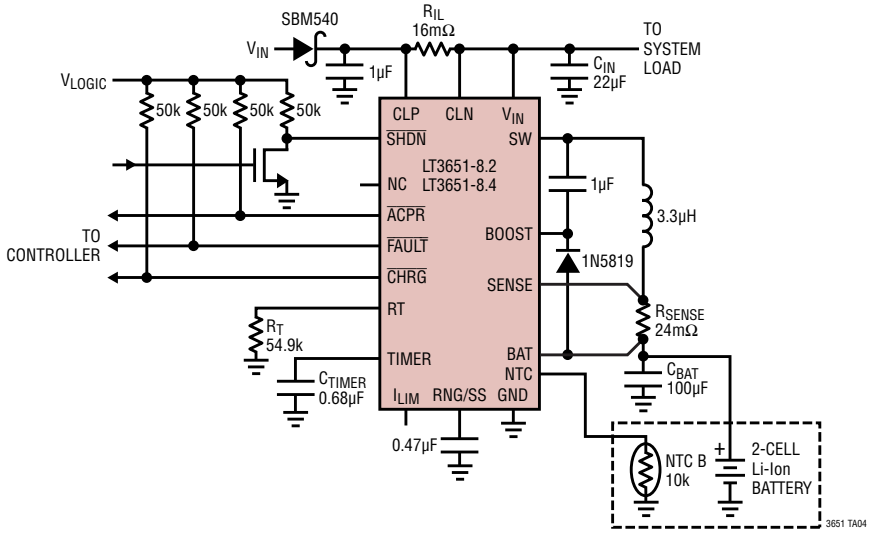
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/15	Modified Typical Application circuit.	1
		Modified Efficiency/Power Loss curve.	1
		Changed typical values of Boost Supply Current/ Switch Drive.	3
		Modified Typical Performance Characteristic curves.	6
		Clarified GND Pin Function description.	7

TYPICAL APPLICATION

9V to 32V 4A Charger with 3-Hour Charge Timeout, 6.3A Input Current Limit, 10ms Soft-Start and Battery Temperature Monitoring



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3651-4.1/LT3651-4.2	Monolithic 4A Switch Mode Synchronous 1-Cell Li-Ion Battery Charger	Standalone, 4.75 ≤ V_{IN} ≤ 32V (40V Abs Max), 1MHz, 4A, Programmable Charge Current Timer or V/10 Termination 5mm × 6mm QFN-36 Package
LT3650	2A Monolithic Li-Ion Battery Charger	High Efficiency, Wide Input Voltage Range Charger, Time or Charge Current Termination, Automatic Restart, Temperature Monitoring, Programmable Charge Current, Input Current Limit, 12-Lead DFN and MSOP Packages
LT3652/LT3652HV	Power Tracking 2A Battery Charger	Input Supply Voltage Regulation Loop for Peak Power Tracking in (MPPT) Solar Applications, Standalone, 4.95V ≤ V_{IN} ≤ 32V (40V Abs Max), 1MHz, 2A Programmable Charge Current, Timer or C/10 Termination, 3mm × 3mm DFN-12 Package and MSOP-12 Packages. LT3652HV Version Up to V_{IN} = 34V
LTC4000	High Voltage High Current Controller for Battery Charging and Power Management	Complete High Performance Battery Charger When Paired with a DC/DC Converter Wide Input and Output Voltage Range: 3V to 60V ±0.25% Accurate Programmable Float Voltage, Programmable C/X or Timer Based Charge Termination NTC Input for Temperature Qualified Charging, 28-Lead 4mm × 5mm QFN or SSOP Packages
LTC4002	Standalone Li-Ion Switch Mode Battery Charger	Complete Charger for 1- or 2-Cell Li-Ion Batteries, Onboard Timer Termination, Up to 4A Charge Current, 10-Lead DFN and SO-8 Packages
LTC4006	Small, High Efficiency, Fixed Voltage Li-Ion Battery Charger with Termination	Complete Charger for 2-, 3- or 4-Cell Li-Ion Batteries, AC Adapter Current Limit and Thermistor Sensor, 16-Lead Narrow SSOP Package
LTC4007	High Efficiency, Programmable Voltage Battery Charger with Termination	Complete Charger for 3- or 4-Cell Li-Ion Batteries, AC Adapter Current Limit, Thermistor Sensor and Indicator Outputs, 24-Lead SSOP Package
LTC4008	4A, High Efficiency, Multi-Chemistry Battery Charger	Complete Charger for 2- to 6-Cell Li-Ion Batteries or 4- to 18-Cell Nickel Batteries, Up to 96% Efficiency, 20-Lead SSOP Package
LTC4009/LTC4009-1 LTC4009-2	High Efficiency, Multi-Chemistry Battery Charger	Complete Charger for 1- to 4-Cell Li-Ion Batteries or 4- to 18-Cell Nickel Batteries, Up to 93% Efficiency, 20-Lead (4mm × 4mm) QFN Package, LTC4009-1 for 4.1V Float Voltage, LTC4009-2 for 4.2V Float Voltage
LTC4012/LTC4012-1/ LTC4012-2/LTC4012-3	4A, High Efficiency, Multi-Chemistry Battery Charger with PowerPath Control	PowerPath Control, Constant-Current/Constant-Voltage Switching Regulator Charger, Resistor, Voltage/Current Programming, AC Adapter Current Limit and Thermistor Sensor and Indicator Outputs, 1 to 4-cell Li, Up to 18-cell Ni, SLA and SuperCap Compatible; 4mm × 4mm QFN-20 Package; LTC4012-1 Version for 4.1V Li Cells, LTC4012-2 Version for 4.2V Li Cells, LTC4012-3 Version Has Extra GND Pin

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LT3651-8.2
LT 0715 REV A • PRINTED IN USA