
ML610Q411/Q412

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

ML610Q411/Q412 is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I²C bus interface (master), buzzer driver, battery level detect circuit, RC oscillation type A/D converter, 12-bit successive approximation type A/D converter, and LCD driver, are incorporated around LAPIS Semiconductor -original 8-bit CPU nX-U8/100.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications. The on-chip debug function that is installed enables program debugging and programming.

M L610Q411/Q412 has a dual clock, runs at 32.768kHz crystal oscillation clock or a built-in 500kHz RC oscillation clock, used for a system requires the accurate clock or timer.

FEATURES

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time
 - 30.5 μs (@32.768 kHz system clock)
 - 2μs (@500kHz system clock)
- Internal memory
 - Internal 16KByte Flash ROM (8K×16 bits) (including unusable 1KByte TEST area)
 - Internal 1KByte Data RAM (1024×8 bits)
- Interrupt controller
 - 2 non-maskable interrupt sources
 - Internal source: 1 (Watch dog timer)
 - External source: 1 (NMI)
 - 19 maskable interrupt sources
 - Internal sources: 15 (SSIO, SA-A/D converter, I2C, Timer0, Timer1, Timer2, Timer3, 1kHz timer, UART, RC-A/D converter, PWM, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
 - External sources: 4 (P00, P01, P02, P03)
- Time base counter
 - Low-speed time base counter ×1 channel
 - Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
 - High-speed time base counter ×1 channel



- Watchdog timer
 - Non-maskable interrupt and reset
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timers
 - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
 - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)
- 1 kHz timer
 - 10 Hz/1 Hz interrupt function
- Capture
 - Time base capture × 2 channels (4096 Hz to 32 Hz)
- PWM
 - Resolution 16 bits × 1 channel
- Synchronous serial port
 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- UART
 - TXD/RXD × 1 channel
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I²C bus interface
 - Master function only
 - Standard mode (50kbps)
- Buzzer driver
 - 4 output modes, 8 frequencies, 16 duty levels
- RC oscillation type A/D converter
 - 24-bit counter
 - Time division × 2 channels
- Successive approximation type A/D converter
 - 12-bit A/D converter
 - Input × 2 channels
 - Conversion time: 46us/1ch@500kHz
- General-purpose ports
 - Non-maskable interrupt input port × 1 channel
 - Input-only port × 6 channels (including secondary functions)
 - Output-only port × 3 channels (including secondary functions)
 - Input/output port
 - ML610Q411: 22 channels (including secondary functions)
 - ML610Q412: 14 channels (including secondary functions)
- LCD driver
 - The number of segments
 - ML610Q411: 144 dots max. (36 seg × 4 com)
 - ML610Q412: 176 dots max. (44 seg × 4 com)
 - 1/1 to 1/4 duty
 - 1/3 bias (built-in bias generation circuit)

- Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
- Bias voltage multiplying clock selectable (8 types)
- Contrast adjustment (32 steps)
- LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset when oscillation stop of the low-speed clock is detected
 - Reset by the watchdog timer (WDT) overflow

- Battery Level Detector
 - Threshold voltages: One of 16 levels
 - Accuracy: $\pm 2\%$ (Typ.)

- Clock
 - Low-speed clock: (This LSI can not guarantee the operation without low-speed crystal oscillation clock)
Crystal oscillation (32.768 kHz)
 - High-speed clock:
 - Built-in RC oscillation (500 kHz)
 - External clock (500kHz or less)
 - High-speed Clock gear: 1/2(250kHz), 1/4(125kHz), 1/8(62.5kHz: default)
 - Selection of high-speed clock mode by software:
Built-in RC oscillation, External clock

- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
 - Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Guaranteed operating range
 - Operating temperature: -20°C to $+70^{\circ}\text{C}$ (P version: -40°C to $+85^{\circ}\text{C}$)
 - Operating voltage: $V_{\text{DD}} = 1.1\text{V}$ to 3.6V , $AV_{\text{DD}} = 2.2\text{V}$ to 3.6V

• Product name – Supported Function

The line-up of the ML610Q411 and the ML610Q412 is below.

| - Chip (Die) - | ROM type | Low-speed oscillation stop detect reset | Operating temperature | Product availability |
|-------------------|-----------|---|-----------------------|----------------------|
| ML610Q411-xxxWA | Flash ROM | Yes | -20°C to +70°C | Yes |
| ML610Q411P-xxxWA | Flash ROM | Yes | -40°C to +85°C | Yes |
| ML610Q411PA-xxxWA | Flash ROM | Selectable to disable always | -40°C to +85°C | Yes |
| ML610Q412-xxxWA | Flash ROM | Yes | -20°C to +70°C | Yes |
| ML610Q412P-xxxWA | Flash ROM | Yes | -40°C to +85°C | Yes |

| -120-pin plastic TQFP - | ROM type | Low-speed oscillation stop detect reset | Operating temperature | Product availability |
|-------------------------|-----------|---|-----------------------|----------------------|
| ML610Q411-xxxTB | Flash ROM | Yes | -20°C to +70°C | Yes |
| ML610Q411P-xxxTB | Flash ROM | Yes | -40°C to +85°C | Yes |
| ML610Q411PA-xxxTB | Flash ROM | Selectable to disable always | -40°C to +85°C | Yes |
| ML610Q412-xxxTB | Flash ROM | Yes | -20°C to +70°C | Yes |
| ML610Q412P-xxxTB | Flash ROM | Yes | -40°C to +85°C | Yes |

xxx:ROM code number (xxx of the blank product is NNN)

Q:Flash ROM version

P:Wide range temperature version

A: Low-speed clock oscillation stop detection reset is selectable to disable always (See chapter3 and chapter4 in the user's manual for more detail).

WA:Chip (Die)

TB:TQFP

BLOCK DIAGRAM
ML610Q411 Block Diagram

Figure 1 show the block diagram of the ML610Q411.
 "*" indicates the secondary function of each port.

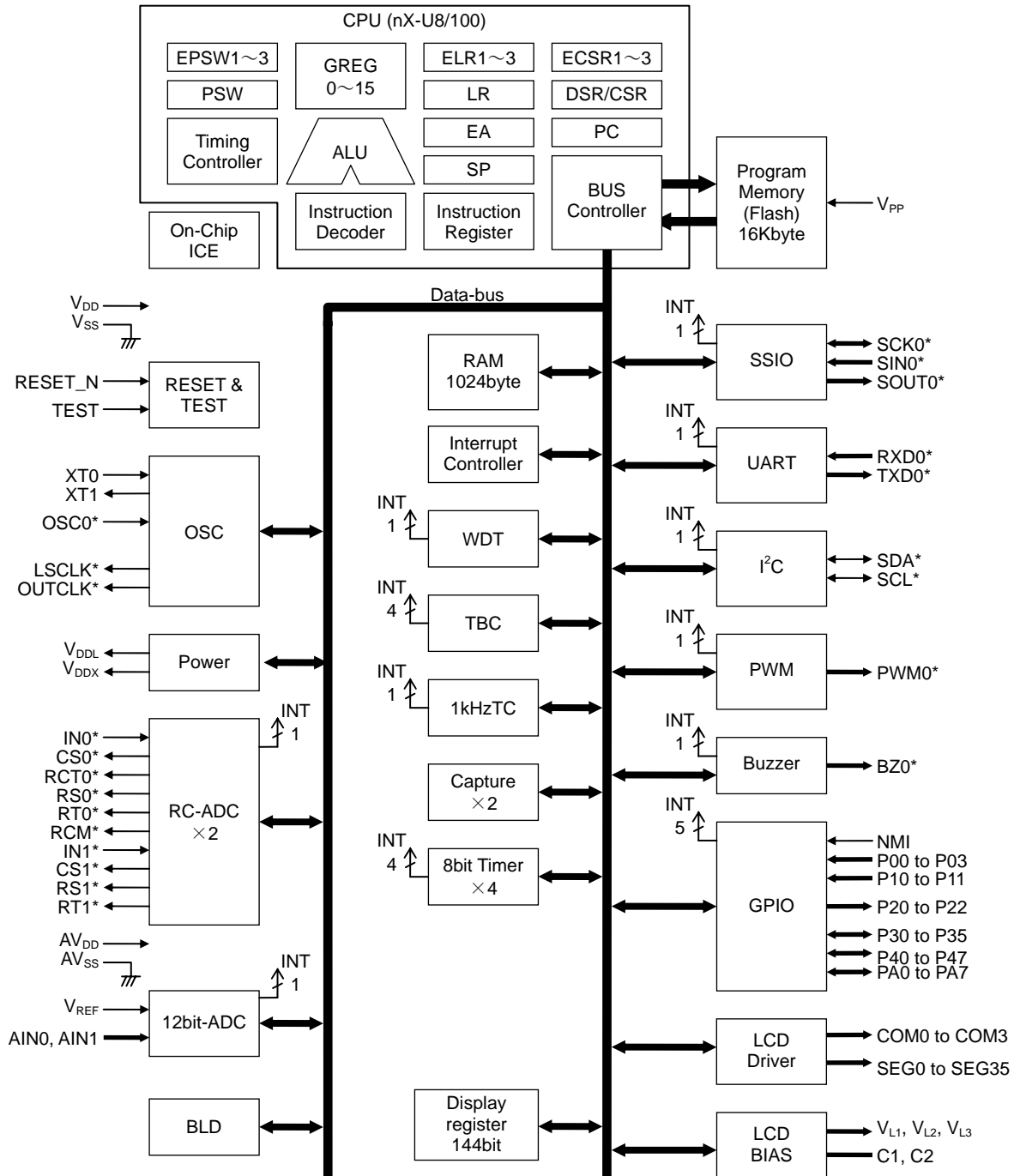


Figure 1 ML610Q411 Block Diagram

ML610Q412 Block Diagram

Figure 2 show the block diagram of the ML610Q412.
 "*" indicates the secondary function of each port.

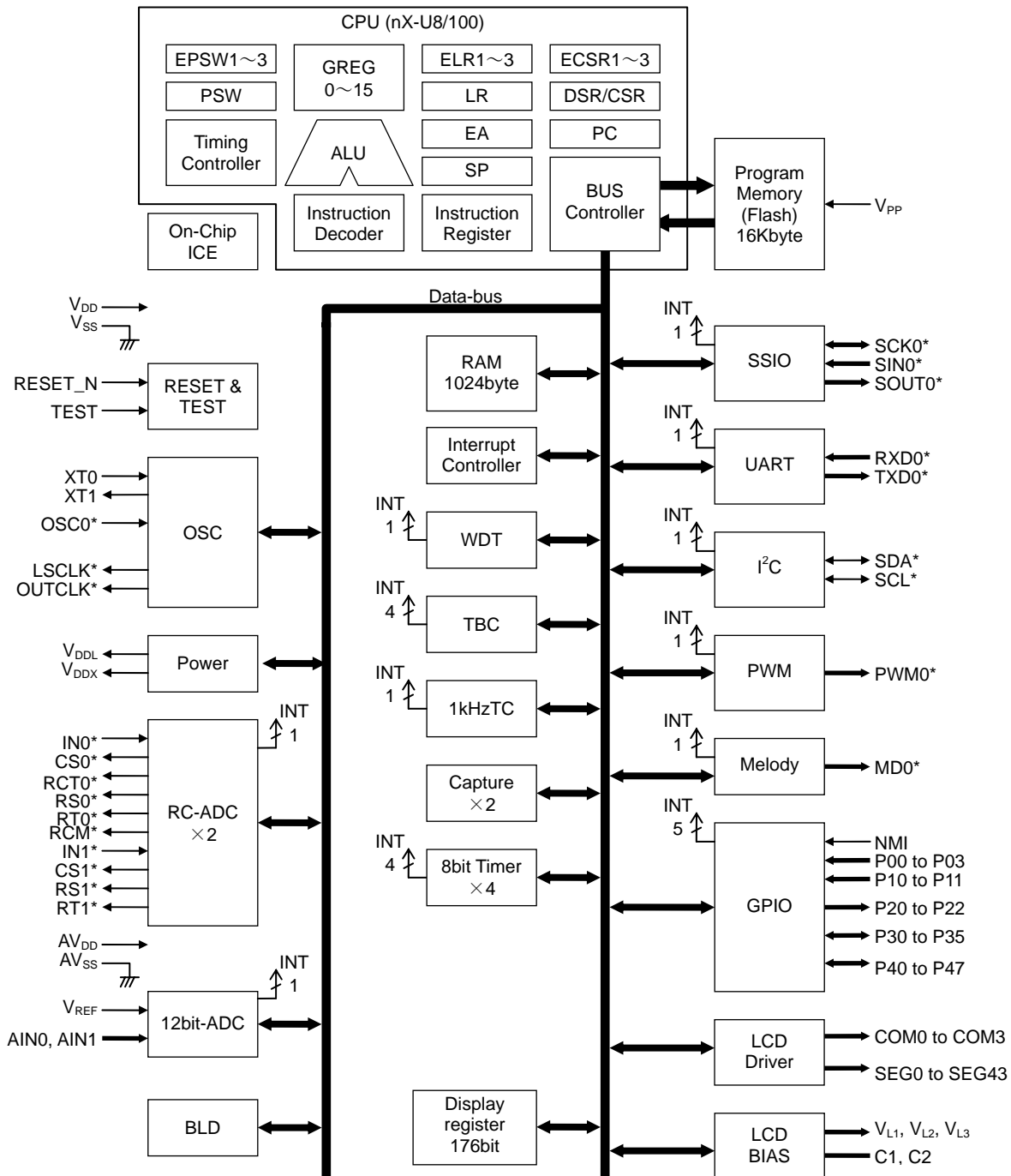
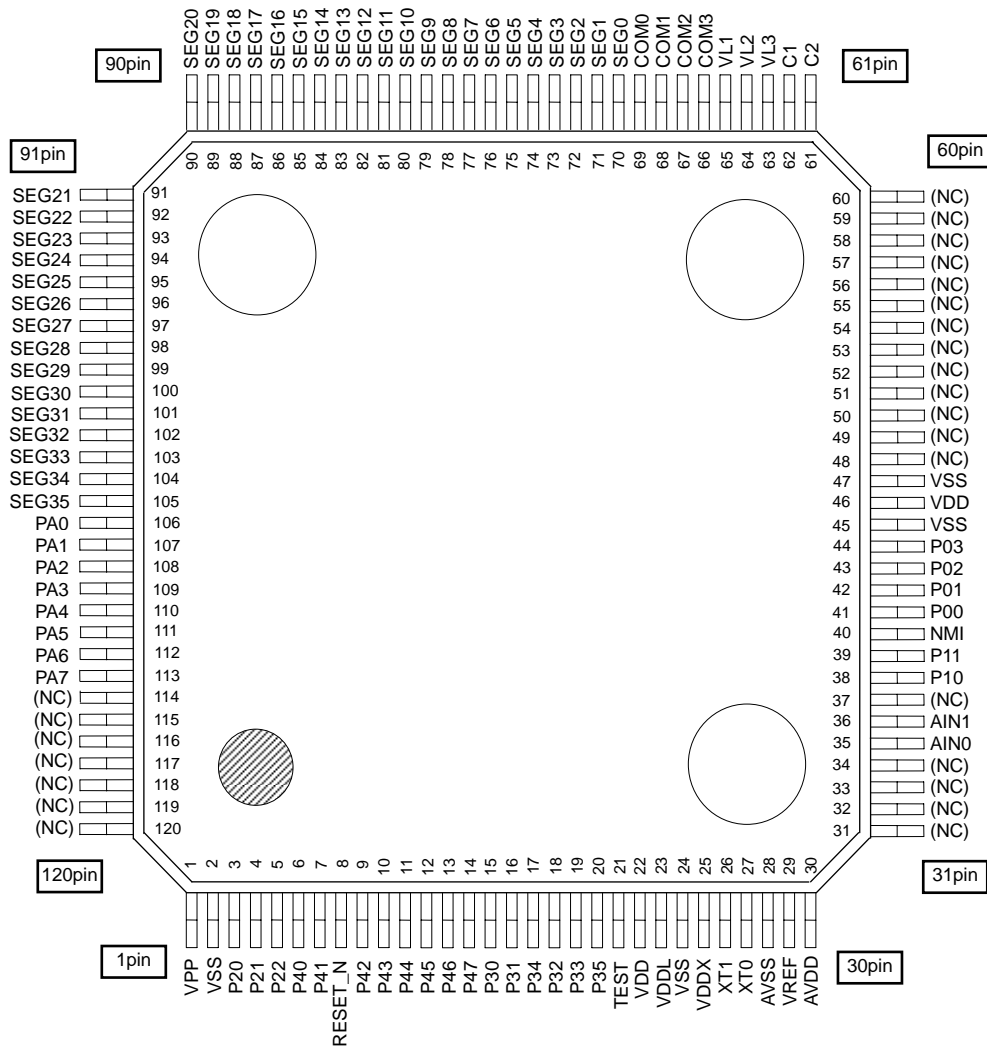


Figure 2 ML610Q412 Block Diagram

PIN CONFIGURATION

ML610Q411 TQFP120 Pin Layout



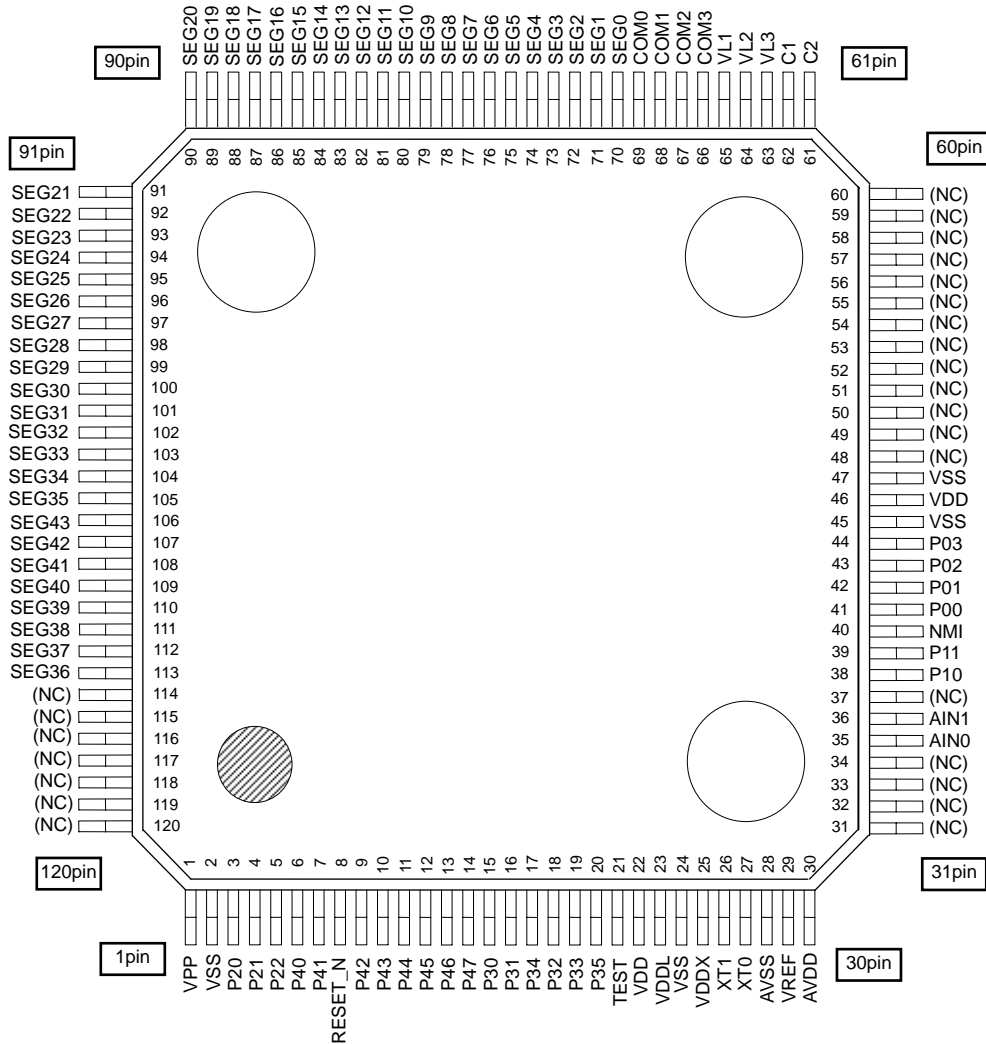
(NC): No Connection

Note:

The assignment of the P30 to P35 are not in order.

Figure 3 ML610Q411 TQFP120 Pin Configuration

ML610Q412 TQFP120 Pin Layout



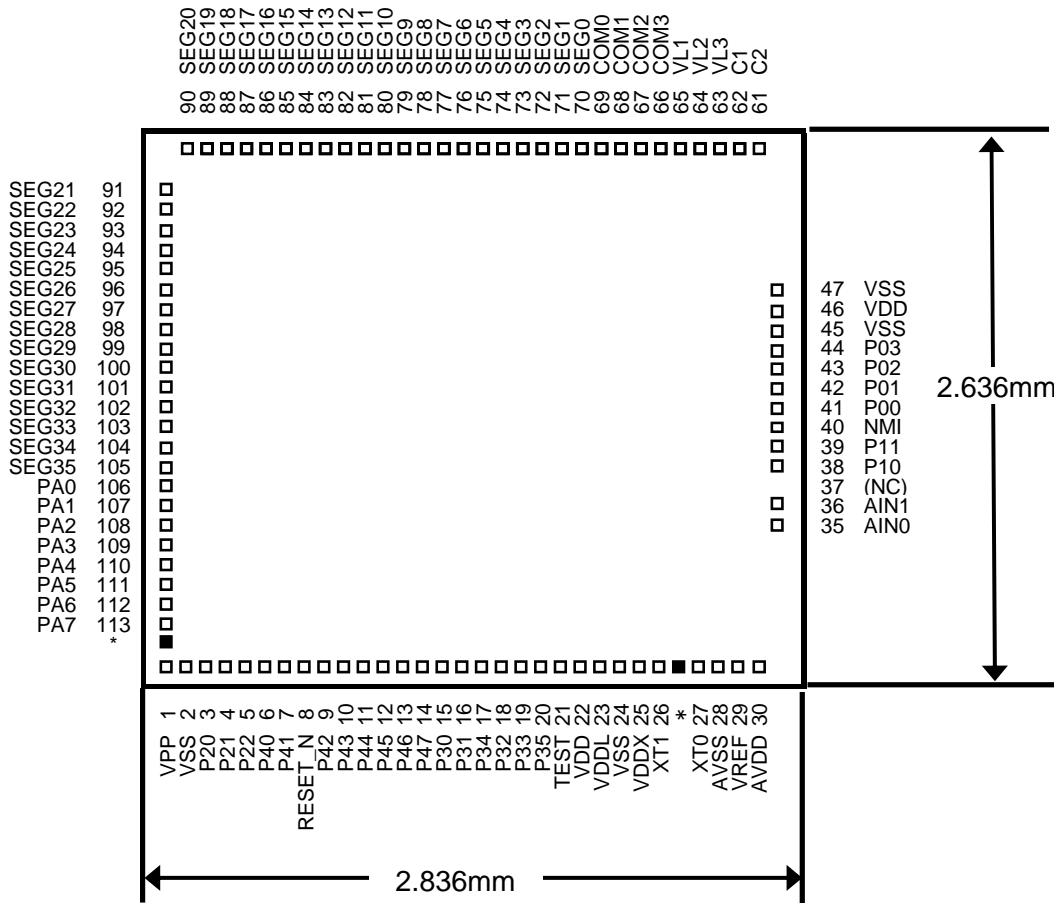
(NC): No Connection

Note:

The assignment of the P30 to P35 are not in order.

Figure 4 ML610Q412 TQFP120 Pin Configuration

ML610Q411 Chip Pin Layout & Dimension



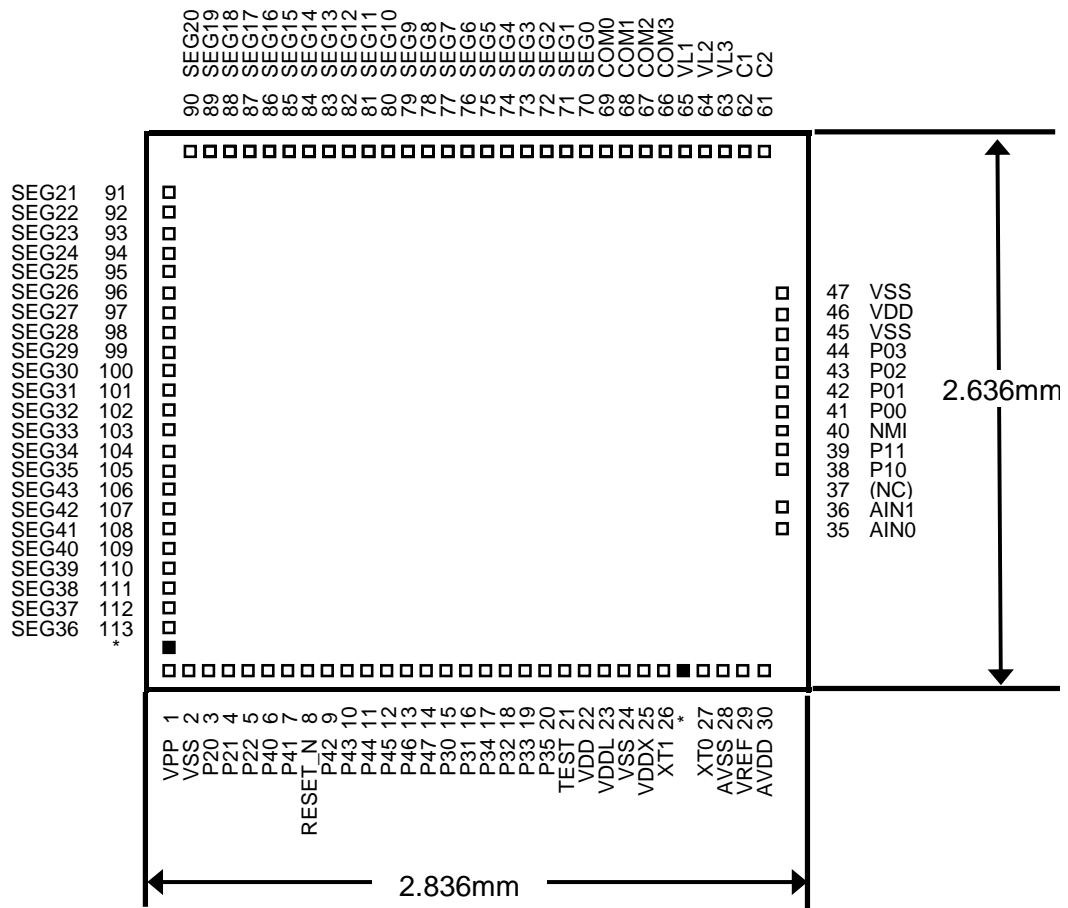
* Dummy pad

Note: These dummy pads are visible and do not have any function, they are placed for a mechanical evaluation in LAPIS Semiconductor. Please do NOT implement wire-bonding to the dummy pad.

| | |
|-----------------------------------|-----------------------|
| Chip size: | 2.836mm x 2.636mm |
| PAD count: | 95 pins |
| Minimum PAD pitch: | 80 μm |
| PAD aperture: | 70 μm × 70 μm |
| Chip thickness: | 350 μm |
| Voltage of the rear side of chip: | V _{SS} level |

Figure 5 ML610Q411 Chip Layout & Dimension

ML610Q412 Chip Pin Layout & Dimension



* Dummy pad

Note: These dummy pads are visible and do not have any function, they are placed for a mechanical evaluation in LAPIS Semiconductor. Please do NOT implement wire-bonding to the dummy pad.

| | |
|-----------------------------------|-----------------------|
| Chip size: | 2.836mm x 2.636mm |
| PAD count: | 95 pins |
| Minimum PAD pitch: | 80 μm |
| PAD aperture: | 70 μm × 70 μm |
| Chip thickness: | 350 μm |
| Voltage of the rear side of chip: | V _{SS} level |

Figure 6 ML610Q412 Chip Layout & Dimension

ML610Q411 Pad Coordinates

Table 1 ML610Q411 Pad Coordinates

Chip Center: X=0,Y=0

| PAD No. | Pad Name | X (μm) | Y (μm) | PAD No. | Pad Name | X (μm) | Y (μm) | PAD No. | Pad Name | X (μm) | Y (μm) |
|---------|----------|--------|--------|---------|----------|--------|--------|---------|----------|--------|--------|
| 1 | VPP | -1230 | -1212 | 51 | (NC) | - | - | 101 | SEG31 | -1312 | 160 |
| 2 | VSS | -1150 | -1212 | 52 | (NC) | - | - | 102 | SEG32 | -1312 | 80 |
| 3 | P20 | -1070 | -1212 | 53 | (NC) | - | - | 103 | SEG33 | -1312 | 0 |
| 4 | P21 | -990 | -1212 | 54 | (NC) | - | - | 104 | SEG34 | -1312 | -80 |
| 5 | P22 | -910 | -1212 | 55 | (NC) | - | - | 105 | SEG35 | -1312 | -160 |
| 6 | P40 | -830 | -1212 | 56 | (NC) | - | - | 106 | PA0 | -1312 | -240 |
| 7 | P41 | -750 | -1212 | 57 | (NC) | - | - | 107 | PA1 | -1312 | -320 |
| 8 | RESET_N | -670 | -1212 | 58 | (NC) | - | - | 108 | PA2 | -1312 | -400 |
| 9 | P42 | -590 | -1212 | 59 | (NC) | - | - | 109 | PA3 | -1312 | -480 |
| 10 | P43 | -510 | -1212 | 60 | (NC) | - | - | 110 | PA4 | -1312 | -560 |
| 11 | P44 | -430 | -1212 | 61 | C2 | 1220 | 1212 | 111 | PA5 | -1312 | -640 |
| 12 | P45 | -350 | -1212 | 62 | C1 | 1140 | 1212 | 112 | PA6 | -1312 | -720 |
| 13 | P46 | -270 | -1212 | 63 | VL3 | 1060 | 1212 | 113 | PA7 | -1312 | -800 |
| 14 | P47 | -190 | -1212 | 64 | VL2 | 980 | 1212 | -- | Dummy | -1312 | -908 |
| 15 | P30 | -110 | -1212 | 65 | VL1 | 900 | 1212 | | | | |
| 16 | P31 | -30 | -1212 | 66 | COM3 | 820 | 1212 | | | | |
| 17 | P34 | 50 | -1212 | 67 | COM2 | 740 | 1212 | | | | |
| 18 | P32 | 130 | -1212 | 68 | COM1 | 660 | 1212 | | | | |
| 19 | P33 | 210 | -1212 | 69 | COM0 | 580 | 1212 | | | | |
| 20 | P35 | 290 | -1212 | 70 | SEG0 | 500 | 1212 | | | | |
| 21 | TEST | 370 | -1212 | 71 | SEG1 | 420 | 1212 | | | | |
| 22 | VDD | 450 | -1212 | 72 | SEG2 | 340 | 1212 | | | | |
| 23 | VDDL | 530 | -1212 | 73 | SEG3 | 260 | 1212 | | | | |
| 24 | VSS | 610 | -1212 | 74 | SEG4 | 180 | 1212 | | | | |
| 25 | VDDX | 690 | -1212 | 75 | SEG5 | 100 | 1212 | | | | |
| 26 | XT1 | 770 | -1212 | 76 | SEG6 | 20 | 1212 | | | | |
| - | Dummy | 850 | -1212 | 77 | SEG7 | -60 | 1212 | | | | |
| 27 | XT0 | 930 | -1212 | 78 | SEG8 | -140 | 1212 | | | | |
| 28 | AVSS | 1030 | -1212 | 79 | SEG9 | -220 | 1212 | | | | |
| 29 | VREF | 1110 | -1212 | 80 | SEG10 | -300 | 1212 | | | | |
| 30 | AVDD | 1190 | -1212 | 81 | SEG11 | -380 | 1212 | | | | |
| 31 | (NC) | - | - | 82 | SEG12 | -460 | 1212 | | | | |
| 32 | (NC) | - | - | 83 | SEG13 | -540 | 1212 | | | | |
| 33 | (NC) | - | - | 84 | SEG14 | -620 | 1212 | | | | |
| 34 | (NC) | - | - | 85 | SEG15 | -700 | 1212 | | | | |
| 35 | A IN0 | 1312 | -522 | 86 | SEG16 | -780 | 1212 | | | | |
| 36 | A IN1 | 1312 | -350 | 87 | SEG17 | -860 | 1212 | | | | |
| 37 | (NC) | - | - | 88 | SEG18 | -940 | 1212 | | | | |
| 38 | P10 | 1312 | -210 | 89 | SEG19 | -1020 | 1212 | | | | |
| 39 | P11 | 1312 | -130 | 90 | SEG20 | -1100 | 1212 | | | | |
| 40 | NMI | 1312 | -50 | 91 | SEG21 | -1312 | 960 | | | | |
| 41 | P00 | 1312 | 30 | 92 | SEG22 | -1312 | 880 | | | | |
| 42 | P01 | 1312 | 110 | 93 | SEG23 | -1312 | 800 | | | | |
| 43 | P02 | 1312 | 190 | 94 | SEG24 | -1312 | 720 | | | | |
| 44 | P03 | 1312 | 270 | 95 | SEG25 | -1312 | 640 | | | | |
| 45 | VSS | 1312 | 350 | 96 | SEG26 | -1312 | 560 | | | | |
| 46 | VDD | 1312 | 430 | 97 | SEG27 | -1312 | 480 | | | | |
| 47 | VSS | 1312 | 510 | 98 | SEG28 | -1312 | 400 | | | | |
| 48 | (NC) | - | - | 99 | SEG29 | -1312 | 320 | | | | |
| 49 | (NC) | - | - | 100 | SEG30 | -1312 | 240 | | | | |
| 50 | (NC) | - | - | | | | | | | | |

ML610Q412 Pad Coordinates

Table 2 ML610Q412 Pad Coordinates

Chip Center: X=0,Y=0

| PAD No. | Pad Name | X (μm) | Y (μm) | PAD No. | Pad Name | X (μm) | Y (μm) | PAD No. | Pad Name | X (μm) | Y (μm) |
|---------|----------|--------|--------|---------|----------|--------|--------|---------|----------|--------|--------|
| 1 | VPP | -1230 | -1212 | 51 | (NC) | - | - | 101 | SEG31 | -1312 | 160 |
| 2 | VSS | -1150 | -1212 | 52 | (NC) | - | - | 102 | SEG32 | -1312 | 80 |
| 3 | P20 | -1070 | -1212 | 53 | (NC) | - | - | 103 | SEG33 | -1312 | 0 |
| 4 | P21 | -990 | -1212 | 54 | (NC) | - | - | 104 | SEG34 | -1312 | -80 |
| 5 | P22 | -910 | -1212 | 55 | (NC) | - | - | 105 | SEG35 | -1312 | -160 |
| 6 | P40 | -830 | -1212 | 56 | (NC) | - | - | 106 | SEG43 | -1312 | -240 |
| 7 | P41 | -750 | -1212 | 57 | (NC) | - | - | 107 | SEG42 | -1312 | -320 |
| 8 | RESET_N | -670 | -1212 | 58 | (NC) | - | - | 108 | SEG41 | -1312 | -400 |
| 9 | P42 | -590 | -1212 | 59 | (NC) | - | - | 109 | SEG40 | -1312 | -480 |
| 10 | P43 | -510 | -1212 | 60 | (NC) | - | - | 110 | SEG39 | -1312 | -560 |
| 11 | P44 | -430 | -1212 | 61 | C2 | 1220 | 1212 | 111 | SEG38 | -1312 | -640 |
| 12 | P45 | -350 | -1212 | 62 | C1 | 1140 | 1212 | 112 | SEG37 | -1312 | -720 |
| 13 | P46 | -270 | -1212 | 63 | VL3 | 1060 | 1212 | 113 | SEG36 | -1312 | -800 |
| 14 | P47 | -190 | -1212 | 64 | VL2 | 980 | 1212 | - | Dummy | -1312 | -908 |
| 15 | P30 | -110 | -1212 | 65 | VL1 | 900 | 1212 | | | | |
| 16 | P31 | -30 | -1212 | 66 | COM3 | 820 | 1212 | | | | |
| 17 | P34 | 50 | -1212 | 67 | COM2 | 740 | 1212 | | | | |
| 18 | P32 | 130 | -1212 | 68 | COM1 | 660 | 1212 | | | | |
| 19 | P33 | 210 | -1212 | 69 | COM0 | 580 | 1212 | | | | |
| 20 | P35 | 290 | -1212 | 70 | SEG0 | 500 | 1212 | | | | |
| 21 | TEST | 370 | -1212 | 71 | SEG1 | 420 | 1212 | | | | |
| 22 | VDD | 450 | -1212 | 72 | SEG2 | 340 | 1212 | | | | |
| 23 | VDDL | 530 | -1212 | 73 | SEG3 | 260 | 1212 | | | | |
| 24 | VSS | 610 | -1212 | 74 | SEG4 | 180 | 1212 | | | | |
| 25 | VDDX | 690 | -1212 | 75 | SEG5 | 100 | 1212 | | | | |
| 26 | XT1 | 770 | -1212 | 76 | SEG6 | 20 | 1212 | | | | |
| - | Dummy | 850 | -1212 | 77 | SEG7 | -60 | 1212 | | | | |
| 27 | XT0 | 930 | -1212 | 78 | SEG8 | -140 | 1212 | | | | |
| 28 | AVSS | 1030 | -1212 | 79 | SEG9 | -220 | 1212 | | | | |
| 29 | VREF | 1110 | -1212 | 80 | SEG10 | -300 | 1212 | | | | |
| 30 | AVDD | 1190 | -1212 | 81 | SEG11 | -380 | 1212 | | | | |
| 31 | (NC) | - | - | 82 | SEG12 | -460 | 1212 | | | | |
| 32 | (NC) | - | - | 83 | SEG13 | -540 | 1212 | | | | |
| 33 | (NC) | - | - | 84 | SEG14 | -620 | 1212 | | | | |
| 34 | (NC) | - | - | 85 | SEG15 | -700 | 1212 | | | | |
| 35 | AIN0 | 1312 | -522 | 86 | SEG16 | -780 | 1212 | | | | |
| 36 | AIN1 | 1312 | -350 | 87 | SEG17 | -860 | 1212 | | | | |
| 37 | (NC) | - | - | 88 | SEG18 | -940 | 1212 | | | | |
| 38 | P10 | 1312 | -210 | 89 | SEG19 | -1020 | 1212 | | | | |
| 39 | P11 | 1312 | -130 | 90 | SEG20 | -1100 | 1212 | | | | |
| 40 | NMI | 1312 | -50 | 91 | SEG21 | -1312 | 960 | | | | |
| 41 | P00 | 1312 | 30 | 92 | SEG22 | -1312 | 880 | | | | |
| 42 | P01 | 1312 | 110 | 93 | SEG23 | -1312 | 800 | | | | |
| 43 | P02 | 1312 | 190 | 94 | SEG24 | -1312 | 720 | | | | |
| 44 | P03 | 1312 | 270 | 95 | SEG25 | -1312 | 640 | | | | |
| 45 | VSS | 1312 | 350 | 96 | SEG26 | -1312 | 560 | | | | |
| 46 | VDD | 1312 | 430 | 97 | SEG27 | -1312 | 480 | | | | |
| 47 | VSS | 1312 | 510 | 98 | SEG28 | -1312 | 400 | | | | |
| 48 | (NC) | - | - | 99 | SEG29 | -1312 | 320 | | | | |
| 49 | (NC) | - | - | 100 | SEG30 | -1312 | 240 | | | | |
| 50 | (NC) | - | - | | | | | | | | |

PIN LIST

| PAD No. | Primary function | | | Secondary function | | | Tertiary function | | |
|----------------|------------------|-----|---|--------------------|-----|----------|-------------------|-----|----------|
| | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function |
| 2, 24,45,47 | V _{SS} | — | Negative power supply pin | — | — | — | — | — | — |
| 22, 46 | V _{DD} | — | Positive power supply pin | — | — | — | — | — | — |
| 23 | V _{DDL} | — | Power supply pin for internal logic (internally generated) | — | — | — | — | — | — |
| 25 | V _{DDX} | — | Power supply pin for low-speed oscillation (internally generated) | — | — | — | — | — | — |
| 1 | V _{PP} | — | Power supply pin for Flash ROM | — | — | — | — | — | — |
| 28 | AV _{SS} | — | Negative power supply pin for successive approximation type ADC | — | — | — | — | — | — |
| 30 | AV _{DD} | — | Positive power supply pin for successive approximation type ADC | — | — | — | — | — | — |
| 65 | V _{L1} | — | Power supply pin for LCD bias (internally generated) | — | — | — | — | — | — |
| 64 | V _{L2} | — | Power supply pin for LCD bias (internally generated) | — | — | — | — | — | — |
| 63 | V _{L3} | — | Power supply pin for LCD bias (internally generated) | — | — | — | — | — | — |
| 62 | C1 | — | Capacitor connection pin for LCD bias generation | — | — | — | — | — | — |
| 61 | C2 | — | Capacitor connection pin for LCD bias generation | — | — | — | — | — | — |
| 21 | TEST | I/O | Input/output pin for testing | — | — | — | — | — | — |
| 8 | RESET_N | I | Reset input pin | — | — | — | — | — | — |
| 27 | XT0 | I | Low-speed clock oscillation pin | — | — | — | — | — | — |
| 26 | XT1 | O | Low-speed clock oscillation pin | — | — | — | — | — | — |
| 29 | V _{REF} | — | Reference power supply pin for successive approximation type ADC | — | — | — | — | — | — |

| PAD No. | Primary function | | | Secondary function | | | Tertiary function | | |
|---------|-------------------|-----|--|--------------------|-----|---|-------------------|-----|-------------------------|
| | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function |
| 35 | AIN0 | I | Successive approximation type ADC input | — | — | — | — | — | — |
| 36 | AIN1 | I | Successive approximation type ADC input | — | — | — | — | — | — |
| 40 | NMI | I | Non-maskable interrupt pin | — | — | — | — | — | — |
| 41 | P00/EXI0/ CAP0 | I | Input port, External interrupt 0, Capture 0 input | — | — | — | — | — | — |
| 42 | P01/EXI1/ CAP1 | I | Input port, External interrupt 1, Capture 1 input | — | — | — | — | — | — |
| 43 | P02/EXI2/ RXD0 | I | Input port, External interrupt 2, UART0 receive | — | — | — | — | — | — |
| 44 | P03/EXI3 | I | Input port, External interrupt 3 | — | — | — | — | — | — |
| 38 | P10 OSC0 | I | Input port External clock input | — | — | — | — | — | — |
| 39 | P11 | I | Input port | — | — | — | — | — | — |
| 3 | P20/LED0 | O | Output port | LSCLK | O | Low-speed clock output | — | — | — |
| 4 | P21/LED1 | O | Output port | OUTCLK | O | High-speed clock output | — | — | — |
| 5 | P22/LED2 | O | Output port | MD0 | O | Melody output | — | — | — |
| 15 | P30 | I/O | Input/output port | IN0 | I | RC type ADC0 oscillation input pin | — | — | — |
| 16 | P31 | I/O | Input/output port | CS0 | O | RC type ADC0 reference capacitor connection pin | — | — | — |
| 17 | P34 | I/O | Input/output port | RCT0 | O | RC type ADC0 resistor/capacitor sensor connection pin | PWM0 | O | PWM output |
| 18 | P32 | I/O | Input/output port | RS0 | O | RC type ADC0 reference resistor connection pin | — | — | — |
| 19 | P33 | I/O | Input/output port | RT0 | O | RC type ADC0 resistor sensor connection pin | — | — | — |
| 20 | P35 | I/O | Input/output port | RCM | O | RC type ADC oscillation monitor | — | — | — |
| 6 | P40 | I/O | Input/output port | SDA | I/O | I ² C data input/output | SIN0 | I | SSIO data input |
| 7 | P41 | I/O | Input/output port | SCL | I/O | I ² C clock input/output | SCK0 | I/O | SSIO synchronous clock |
| 9 | P42 | I/O | Input/output port | RXD0 | I | UART data input | SOUT0 | I | SSIO data output |
| 10 | P43 | I/O | Input/output port | TXD0 | O | UART data output | PWM0 | O | PWM output |
| 11 | P44/T02P0 CK | I/O | Input/output port, Timer 0/Timer 2/PWM0 external clock input | IN1 | I | RC type ADC1 oscillation input pin | SIN0 | I | SSIO0 data input |
| 12 | P45/T13P1 CK | I/O | Input/output port, Timer 1/Timer 3 external clock input | CS1 | O | RC type ADC1 reference capacitor connection pin | SCK0 | I/O | SSIO0 synchronous clock |
| 13 | P46 | I/O | Input/output port | RS1 | O | RC type ADC1 reference resistor connection pin | SOUT0 | O | SSIO0 data output |
| 14 | P47 | I/O | Input/output port | RT1 | O | RC type ADC1 resistor sensor connection pin | — | — | — |
| 106 | PA0(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG43(*2) | O | LCD segment pin | — | — | — | — | — | — |
| 107 | PA1(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG42(*2) | O | LCD segment pin | — | — | — | — | — | — |
| 108 | PA2(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG41(*2) | O | LCD segment pin | — | — | — | — | — | — |
| 109 | PA3(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG40(*2) | O | LCD segment pin | — | — | — | — | — | — |

| PAD No. | Primary function | | | Secondary function | | | Tertiary function | | |
|---------|-----------------------|-----|-------------------|--------------------|-----|----------|-------------------|-----|----------|
| | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function |
| 110 | PA4 ^(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG39 ^(*2) | O | LCD segment pin | — | — | — | — | — | — |
| 111 | PA5 ^(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG38 ^(*2) | O | LCD segment pin | — | — | — | — | — | — |
| 112 | PA6 ^(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG37 ^(*2) | O | LCD segment pin | — | — | — | — | — | — |
| 113 | PA7 ^(*1) | I/O | Input/output port | — | — | — | — | — | — |
| | SEG36 ^(*2) | O | LCD segment pin | — | — | — | — | — | — |
| 69 | COM0 | O | LCD common pin | — | — | — | — | — | — |
| 68 | COM1 | O | LCD common pin | — | — | — | — | — | — |
| 67 | COM2 | O | LCD common pin | — | — | — | — | — | — |
| 66 | COM3 | O | LCD common pin | — | — | — | — | — | — |
| 70 | SEG0 | O | LCD segment pin | — | — | — | — | — | — |
| 71 | SEG1 | O | LCD segment pin | — | — | — | — | — | — |
| 72 | SEG2 | O | LCD segment pin | — | — | — | — | — | — |
| 73 | SEG3 | O | LCD segment pin | — | — | — | — | — | — |
| 74 | SEG4 | O | LCD segment pin | — | — | — | — | — | — |
| 75 | SEG5 | O | LCD segment pin | — | — | — | — | — | — |
| 76 | SEG6 | O | LCD segment pin | — | — | — | — | — | — |
| 77 | SEG7 | O | LCD segment pin | — | — | — | — | — | — |
| 78 | SEG8 | O | LCD segment pin | — | — | — | — | — | — |
| 79 | SEG9 | O | LCD segment pin | — | — | — | — | — | — |
| 80 | SEG10 | O | LCD segment pin | — | — | — | — | — | — |
| 81 | SEG11 | O | LCD segment pin | — | — | — | — | — | — |
| 82 | SEG12 | O | LCD segment pin | — | — | — | — | — | — |
| 83 | SEG13 | O | LCD segment pin | — | — | — | — | — | — |
| 84 | SEG14 | O | LCD segment pin | — | — | — | — | — | — |
| 85 | SEG15 | O | LCD segment pin | — | — | — | — | — | — |
| 86 | SEG16 | O | LCD segment pin | — | — | — | — | — | — |
| 87 | SEG17 | O | LCD segment pin | — | — | — | — | — | — |
| 88 | SEG18 | O | LCD segment pin | — | — | — | — | — | — |
| 89 | SEG19 | O | LCD segment pin | — | — | — | — | — | — |
| 90 | SEG20 | O | LCD segment pin | — | — | — | — | — | — |
| 91 | SEG21 | O | LCD segment pin | — | — | — | — | — | — |
| 92 | SEG22 | O | LCD segment pin | — | — | — | — | — | — |
| 93 | SEG23 | O | LCD segment pin | — | — | — | — | — | — |
| 94 | SEG24 | O | LCD segment pin | — | — | — | — | — | — |
| 95 | SEG25 | O | LCD segment pin | — | — | — | — | — | — |
| 96 | SEG26 | O | LCD segment pin | — | — | — | — | — | — |
| 97 | SEG27 | O | LCD segment pin | — | — | — | — | — | — |
| 98 | SEG28 | O | LCD segment pin | — | — | — | — | — | — |
| 99 | SEG29 | O | LCD segment pin | — | — | — | — | — | — |
| 100 | SEG30 | O | LCD segment pin | — | — | — | — | — | — |
| 101 | SEG31 | O | LCD segment pin | — | — | — | — | — | — |
| 102 | SEG32 | O | LCD segment pin | — | — | — | — | — | — |
| 103 | SEG33 | O | LCD segment pin | — | — | — | — | — | — |
| 104 | SEG34 | O | LCD segment pin | — | — | — | — | — | — |
| 105 | SEG35 | O | LCD segment pin | — | — | — | — | — | — |

(^{*1}) Pins on ML610Q411.

(^{*2}) Pins on ML610Q412.

PIN DESCRIPTION

| Pin name | I/O | Description | Primary/ Secondary/ Tertiary | Logic |
|--|-----|---|------------------------------------|----------|
| System | | | | |
| RESET_N | I | Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected. | — | Negative |
| XT0 | I | Crystal connection pin for low-speed clock. | — | — |
| XT1 | O | A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V _{SS} as required. | — | — |
| OSC0 | I | High-speed external clock input pin. This pin is used as the secondary function of the P10. | Secondary | — |
| LSCLK | O | Low-speed clock output pin. This pin is used as the secondary function of the P20 pin. | Secondary | — |
| OUTCLK | O | High-speed clock output pin. This pin is used as the secondary function of the P21 pin. | Secondary | — |
| General-purpose input port | | | | |
| P00-P03 | I | General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. | Primary | Positive |
| P10-P11 | I | General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. | Primary | Positive |
| General-purpose output port | | | | |
| P20-P22 | O | General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. | Primary | Positive |
| General-purpose input/output port | | | | |
| P30-P35 | I/O | General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. | Primary | Positive |
| P40-P47 | I/O | General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. | Primary | Positive |
| PA0-PA7 | I/O | General-purpose input/output port. These pins are for the ML610Q411, but are not provided in the ML610Q412. | Primary | Positive |

| Pin name | I/O | Description | Primary/ Secondary/ Tertiary | Logic |
|-------------------------------------|-----|--|------------------------------------|-------------------|
| UART | | | | |
| TXD0 | O | UART data output pin. This pin is used as the secondary function of the P43 pin. | Secondary | Positive |
| RXD0 | I | UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin. | Primary/Secondary | Positive |
| I²C bus interface | | | | |
| SDA | I/O | I ² C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor. | Secondary | Positive |
| SCL | O | I ² C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor. | Secondary | Positive |
| Synchronous serial (SSIO) | | | | |
| SCK0 | I/O | Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin. | Tertiary | — |
| SIN0 | I | Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin. | Tertiary | Positive |
| SOUT0 | O | Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin. | Tertiary | Positive |
| PWM | | | | |
| PWM0 | O | PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin. | Tertiary | Positive |
| T02P0CK | O | PWM0 external clock input pin. This pin is used as the primary function of the P44 pin. | Primary | — |
| External interrupt | | | | |
| NMI | I | External non-maskable interrupt input pin. An interrupt is generated on both edges. | Primary | Positive/negative |
| EXI0-3 | I | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins. | Primary | Positive/negative |
| Capture | | | | |
| CAP0 | I | Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1). | Primary | Positive/negative |
| CAP1 | I | | Primary | Positive/negative |
| Timer | | | | |
| T02P0CK | I | External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin. | Primary | — |
| T13P1CK | I | External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin. | Primary | — |
| Buzzer | | | | |
| BZ0 | O | Buzzer signal output pin. This pin is used as the secondary function of the P22 pin. | Secondary | Positive/negative |
| LED drive | | | | |
| LED0-2 | O | Nch open drain output pins to drive LED. | Primary | Positive/negative |

| Pin name | I/O | Description | Primary/ Secondary/ Tertiary | Logic |
|--|-----|--|------------------------------------|-------|
| RC oscillation type A/D converter | | | | |
| IN0 | I | Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin. | Secondary | — |
| CS0 | O | Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin. | Secondary | — |
| RCT0 | O | Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin. | Secondary | — |
| RS0 | O | This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0. | Secondary | — |
| RT0 | O | Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin. | Secondary | — |
| RCM | O | RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin. | Secondary | — |
| IN1 | I | Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin. | Secondary | — |
| CS1 | O | Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin. | Secondary | — |
| RS1 | O | Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin. | Secondary | — |
| RT1 | O | Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin. | Secondary | — |
| Successive approximation type A/D converter | | | | |
| AV _{SS} | — | Negative power supply pin for successive approximation type A/D converter. | — | — |
| AV _{DD} | — | Positive power supply pin for successive approximation type A/D converter. | — | — |
| V _{REF} | — | Reference power supply pin for successive approximation type A/D converter. | — | — |
| AIN0 | I | Channel 0 analog input for successive approximation type A/D converter. | — | — |
| AIN1 | I | Channel 1 analog input for successive approximation type A/D converter. | — | — |
| LCD drive signal | | | | |
| COM0-3 | O | Common output pins. | — | — |
| SEG0-35 | O | Segment output pins. | — | — |
| SEG36-43 | O | Segment output pin. These pins are for the ML610Q412, but are not provided in the ML610Q411. | — | — |
| LCD driver power supply | | | | |
| V _{L1} | — | Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, and Cc (see measuring circuit 1) are connected between V _{SS} and V _{L1} , V _{L2} , and V _{L3} , respectively. | — | — |
| V _{L2} | — | | — | — |
| V _{L3} | — | | — | — |
| C1 | — | Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2. | — | — |
| C2 | — | | — | — |
| For testing | | | | |
| TEST | I/O | Input/output pin for testing. A pull-down resistor is internally connected. | — | — |
| Power supply | | | | |
| V _{SS} | — | Negative power supply pin. | — | — |
| V _{DD} | — | Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset. | — | — |
| V _{DDL} | — | Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V _{SS} . | — | — |
| V _{DDX} | — | Positive power supply pin (internally generated) for low-speed oscillation. When using ML610Q411 and ML610Q412, connect capacitor Cx (see measuring circuit 1) between this pin and V _{SS} . | — | — |
| V _{PP} | — | Power supply pin for programming Flash ROM. A pull-down resistor is internally connected. | — | — |

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

| Pin | Recommended pin termination |
|---|------------------------------------|
| V _{PP} | Open |
| AV _{DD} | V _{SS} |
| AV _{SS} | V _{SS} |
| V _{REF} | V _{SS} |
| AIN0, AIN1 | Open |
| V _{L1} , V _{L2} , V _{L3} | Open |
| C1, C2 | Open |
| RESET_N | Open |
| TEST | Open |
| NMI | Open |
| P00 to P03 | V _{DD} or V _{SS} |
| P10 to P11 | V _{DD} |
| P20 to P22 | Open |
| P30 to P35 | Open |
| P40 to P47 | Open |
| PA0 to PA7 | Open |
| COM0 to 3 | Open |
| SEG0 to 43 | Open |

Note:

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

| Parameter | Symbol | Condition | Rating | Unit |
|------------------------|-------------------|--------------------|------------------------------|------|
| Power supply voltage 1 | V _{DD} | Ta = 25°C | -0.3 to +4.6 | V |
| Power supply voltage 2 | AV _{DD} | Ta = 25°C | -0.3 to +4.6 | V |
| Power supply voltage 3 | V _{PP} | Ta = 25°C | -0.3 to +9.5 | V |
| Power supply voltage 4 | V _{DDL} | Ta = 25°C | -0.3 to +3.6 | V |
| Power supply voltage 5 | V _{DDX} | Ta = 25°C | -0.3 to +3.6 | V |
| Power supply voltage 6 | V _{L1} | Ta = 25°C | -0.3 to +1.75 | V |
| Power supply voltage 7 | V _{L2} | Ta = 25°C | -0.3 to +3.5 | V |
| Power supply voltage 8 | V _{L3} | Ta = 25°C | -0.3 to +5.25 | V |
| Input voltage | V _{IN} | Ta = 25°C | -0.3 to V _{DD} +0.3 | V |
| Output voltage | V _{OUT} | Ta = 25°C | -0.3 to V _{DD} +0.3 | V |
| Output current 1 | I _{OUT1} | Port3-A, Ta = 25°C | -12 to +11 | mA |
| Output current 2 | I _{OUT2} | Port2, Ta = 25°C | -12 to +20 | mA |
| Power dissipation | PD | Ta = 25°C | 1.25 | W |
| Storage temperature | T _{STG} | — | -55 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|----------------------|--|------------------------------|------|
| Operating temperature | T _{OP} | ML610Q411, ML610Q412, | -20 to +70 | °C |
| | | ML610Q411P, ML610Q411PA, ML610Q412P | -40 to +85 | |
| Operating voltage | V _{DD} | — | 1.1 to 3.6 | V |
| | AV _{DD} | — | 2.2 to 3.6 | |
| Operating frequency (CPU) | f _{OP} | V _{DD} = 1.1 to 3.6V | 30k to 36k 46.9k to 78.1k | Hz |
| | | V _{DD} = 1.3 to 3.6V | 30k to 625k 23k to 625k | |
| Capacitor externally connected to V _{DDL} pin | C _{L0} | — | 1.0±30% | μF |
| | C _{L1} | — | 0.1±30% | |
| Capacitor externally connected to V _{DDX} pin | C _X | — | 0.1±30% | μF |
| Capacitors externally connected to V _{L1, 2, 3} pins | C _{1, 2, 3} | — | 1.0±30% | μF |
| Capacitors externally connected across C1 and C2 pins | C ₁₂ | — | 1.0±30% | μF |

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|----------------------------------|--|--------|---------|------|------|
| | | | Min. | Typ. | Max. | |
| Low-speed crystal oscillation frequency | f _{XTL} | — | — | 32.768k | — | Hz |
| Recommended equivalent series resistance value of low-speed crystal oscillation | R _L | — | — | — | 40k | Ω |
| Low-speed crystal oscillation external capacitor ^{*1} | C _{DL} /C _{GL} | C _L =6pF of crystal oscillation ^{*2} | — | 0 | — | pF |
| | | C _L =9pF of crystal oscillation | — | 6 | — | |
| | | C _L =12pF of crystal oscillation | — | 12 | — | |
| | C _{GH} | — | — | 24 | — | |

^{*1}: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.

^{*2}: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = AV_{SS} = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|-----------------------|------------------|------------------------------|-------------|--------|
| Operating temperature | T _{OP} | At write/erase | 0 to +40 | °C |
| Operating voltage | V _{DD} | At write/erase ^{*1} | 2.75 to 3.6 | V |
| | V _{DDL} | At write/erase ^{*1} | 2.5 to 2.75 | |
| | V _{PP} | At write/erase ^{*1} | 7.7 to 8.3 | |
| Write cycles | C _{EP} | — | 80 | cycles |
| Data retention | Y _{DR} | — | 10 | years |

^{*1}: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and erasing Flash ROM. V_{PP} pin has an internal pulldown resistor.

DC CHARACTERISTICS (1/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (1/5)

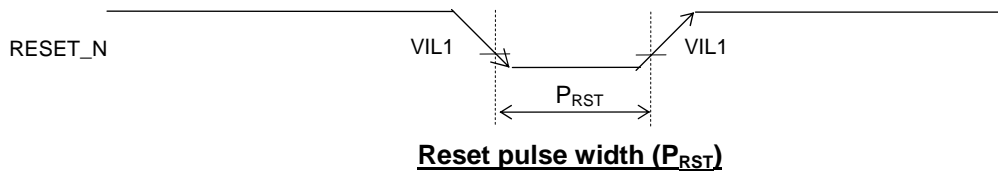
| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|--|------------|--------------------------|--------------------|-----------|------|-----------|-------------------|
| | | | Min. | Typ. | Max. | | |
| 500kHz RC oscillation frequency | f_{RC} | $V_{DD} = 1.3$ to $3.6V$ | $T_a = 25^\circ C$ | Typ. -10% | 500 | Typ. +10% | kHz |
| | | | *3 | Typ. -25% | 500 | Typ. +25% | |
| Low-speed crystal oscillation start time*2 | T_{XTL} | — | — | 0.3 | 2 | s | 1 |
| 500kHz RC oscillation start time | T_{RC} | — | — | 50 | 500 | μs | |
| Low-speed oscillation stop detect time*1 | T_{STOP} | — | 0.2 | 3 | 20 | ms | |
| Reset pulse width | P_{RST} | — | 200 | — | — | μs | |
| Reset noise elimination pulse width | P_{NRST} | — | — | — | 0.3 | | |
| Power-on reset activation power rise time | T_{POR} | — | — | — | 10 | ms | |

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

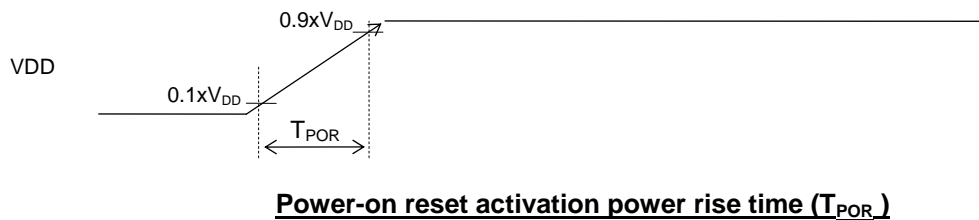
*2: Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance $C_{GL}/C_{DL} = 0pF$.

*3: Recommended operating temperature ($T_a = -40$ to $+85^\circ C$ for P version, $T_a = -20$ to $+70^\circ C$ for non-P version)

[Reset pulse width]



[Power-on reset activation power rise time]



DC CHARACTERISTICS (2/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (2/5)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit | |
|-----------------------------------|-----------------|---|--------------|-------------------|-------------|-------|-------------------|---|
| | | | Min. | Typ. | Max. | | | |
| V_{L1} voltage | V_{L1} | $V_{DD} = 3.0V$, $T_j = 25^\circ C$ | CN4-0 = 00H | 0.89 | 0.94 | 0.99 | V | 1 |
| | | | CN4-0 = 01H | 0.91 | 0.96 | 1.01 | | |
| | | | CN4-0 = 02H | 0.93 | 0.98 | 1.03 | | |
| | | | CN4-0 = 03H | 0.95 | 1.00 | 1.05 | | |
| | | | CN4-0 = 04H | 0.97 | 1.02 | 1.07 | | |
| | | | CN4-0 = 05H | 0.99 | 1.04 | 1.09 | | |
| | | | CN4-0 = 06H | 1.01 | 1.06 | 1.11 | | |
| | | | CN4-0 = 07H | 1.03 | 1.08 | 1.13 | | |
| | | | CN4-0 = 08H | 1.05 | 1.10 | 1.15 | | |
| | | | CN4-0 = 09H | 1.07 | 1.12 | 1.17 | | |
| | | | CN4-0 = 0AH | 1.09 | 1.14 | 1.19 | | |
| | | | CN4-0 = 0BH | 1.11 | 1.16 | 1.21 | | |
| | | | CN4-0 = 0CH | 1.13 | 1.18 | 1.23 | | |
| | | | CN4-0 = 0DH | 1.15 | 1.20 | 1.25 | | |
| | | | CN4-0 = 0EH | 1.17 | 1.22 | 1.27 | | |
| | | | CN4-0 = 0FH | 1.19 | 1.24 | 1.29 | | |
| | | | CN4-0 = 10H | 1.21 | 1.26 | 1.31 | | |
| | | | CN4-0 = 11H | 1.23 | 1.28 | 1.33 | | |
| | | | CN4-0 = 12H | 1.25 | 1.30 | 1.35 | | |
| | | | CN4-0 = 13H | 1.27 | 1.32 | 1.37 | | |
| | | | CN4-0 = 14H | 1.29 | 1.34 | 1.39 | | |
| | | | CN4-0 = 15H | 1.31 | 1.36 | 1.41 | | |
| | | | CN4-0 = 16H | 1.33 | 1.38 | 1.43 | | |
| | | | CN4-0 = 17H | 1.35 | 1.40 | 1.45 | | |
| CN4-0 = 18H | 1.37 | 1.42 | 1.47 | | | | | |
| CN4-0 = 19H | 1.39 | 1.44 | 1.49 | | | | | |
| CN4-0 = 1AH | 1.41 | 1.46 | 1.51 | | | | | |
| CN4-0 = 1BH | 1.43 | 1.48 | 1.53 | | | | | |
| CN4-0 = 1CH | 1.45 | 1.50 | 1.55 | | | | | |
| CN4-0 = 1DH | 1.47 | 1.52 | 1.57 | | | | | |
| CN4-0 = 1EH | 1.49 | 1.54 | 1.59 | | | | | |
| CN4-0 = 1FH | 1.51 | 1.56 | 1.61 | | | | | |
| V_{L1} temperature deviation *1 | ΔV_{L1} | $V_{DD} = 3.0V$ | — | -1.5 | — | mV/°C | | |
| V_{L1} voltage dependency *1 | ΔV_{L1} | $V_{DD} = 1.3$ to $3.6V$ | — | 5 | 20 | mV/V | | |
| V_{L2} voltage | V_{L2} | $V_{DD} = 3.0V$, $T_j = 25^\circ C$ $1M\Omega$ load ($V_{L3} - V_{SS}$) | Typ. -10% | $V_{L1} \times 2$ | Typ. +4% | V | | |
| V_{L3} voltage | V_{L3} | | Typ. -10% | $V_{L1} \times 3$ | Typ. +4% | | | |
| LCD bias voltage generation time | T_{BIAS} | — | — | — | 600 | ms | | |

*1: V_{L1} can not exceed V_{DD} level. The maximum V_{L1} becomes V_{DD} level when the V_{L1} calculated by the temperature deviation and voltage dependency is going to exceed the V_{DD} level.

DC CHARACTERISTICS (3/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (3/5)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit | |
|---|------------------|--|--------------------|-------------|------|-------------|-------------------|---|
| | | | Min. | Typ. | Max. | | | |
| BLD threshold voltage | V_{BLD} | $V_{DD} = 1.35$ to $3.6V$ | LD3-0 = 0H | Typ. -2% | 1.35 | Typ. +2% | V | 1 |
| | | | LD3-0 = 1H | | 1.4 | | | |
| | | | LD3-0 = 2H | | 1.45 | | | |
| | | | LD3-0 = 3H | | 1.5 | | | |
| | | | LD3-0 = 4H | | 1.6 | | | |
| | | | LD3-0 = 5H | | 1.7 | | | |
| | | | LD3-0 = 6H | | 1.8 | | | |
| | | | LD3-0 = 7H | | 1.9 | | | |
| | | | LD3-0 = 8H | | 2.0 | | | |
| | | | LD3-0 = 9H | | 2.1 | | | |
| | | | LD3-0 = 0AH | | 2.2 | | | |
| | | | LD3-0 = 0BH | | 2.3 | | | |
| | | | LD3-0 = 0CH | | 2.4 | | | |
| | | | LD3-0 = 0DH | | 2.5 | | | |
| LD3-0 = 0EH | 2.7 | | | | | | | |
| LD3-0 = 0FH | 2.9 | | | | | | | |
| BLD threshold voltage temperature deviation | ΔV_{BLD} | $V_{DD} = 1.35$ to $3.6V$ | — | 0 | — | %/°C | | |
| Supply current 1 | IDD1 | CPU: In STOP state. Low-speed/high-speed RC500kHz oscillation: stopped. | $T_a = 25^\circ C$ | — | 0.15 | 0.5 | μA | |
| | | | *5 | — | — | 2.5 | | |
| Supply current 2 | IDD2 | CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped). ^{*3*4} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Stopped. | $T_a = 25^\circ C$ | — | 0.5 | 1.3 | μA | |
| | | | *5 | — | — | 3.5 | | |
| Supply current 3 | IDD3 | CPU: In HALT state (LTBC and WDT are Operating. Low speed oscillation stop detector is Stopped). ^{*3} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. ^{*2} | $T_a = 25^\circ C$ | — | 1.28 | 1.6 | μA | 1 |
| | | | *5 | — | — | 11 | | |
| Supply current 4 | IDD4 | CPU: In 32.768kHz operating state. ^{*1*3} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. ^{*2} | $T_a = 25^\circ C$ | — | 5.5 | 7 | μA | |
| | | | *5 | — | — | 12 | | |
| Supply current 5 | IDD5 | CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. ^{*2} | $T_a = 25^\circ C$ | — | 80 | 90 | μA | |
| | | | *5 | — | — | 100 | | |
| Supply current 6 | IDD6 | CPU: In RC 500kHz operating state. ^{*2} LCD and BIAS circuits: Operating. ^{*2} A/D: In operating state. $V_{DD} = AV_{DD} = 3.0V$ | $T_a = 25^\circ C$ | — | 0.4 | 0.5 | mA | 1 |
| | | | *5 | — | — | 0.6 | | |

*1: When the CPU operating rate is 100% (No HALT state).

*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

*3: Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance $C_{GL}/C_{DL} = 0pF$.

*4: Significant bits of BLKCON0~BLKCON4 registers are all "1".

*5: Recommended operating temperature ($T_a = -40$ to $+85^\circ C$ for P version, $T_a = -20$ to $+70^\circ C$ for non-P version)

DC CHARACTERISTICS (4/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (4/5)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit | | |
|---|---------------------------------------|---|--------------------------|------|------------------|---------|-------------------|------|---|
| | | | Min. | Typ. | Max. | | | | |
| Output voltage 1 (P20–P22/2 nd function is selected) (P30–P36) (P40–P47) (PB0–PB7) ^{*1} | VOH1 | IOH1 = -0.5mA, $V_{DD} = 1.8$ to $3.6V$ | V_{DD} -0.5 | — | — | V | 2 | | |
| | | IOH1 = -0.1mA, $V_{DD} = 1.3$ to $3.6V$ | V_{DD} -0.3 | — | — | | | | |
| | | IOH1 = -0.03mA, $V_{DD} = 1.1$ to $3.6V$ | V_{DD} -0.3 | — | — | | | | |
| | VOL1 | IOL1 = +0.5mA, $V_{DD} = 1.8$ to $3.6V$ | — | — | 0.5 | | | | |
| | | IOL1 = +0.1mA, $V_{DD} = 1.3$ to $3.6V$ | — | — | 0.5 | | | | |
| | | IOL1 = +0.03mA, $V_{DD} = 1.1$ to $3.6V$ | — | — | 0.3 | | | | |
| Output voltage 2 (P20–P22/2 nd function is Not selected) | VOH1 | IOH1 = -0.5mA, $V_{DD} = 1.8$ to $3.6V$ | V_{DD} -0.5 | — | — | V | 2 | | |
| | | IOH1 = -0.1mA, $V_{DD} = 1.3$ to $3.6V$ | V_{DD} -0.3 | — | — | | | | |
| | | IOH1 = -0.03mA, $V_{DD} = 1.1$ to $3.6V$ | V_{DD} -0.3 | — | — | | | | |
| VOL2 | IOL2 = +5mA, $V_{DD} = 1.8$ to $3.6V$ | — | — | 0.5 | | | | | |
| Output voltage 3 (P40–P41) | VOL3 | IOL3 = +3mA, $V_{DD} = 2.0$ to $3.6V$ (when I ² C mode is selected) | — | — | 0.4 | | | V | 2 |
| Output voltage 4 (COM0–3) (SEG0–35) ^{*1} (SEG0–43) ^{*2} | VOH4 | IOH4 = -0.2mA, $V_{L1}=1.2V$ | V_{L3} -0.2 | — | — | | | | |
| | VOMH4 | IOMH4 = +0.2mA, $V_{L1}=1.2V$ | — | — | V_{L2} +0.2 | | | | |
| | VOM4S | IOM4S = -0.2mA, $V_{L1}=1.2V$ | V_{L2} -0.2 | — | — | | | | |
| | VOML4 | IOML4 = +0.2mA, $V_{L1}=1.2V$ | — | — | V_{L1} +0.2 | | | | |
| | VOML4S | IOML4S = -0.2mA, $V_{L1}=1.2V$ | V_{L1} -0.2 | — | — | | | | |
| | VOL4 | IOL4 = +0.2mA, $V_{L1}=1.2V$ | — | — | 0.2 | | | | |
| Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA7) ^{*1} | IOOH | VOH = V_{DD} (in high-impedance state) | — | — | 1 | μA | 3 | | |
| | IOOL | VOL = V_{SS} (in high-impedance state) | -1 | — | — | | | | |
| Input current 1 (RESET_N) | IIH1 | $V_{IH1} = V_{DD}$ | 0 | — | 1 | μA | 4 | | |
| | IIL1 | $V_{IL1} = V_{SS}$ | $V_{DD} = 1.3$ to $3.6V$ | -600 | -300 | | | -10 | |
| $V_{DD} = 1.1$ to $3.6V$ | | | -600 | -300 | -2 | | | | |
| Input current 1 (TEST) | IIH1 | $V_{IH1} = V_{DD}$ | $V_{DD} = 1.3$ to $3.6V$ | 10 | 300 | | | 600 | |
| | | | $V_{DD} = 1.1$ to $3.6V$ | 2 | 300 | | | 600 | |
| IIL1 | $V_{IL1} = V_{SS}$ | $V_{DD} = 1.3$ to $3.6V$ | 0.2 | 30 | 200 | | | | |
| | | $V_{DD} = 1.1$ to $3.6V$ | 0.01 | 30 | 200 | | | | |
| Input current 2 (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7) ^{*1} | IIL2 | $V_{IL2} = V_{SS}$ (when pulled-up) | $V_{DD} = 1.3$ to $3.6V$ | -200 | -30 | | | -0.2 | |
| | | | $V_{DD} = 1.1$ to $3.6V$ | -200 | -30 | -0.01 | | | |
| | IIH2Z | $V_{IH2} = V_{DD}$ (in high-impedance state) | — | — | 1 | | | | |
| | IIL2Z | $V_{IL2} = V_{SS}$ (in high-impedance state) | -1 | — | — | | | | |

*1: ML610Q411

*2: ML610Q412

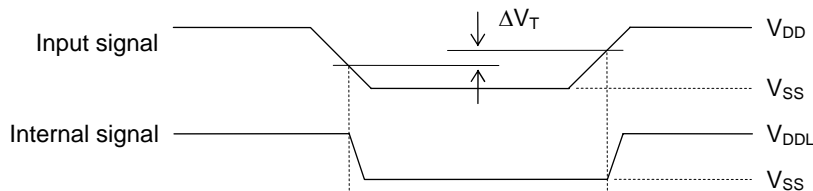
DC CHARACTERISTICS (5/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (5/5)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|--|--------------|---|----------------------|----------------------|---------------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7) ^{*1} | VIH1 | $V_{DD} = 1.3$ to $3.6V$ | $0.7 \times V_{DD}$ | — | V_{DD} | V | 5 |
| | | $V_{DD} = 1.1$ to $3.6V$ | $0.7 \times V_{DD}$ | — | V_{DD} | | |
| | VIL1 | $V_{DD} = 1.3$ to $3.6V$ | 0 | — | $0.3 \times V_{DD}$ | | |
| | | $V_{DD} = 1.1$ to $3.6V$ | 0 | — | $0.2 \times V_{DD}$ | | |
| Hysteresis width (RESET_N) (TEST_N) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7) ^{*1} | ΔV_T | $V_{DD} = 2.0$ to $3.6V$ | $0.05 \times V_{DD}$ | $0.18 \times V_{DD}$ | $0.4 \times V_{DD}$ | V | 5 |
| | | $V_{DD} = 1.1$ to $3.6V$ | $0.02 \times V_{DD}$ | $0.18 \times V_{DD}$ | $0.4 \times V_{DD}$ | | |
| Input voltage 2 (P30, P44) | VIH2 | — | $0.7 \times V_{DD}$ | — | V_{DD} | pF | — |
| | VIL2 | — | 0 | — | $0.3 \times V_{DD}$ | | |
| Input pin capacitance (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7) ^{*1} | CIN | $f = 10kHz$ $V_{rms} = 50mV$ $T_a = 25^\circ C$ | — | — | 5 | pF | — |

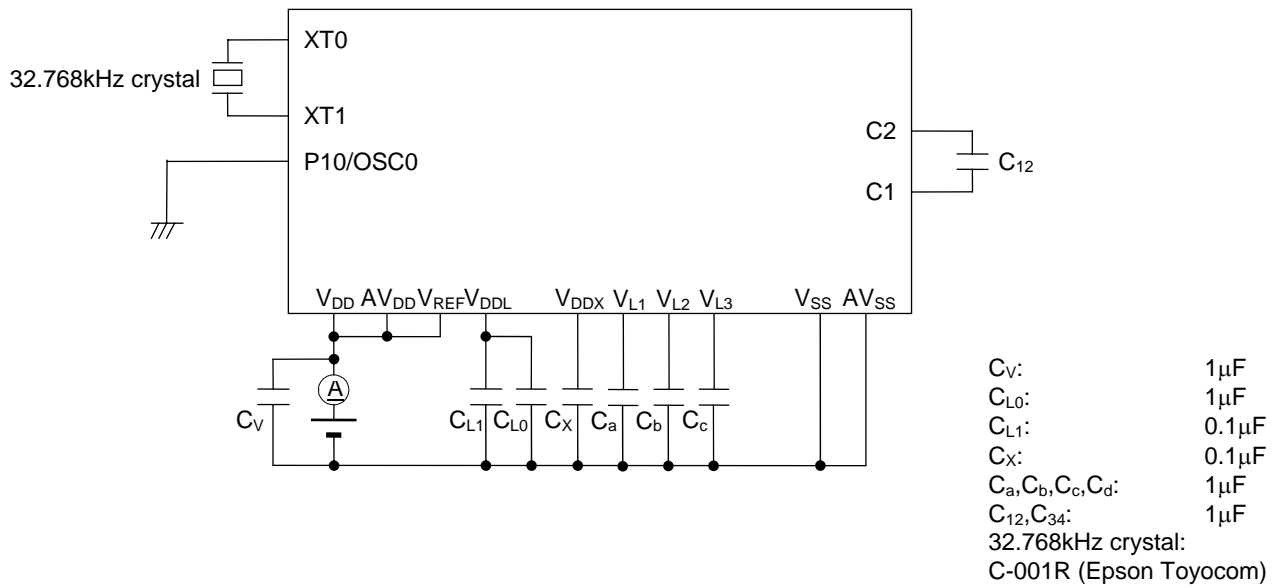
*1: ML610Q411

HYSTERESIS WIDTH

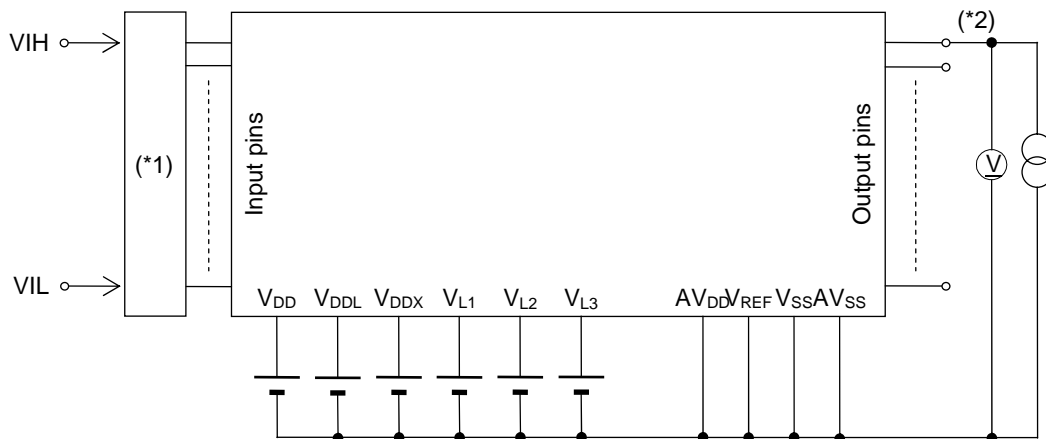


MEASURING CIRCUITS

MEASURING CIRCUIT 1



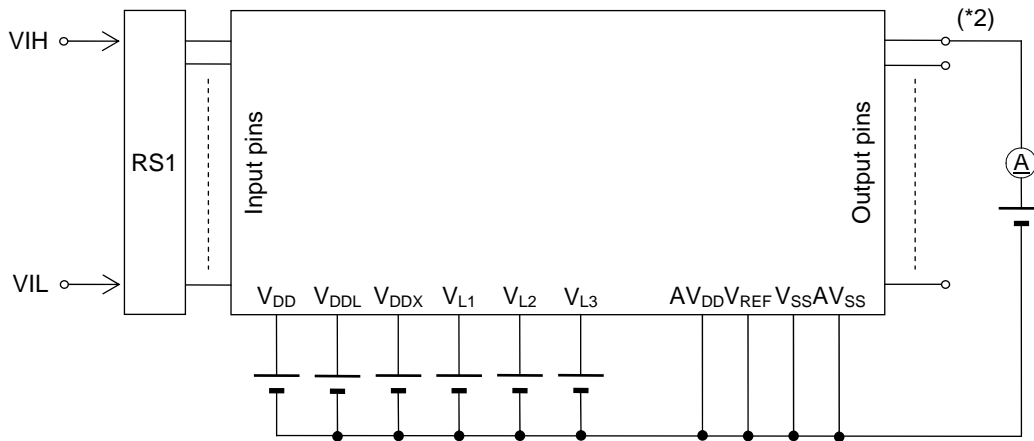
MEASURING CIRCUIT 2



(*1) Input logic circuit to determine the specified measuring conditions.

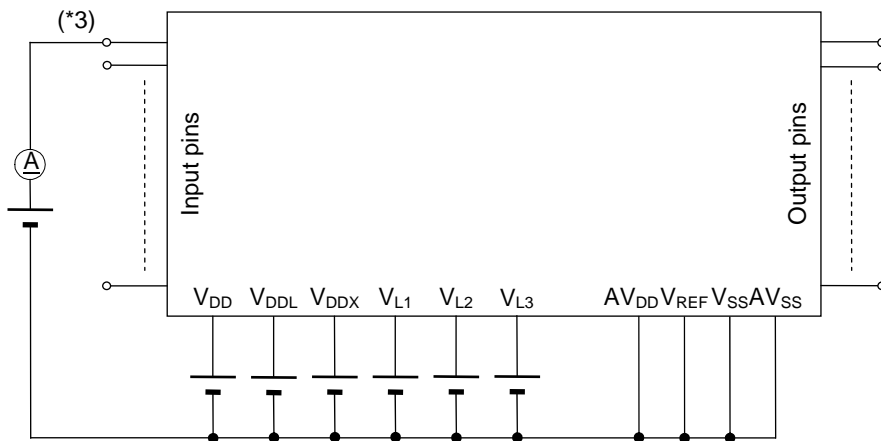
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



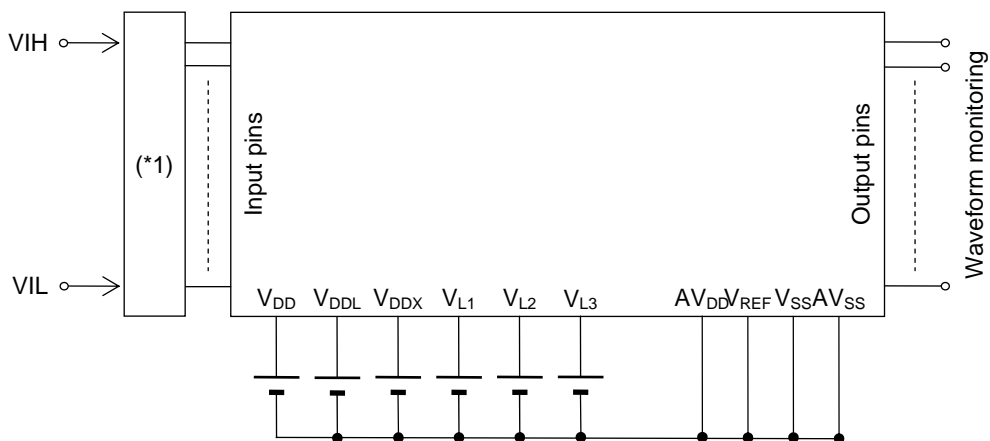
*1: Input logic circuit to determine the specified measuring conditions.
 *2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

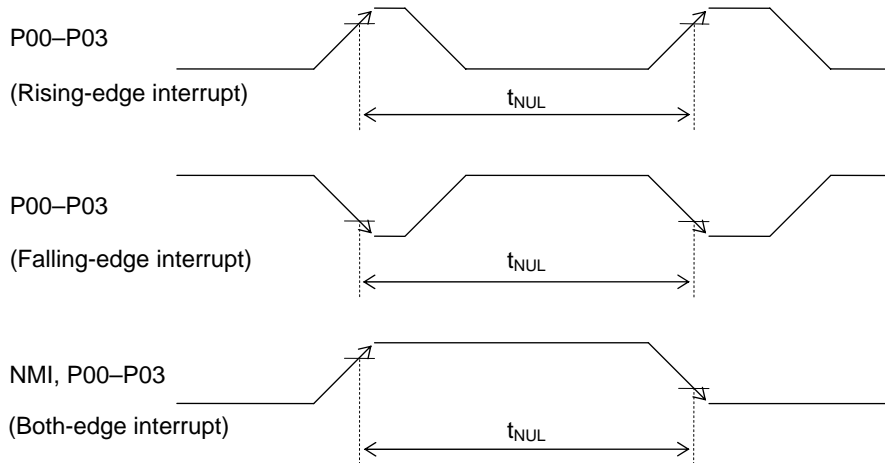


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|-----------------------------------|-----------|--|--------|------|-------|---------|
| | | | Min. | Typ. | Max. | |
| External interrupt disable period | T_{NUL} | Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz | 76.8 | — | 106.8 | μs |

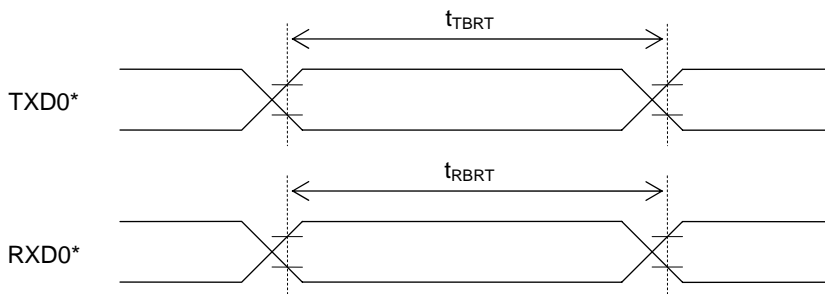


AC CHARACTERISTICS (Serial Port)

($V_{DD} = 1.3$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--------------------|------------|-----------|-------------------|------------|-------------------|------|
| | | | Min. | Typ. | Max. | |
| Transmit baud rate | t_{TBRT} | — | — | BRT^{*1} | — | s |
| Receive baud rate | t_{RBRT} | — | BRT^{*1} -3% | BRT^{*1} | BRT^{*1} +3% | s |

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



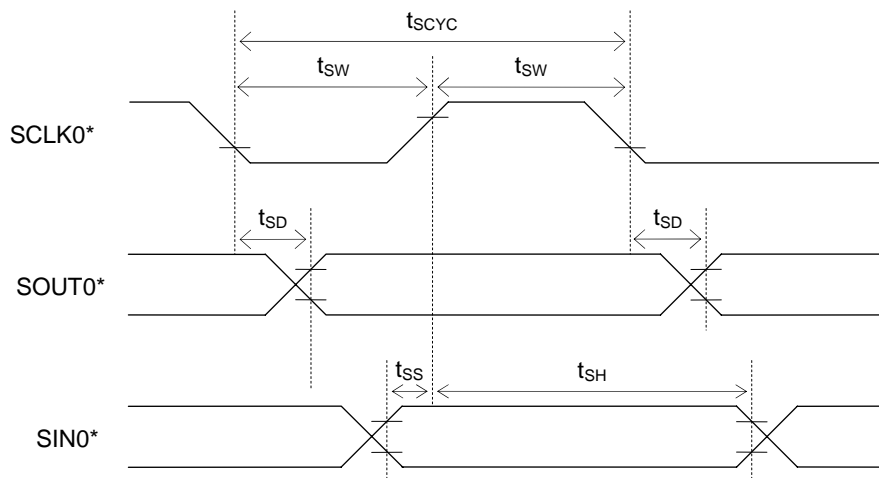
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

($V_{DD} = 1.3$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---------------------------------------|------------|---|------------------------|------------------------|------------------------|---------|
| | | | Min. | Typ. | Max. | |
| SCLK input cycle (slave mode) | t_{SCYC} | When high-speed oscillation is not active | 10 | — | — | μs |
| SCLK output cycle (master mode) | t_{SCYC} | — | — | $SCLK^{*1}$ | — | s |
| SCLK input pulse width (slave mode) | t_{SW} | When high-speed oscillation is not active | 4 | — | — | μs |
| SCLK output pulse width (master mode) | t_{SW} | — | $SCLK^{*1} \times 0.4$ | $SCLK^{*1} \times 0.5$ | $SCLK^{*1} \times 0.6$ | s |
| SOUT output delay time (slave mode) | t_{SD} | — | — | — | 500 | ns |
| SOUT output delay time (master mode) | t_{SD} | — | — | — | 500 | ns |
| SIN input setup time (slave mode) | t_{SS} | — | 80 | — | — | ns |
| SIN input setup time (master mode) | t_{SS} | — | 500 | — | — | ns |
| SIN input hold time | t_{SH} | — | 300 | — | — | ns |

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)

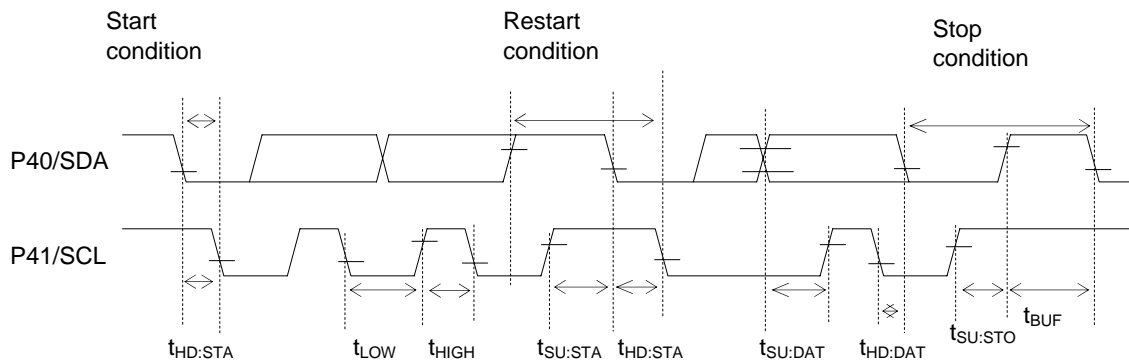


*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I²C Bus Interface: Standard Mode)

($V_{DD} = 1.8$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--|--------------|-----------|--------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | f_{SCL} | — | — | 50 | — | kHz |
| SCL hold time (start/restart condition) | $t_{HD:STA}$ | — | 4.0 | — | — | μs |
| SCL "L" level time | t_{LOW} | — | 4.7 | — | — | μs |
| SCL "H" level time | t_{HIGH} | — | 4.0 | — | — | μs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 4.7 | — | — | μs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | — | μs |
| SDA setup time | $t_{SU:DAT}$ | — | 0.25 | — | — | μs |
| SDA setup time (stop condition) | $t_{SU:STO}$ | — | 4.0 | — | — | μs |
| Bus-free time | t_{BUF} | — | 4.7 | — | — | μs |



AC CHARACTERISTICS (RC Oscillation A/D Converter)

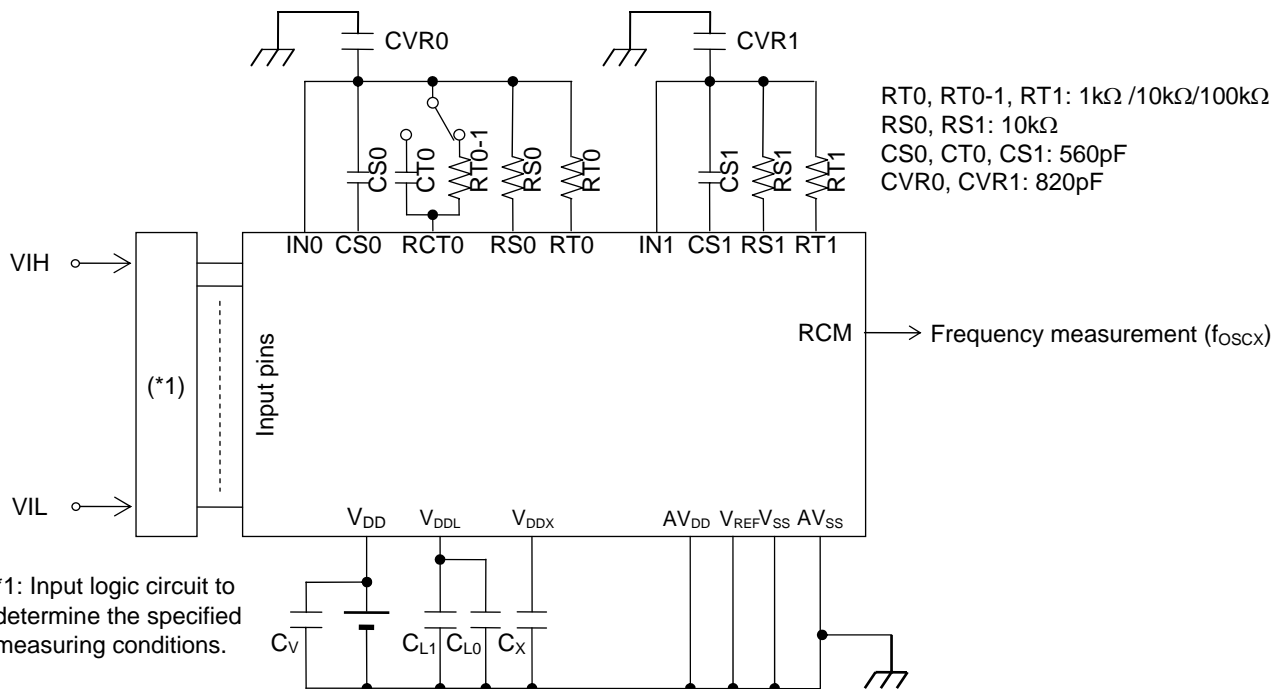
(V_{DD} = 1.3 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--|---------------------------|----------------------------------|--------|-------|-------|------|
| | | | Min. | Typ. | Max. | |
| Resistors for oscillation | RS0, RS1, RT0, RT0-1, RT1 | CS0, CT0, CS1 ≥ 740pF | 1 | — | — | kΩ |
| Oscillation frequency VDD = 1.5V | f _{OSC1} | Resistor for oscillation = 1kΩ | 209.4 | 330.6 | 435.1 | kHz |
| | f _{OSC2} | Resistor for oscillation = 10kΩ | 41.29 | 55.27 | 64.16 | kHz |
| | f _{OSC3} | Resistor for oscillation = 100kΩ | 4.71 | 5.97 | 7.06 | kHz |
| RS to RT oscillation frequency ratio ^{*1} VDD = 1.5V | Kf1 | RT0, RT0-1, RT1 = 1kHz | 5.567 | 5.982 | 6.225 | — |
| | Kf2 | RT0, RT0-1, RT1 = 10kHz | 0.99 | 1 | 1.01 | — |
| | Kf3 | RT0, RT0-1, RT1 = 100kHz | 0.104 | 0.108 | 0.118 | — |
| Oscillation frequency VDD = 3.0V | f _{OSC1} | Resistor for oscillation = 1kΩ | 407.3 | 486.7 | 594.6 | kHz |
| | f _{OSC2} | Resistor for oscillation = 10kΩ | 49.76 | 59.28 | 72.76 | kHz |
| | f _{OSC3} | Resistor for oscillation = 100kΩ | 5.04 | 5.993 | 7.04 | kHz |
| RS to RT oscillation frequency ratio ^{*1} VDD = 3.0V | Kf1 | RT0, RT0-1, RT1 = 1kHz | 8.006 | 8.210 | 8.416 | — |
| | Kf2 | RT0, RT0-1, RT1 = 10kHz | 0.99 | 1 | 1.01 | — |
| | Kf3 | RT0, RT0-1, RT1 = 100kHz | 0.100 | 0.108 | 0.115 | — |

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{oscx}(RT0-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \quad \frac{f_{oscx}(RT0-1-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \quad \frac{f_{oscx}(RT1-CS1 \text{ oscillation})}{f_{oscx}(RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)



Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

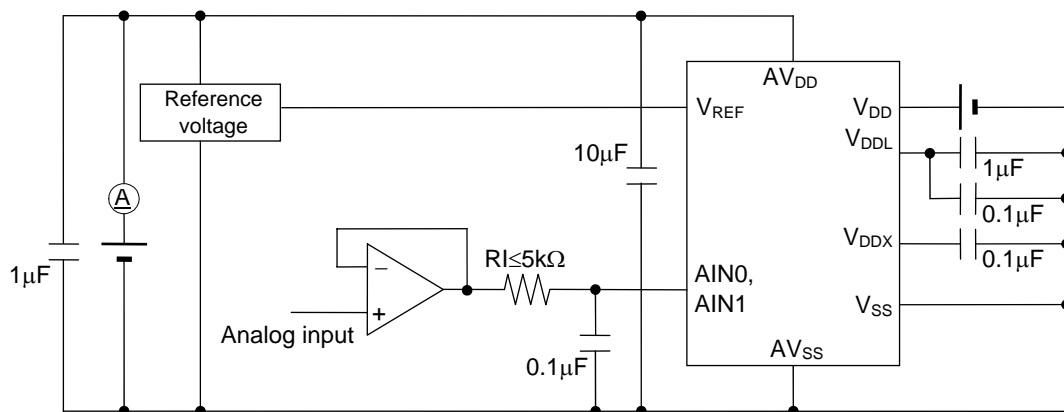
Electrical Characteristics of Successive Approximation Type A/D Converter

($V_{DD} = 1.8$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|----------------------------------|------------|-------------------------------|--------|-----------|-----------|-----------|
| | | | Min. | Typ. | Max. | |
| Resolution | n | — | — | — | 12 | bit |
| Integral non-linearity error | IDL | $2.7V \leq V_{REF} \leq 3.6V$ | -4 | — | +4 | LSB |
| | | $2.2V \leq V_{REF} \leq 2.7V$ | -6 | — | +6 | |
| Differential non-linearity error | DNL | $2.7V \leq V_{REF} \leq 3.6V$ | -3 | — | +3 | |
| | | $2.2V \leq V_{REF} \leq 2.7V$ | -5 | — | +5 | |
| Zero-scale error | V_{OFF} | — | -6 | — | +6 | |
| Full-scale error | FSE | — | -6 | — | +6 | |
| Reference voltage | V_{REF} | — | 2.2 | — | AV_{DD} | V |
| Conversion time | t_{CONV} | — | — | 23^{*1} | — | ϕ/CH |

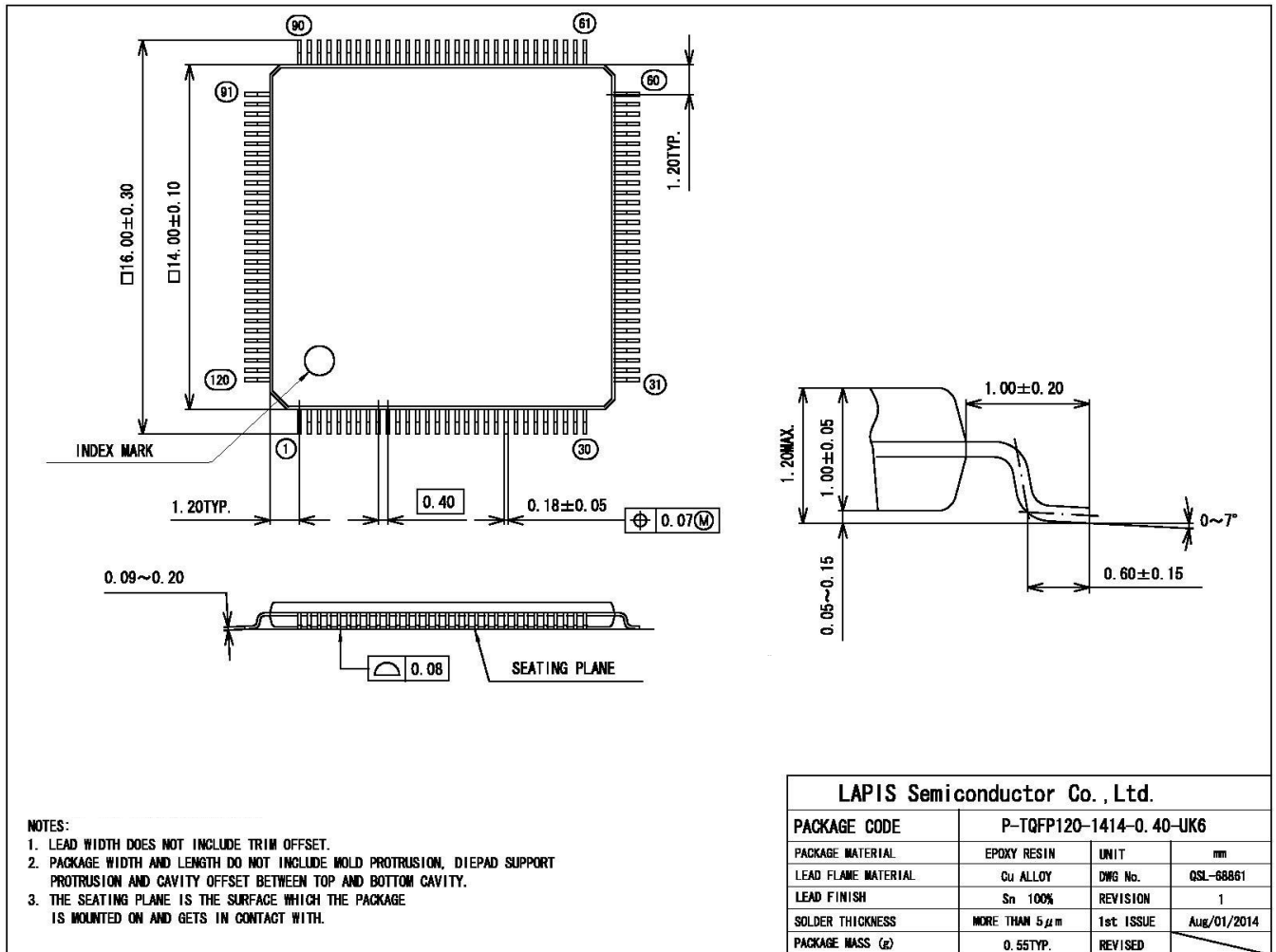
ϕ : Period of high-speed clock (HSCLK)

*1: $2\phi / CH$ is required as an interval time for each conversion in the case of consecutive A/D conversion.



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|----------------|--------------|------------------|-----------------|--|
| | | Previous Edition | Current Edition | |
| FEDL610Q411-01 | Jul.17,2010 | – | – | Formally edition 1 |
| FEDL610Q411-02 | Mar.23,2011 | 3, 4, 21 | 3, 4, 21 | Add the explanation of ML610Q411PC. |
| | | 34 | 34 | Replace the package dimension (Only the format is changed. Package size and material are not changed.) |
| FEDL610Q411-03 | Apr.15,2015 | All | All | Change header and footer. |
| | | 1~3 | 1~3 | Delete ML610Q415 and ML610Q411PC |
| | | 5 | 5 | |
| | | 7 | 7 | |
| | | 9 | 9 | |
| | | 11 | 11 | |
| | | 13 | 13 | |
| | | 15 | 15 | |
| | | 16 | 16 | |
| | | 18~20 | 18~20 | |
| | | 21 | 22 | |
| 23 | 24 | | | |
| 24 | 25 | | | |
| 25 | 26 | | | |
| 27 | 27 | | | |
| | | 4 | 4 | Change from "Shipment" to "Product name – Supported Function" |
| | | – | 21 | Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS |
| | | 21 | 22 | Change "RESET" to "Reset pulse width (P _{RST}) " and "Power-on reset activation power rise time (T _{POR}) ". |
| | | 36 | 36 | Change description in Note. |
| FEDL610Q411-04 | July.13,2015 | 14 | 14 | Corrected a typo. -PAD No,"37" is corrected to "36". -PAD No,"36" is corrected to "35". |

Notes

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