RMLV0416E Series

4Mb Advanced LPSRAM (256-kword × 16-bit)

R10DS0205EJ0200
Rev.2.00
2016.1.12

Description

The RMLV0416E Series is a family of 4-Mbit static RAMs organized 262,144-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0416E Series has realized higher density, higher performance and low power consumption. The RMLV0416E Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 44-pin TSOP (II) or 48-ball fine pitch ball grid array.

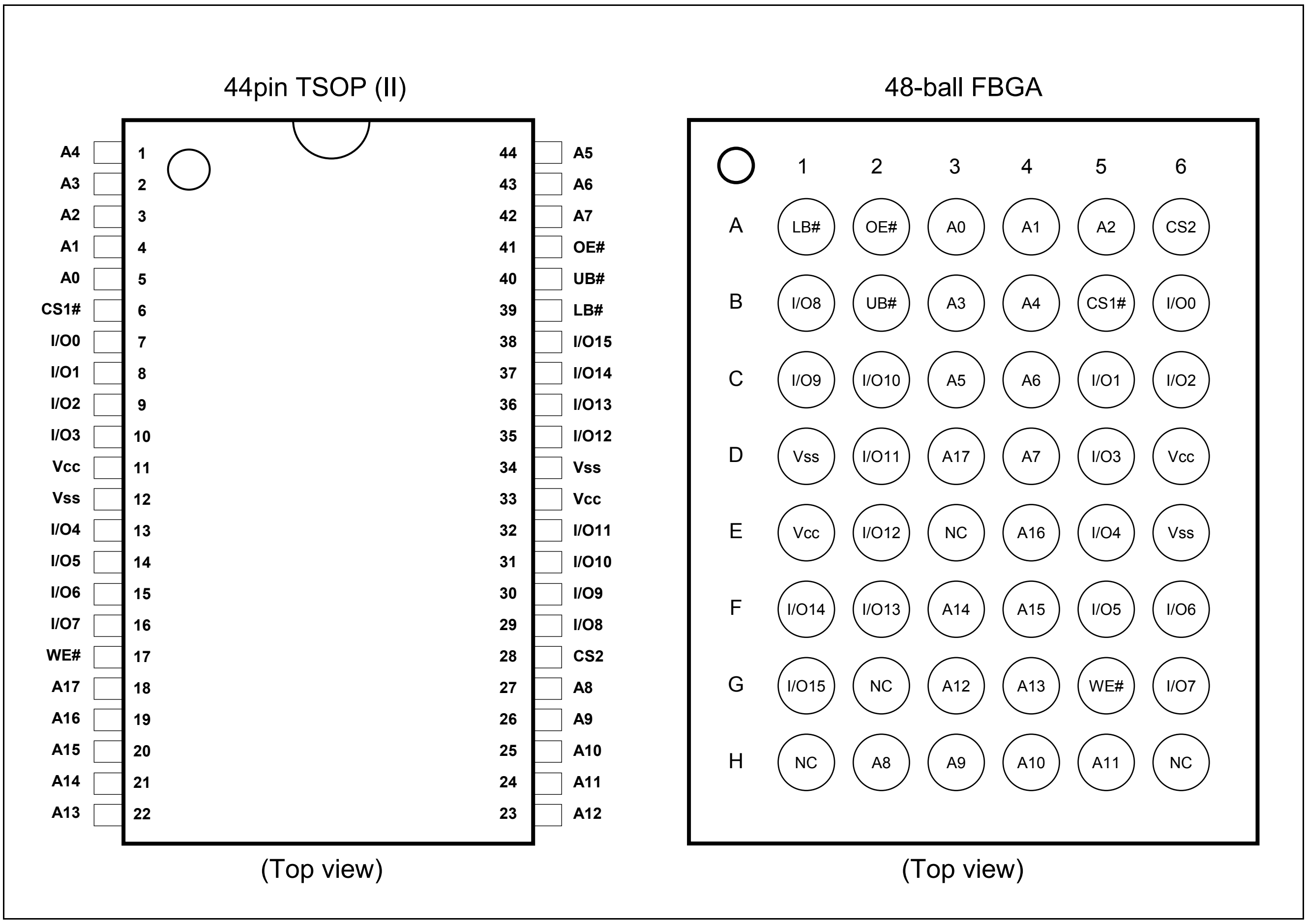
Features

- Single 3V supply: 2.7V to 3.6V
- Access time: 45ns (max.)
- Current consumption:
  — Standby: 0.4µA (typ.)
- Equal access and cycle times
- Common data input and output
  — Three state output
- Directly TTL compatible
  — All inputs and outputs
- Battery backup operation

Orderable part number information

Orderable part number	Access time	Temperature range	Package	Shipping container
RMLV0416EGSB-4S2#AA∗	45 ns	-40 ~ +85°C	400-mil 44pin plastic TSOP (II)	Tray
RMLV0416EGSB-4S2#HA∗				Embossed tape
RMLV0416EGBG-4S2#AC∗			48-ball FBGA with 0.75mm ball pitch	Tray
RMLV0416EGBG-4S2#KC∗				Embossed tape

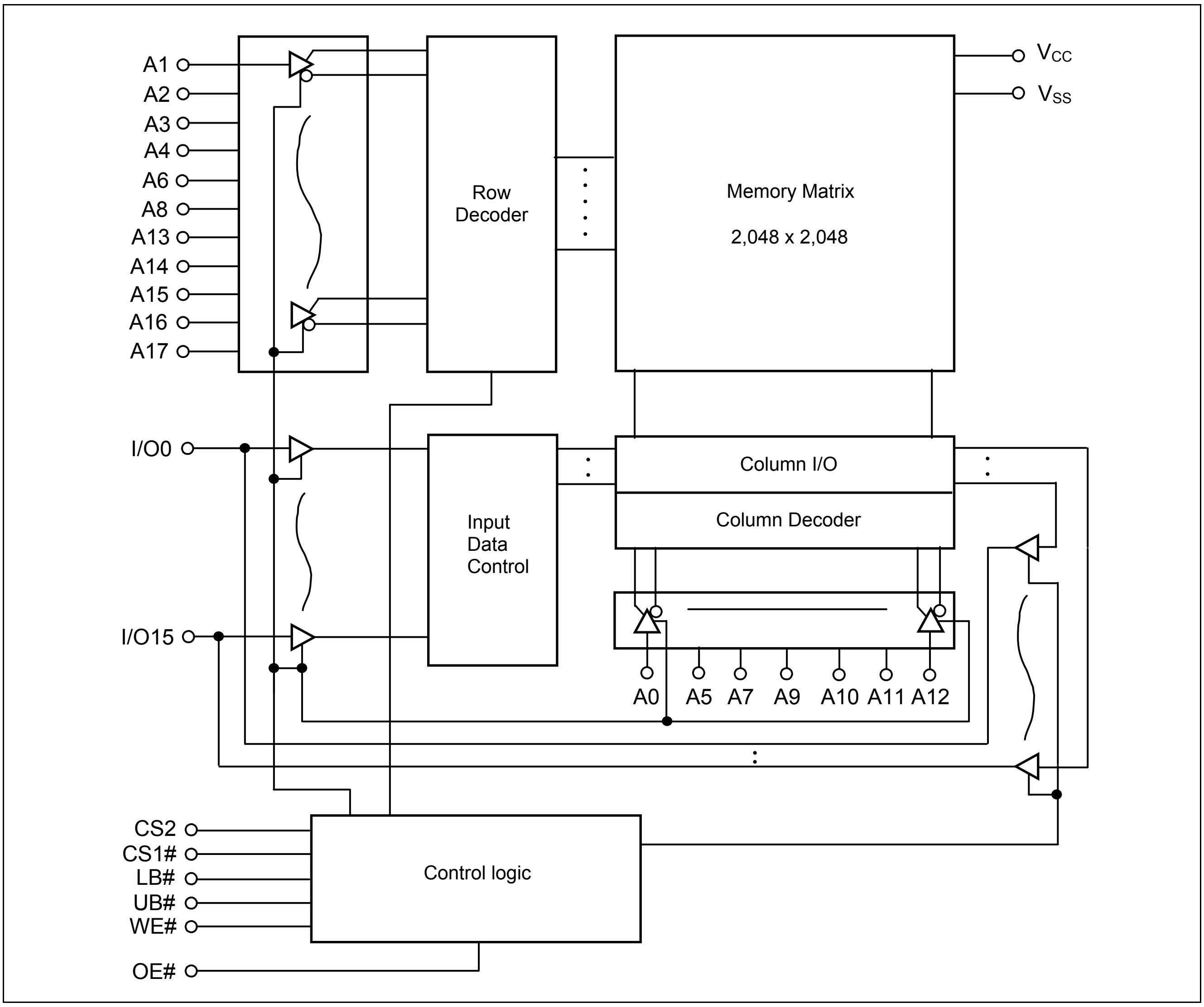
Pin Arrangement



Pin Description

Pin name	Function
V_{CC}	Power supply
V_{SS}	Ground
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	X	X	X	X	X	High-Z	High-Z	Standby
X	L	X	X	X	X	High-Z	High-Z	Standby
X	X	X	X	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	X	L	L	Din	Din	Write
L	H	L	X	H	L	Din	High-Z	Lower byte write
L	H	L	X	L	H	High-Z	Din	Upper byte write
L	H	H	H	X	X	High-Z	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5[*2] to V_{CC}+0.3[*3]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 2. -3.0V for pulse ≤ 30ns (full width at half maximum)
3. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	4
Ambient temperature range	Ta	-40	—	+85	°C	

Note 4. -3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current	$\lvert I_{LI} \rvert$	—	—	1	μA	Vin = V_{SS} to V_{CC}
Output leakage current	$\lvert I_{LO} \rvert$	—	—	1	μA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current	I_{CC}	—	—	10	mA	CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0mA
Average operating current	I_{CC1}	—	—	20	mA	Cycle = 55ns, duty =100%, $I_{I/O}$ = 0mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
		—	—	25	mA	Cycle = 45ns, duty =100%, $I_{I/O}$ = 0mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	—	2.5	mA	Cycle =1μs, duty =100%, $I_{I/O}$ = 0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, V_{IH} ≥ V_{CC}-0.2V, V_{IL} ≤ 0.2V
Standby current	I_{SB}	—	0.1[*5]	0.3	mA	CS2 = V_{IL}, Others = V_{SS} to V_{CC}
Standby current	I_{SB1}	—	0.4[*5]	2	μA	~+25°C Vin = V_{SS} to V_{CC}, (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V
		—	—	3	μA	~+40°C
		—	—	5	μA	~+70°C
		—	—	7	μA	~+85°C
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = -1mA
	V_{OH2}	V_{CC}-0.2	—	—	V	I_{OH} = -0.1mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2mA
	V_{OL2}	—	—	0.2	V	I_{OL} = 0.1mA

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.

Capacitance

(Vcc = 2.7V ~ 3.6V, f = 1MHz, Ta = -40 ~ +85°C)

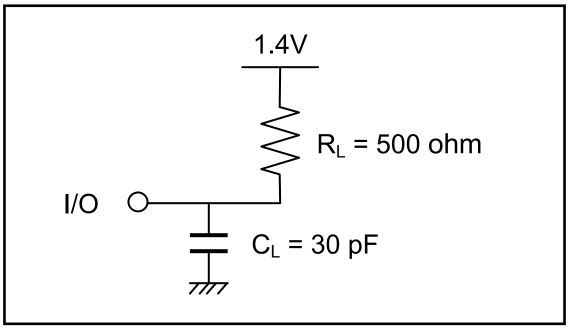
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	—	—	8	pF	Vin =0V	6
Input / output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ =0V	6

Note 6. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.7V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels: V_{IL} = 0.4V, V_{IH} = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	45		ns	
Address access time	t_{AA}	—	45	ns	
Chip select access time	t_{ACS1}	—	45	ns	
	t_{ACS2}	—	45	ns	
Output enable to output valid	t_{OE}	—	22	ns	
Output hold from address change	t_{OH}	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	ns	7,8
	t_{CLZ2}	10	—	ns	7,8
LB#, UB# enable to low-Z	t_{BLZ}	5	—	ns	7,8
Output enable to output in low-Z	t_{OLZ}	5	—	ns	7,8
Chip deselect to output in high-Z	t_{CHZ1}	0	18	ns	7,8,9
	t_{CHZ2}	0	18	ns	7,8,9
LB#, UB# disable to high-Z	t_{BHZ}	0	18	ns	7,8,9
Output disable to output in high-Z	t_{OHZ}	0	18	ns	7,8,9

Note 7. This parameter is sampled and not 100% tested.

8. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.
9. t_{CHZ1}, t_{CHZ2}, t_{BHZ} and t_{OHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	45	—	ns	
Address valid to write end	t_{AW}	35	—	ns	
Chip select to write end	t_{CW}	35	—	ns	
Write pulse width	t_{WP}	35	—	ns	10
LB#,UB# valid to write end	t_{BW}	35	—	ns	
Address setup time to write start	t_{AS}	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	ns	
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write end	t_{DH}	0	—	ns	
Output enable from write end	t_{OW}	5	—	ns	11
Output disable to output in high-Z	t_{OHZ}	0	18	ns	11,12
Write to output in high-Z	t_{WHZ}	0	18	ns	11,12

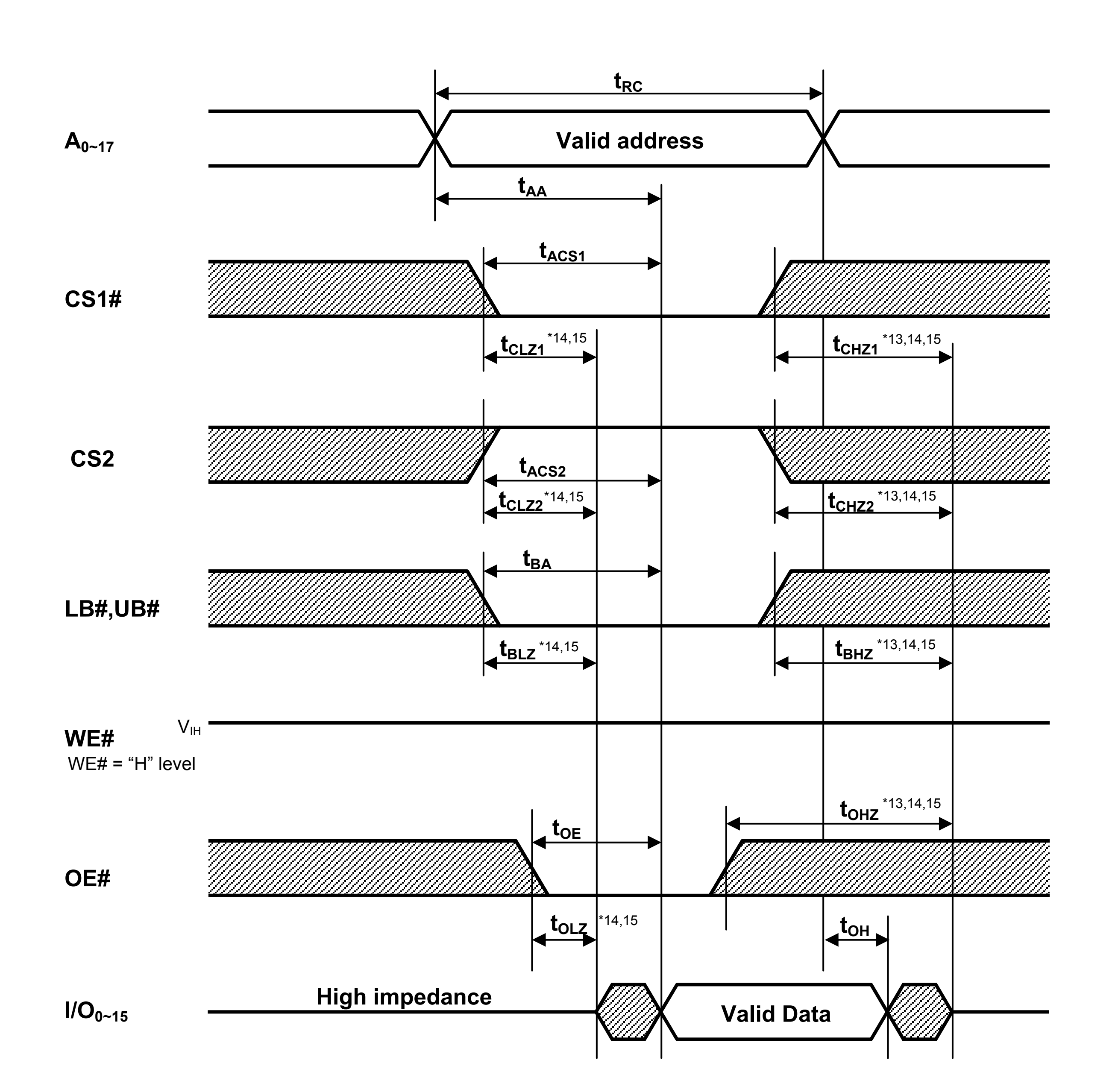
Note 10. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

11. This parameter is sampled and not 100% tested.

12. t_{OHZ} and t_{WHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

Timing Waveforms

Read Cycle

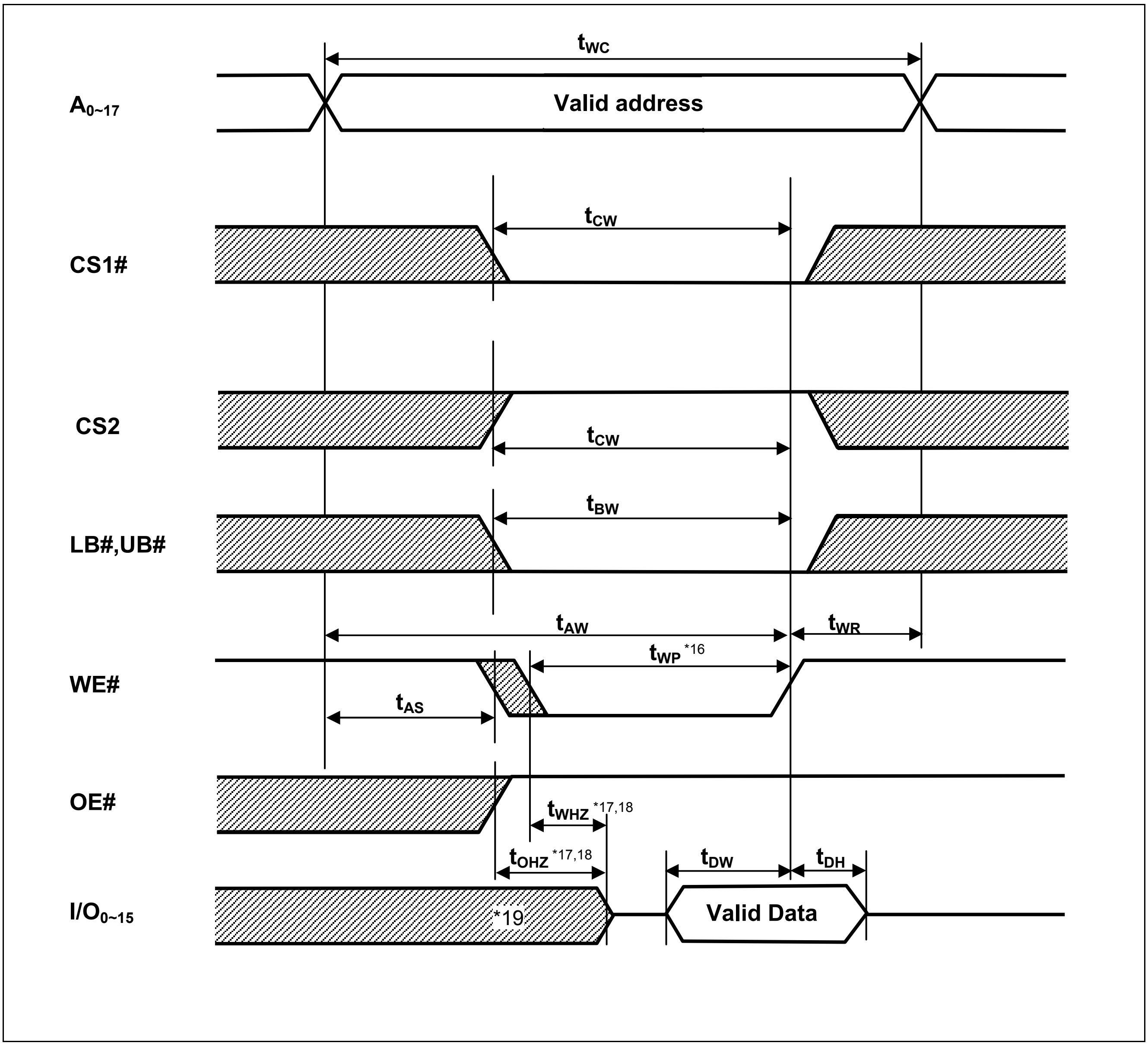


Note 13. t_{CHZ1}, t_{CHZ2}, t_{BHZ} and t_{OHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

14. This parameter is sampled and not 100% tested

15. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

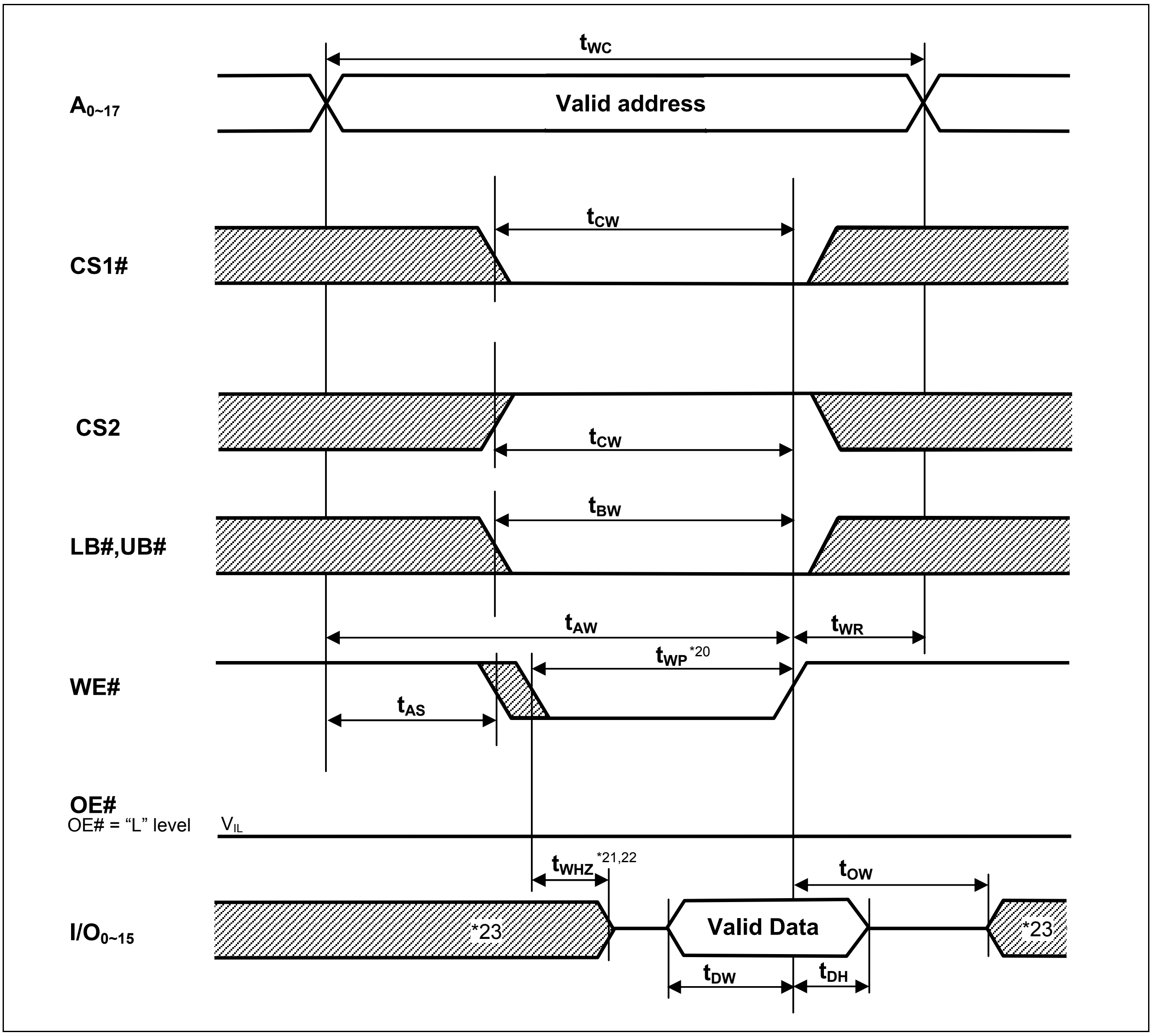
Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 16. t_{WP} is the minimum time to perform a write.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

17. t_{OHZ} and t_{WHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
18. This parameter is sampled and not 100% tested
19. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

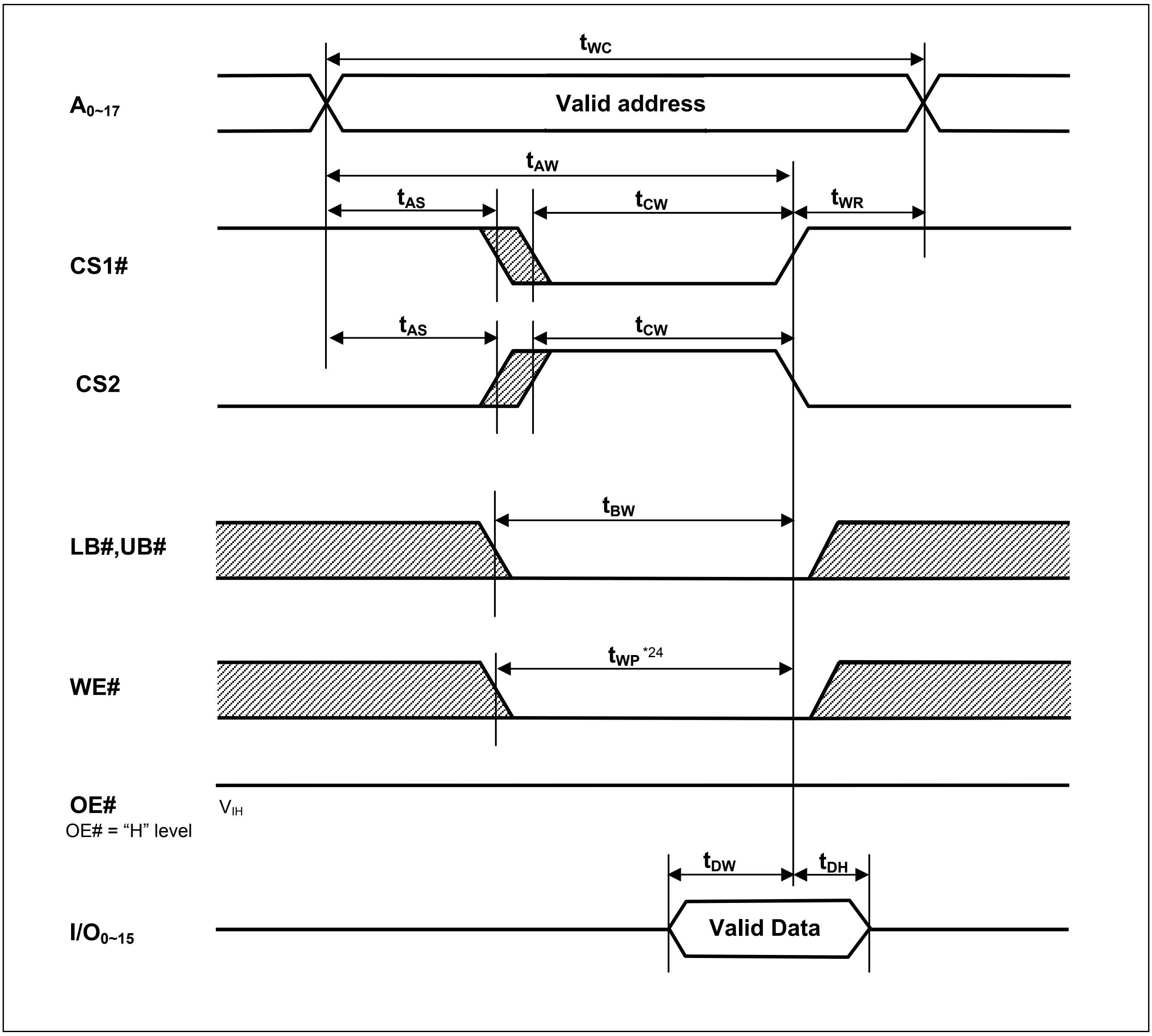
Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



Note 20. t_{WP} is the minimum time to perform a write.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

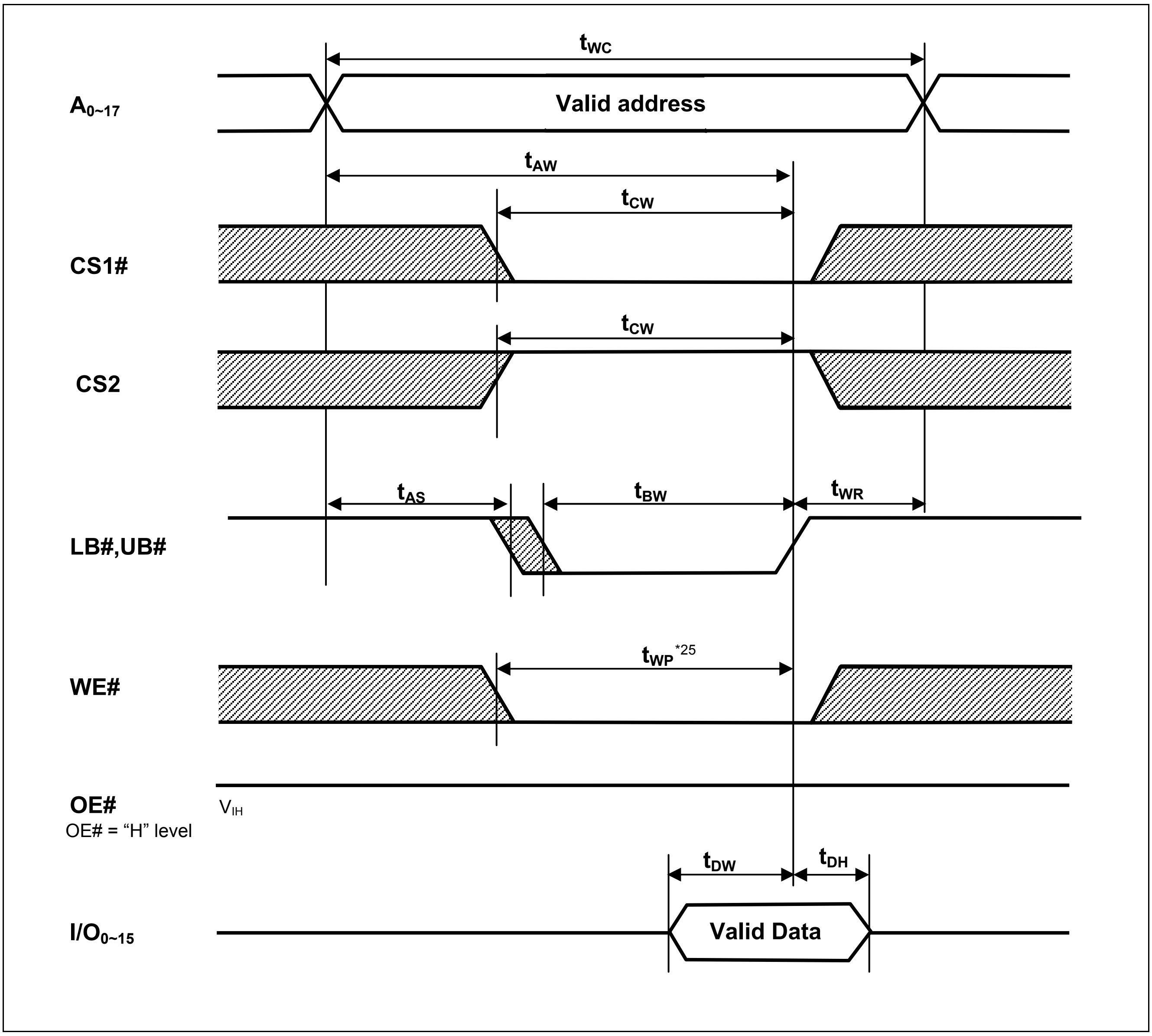
21. t_{WHZ} is defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
22. This parameter is sampled and not 100% tested.
23. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

Write Cycle (3) (CS1#, CS2 CLOCK)



Note 24. t_{WP} is the minimum time to perform a write.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4) (LB#, UB# CLOCK)



Note 25. t_{WP} is the minimum time to perform a write.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

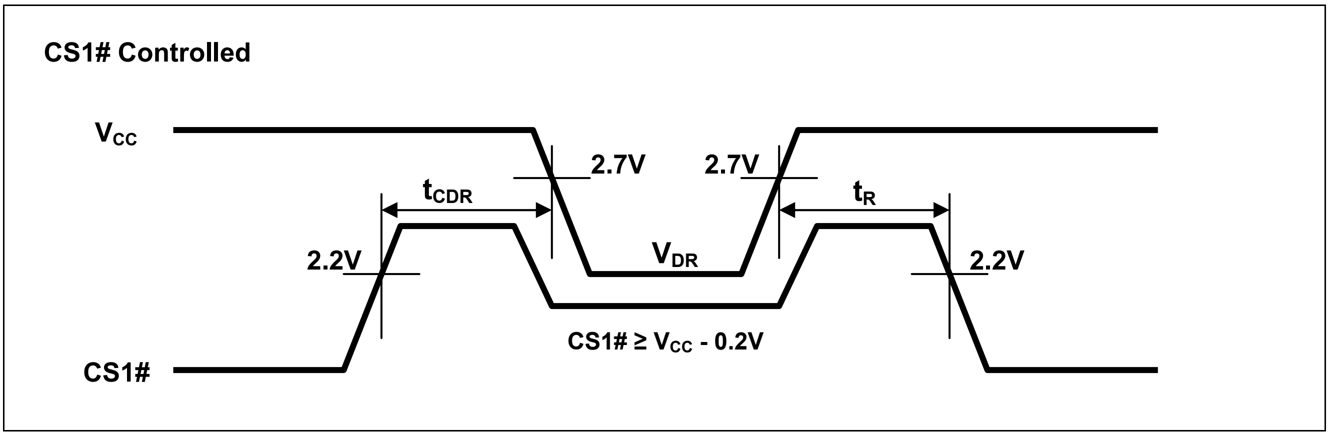
Low V_{CC} Data Retention Characteristics

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th colspan="2">Test conditions[27]</th></tr>
<tr><td>V_{CC} for data retention</td><td>V_{DR}</td><td>1.5</td><td>—</td><td>—</td><td>V</td><td colspan="2">Vin ≥ 0V,
(1) CS2 ≤ 0.2V
or
(2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V
or
(3) LB# = UB# ≥ V_{CC}-0.2V,
CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V</td></tr>
<tr><td rowspan="4">Data retention current</td><td rowspan="4">I_{CCDR}</td><td>—</td><td>0.4[26]</td><td>2</td><td>µA</td><td>~+25°C</td><td rowspan="4">V_{CC} = 3.0V, Vin ≥ 0V,
(1) CS2 ≤ 0.2V
or
(2) CS1# ≥ V_{CC}-0.2V,
CS2 ≥ V_{CC}-0.2V
or
(3) LB# = UB# ≥ V_{CC}-0.2V,
CS1# ≤ 0.2V,
CS2 ≥ V_{CC}-0.2V</td></tr>
<tr><td>—</td><td>—</td><td>3</td><td>µA</td><td>~+40°C</td></tr>
<tr><td>—</td><td>—</td><td>5</td><td>µA</td><td>~+70°C</td></tr>
<tr><td>—</td><td>—</td><td>7</td><td>µA</td><td>~+85°C</td></tr>
<tr><td>Chip deselect time to data retention</td><td>t_{CDR}</td><td>0</td><td>—</td><td>—</td><td>ns</td><td colspan="2" rowspan="2">See retention waveform.</td></tr>
<tr><td>Operation recovery time</td><td>t_R</td><td>5</td><td>—</td><td>—</td><td>ms</td></tr>
</table>

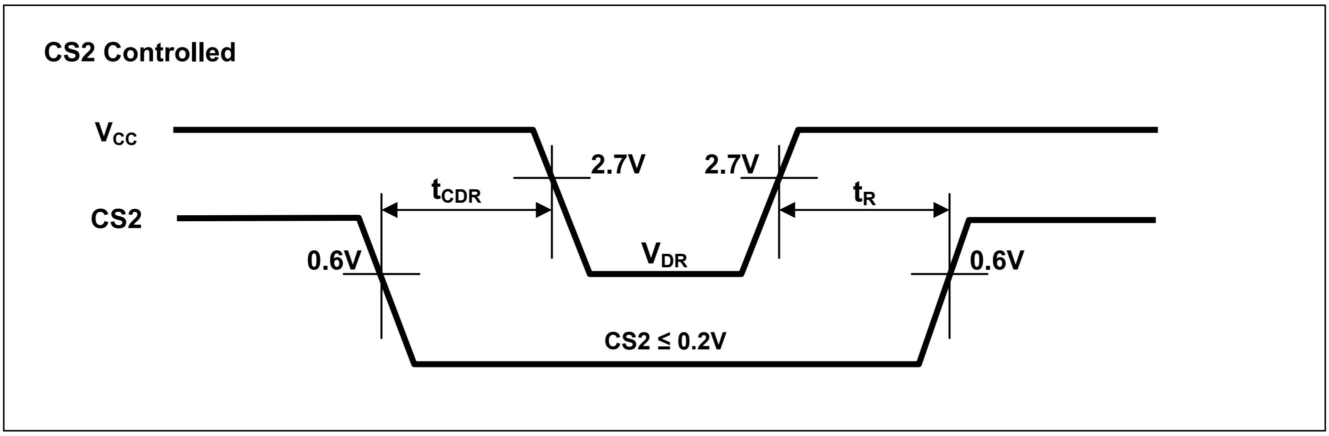
Note 26. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.

27. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and I/O buffer. If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V. The other inputs levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high-impedance state.

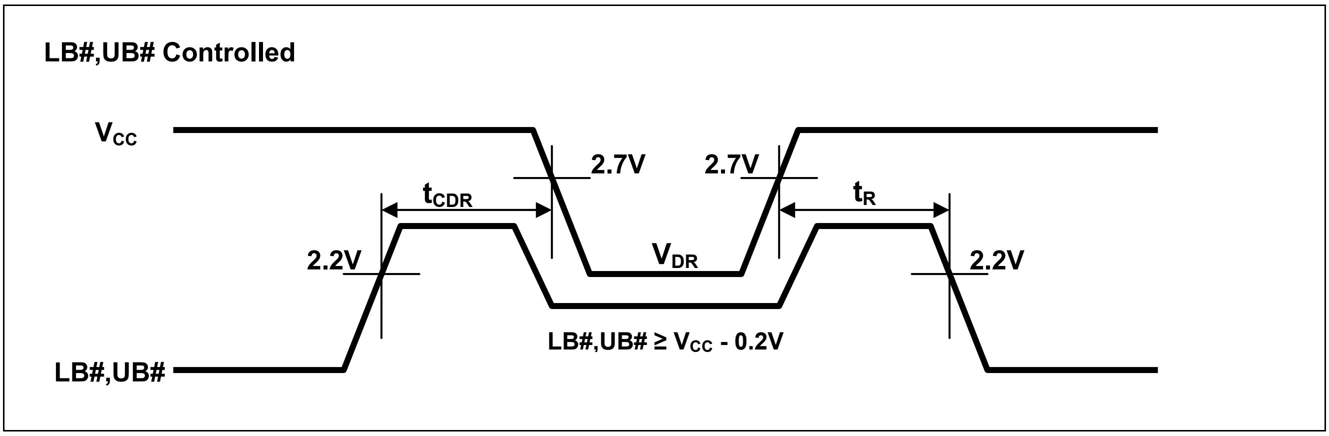
Low Vcc Data Retention Timing Waveforms (CS1# controlled)



Low Vcc Data Retention Timing Waveforms (CS2 controlled)



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled)



Revision History	RMLV0416E Series Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2014.2.27	—	First edition issued
2.00	2016.1.12	1	Changed section from “Part Name Information” to “Orderable part number information”

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