TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7SB66CFU, TC7SB67CFU

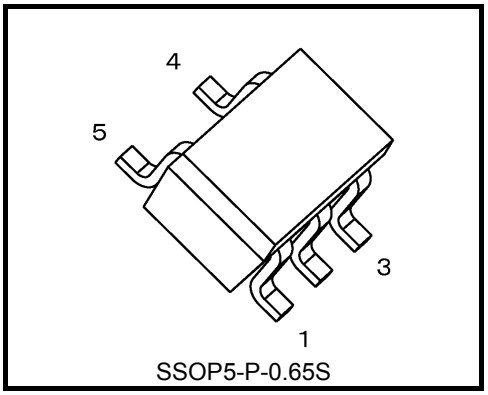
Low Capacitance Single Bus Switch (analog)

The TC7SB66C and TC7SB67C are low ON-resistance, high-speed CMOS 2-bit bus switches. These bus switches allow connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

The TC7SB66C requires the output enable (OE) input to be set low to place the output into the high impedance state,whereas the TC7SB67C requires the output enable ($\overline{OE}$) input to be set high to place the output into the high impedance.

These Bus switches consist of P-MOS and N-MOS structure, meaning these devices are suitable for analog signal transmission.

All inputs are equipped with protector circuits to protect the device from static discharge.



SSOP5-P-0.65S

Weight : 0.006 g (typ.)

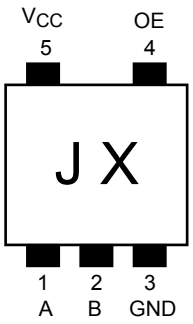
Features

- Operating voltage : V_{CC} = 1.65 to 5.5 V
- On capacitance : $C_{I/O}$ = 10pF Switch On(typ.) @V_{CC}=5.0V
- On resistance : R_{ON} = 4 Ω (typ.) @V_{CC}=4.5V, V_{IS}=0 V
- ESD performance : Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Package: USV

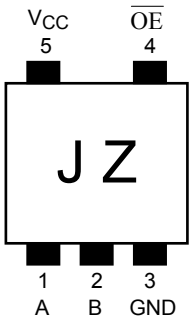
Start of commercial production
2011-04

Pin Assignment (top view)

TC7SB66CFU



TC7SB67CFU

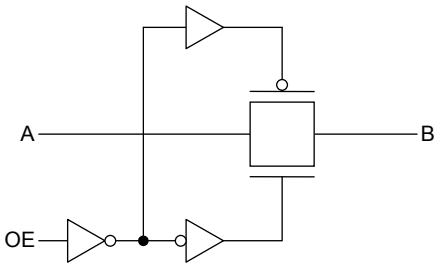


Truth Table

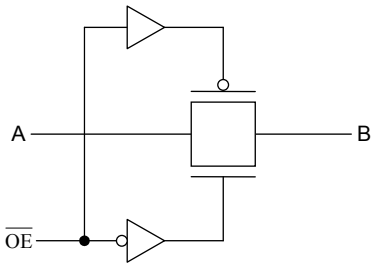
Inputs (66C)	Inputs (67C)	Function
OE	$\overline{OE}$	
H	L	A port = B port
L	H	Disconnect

System Diagram

TC7SB66CFU



TC7SB67CFU



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 7.0	V
Control pin input voltage	V_{IN}	−0.5 to 7.0	V
Switch terminal I/O voltage	V_S	−0.5 to V_{CC}+0.5	V
Clump diode current	I_{IK}	−50	mA
Switch I/O current	I_S	50	mA
Power dissipation	P_D	200	mW
DC V_{CC}/GND current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.65 to 5.5	V
Control pin input voltage	V_{IN}	0 to 5.5	V
Switch I/O voltage	V_S	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Control pin input rise/fall time	dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
High-level input Voltage (OE, $\overline{OE}$)	V_{IH}	—	1.65 to 1.95	0.8 × V_{CC}	—	—	V
			2.3 to 5.5	0.7 × V_{CC}	—	—	
Low-level input Voltage (OE, $\overline{OE}$)	V_{IL}	—	1.65 to 1.95	—	—	0.2 × V_{CC}	
			2.3 to 5.5	—	—	0.3 × V_{CC}	
Input leakage current (OE, $\overline{OE}$)	I_{IN}	V_{IN} = 0 to 5.5V	1.65 to 5.5	—	—	±1.0	μA
Switch terminal Off-state leakage current	I_{SZ}	A, B = 0 to V_{CC}, OE = GND (66C), $\overline{OE}$ = V_{CC} (67C)	1.65 to 5.5	—	—	±10	μA
ON resistance (Note 2)	R_{ON}	V_{IS} = 0 V, I_{IS} = 30 mA (Note 1)	4.5	—	4	7	Ω
		V_{IS} = 2.4 V, I_{IS} = 30 mA (Note 1)	4.5	—	5	12	
		V_{IS} = 4.5 V, I_{IS} = 15 mA (Note 1)	4.5	—	6	10	
		V_{IS} = 0 V, I_{IS} = 24 mA (Note 1)	3.0	—	5	9	
		V_{IS} = 3.0 V, I_{IS} = 24 mA (Note 1)	3.0	—	7	14	
		V_{IS} = 0 V, I_{IS} = 8 mA (Note 1)	2.3	—	6	12	
		V_{IS} = 2.3 V, I_{IS} = 8 mA (Note 1)	2.3	—	9	18	
		V_{IS} = 0 V, I_{IS} = 4 mA (Note 1)	1.65	—	8	20	
		V_{IS} = 1.65 V, I_{IS} = 4 mA (Note 1)	1.65	—	15	30	
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0A	5.5	—	—	10	μA
	ΔI_{CC}	V_{IN} = V_{CC}–0.6 V	5.5	—	—	50	μA

Note 1: All typical values are at Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = −40 to 85°C)

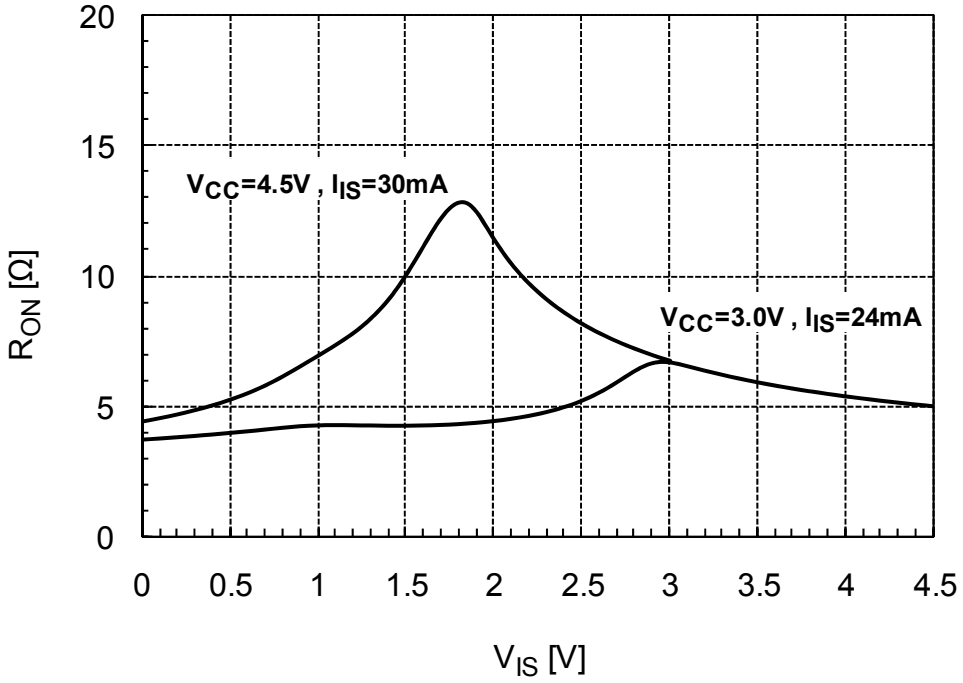
Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 2	5.0 ± 0.5	—	4	ns
			3.3 ± 0.3	—	6	
			2.5 ± 0.2	—	9	
			1.8 ± 0.15	—	18	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 2	5.0 ± 0.5	—	4.5	ns
			3.3 ± 0.3	—	7	
			2.5 ± 0.2	—	9	
			1.8 ± 0.15	—	18	

Capacitive Characteristics (Ta = 25°C)

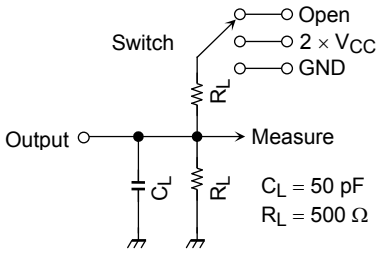
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control pin input capacitance	C_{IN}	V_{IN} = 0 V (Note)	5.0	4	pF
Switch terminal OFF capacitance	$C_{I/O}$	OE = GND (66C), $\overline{OE}$ = V_{CC} (67C), V_{IS} = 0 V (Note)	5.0	5	pF
Switch terminal ON capacitance	$C_{I/O}$	OE = V_{CC} (66C), $\overline{OE}$ = GND (67C), V_{IS} = 0 V (Note)	5.0	10	pF

Note: Parameter guaranteed by design.

R_{ON} - V_{IS} Characteristic (Typ.) Ta = 25°C



AC Test Circuit



Parameter	Switch
t_{pLZ}, t_{pZL}	2 × V_{CC}
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

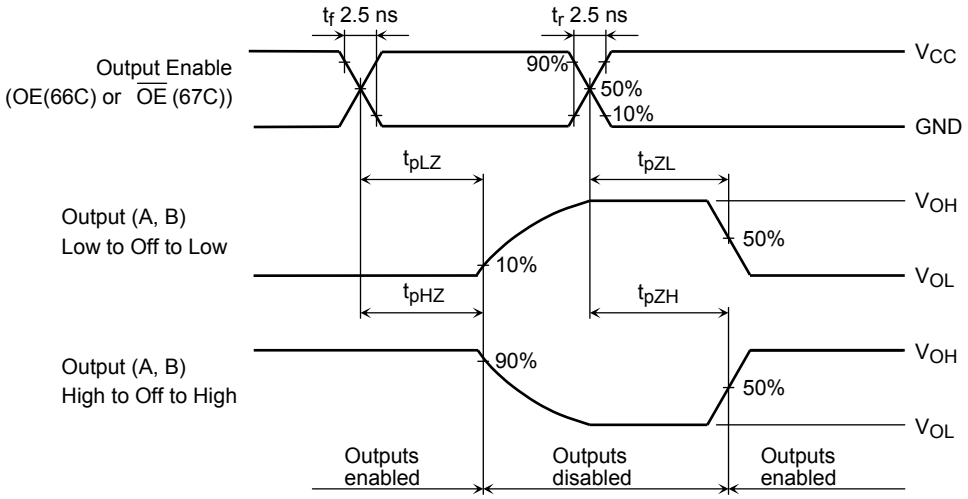


Figure 2 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Rise and Fall Time (tr / tf) of the TC7SB66C, 67C I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance (R_{ON}) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7SB66C, 67C.

The tr / tf(out) values can be approximated as follows. (Figure 3 shows the test circuit.)

$$tr / tf(out)\ (approx) = -(C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln(((V_{OH} - V_{OL}) - V_M) / (V_{OH} - V_{OL}))$$

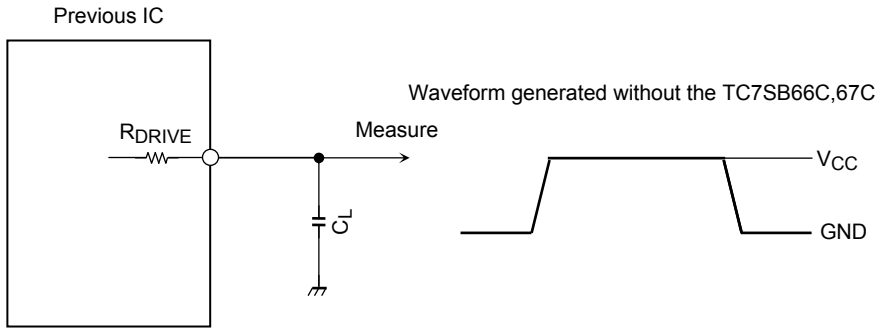
where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

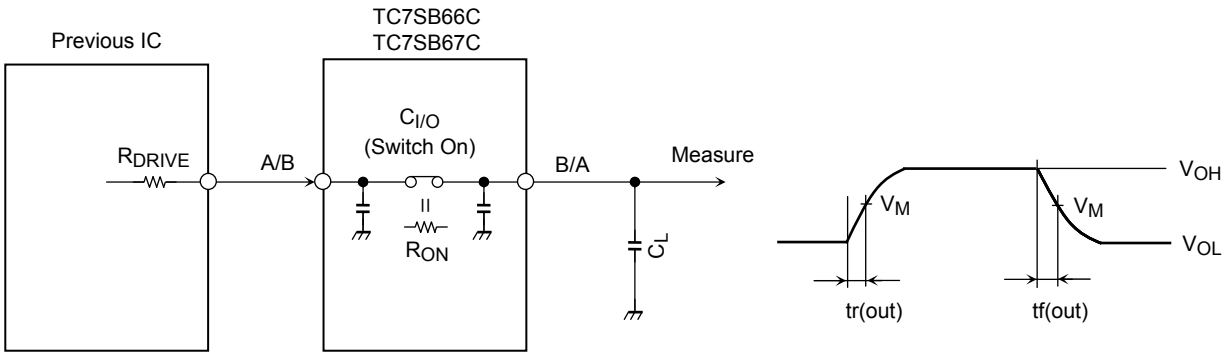
$$tr / tf(out)\ (approx) = -(10 + 15)E{-}12 \cdot (120 + 4) \cdot \ln(((4.5 - 0) - 2.25) / (4.5 - 0))$$
$$\approx 2.1\ ns$$

Calculation conditions:

V_{CC} = 4.5 V, C_L = 15 pF, R_{DRIVE} = 120 Ω (output impedance of the previous IC), V_M = 2.25 V (V_{CC} / 2)
Output voltage of the previous IC = digital (i.e., high-level voltage = V_{CC}; low-level voltage = GND)



R_{DRIVE} = output impedance of the previous IC



R_{DRIVE} = output impedance of the previous IC

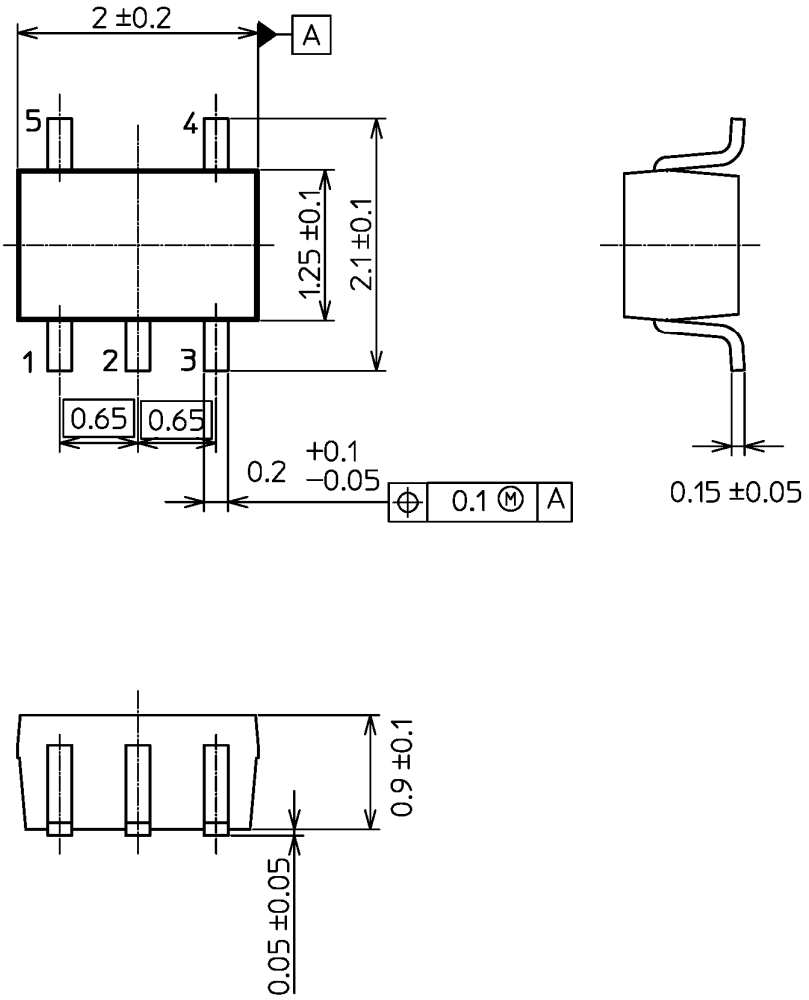
Parameter	V_{CC}			
	5.0 ± 0.5 V	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 ± 0.15 V
V_M	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2

Figure 3 Test Circuit

Package Dimensions

SSOP5-P-0.65S

Unit: mm



Weight: 0.006 g (typ.)

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