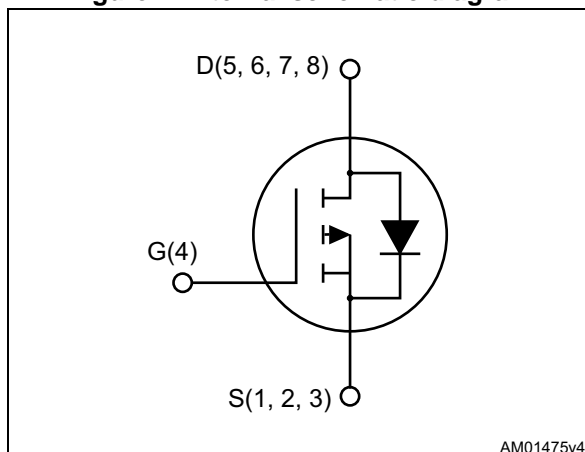


P-channel 60 V, 0.13 Ω typ., 12 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D
STL12P6F6	60 V	0.16 Ω @ 10 V	12 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits a very low $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL12P6F6	12P6F6	PowerFLAT 5x6	Tape and reel

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Packaging mechanical data	13
6	Revision history	15

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	12	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8.5	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	48	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	2.8	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	75	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_j	Operating junction temperature	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

1. The value is according to $R_{thj-case}$
2. Pulse width is limited by safe operating area.
3. The value is according to $R_{thj-pcb}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 15 mm^2 , 2 Oz Cu, $t < 10\text{ sec}$

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	60			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 60 V			1	μA
		V _{GS} = 0, V _{DS} = 60 V, T _C = 125 °C			10	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0, V _{GS} = ± 20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 1.5 A		0.13	0.16	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 48 V, f = 1 MHz	-	340	-	pF
C _{oss}	Output capacitance		-	40	-	pF
C _{rss}	Reverse transfer capacitance		-	20	-	pF
Q _g	Total gate charge	V _{DD} = 30 V, I _D = 3 A,	-	6.4	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	1.7	-	nC
Q _{gd}	Gate-drain charge	(see Figure 14)	-	1.7	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 48 V, I _D = 1.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13)	-	64	-	ns
t _r	Rise time		-	5.3	-	ns
t _{d(off)}	Turn-off delay time		-	14	-	ns
t _f	Fall time		-	3.7	-	ns

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 3 \text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	20		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 16 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	17.8		nC
I_{RRM}	Reverse recovery current	(see Figure 15)	-	1.8		A

1. Pulse width limited by safe operating area.

2. Pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

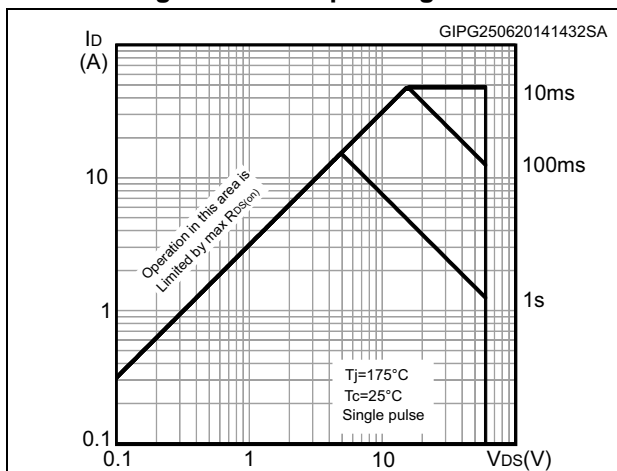


Figure 3. Thermal impedance

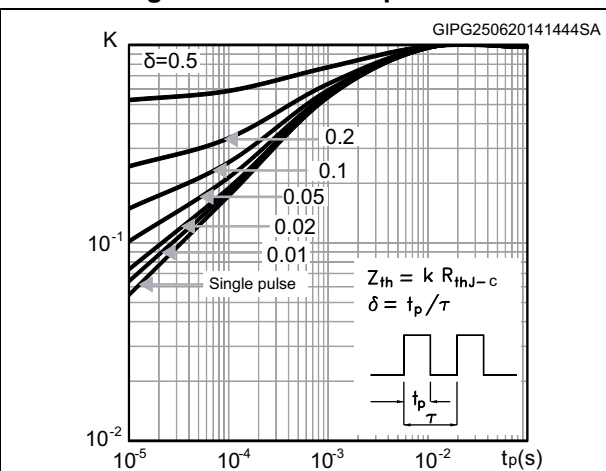


Figure 4. Output characteristics

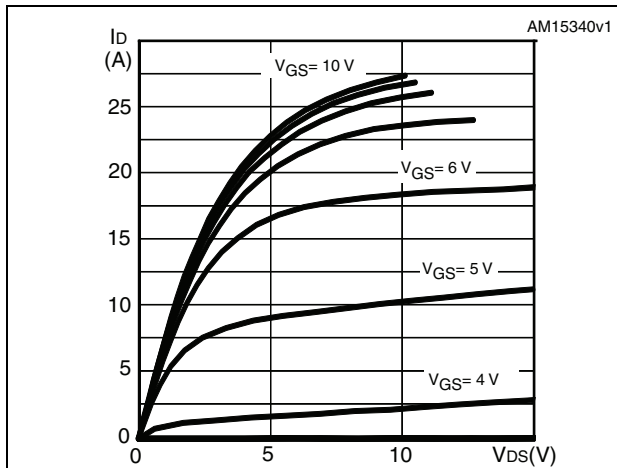


Figure 5. Transfer characteristics

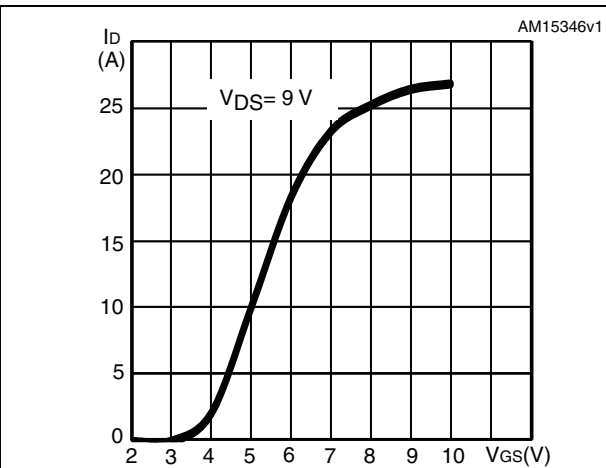


Figure 6. Gate charge vs gate-source voltage

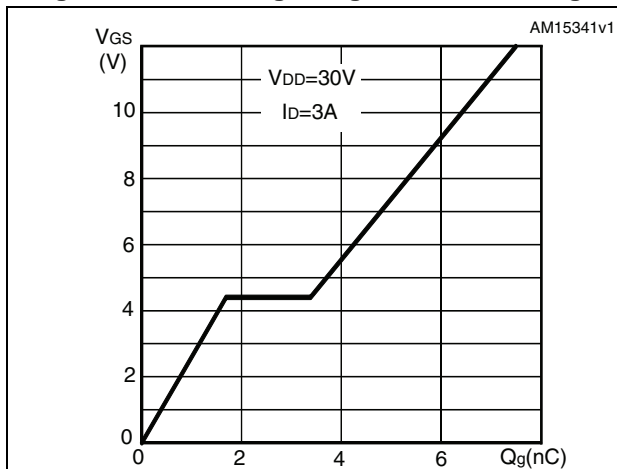


Figure 7. Static drain-source on-resistance

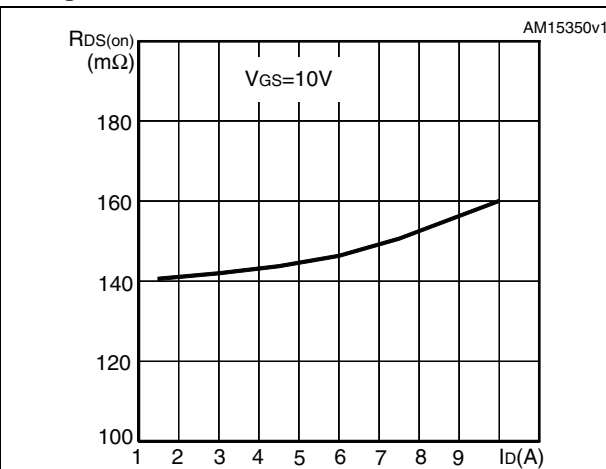


Figure 8. Capacitance variations

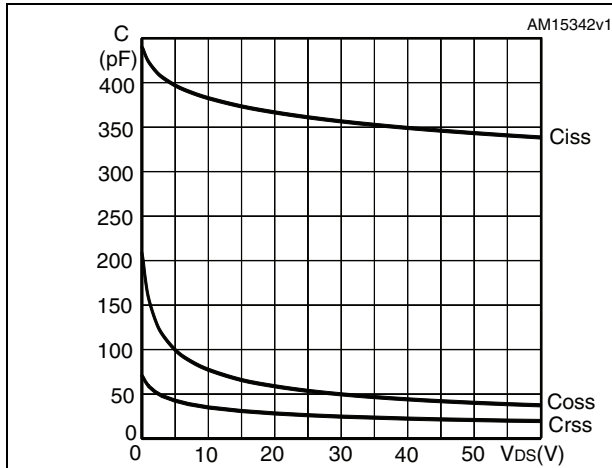


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

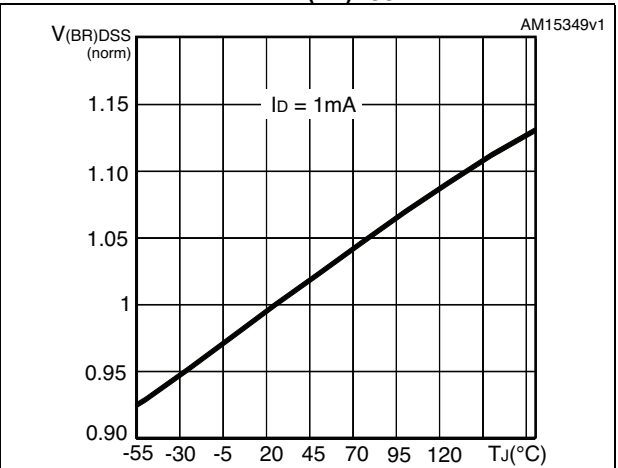


Figure 10. Normalized gate threshold voltage vs temperature

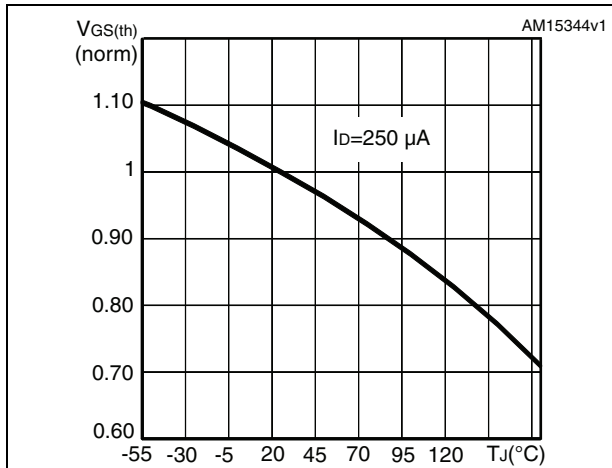


Figure 11. Normalized on-resistance vs temperature

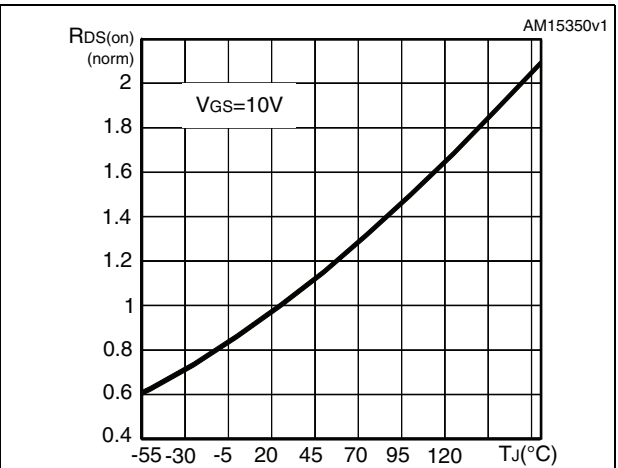
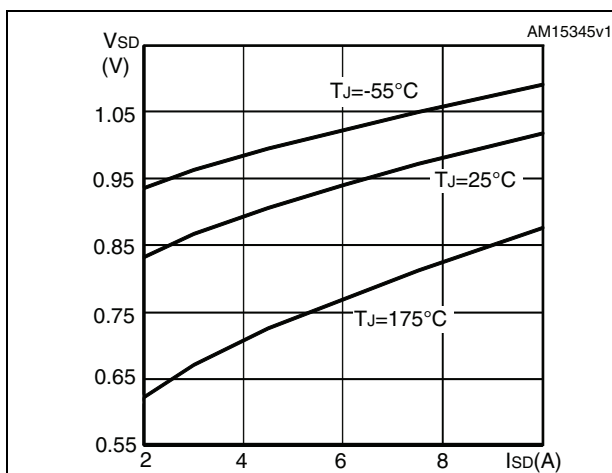


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

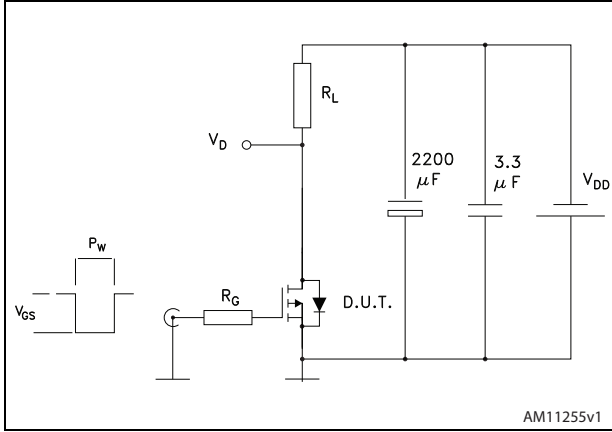


Figure 14. Gate charge test circuit

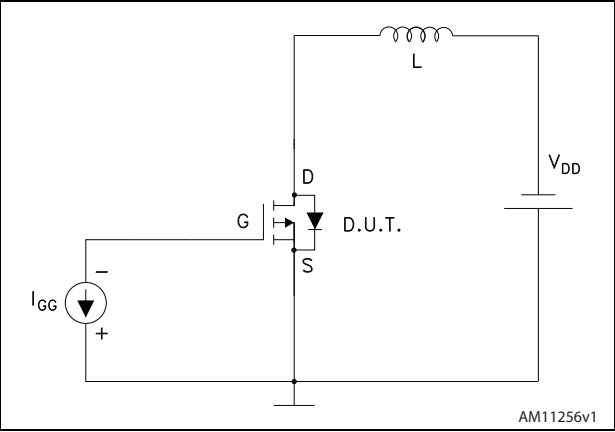
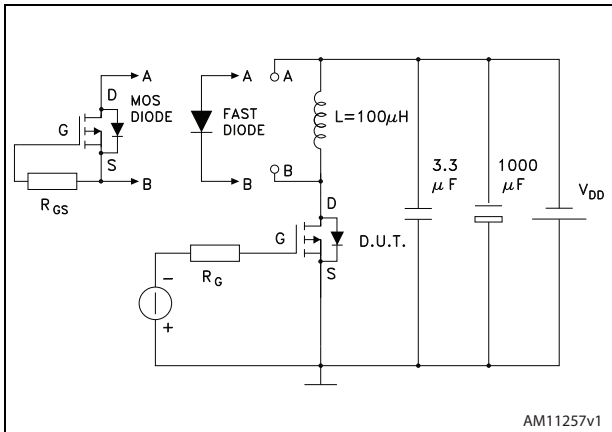


Figure 15. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 16. PowerFLAT™ 5x6 type S-R drawing

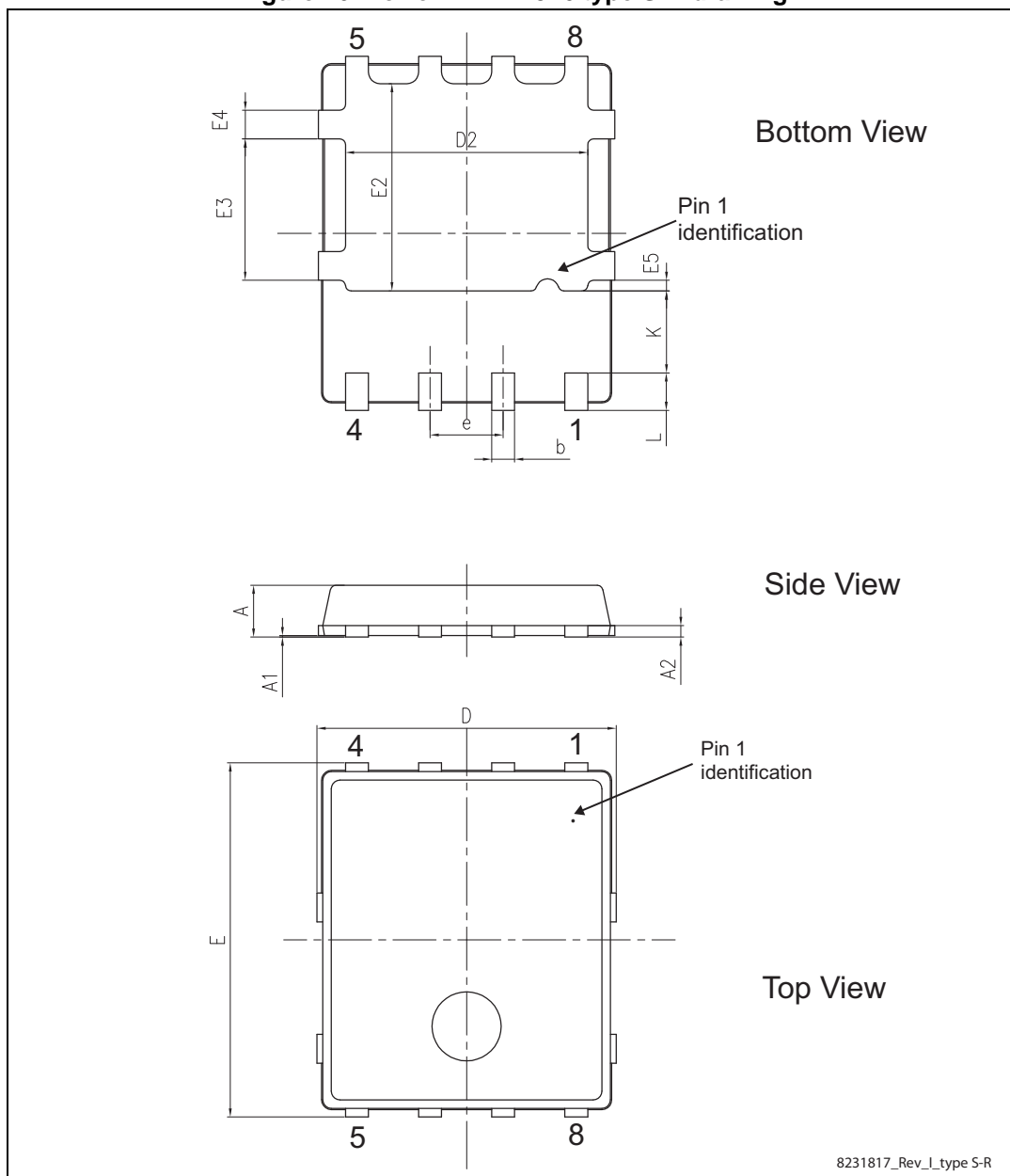
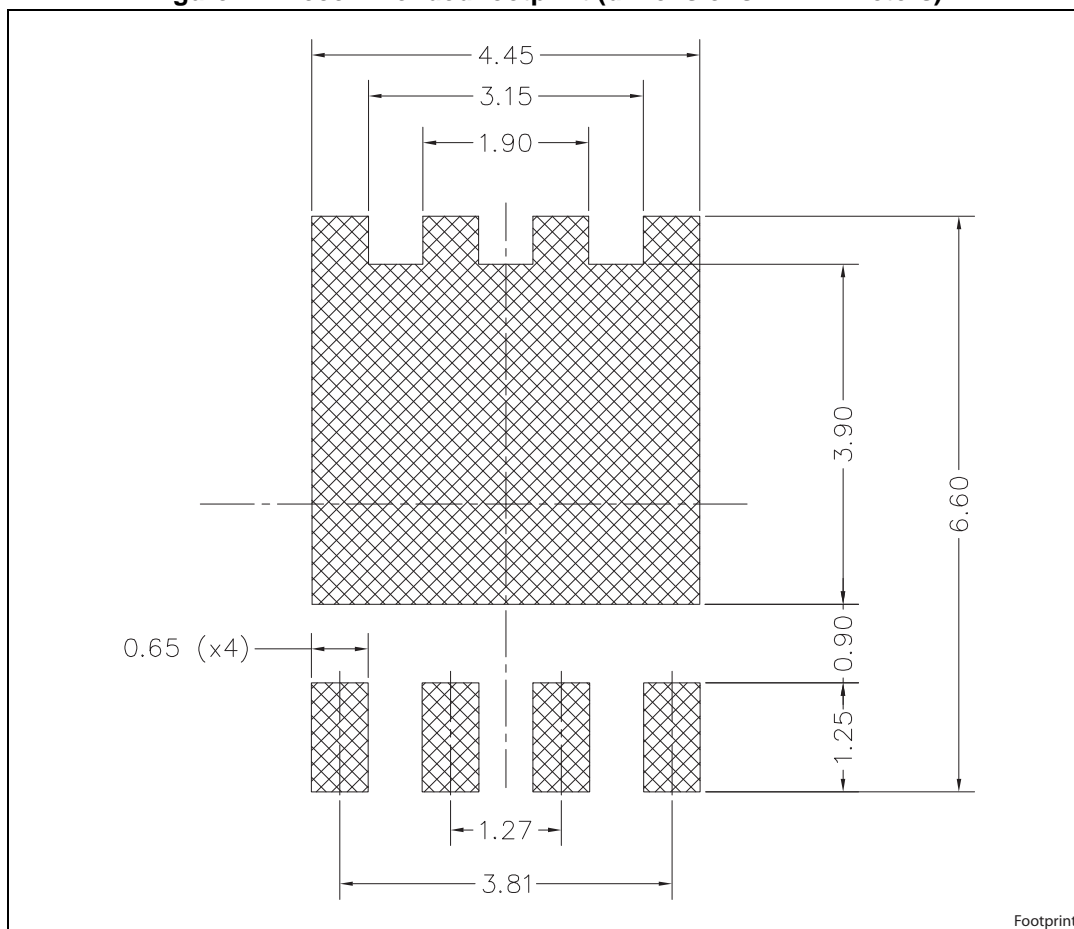


Table 8. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
D2	4.11		4.31
E	5.95	6.15	6.35
e		1.27	
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
K	1.275		1.575
L	0.60		0.80

Figure 17. Recommended footprint (dimensions in millimeters)



5 Packaging mechanical data

Figure 18. PowerFLAT™ 5x6 tape^(a)

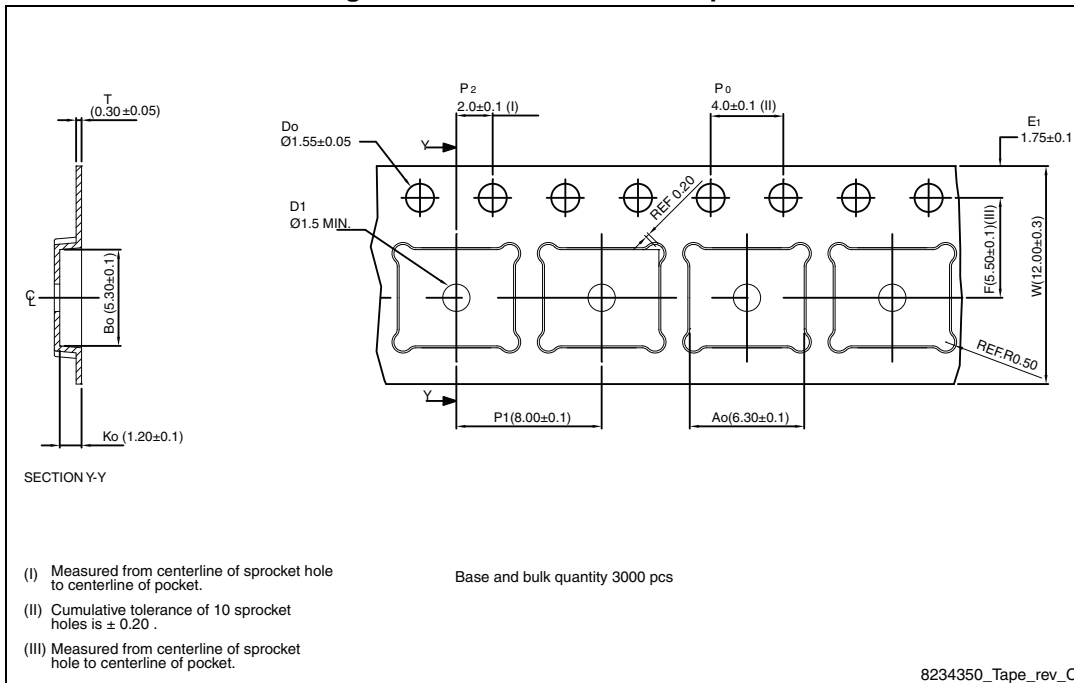
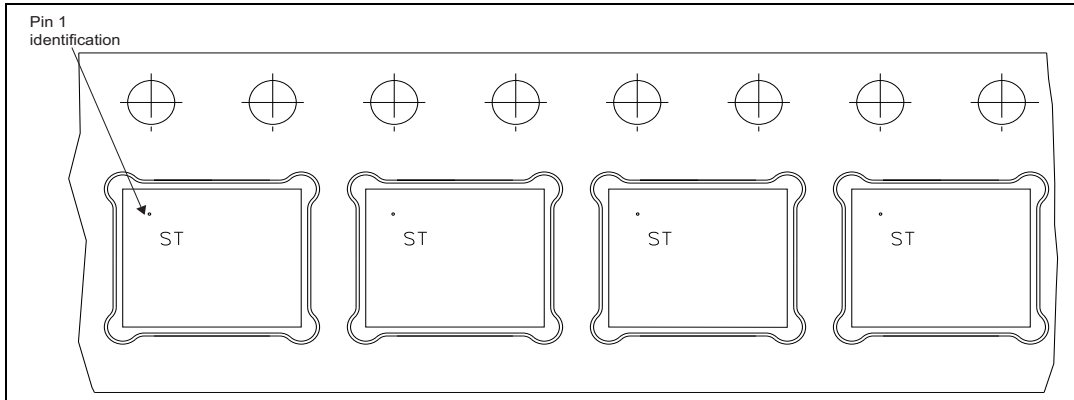


Figure 19. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Mar-2013	1	First release.
14-Jul-2014	2	<ul style="list-style-type: none">– Modified: I_D and I_{DM} values in Table 2– Modified: the entire typical values in Table 6– Modified: I_{SD} and I_{SDM} max values in Table 7– Added: Section 2.1: Electrical characteristics (curves)– Updated: Section 4: Package mechanical data– Minor text changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved