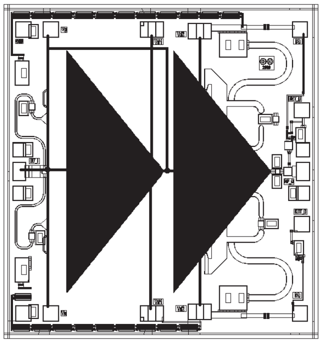
AMMC-6408

6-18 GHz 1W Power Amplifier

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant



Chip Size: 2000 x 2000 µm (78.5 x 78.5 mils)
Chip Size Tolerance: ± 10 µm (±0.4 mils)
Chip Thickness: 100 ± 10 µm (4 ± 0.4 mils)
Pad Dimensions: 100 x 100 µm (4 ± 0.4 mils)

Description

The AMMC-6408 MMIC is a broadband 1W power amplifier in a surface mount package designed for use in transmitters that operate in various frequency bands between 6GHz and 18GHz. At 8GHz, it provides 29 dBm of output power (P-1dB) and 20dB of small-signal gain from a small easy-to-use device. This MMIC is optimized for linear operation with an output third order intercept point (OIP3) of 38dBm.

Applications

- Microwave Radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Features

- Wide Frequency Range 6-18GHz
- Highly linear: OIP3=38dBm
- Integrated RF power detector
- ESD protection (40V MM, and 200V HBM)
- Input port partially matched (For narrowband applications, customer may obtain optimum matching and gain with an additional matching circuit)
- Specifications (Vdd=5V, Idq=650mA)
- Frequency range 6 to 18 GHz
- Small signal Gain of 18dB
- Return loss: Input: -3 dB, Output: -9 dB
- High Power: @ 8 GHz, P-1dB = 29 dBm

Attention: Observe Precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class0)
Refer to Avago Application Note A0040R:
Electro Discharge Damage and Control.
Note: This MMIC uses depletion mode pHEMT devices. Negative supply is used for the DC gate biasing.

Absolute Maximum Ratings

Symbols	Parameters	Units	Minimum	Maximum	Notes
Vd-Vg	Drain to Gate Voltage	V		8	
Vd	Positive Supply Voltage	V		5.5	
Vg	Gate Supply Voltage	V	-2.5	0.5	
Id	Drain Current	mA		TBD	2
PD	Power Dissipation	W		3.5	2 and 3
Pin	CW Input Power	dBm		20	2
Tch	Operating Channel Temp	°C		+150	4
Tstg	Storage Case Temp.	°C		-65 to +155	
Tmax	Maximum Assembly Temp (30 sec max)	°C		+320	

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. Functional operation at or near these limitations will significantly reduce the lifetime of the device.
2. Dissipated power PD is in any combination of DC voltage, Drain Current, input power and power delivered to the load.
3. When operated at maximum PD with a base plate temperature of 85 °C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET. The operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures (Tj) be maintained at the lowest possible levels. See MTTF vs. Tchannel Temperature Table.

DC Specifications/ Physical Properties

Symbol	Parameters and Test Conditions	Units	Value
I_{dq}	Drain Supply Current (V_{dd}=5 V, V_g set for I_d Typical)	mA	650
V_g	Gate Supply Operating Voltage ($I_{d(Q)}$ = 650 (mA))	V	-1.1
$R_{\theta jc}$	Thermal Resistance[6] (Channel-to-Base Plate)	°C/W	22
T_{ch}	Channel Temperature	°C	150.6

Notes:

6. Channel-to-backside Thermal Resistance (θch-b) = 10°C/W at Tchannel (Tc) = 107°C as measured using infrared microscopy. Thermal Resistance at backside temperature (Tb) = 25°C calculated from measured data.

Thermal Properties

Parameter	Test Conditions	Value
Maximum Power Dissipation	Tbaseplate = 85°C	PD = 3.5W Tchannel = 150°C
Thermal Resistance (θjc)	Vd = 5V Id = 650mA PD = 3.25W Tbaseplate = 75°C	θjc = 22°C/W Tchannel = 146°C
Thermal Resistance (θjc) Under RF Drive	Vd = 5V Id = 810mA Pout = 29dBm Pd = 3.3W Tbaseplate = 85°C	θjc = 22°C/W Tchannel = 147°C

MTTF vs. Tchannel Temperature

Operation	60% Confidence Level		90% Confidence Level		Point Data R=	
Tj	**λ (ΦIT)**	**MTTF (hrs)**	**λ (ΦIT)**	**MTTF (hrs)**	**λ (ΦIT)**	**MTTF (Yrs)**
150	3511	2.8E+05	8822	1.1E+05	3831	2.6E+05
140	1298	7.7E+05	3260	3.1E+05	1416	7.1E+05
130	456	2.2E+06	1147	8.7E+05	498	2.0E+05
120	152	6.6E+06	382	2.6E+06	166	6.0E+06
110	48	2.1E+07	120	8.3E+06	52	1.9E+06
100	14	7.0E+07	36	2.8E+07	15	6.5E+07
90	4	2.5E+08	10	1.0E+08	4	2.3E+08
80	1	9.9E+08	3	3.9E+08	1	9.1E+08
70	0	4.2E+09	1	1.7E+09	0	3.8E+09
60	0	1.9E+10	0	7.6E+09	0	1.7E+10
50	0	9.6E+10	0	3.8E+10	0	8.8E+10

RF Specifications [7,8,9]

T_A= 25°C, V_{dd} = 5V, $I_{d(Q)}$ = 650mA, Z_o=50Ω

Symbol	Parameters and Test Conditions	Units	Minimum	Typical	Maximum
Freq	Operational Frequency	GHz	6		18
Gain	Small-signal Gain S21[9,10]	dB	16	19	
P_{-1dB}	Output Power at 1dB [9,10] Gain Compression[8]	dBm	26	29	
P_{-3dB}	Output Power at 3dB Gain Compression[9]	dBm		29.5	
OIP_3	Third Order Intercept Point; Δf=10MHz; Pin=-20dBm	dBm		38	
RL_{in}	Input Return Loss[8]	dB		3	
RL_{out}	Output Return Loss[8]	dB		9	
Isolation	Reverse Isolation	dB		45	

Notes:
7. Small/Large -signal data measured in packaged form on a 2.4mm connecter based evaluation board at TA = 25°C.
8. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies
9. Pre-assembly into package performance verified 100% on-wafer published specifications at Frequencies=8, 12, and 17GHz

Typical Performances

Data obtained from 3.5-mm connector based test fixture, and this data is including connecter loss, and board loss. (TA = 25°C, Vdd =5 V, Idq = 650 mA, Zin = Zout = 50Ω)

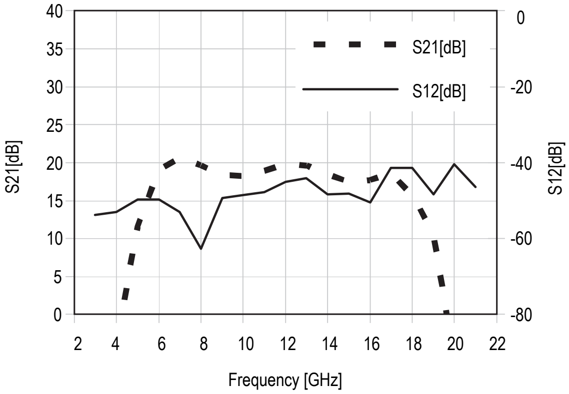


Figure 1. Typical Gain and Reverse Isolation

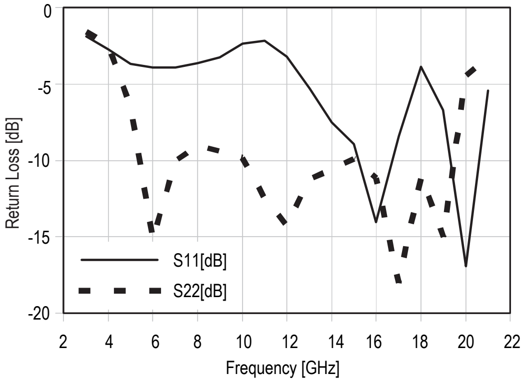


Figure 2. Typical Return Loss (Input and Output)

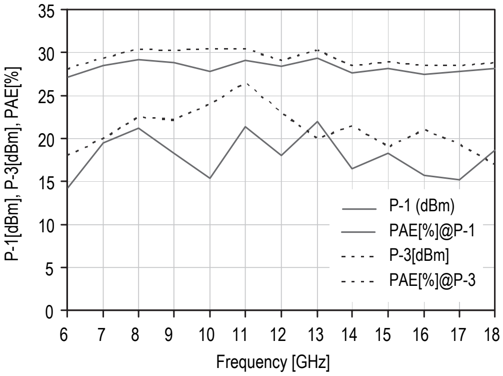


Figure 3. Typical Output Power (@P-1, P-3) and PAE and Frequency

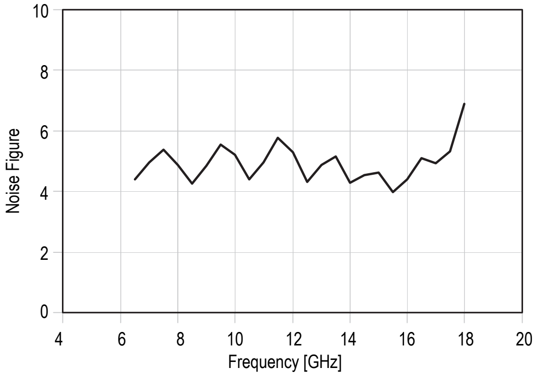


Figure 4. Typical Noise Figure

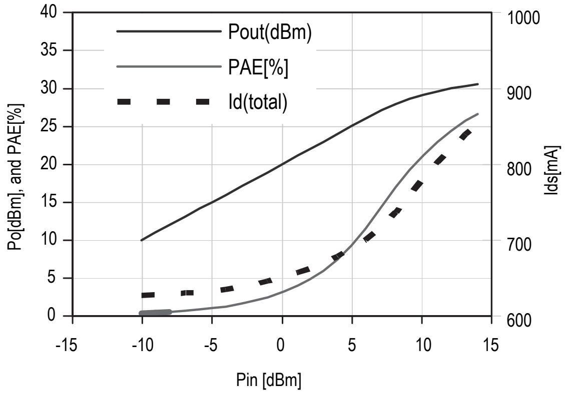


Figure 5. Typical Output Power, PAE, and Total Drain Current versus Input Power at 8GHz

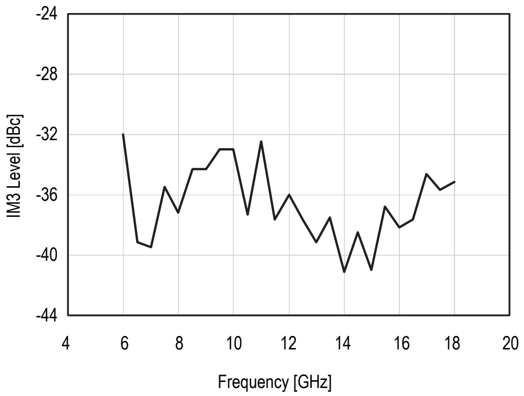


Figure 6. Typical IM3 level vs. Frequency at +20dBm output single carrier level (SCL)

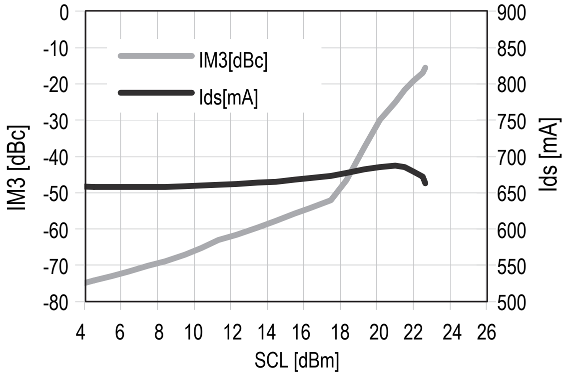


Figure 7. Typical IM3 level and Ids vs. single carrier output level at 6GHz

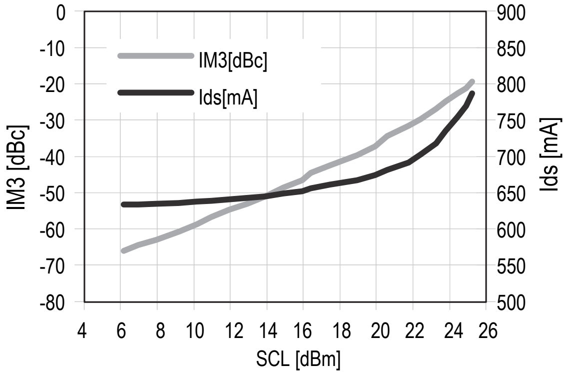


Figure 8. Typical IM3 level and Ids vs. single carrier output level at 8GHz

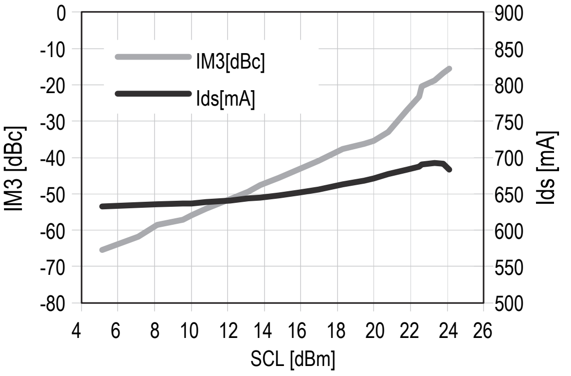


Figure 9. Typical IM3 level and Ids vs. single carrier output level at 12GHz

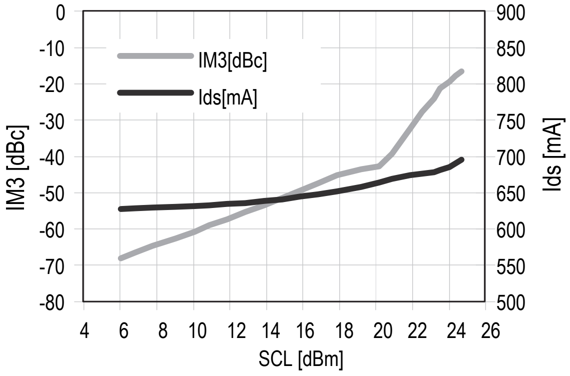


Figure 10. Typical IM3 level and Ids vs. single carrier output level at 14GHz

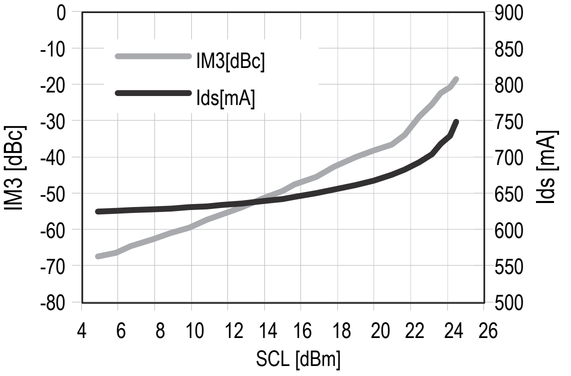


Figure 11. Typical IM3 level and Ids vs. single carrier output level at 16GHz

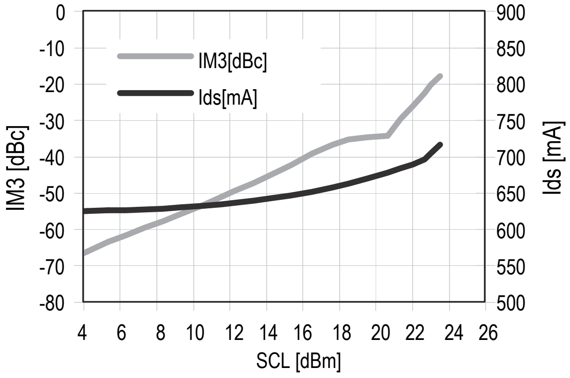


Figure 12. Typical IM3 level and Ids vs. single carrier output level at 18GHz

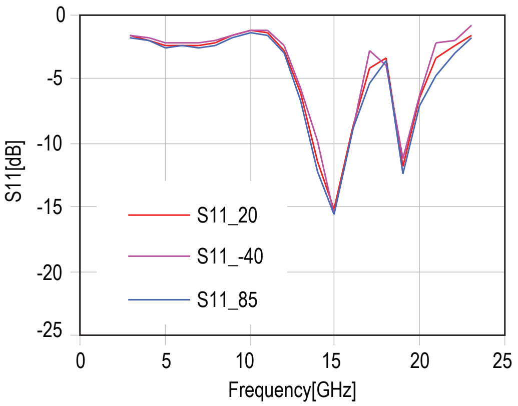


Figure 13. Typical S11 over temperature

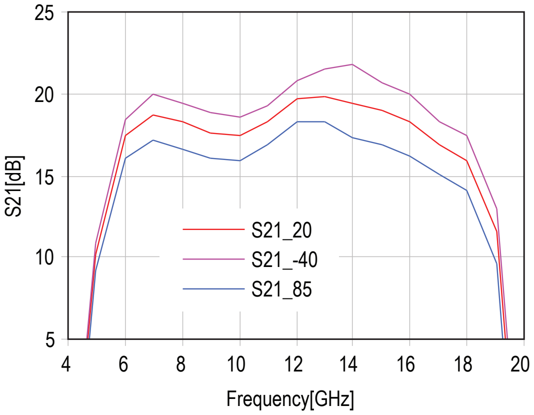


Figure 14. Typical Gain over temperature

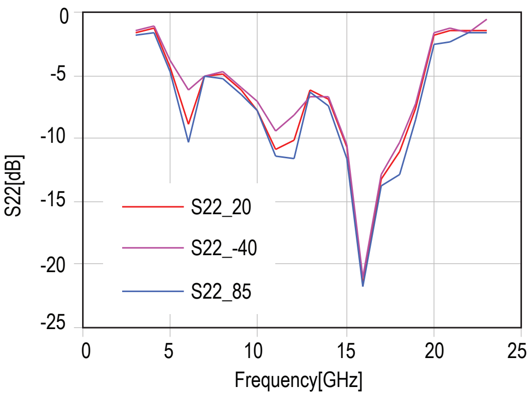


Figure 15. Typical S22 over temperature

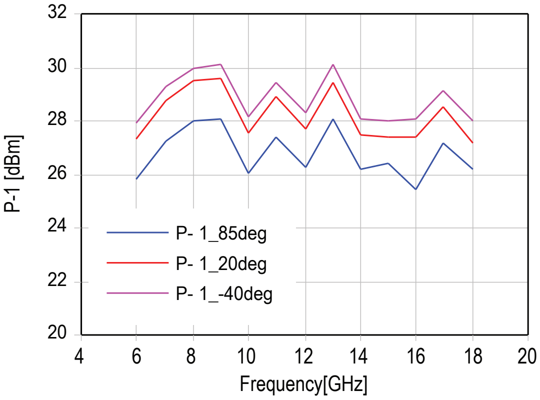


Figure 16. Typical P-1 over temperature

Typical Scattering Parameters [1],

(TA = 25°C, V_{dd} =5 V, I_{dq} = 650mA, Z_{in} = Z_{out} = 50Ω)

Freq [GHz]	S11			S21			S12			S22		
	dB	**Mag**	**Phase**	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**
1	-0.98	0.89	-80.89	-26.63	0.05	-149.73	-66.01	5.01E-04	82.37	-0.74	0.92	-51.38
2	-1.53	0.84	-142.21	-12.58	0.23	117.14	-54.78	1.82E-03	-62.88	-1.05	0.89	-106.38
3	-1.65	0.83	173.02	-13.18	0.22	-55.39	-56.68	1.47E-03	73.25	-1.66	0.83	-148.41
4	-2.03	0.79	136.42	-7.96	0.40	109.98	-57.34	1.36E-03	-176.84	-1.30	0.86	149.67
5	-2.34	0.76	112.17	10.21	3.24	-10.22	-56.51	1.49E-03	82.87	-4.28	0.61	102.57
6	-2.35	0.76	91.21	17.48	7.48	-132.19	-54.26	1.94E-03	-4.69	-8.91	0.36	101.45
7	-2.36	0.76	74.67	18.75	8.66	120.64	-53.94	2.01E-03	-93.95	-5.09	0.56	91.13
8	-2.14	0.78	60.18	18.27	8.19	33.98	-53.73	2.06E-03	-175.11	-4.94	0.57	62.98
9	-1.63	0.83	44.98	17.60	7.58	-40.91	-52.62	2.34E-03	112.21	-6.24	0.49	45.08
10	-1.22	0.87	25.72	17.40	7.41	-108.19	-50.54	2.97E-03	55.24	-7.78	0.41	32.69
11	-1.36	0.85	1.75	18.33	8.25	-174.84	-48.56	3.73E-03	-2.84	-10.88	0.29	28.56
12	-2.70	0.73	-26.91	19.67	9.62	109.90	-45.36	5.40E-03	-66.52	-10.09	0.31	54.94
13	-6.06	0.50	-57.44	19.89	9.88	28.25	-44.34	6.06E-03	-135.27	-6.12	0.49	37.90
14	-11.40	0.27	-98.95	19.46	9.40	-52.18	-44.63	5.87E-03	150.30	-6.84	0.45	8.18
15	-15.19	0.17	174.48	18.96	8.87	-134.19	-43.78	6.47E-03	70.74	-10.65	0.29	-14.37
16	-8.74	0.37	103.71	18.22	8.15	138.55	-43.20	6.92E-03	-13.73	-21.50	0.08	-6.63
17	-4.18	0.62	54.74	16.91	7.00	45.40	-43.60	6.61E-03	-101.77	-13.30	0.22	72.25
18	-3.28	0.69	0.17	15.93	6.26	-57.17	-45.33	5.41E-03	141.97	-11.09	0.28	34.37
19	-11.87	0.26	-103.07	11.58	3.79	147.53	-42.29	7.68E-03	-60.99	-7.67	0.41	109.95
20	-6.57	0.47	42.09	-9.31	0.34	26.24	-48.32	3.84E-03	177.93	-1.90	0.80	48.19
21	-3.36	0.68	-19.76	-24.98	0.06	49.50	-58.04	1.25E-03	133.54	-1.44	0.85	12.31
22	-2.30	0.77	-75.71	-26.16	0.05	-0.95	-60.28	9.69E-04	-167.20	-1.43	0.85	-20.28
23	-1.56	0.84	-136.88	-31.52	0.03	-94.80	-53.26	2.17E-03	152.87	-1.43	0.85	-60.80
24	-0.68	0.92	171.66	-44.35	0.01	154.42	-52.33	2.42E-03	100.99	-1.40	0.85	-112.04
25	-0.50	0.94	135.92	-54.20	0.00	113.23	-55.59	1.66E-03	64.13	-1.09	0.88	-165.45

Note:

1. This data represents package part performances, and does not contain test fixture losses.

Biasing and Operation

The recommended quiescent DC bias condition for optimum efficiency, performance, and reliability is V_{dd}=5 volts with V_g set for I_{dd}=650 mA. Minor improvements in performance are possible depending on the application. The drain bias voltage range is 3 to 5V. A single DC gate supply connected to Vg will bias all gain stages. Muting can be accomplished by setting Vgg to the pinch-off voltage V_p.

A simplified schematic for the AMMC6408 MMIC die is shown in Figure 17. The MMIC die contains ESD and over voltage protection diodes for V_g, Vd1, and Vd2 terminals. In a finalized package form, Vd1 and Vd2 terminals are commonly connected to the V_{dd} terminal. The bonding diagram for the recommended assembly is shown in Figure 18. ESD diodes protect all possible ESD or over voltage damages between V_{gg} and ground, V_{gg} and V_{dd}, V_{dd} and ground. Typical ESD diode current versus diode voltage for 11-connected diodes in series is shown in Figure 19. Under the recommended DC quiescent biasing condition at V_{ds}=5V, I_{ds}=650mA, V_{gg}=-1V, typical gate terminal current is approximately 0.3mA. If an active biasing technique is selected for the AMMC6408 MMIC PA DC biasing, the active biasing circuit must have more than 10-times higher internal current that the gate terminal current.

An optional output power detector network is also provided. A typical measured detector voltage versus output power at 18GHz is shown Figure 20. The differential voltage between the Det-Ref and Det-Out pads can be correlated with the RF power emerging from the RF output port. The detected voltage is given by,

$$V = (V_{ref} - V_{det}) - V_{ofs}$$

where V_{ref} is the voltage at the DET_R port, V_{det} is a voltage at the DET_O port, V_{ofs} and is the zero-input-power offset voltage. There are three methods to calculate V_{ofs}:

1. V_{ofs} can be measured before each detector measurement (by removing or switching off the power source and measuring V_{ref} - V_{det}). This method gives an error due to temperature drift of less than 0.01dB/50°C.
2. V_{ofs} can be measured at a single reference temperature. The drift error will be less than 0.25dB.
3. V_{ofs} can either be characterized over temperature and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate V_{ofs} at any temperature. This method gives an error close to the method #1.

The RF ports are AC coupled at the RF input to the first stage and the RF output of the final stage. No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

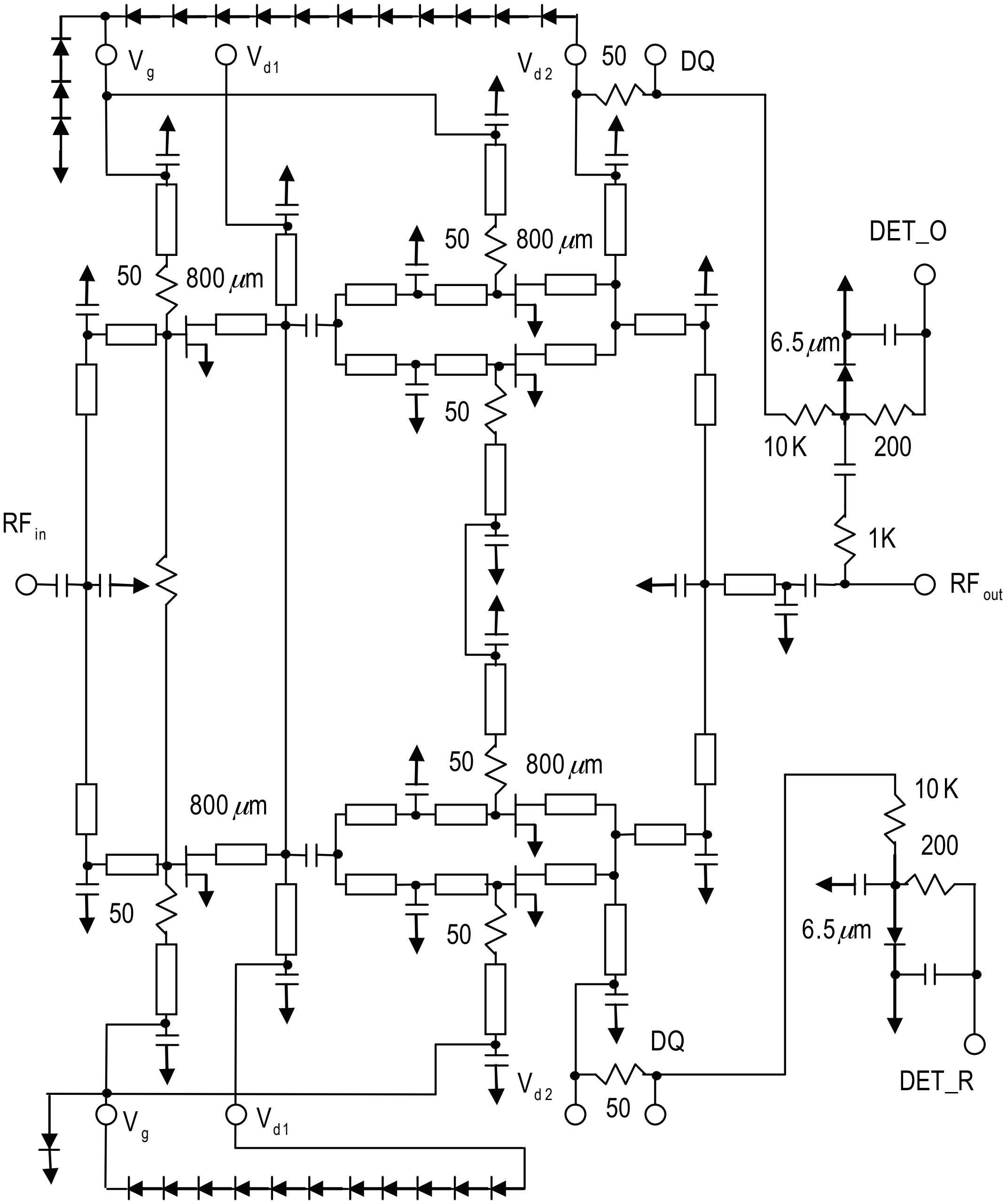


Figure 17. Simplified schematic for the MMIC die

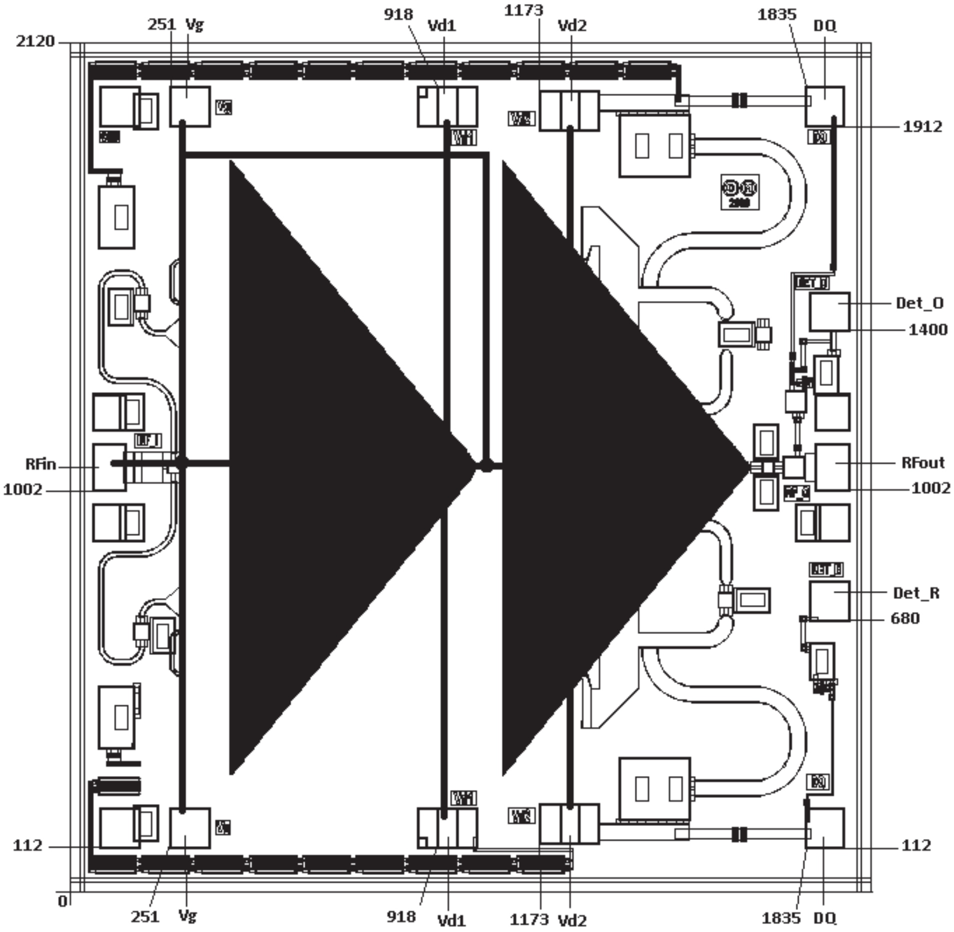


Figure 18. AMMC-6408 Bonding Pad Locations

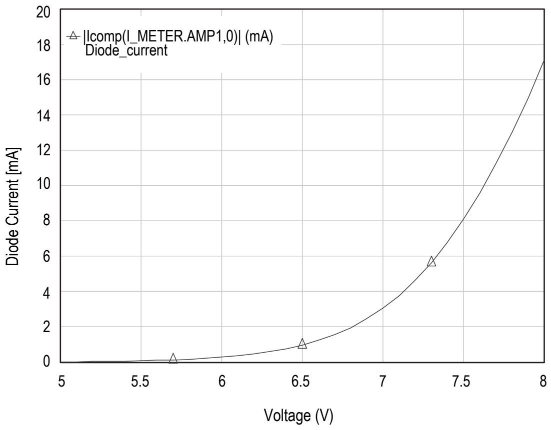


Figure 19. Typical ESD diode current versus diode voltage for 11-connected diodes in series

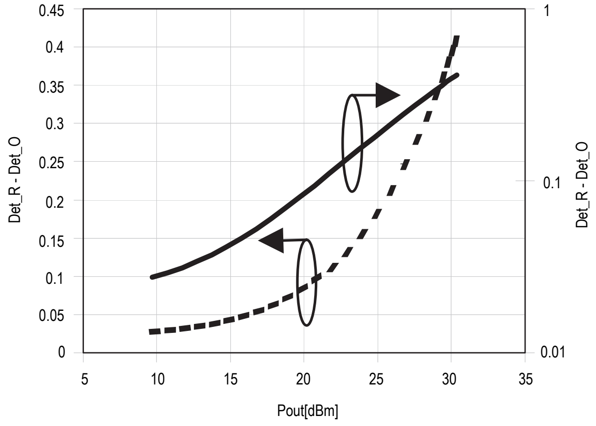
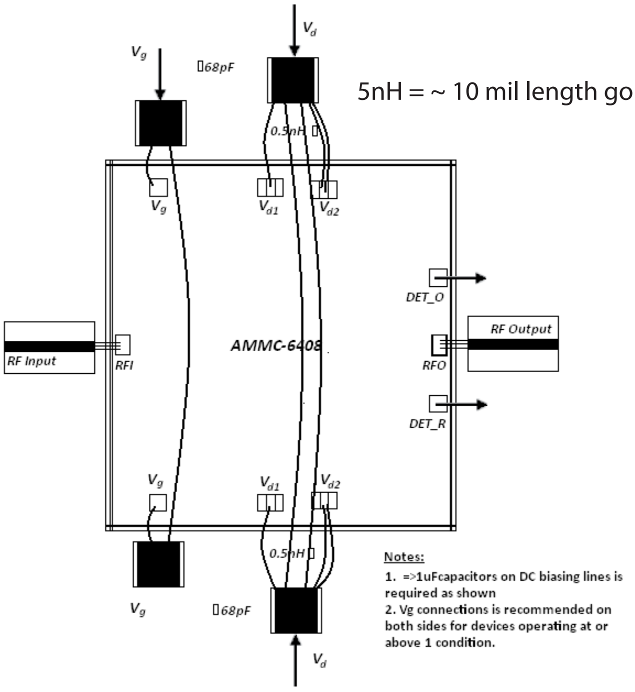


Figure 20. Typical Detector Voltage and Output Power, Freq=18GHz



5nH = ~ 10 mil length gold wire bond (0.7 to 1 mil diameter)

Notes:

1. =>1uFcapacitors on DC biasing lines is required as shown
2. Vg connections is recommended on both sides for devices operating at or above 1 condition.

Figure 21. AMMC-6408 Bonding Diagram

Ordering Information:

AMMC-6408-W10 = 10 devices per tray

AMMC-6408-W50 = 50 devices per tray

Names and Contents of the Toxic and Hazardous Substances or Elements in the Products
产品中有毒有害物质或元素的名称及含量

Part Name 部件名称	Toxic and Hazardous Substances or Elements 有毒有害物质或元素					
	Lead (Pb) 铅 (Pb)	Mercury (Hg) 汞 （Hg ）	Cadmium (Cd) 镉 （Cd ）	Hexavalent (Cr(VI)) 六价 铬（Cr(VI) ）	Polybrominated biphenyl (PBB) 多 溴联苯（PBB ）	Polybrominated diphenylether (PBDE) 多溴二苯醚（PBDE ）
100pF capacitor	○	○	○	○	○	○

○: indicates that the content of the toxic and hazardous substance in all the homogeneous materials of the part is below the concentration limit requirement as described in SJ/T 11363-2006.
×: indicates that the content of the toxic and hazardous substance in at least one homogeneous material of the part exceeds the concentration limit requirement as described in SJ/T 11363-2006.
(The enterprise may further explain the technical reasons for the “x” indicated portion in the table in accordance with the actual situations.)

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。
×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。
（企业可在此处，根据实际情况对上表中打“×” 的技术原因进行进一步说明。）

Note: EU RoHS compliant under exemption clause of “lead in electronic ceramic parts (e.g. piezoelectronic devices)”

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**