User's Manual

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R8C/M11A Group, R8C/M12A Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/Mx Series

Renesas Electronics
www.renesas.com

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(2012.4)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. For details, see the text of the manual.

The following documents apply to the R8C/M11A Group and R8C/M12A Group. Make sure to see the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/M11A Group, R8C/M12A Group Datasheet	R01DS0010EJ
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: For details on using peripheral functions, see the application notes.	R8C/M11A Group, R8C/M12A Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the SRST bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	—	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b3	—	Reserved	Set to 0.	W
b4	—			
b5	XXX5	XXX bits	Function varies depending on the operating mode.	R/W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2 *3

*1
R/W: Read and write.
R: Read only.
W: Write only.
—: Nothing is assigned.

*2
• Reserved
Reserved bits. Set to the specified value.

*3
• Nothing is assigned.
Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
• Do not set.
Operation is not guaranteed when a value is set.
• Function varies depending on the operating mode.
The function of the bit varies with the peripheral function mode. For information on the individual modes, see the register diagram.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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0000Ch			
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00027h			
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Address	Register Name	Symbol	Page
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0004Bh	Interrupt Priority Level Register B	ILVLB	115
0004Ch	Interrupt Priority Level Register C	ILVLC	115
0004Dh	Interrupt Priority Level Register D	ILVLD	115
0004Eh	Interrupt Priority Level Register E	ILVLE	115
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Note:
1. The blank areas are reserved. No access is allowed.

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Note:
1. The blank areas are reserved. No access is allowed.

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Note:

1. The blank areas are reserved. No access is allowed.

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Note:
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001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			
:			
0FFDBh	Option Function Select Register 2	OFS2	31, 40
:			
0FFFFh	Option Function Select Register	OFS	32, 41

1. Overview

1.1 Features

The R8C/M11A Group and R8C/M12A Group of single-chip microcontrollers (MCUs) incorporate the R8C CPU core, which provides sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, the CPU core is capable of executing instructions at high speed. In addition, it features a multiplier for high-speed arithmetic processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions on the same chip, including multifunction timer and serial interface, reduces the number of system components.
The R8C/M11A Group and R8C/M12A Group include data flash (1 KB × 2 blocks).

1.1.1 Applications

Home appliances, office equipment, audio equipment, consumer products, etc.

1.1.2 Differences between Groups

Table 1.1 lists the Specification Comparison between R8C/M11A Group and R8C/M12A Group. The explanations in 1.1.3 and subsequent sections apply to the R8C/M12A Group specifications only, unless otherwise specified.

Table 1.1 Specification Comparison between R8C/M11A Group and R8C/M12A Group

Item	Function	R8C/M11A Group	R8C/M12A Group
Interrupts	External interrupt inputs	6 ($\overline{\text{INT}}$ × 3, key input × 3)	8 ($\overline{\text{INT}}$ × 4, key input × 4)
I/O ports	Number of pins	14 Non-provided pins: P1_0/AN0/TRCIOD/$\overline{\text{KI0}}$ P3_3/IVCMP3/TRCCLK/$\overline{\text{INT3}}$ P3_4/IVREF3/TRCIOC/$\overline{\text{INT2}}$ P3_5/TRCIOD/$\overline{\text{KI2}}$/$\overline{\text{VCOUT}}$3 P4_2/$\overline{\text{TRBO}}$/$\overline{\text{TXD0}}$/$\overline{\text{KI3}}$ P4_5/$\overline{\text{INT0}}$/$\overline{\text{ADTRG}}$	20
	Number of CMOS I/O ports	11 Non-provided ports: P1_0, P3_3, P3_4, P3_5, P4_2, P4_5	17
	Number of high-current drive ports	5 Non-provided ports: P3_3, P3_4, P3_5	8
A/D converter	Number of A/D channels	5 channels Non-provided port: AN0	6 channels
Comparator B	Number of channels	Comparator B1	Comparator B1, comparator B3

Table 1.2 lists the R8C/M11A Group Register Settings. These settings correspond to the specification differences between the R8C/M11A Group and R8C/M12A Group.

Table 1.2 R8C/M11A Group Register Settings

Related Function	Register Name	Address	Bit	Setting Method for Access
$\overline{\text{INT3}}$	INTEN	00038h	INT3EN	Reserved bit. Set to 0.
	INTF0	0003Ah	INT3F0, INT3F1	Reserved bits. Set to 0.
	ISCR0	0003Ch	INT3SA, INT3SB	Reserved bits. Set to 0.
	ILVLD	0004Dh	ILVLD0, ILVLD1	Reserved bits. Set to 0.
	IRR3	00053h	IRI3	Reserved bit. Set to 0.
$\overline{\text{KI0}}$	KIEN	0003Eh	KI0EN, KI0PL	Reserved bits. Set to 0.
Comparator B3 interrupt	ILVL2	00042h	ILVL24, ILVL25	Reserved bits. Set to 0.
	IRR2	00052h	IRCMP3	Reserved bit. Set to 0.
P1_0	PD1	000A9h	PD1_0	Reserved bit. Set to 0.
	P1	000AFh	P1_0	Reserved bit. Set to 0.
	PUR1	000B5h	PU1_0	Reserved bit. Set to 0.
	POD1	000C1h	POD1_0	Reserved bit. Set to 0.
	PML1	000C8h	P10SEL0, P10SEL1	Reserved bits. Set to 0.
P3_3, P3_4, P3_5	PD3	000ABh	PD3_3, PD3_4, PD3_5	Reserved bits. Set to 0.
	P3	000B1h	P3_3, P3_4, P3_5	Reserved bits. Set to 0.
	PUR3	000B7h	PU3_3, PU3_4, PU3_5	Reserved bits. Set to 0.
	DRR3	000BDh	DRR3_3, DRR3_4, DRR3_5	Reserved bits. Set to 0.
	POD3	000C3h	POD3_3, POD3_4, POD3_5	Reserved bits. Set to 0.
	PML3	000CCh	P33SEL0, P33SEL1	Reserved bits. Set to 0.
	PMH3	000CDh	P34SEL0, P34SEL1, P35SEL0, P35SEL1	Reserved bits. Set to 0.
P4_2, P4_5	PD4	000ACh	PD4_2, PD4_5	Reserved bits. Set to 0.
	P4	000B2h	P4_2, P4_5	Reserved bits. Set to 0.
	PUR4	000B8h	PU4_2, PU4_5	Reserved bits. Set to 0.
	POD4	000C4h	POD4_2, POD4_5	Reserved bits. Set to 0.
	PML4	000CEh	P42SEL0, P42SEL1	Reserved bits. Set to 0.
	PMH4	000CFh	P45SEL0, P45SEL1	Reserved bits. Set to 0.
AN0	ADINSEL	0009Dh	CH0, ADGSEL0, ADGSEL1	Do not set to 000.
Comparator B3	WCMPR	00180h	WCB3M0, WCB3OUT	Reserved bits. Set to 0.
	WCB3INTR	00182h	All bits	Reserved register. No access is allowed.

1.1.3 Specifications

Tables 1.3 and 1.4 outline the Specifications.

Table 1.3 Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	See **Table 1.5 Product List**.
Reset sources		• Hardware reset by $\overline{\text{RESET}}$ • Power-on reset • Watchdog timer reset • Software reset • Reset by voltage detection 0
Voltage detection	Voltage detection circuit	Voltage detection with two check points: Voltage detection 0, voltage detection 1 (detection levels selectable)
Watchdog timer		• 14 bits × 1 (with prescaler) • Reset start function selectable • Count source protection function selectable • Periodic timer function selectable
Clock	Clock generation circuits	• 3 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Clock frequency divider circuit integrated
Power control		• Standard operating mode • Wait mode (CPU stopped, peripheral functions in operation) • Stop mode (CPU and peripheral functions stopped)
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 8 ($\overline{\text{INT}}$ × 4, key input × 4) • Priority levels: 2
I/O ports	Programmable I/O ports	• CMOS I/O: 17 (pull-up resistor selectable) • High-current drive ports: 8
Timer	Timer RJ2	16 bits × 1 Timer mode, pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2	8 bits × 1 (with 8-bit prescaler) or 16 bits × 1 (selectable) Timer mode, programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (output compare function, input capture function), PWM mode (3 outputs), PWM2 mode (1 PWM output)
Serial interface	UART0	Clock synchronous serial I/O. Also used for asynchronous serial I/O.
A/D converter		• Resolution: 10 bits × 6 channels • Sample and hold function, sweep mode
Comparator B		2 circuits

Table 1.4 Specifications (2)

Item	Function	Description
Flash memory		• Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function
Operating frequency/ Power supply voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Temperature range		-20 °C to 85 °C (N version) -40 °C to 85 °C (D version) (1)
Package		14-pin TSSOP: [Package code] PTSP0014JA-B 14-pin DIP: [Package code] PRDP0014AC-A 20-pin LSSOP: [Package code] PLSP0020JB-A 20-pin DIP: [Package code] PRDP0020AD-A

Note:
1. Specify the D version if it is to be used.

1.2 Product List

Table 1.5 lists the Product List. Figure 1.1 shows the Product Part Number Structure.

Table 1.5 Product List **Current of May 2012**

Group Name	Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
		Program ROM	Data Flash			
R8C/M11A Group	R5F2M110ANSP	2 Kbytes	1 Kbyte × 2	256 bytes	PTSP0014JA-B	N version
	R5F2M111ANSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ANSP	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M110ANDD	2 Kbytes	1 Kbyte × 2	256 bytes	PRDP0014AC-A	
	R5F2M111ANDD	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ANDD	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M110ADSP	2 Kbytes	1 Kbyte × 2	256 bytes	PTSP0014JA-B	D version
	R5F2M111ADSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M112ADSP	8 Kbytes	1 Kbyte × 2	512 bytes		
R8C/M12A Group	R5F2M120ANSP	2 Kbytes	1 Kbyte × 2	256 bytes	PLSP0020JB-A	N version
	R5F2M121ANSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ANSP	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M120ANDD	2 Kbytes	1 Kbyte × 2	256 bytes	PRDP0020AD-A	
	R5F2M121ANDD	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ANDD	8 Kbytes	1 Kbyte × 2	512 bytes		
	R5F2M120ADSP	2 Kbytes	1 Kbyte × 2	256 bytes	PLSP0020JB-A	D version
	R5F2M121ADSP	4 Kbytes	1 Kbyte × 2	384 bytes		
	R5F2M122ADSP	8 Kbytes	1 Kbyte × 2	512 bytes		

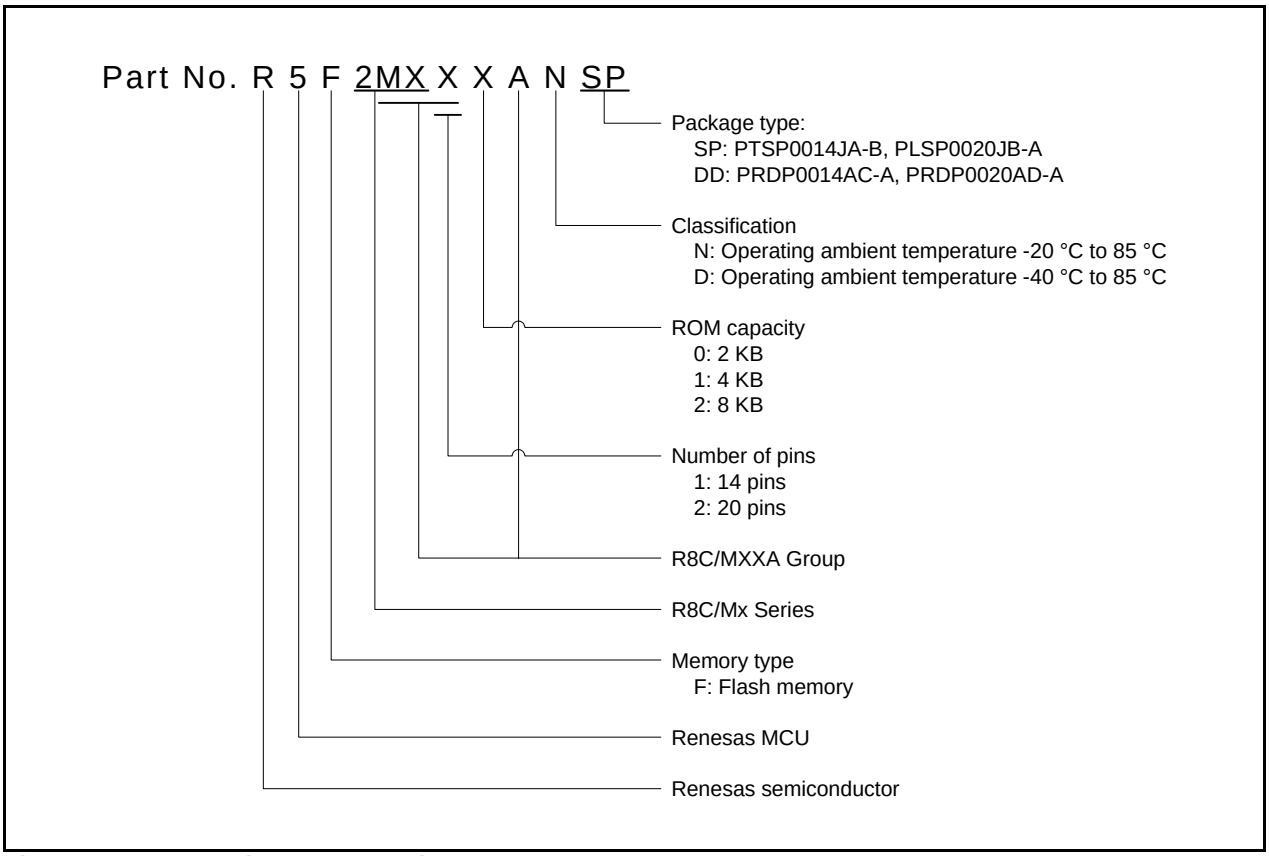


Figure 1.1 Product Part Number Structure

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

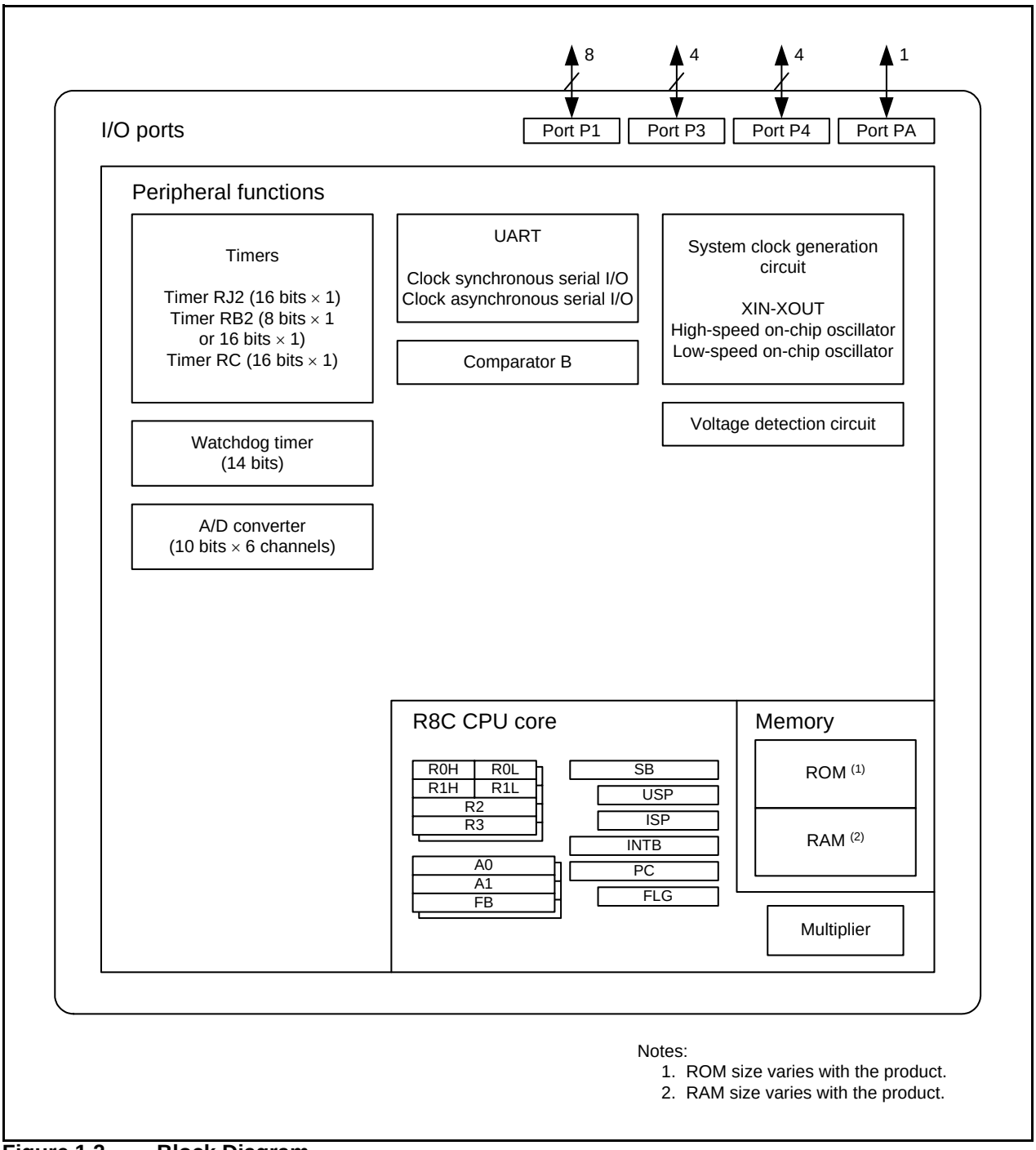
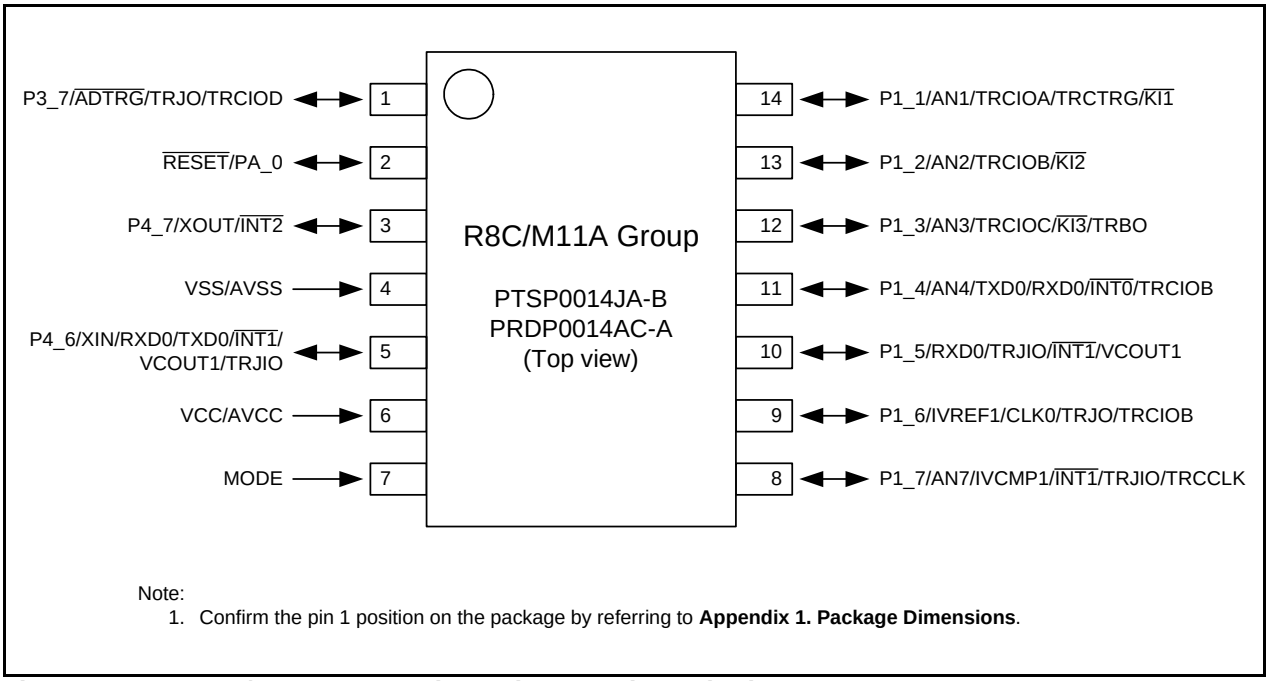


Figure 1.2 Block Diagram

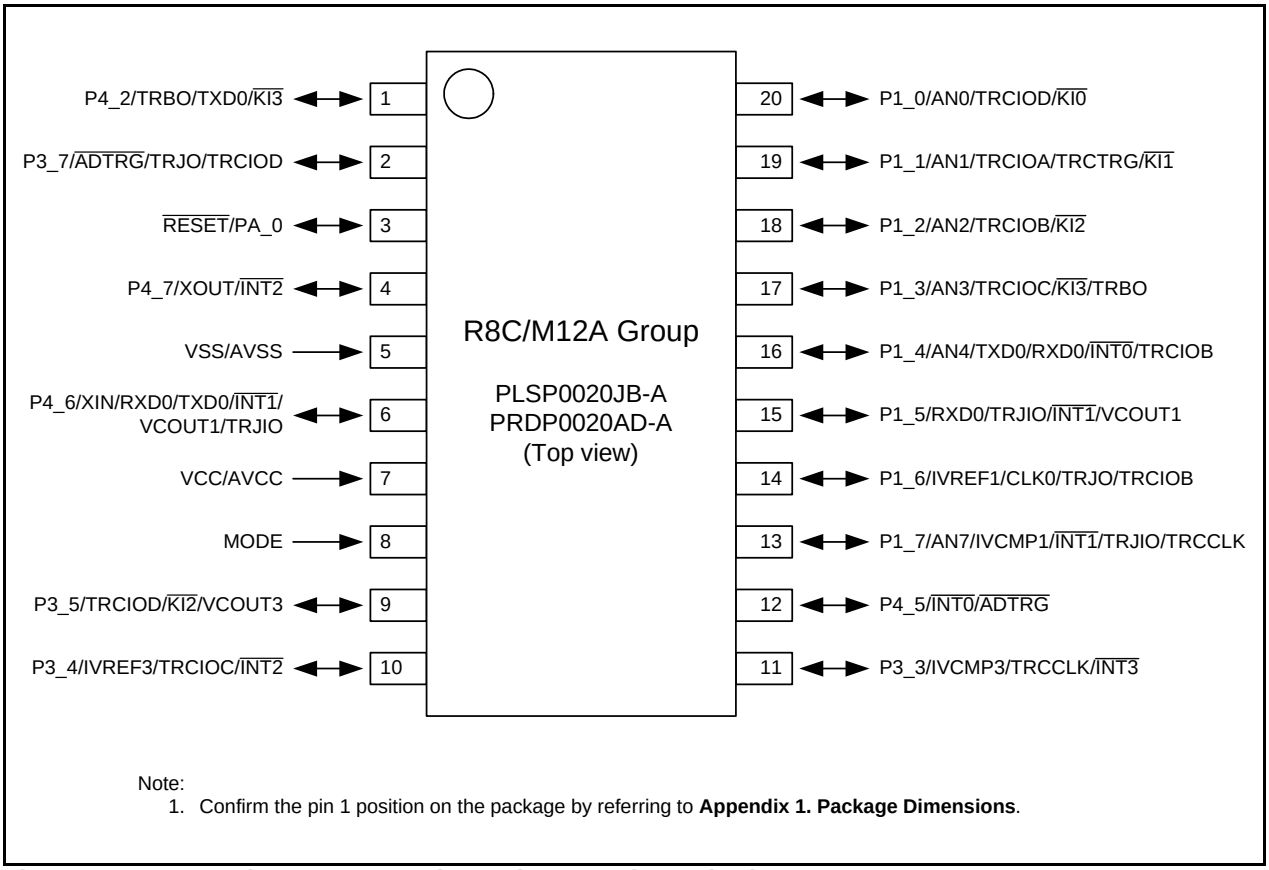
1.4 Pin Assignment

Figures 1.3 and 1.4 show Pin Assignment (Top View). Table 1.6 lists the Pin Name Information by Pin Number.



Note:
1. Confirm the pin 1 position on the package by referring to **Appendix 1. Package Dimensions**.

Figure 1.3 R8C/M11A Group Pin Assignment (Top View)



Note:
1. Confirm the pin 1 position on the package by referring to **Appendix 1. Package Dimensions**.

Figure 1.4 R8C/M12A Group Pin Assignment (Top View)

Table 1.6 Pin Name Information by Pin Number

Pin Number		Control Pin	Port	I/O Pins for Peripheral Functions			
R8C/M11A Group	R8C/M12A Group			Interrupt	Timer	Serial Interface	A/D Converter, Comparator B
	1		P4_2	$\overline{KI3}$	TRBO	TXD0	
1	2		P3_7		TRJO/TRCIOD		$\overline{ADTRG}$
2	3	$\overline{RESET}$	PA_0				
3	4	XOUT	P4_7	$\overline{INT2}$			
4	5	VSS/AVSS					
5	6	XIN	P4_6	$\overline{INT1}$	TRJIO	RXD0/TXD0	VCOUT1
6	7	VCC/AVCC					
7	8	MODE					
	9		P3_5	$\overline{KI2}$	TRCIOD		VCOUT3
	10		P3_4	$\overline{INT2}$	TRCIOC		IVREF3
	11		P3_3	$\overline{INT3}$	TRCCLK		IVCMP3
	12		P4_5	$\overline{INT0}$			$\overline{ADTRG}$
8	13		P1_7	$\overline{INT1}$	TRJIO/TRCCLK		AN7/IVCMP1
9	14		P1_6		TRJO/TRCIOB	CLK0	IVREF1
10	15		P1_5	$\overline{INT1}$	TRJIO	RXD0	VCOUT1
11	16		P1_4	$\overline{INT0}$	TRCIOB	RXD0/TXD0	AN4
12	17		P1_3	$\overline{KI3}$	TRBO/TRCIOC		AN3
13	18		P1_2	$\overline{KI2}$	TRCIOB		AN2
14	19		P1_1	$\overline{KI1}$	TRCIOA/TRCTRG		AN1
	20		P1_0	$\overline{KI0}$	TRCIOD		AN0

1.5 Pin Functions

Table 1.7 lists the Pin Functions.

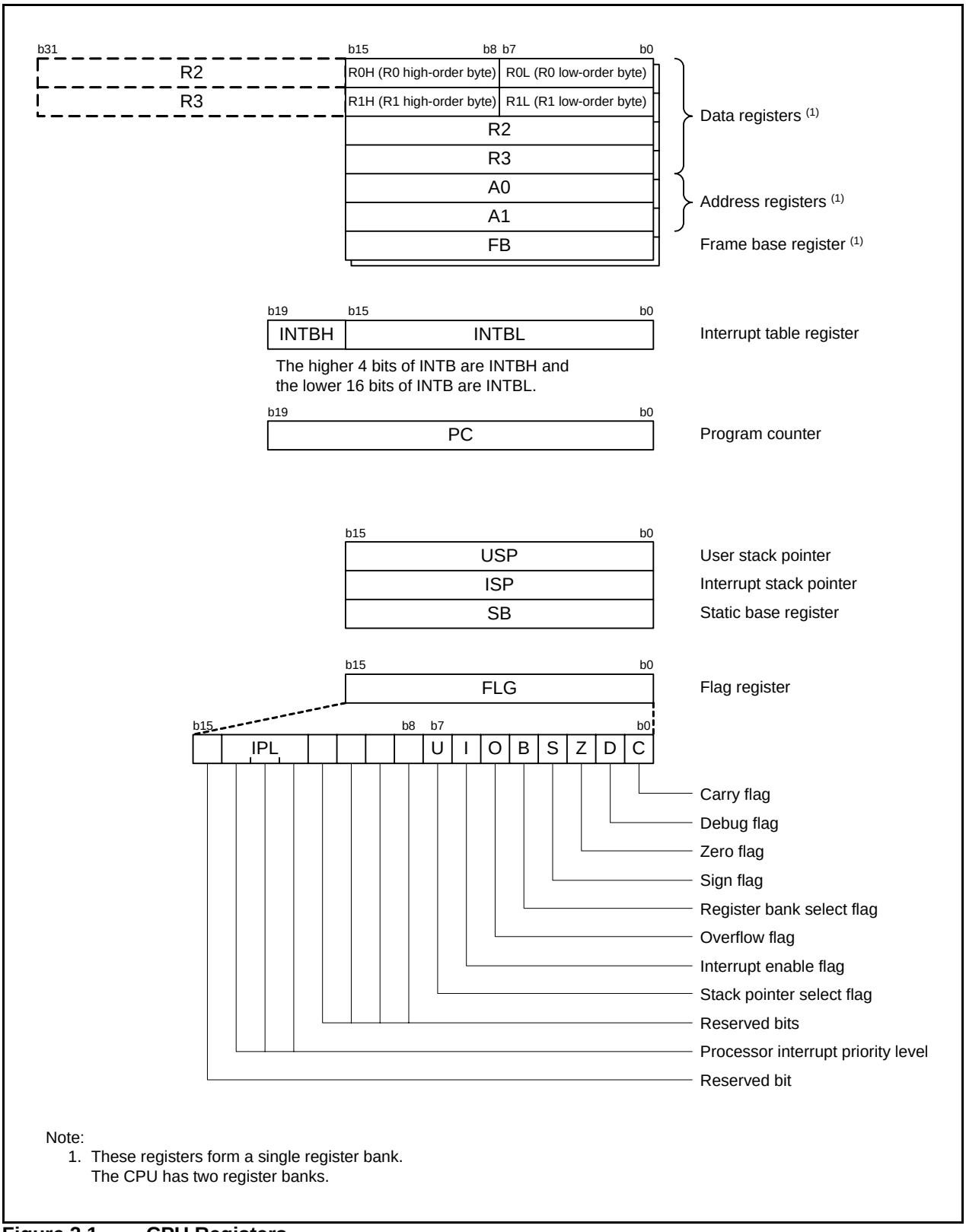
Table 1.7 Pin Functions

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin. P4_7 can be used as an I/O port at this time.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
I/O ports	P1_0 to P1_7, P3_0 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0	I/O	CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports.
Timer RJ2	TRJIO	I/O	Timer RJ2 I/O.
	TRJO	O	Timer RJ2 output.
Timer RB2	TRBO	O	Timer RB2 output.
Timer RC	TRCCLK	I	External clock input.
	TRCTRG	I	External trigger input.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O.
Serial interface	CLK0	I/O	Transfer clock I/O.
	RXD0	I	Serial data input.
	TXD0	O	Serial data output.
A/D converter	AN0 to AN4, AN7	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
	VCOUT1, VCOUT3	O	Comparison result output for comparator B.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers, R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank. The CPU has two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3.
R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). In the same way as with R0 and R2, R3 and R1 can be used as a 32-bit data register (R3R1).

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled. If IPL is set to levels from 2 to 7, all maskable interrupt requests are disabled.

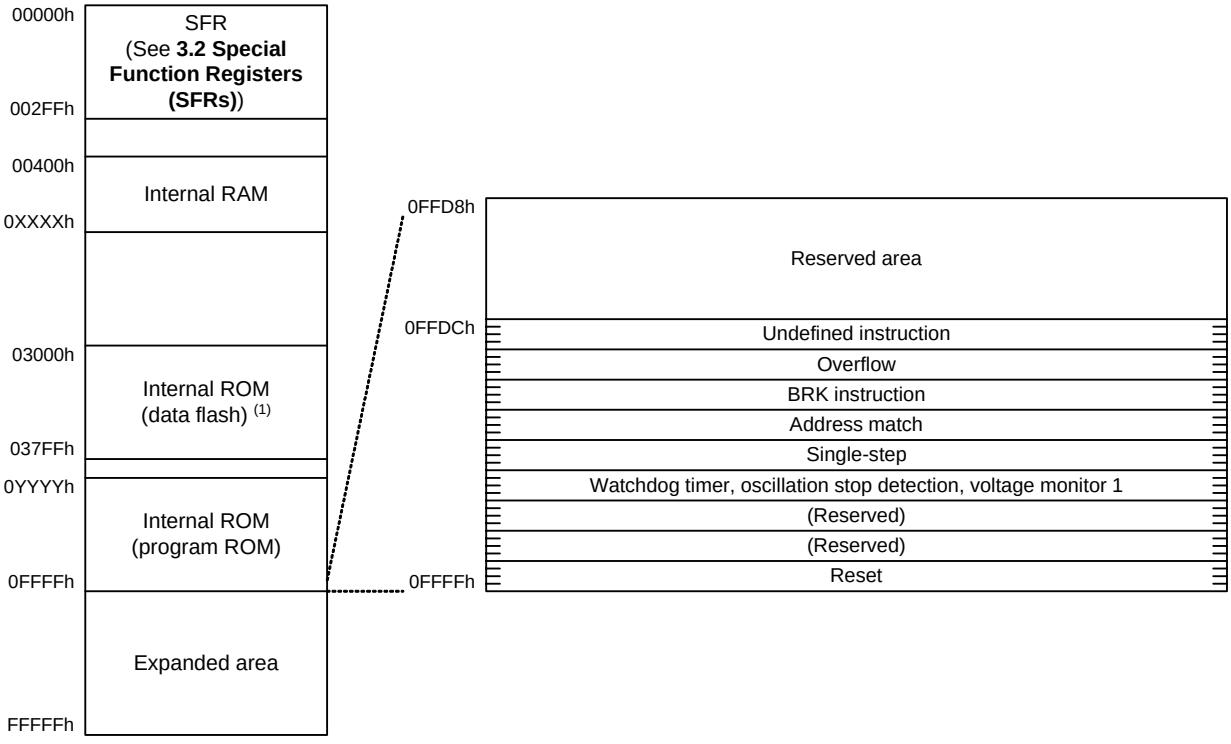
2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/M11A Group and R8C/M12A Group have a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. For example, an 8-Kbyte internal ROM area is allocated at addresses 0E000h to 0FFFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 03000h to 037FFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 512-byte internal RAM area is allocated at addresses 00400h to 005FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte) and block B (1 Kbyte).
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM		Internal RAM	
	Capacity	Address 0YYYYh	Capacity	Address 0XXXXh
R5F2M110ANSP, R5F2M110ANDD, R5F2M110ADSP, R5F2M120ANSP, R5F2M120ANDD, R5F2M120ADSP	2 Kbytes	0F800h	256 bytes	004FFh
R5F2M111ANSP, R5F2M111ANDD, R5F2M111ADSP, R5F2M121ANSP, R5F2M121ANDD, R5F2M121ADSP	4 Kbytes	0F000h	384 bytes	0057Fh
R5F2M112ANSP, R5F2M112ANDD, R5F2M112ADSP, R5F2M122ANSP, R5F2M122ANDD, R5F2M122ADSP	8 Kbytes	0E000h	512 bytes	005FFh

Figure 3.1 Memory Map

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Register Name	Symbol	After Reset
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	00h
00011h			
00012h	Module Standby Control Register	MSTCR	00h (2) 01110111b (3)
00013h	Protect Register	PRCR	00h
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	00h
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	00h
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h
00022h	System Clock f Control Register	SCKCR	00h
00023h	System Clock f Select Register	PHISEL	00h
00024h	Clock Stop Control Register	CKSTPR	00h
00025h	Clock Control Register When Returning from Modes	CKRSCR	00h
00026h	Oscillation Stop Detection Register	BAKCR	00h
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	10000000b (4) 00h (5)
00031h	Watchdog Timer Reset Register	WDTR	XXh
00032h	Watchdog Timer Start Register	WDTS	XXh
00033h	Watchdog Timer Control Register	WDTC	01XXXXXXb
00034h	Count Source Protection Mode Register	CSPR	10000000b (4) 00h (5)
00035h	Periodic Timer Interrupt Control Register	WDTIR	00h
00036h			
00037h			
00038h	External Input Enable Register	INTEN	00h
00039h			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

Table 3.2 SFR Information (2) (1)

Address	Register Name	Symbol	After Reset
0003Ah	INT Input Filter Select Register 0	INTF0	00h
0003Bh			
0003Ch	INT Input Edge Select Register 0	ISCR0	00h
0003Dh			
0003Eh	Key Input Enable Register	KIEN	00h
0003Fh			
00040h	Interrupt Priority Level Register 0	ILVL0	00h
00041h			
00042h	Interrupt Priority Level Register 2	ILVL2	00h
00043h	Interrupt Priority Level Register 3	ILVL3	00h
00044h	Interrupt Priority Level Register 4	ILVL4	00h
00045h	Interrupt Priority Level Register 5	ILVL5	00h
00046h	Interrupt Priority Level Register 6	ILVL6	00h
00047h	Interrupt Priority Level Register 7	ILVL7	00h
00048h	Interrupt Priority Level Register 8	ILVL8	00h
00049h	Interrupt Priority Level Register 9	ILVL9	00h
0004Ah	Interrupt Priority Level Register A	ILVLA	00h
0004Bh	Interrupt Priority Level Register B	ILVLB	00h
0004Ch	Interrupt Priority Level Register C	ILVLC	00h
0004Dh	Interrupt Priority Level Register D	ILVLD	00h
0004Eh	Interrupt Priority Level Register E	ILVLE	00h
0004Fh			
00050h	Interrupt Monitor Flag Register 0	IRR0	00h
00051h	Interrupt Monitor Flag Register 1	IRR1	00h
00052h	Interrupt Monitor Flag Register 2	IRR2	00h
00053h	External Interrupt Flag Register	IRR3	00h
00054h			
00055h			
00056h			
00057h			
00058h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
00059h			
0005Ah	Voltage Detect Register 2	VCA2	00100100b (2) 00000100b (3)
0005Bh	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0005Ch	Voltage Monitor 0 Circuit Control Register	VW0C	1100X011b (2) 1100X010b (3)
0005Dh	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
0005Eh			
0005Fh	Reset Source Determination Register	RSTFR	0000XXXXb (4)
00060h			
00061h			
00062h			
00063h			
00064h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	Value when shipped
00065h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	Value when shipped
00066h			
00067h	High-Speed On-Chip Oscillator Control Register 1	FRV1	Value when shipped
00068h	High-Speed On-Chip Oscillator Control Register 2	FRV2	Value when shipped
00069h			
0006Ah			
0006Bh			
0006Ch			
0006Dh			
0006Eh			
0006Fh			
00070h			
00071h			
00072h			
00073h			
00074h			
00075h			
00076h			
00077h			
00078h			
00079h			

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. The LVDAS bit in the OFS register is 0.
3. The LVDAS bit in the OFS register is 1.
4. The value after a reset differs depending on the reset source.

Table 3.3 SFR Information (3) (1)

Address	Register Name	Symbol	After Reset
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0 Transmit/Receive Mode Register	U0MR	00h
00081h	UART0 Bit Rate Register	U0BRG	XXh
00082h	UART0 Transmit Buffer Register	U0TBL	XXh
00083h		U0TBH	XXh
00084h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00085h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00086h	UART0 Receive Buffer Register	U0RBL	XXh
00087h		U0RBH	XXh
00088h	UART0 Interrupt Flag and Enable Register	U0IR	00h
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	XXh
00099h		AD0H	000000XXb
0009Ah	A/D Register 1	AD1L	XXh
0009Bh		AD1H	000000XXb
0009Ch	A/D Mode Register	ADMOD	00h
0009Dh	A/D Input Select Register	ADINSEL	00h
0009Eh	A/D Control Register 0	ADCON0	00h
0009Fh	A/D Interrupt Control Status Register	ADICSR	00h
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h	Port P1 Direction Register	PD1	00h
000AAh			
000ABh	Port P3 Direction Register	PD3	00h
000ACh	Port P4 Direction Register	PD4	00h
000ADh	Port PA Direction Register	PDA	00h
000AEh			
000AFh	Port P1 Register	P1	00h
000B0h			
000B1h	Port P3 Register	P3	00h
000B2h	Port P4 Register	P4	00h
000B3h	Port PA Register	PA	00h
000B4h			
000B5h	Pull-Up Control Register 1	PUR1	00h
000B6h			
000B7h	Pull-Up Control Register 3	PUR3	00h
000B8h	Pull-Up Control Register 4	PUR4	00h
000B9h	Port I/O Function Control Register	PINSR	00h
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	00h
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	00h
000BEh			
000BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

Address	Register Name	Symbol	After Reset
000C0h			
000C1h	Open-Drain Control Register 1	POD1	00h
000C2h			
000C3h	Open-Drain Control Register 3	POD3	00h
000C4h	Open-Drain Control Register 4	POD4	00h
000C5h	Port PA Mode Control Register	PAMCR	00010001b
000C6h			
000C7h			
000C8h	Port 1 Function Mapping Register 0	PML1	00h
000C9h	Port 1 Function Mapping Register 1	PMH1	00h
000CAh			
000CBh			
000CCh	Port 3 Function Mapping Register 0	PML3	00h
000CDh	Port 3 Function Mapping Register 1	PMH3	00h
000CEh	Port 4 Function Mapping Register 0	PML4	00h
000CFh	Port 4 Function Mapping Register 1	PMH4	00h
000D0h			
000D1h	Port 1 Function Mapping Expansion Register	PMH1E	00h
000D2h			
000D3h			
000D4h			
000D5h	Port 4 Function Mapping Expansion Register	PMH4E	00h
000D6h			
000D7h			
000D8h	Timer RJ Counter Register	TRJ	FFh
000D9h			FFh
000DAh	Timer RJ Control Register	TRJCR	00h
000DBh	Timer RJ I/O Control Register	TRJIOC	00h
000DCh	Timer RJ Mode Register	TRJMR	00h
000DDh	Timer RJ Event Select Register	TRJISR	00h
000DEh	Timer RJ Interrupt Control Register	TRJIR	00h
000DFh			
000E0h	Timer RB Control Register	TRBCR	00h
000E1h	Timer RB One-Shot Control Register	TRBOCR	00h
000E2h	Timer RB I/O Control Register	TRBIOC	00h
000E3h	Timer RB Mode Register	TRBMR	00h
000E4h	Timer RB Prescaler Register (2) Timer RB Primary/Secondary Register (Lower 8 Bits) (3)	TRBPRE	FFh
000E5h	Timer RB Primary Register (2) Timer RB Primary Register (Higher 8 Bits) (3)	TRBPR	FFh
000E6h	Timer RB Secondary Register (2) Timer RB Secondary Register (Higher 8 Bits) (3)	TRBSC	FFh
000E7h	Timer RB Interrupt Control Register	TRBIR	00h
000E8h	Timer RC Counter	TRCCNT	00h
000E9h			00h
000EAh	Timer RC General Register A	TRCGRA	FFh
000EBh			FFh
000ECh	Timer RC General Register B	TRCGRB	FFh
000EDh			FFh
000EEh	Timer RC General Register C	TRCGRC	FFh
000EFh			FFh
000F0h	Timer RC General Register D	TRCGRD	FFh
000F1h			FFh
000F2h	Timer RC Mode Register	TRCMR	01001000b
000F3h	Timer RC Control Register 1	TRCCR1	00h
000F4h	Timer RC Interrupt Enable Register	TRCIER	01110000b
000F5h	Timer RC Status Register	TRCSR	01110000b
000F6h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
000F7h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
000F8h	Timer RC Control Register 2	TRCCR2	00011000b
000F9h	Timer RC Digital Filter Function Select Register	TRCDF	00h
000FAh	Timer RC Output Enable Register	TRCOER	01111111b
000FBh	Timer RC A/D Conversion Trigger Control Register	TRCADCR	11110000b
000FCh	Timer RC Waveform Output Manipulation Register	TRCOPR	00h
000FDh			
000FEh			
000FFh			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The TCNT16 bit in the TRBMR register is 0.
3. The TCNT16 bit in the TRBMR register is 1.

Table 3.5 SFR Information (5) (1)

Address	Register Name	Symbol	After Reset
00100h			
00101h			
00102h			
00103h			
00104h			
00105h			
00106h			
00107h			
00108h			
00109h			
0010Ah			
0010Bh			
0010Ch			
0010Dh			
0010Eh			
0010Fh			
00110h			
00111h			
00112h			
00113h			
00114h			
00115h			
00116h			
00117h			
00118h			
00119h			
0011Ah			
0011Bh			
0011Ch			
0011Dh			
0011Eh			
0011Fh			
00120h			
00121h			
00122h			
00123h			
00124h			
00125h			
00126h			
00127h			
00128h			
00129h			
0012Ah			
0012Bh			
0012Ch			
0012Dh			
0012Eh			
0012Fh			
00130h			
00131h			
00132h			
00133h			
00134h			
00135h			
00136h			
00137h			
00138h			
00139h			
0013Ah			
0013Bh			
0013Ch			
0013Dh			
0013Eh			
0013Fh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Register Name	Symbol	After Reset
00140h			
00141h			
00142h			
00143h			
00144h			
00145h			
00146h			
00147h			
00148h			
00149h			
0014Ah			
0014Bh			
0014Ch			
0014Dh			
0014Eh			
0014Fh			
00150h			
00151h			
00152h			
00153h			
00154h			
00155h			
00156h			
00157h			
00158h			
00159h			
0015Ah			
0015Bh			
0015Ch			
0015Dh			
0015Eh			
0015Fh			
00160h			
00161h			
00162h			
00163h			
00164h			
00165h			
00166h			
00167h			
00168h			
00169h			
0016Ah			
0016Bh			
0016Ch			
0016Dh			
0016Eh			
0016Fh			
00170h			
00171h			
00172h			
00173h			
00174h			
00175h			
00176h			
00177h			
00178h			
00179h			
0017Ah			
0017Bh			
0017Ch			
0017Dh			
0017Eh			
0017Fh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

Address	Register Name	Symbol	After Reset
00180h	Comparator B Control Register	WCMPR	00h
00181h	Comparator B1 Interrupt Control Register	WCB1INTR	00h
00182h	Comparator B3 Interrupt Control Register	WCB3INTR	00h
00183h			
00184h			
00185h			
00186h			
00187h			
00188h			
00189h			
0018Ah			
0018Bh			
0018Ch			
0018Dh			
0018Eh			
0018Fh			
00190h			
00191h			
00192h			
00193h			
00194h			
00195h			
00196h			
00197h			
00198h			
00199h			
0019Ah			
0019Bh			
0019Ch			
0019Dh			
0019Eh			
0019Fh			
001A0h			
001A1h			
001A2h			
001A3h			
001A4h			
001A5h			
001A6h			
001A7h			
001A8h			
001A9h	Flash Memory Status Register	FST	10000000b
001AAh	Flash Memory Control Register 0	FMR0	00h
001ABh	Flash Memory Control Register 1	FMR1	00h
001ACh	Flash Memory Control Register 2	FMR2	00h
001ADh	Flash Memory Refresh Control Register	FREFR	00h
001AEh			
001AFh			
001B0h			
001B1h			
001B2h			
001B3h			
001B4h			
001B5h			
001B6h			
001B7h			
001B8h			
001B9h			
001BAh			
001BBh			
001BCh			
001BDh			
001BEh			
001BFh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Register Name	Symbol	After Reset
001C0h	Address Match Interrupt Register 0	AIADR0L	00h
001C1h		AIADR0M	00h
001C2h		AIADR0H	00h
001C3h	Address Match Interrupt Enable Register 0	AIEN0	00h
001C4h	Address Match Interrupt Register 1	AIADR1L	00h
001C5h		AIADR1M	00h
001C6h		AIADR1H	00h
001C7h	Address Match Interrupt Enable Register 1	AIEN1	00h
001C8h			
001C9h			
001CAh			
001CBh			
001CCh			
001CDh			
001CEh			
001CFh			
001D0h			
001D1h			
001D2h			
001D3h			
001D4h			
001D5h			
001D6h			
001D7h			
001D8h			
001D9h			
001DAh			
001DBh			
001DCh			
001DDh			
001DEh			
001DFh			
001E0h			
001E1h			
001E2h			
001E3h			
001E4h			
001E5h			
001E6h			
001E7h			
001E8h			
001E9h			
001EAh			
001EBh			
001ECh			
001EDh			
001EEh			
001EFh			
001F0h			
001F1h			
001F2h			
001F3h			
001F4h			
001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.9 ID Code Area and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
0FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
0FFDFh	ID1		(Note 2)
:			
0FFE3h	ID2		(Note 2)
:			
0FFEBh	ID3		(Note 2)
:			
0FFEFh	ID4		(Note 2)
:			
0FFF3h	ID5		(Note 2)
:			
0FFF7h	ID6		(Note 2)
:			
0FFFBh	ID7		(Note 2)
:			
0FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the option function select area. Erasure of the block including the option function select area causes the option function select area to be set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the ID code area. Erasure of the block including the ID code area causes the ID code area to be set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

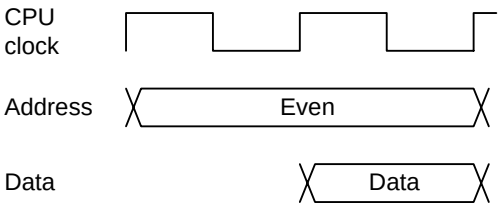
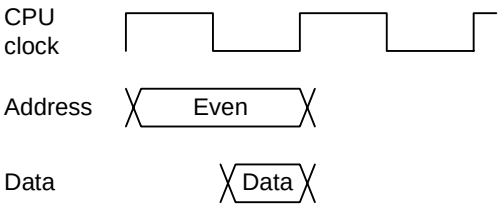
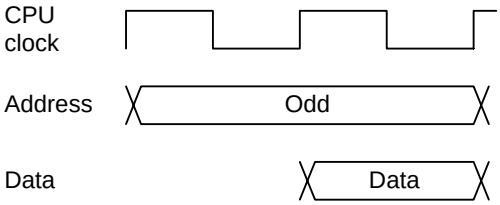
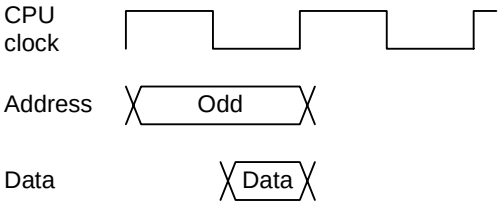
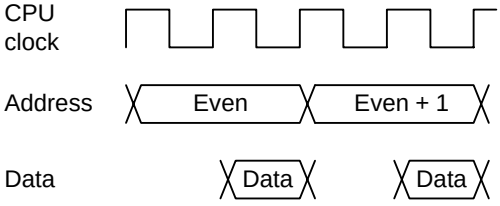
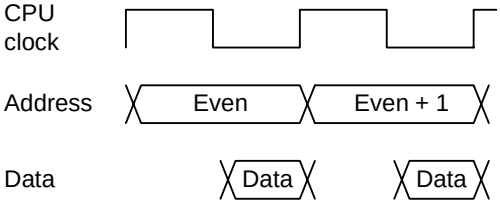
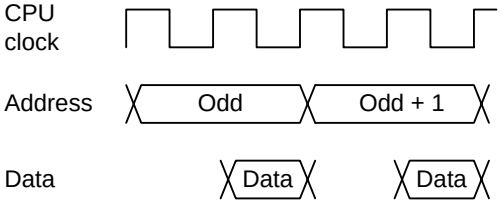
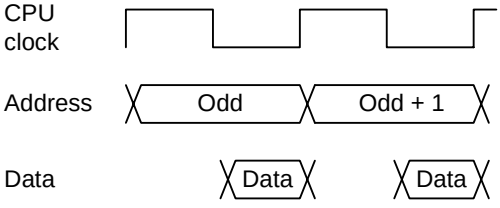
4. Bus Control

The number of bus cycles differ depending on the area accessed: ROM, RAM, or SFR.
Table 4.1 lists the Number of Bus Cycles for Accessing Different Areas. Table 4.2 lists the Access Units and Bus Operations.
The units for SFR access are specified as “Access Size” in the register configuration table in each chapter.
The peripheral function modules are connected to the CPU via an 8-bit bus. Thus, when these areas are accessed as word (16-bit) units, they are accessed twice in 8-bit units.

Table 4.1 Number of Bus Cycles for Accessing Different Areas

Access Area	Bus Cycle
ROM (data flash)	2 cycles of CPU clock
SFR (other than FMR2 register)	
SFR (FMR2 register)	6 cycles of CPU clock
ROM (program ROM)	1 cycle of CPU clock
RAM	

Table 4.2 Access Units and Bus Operations

Area	ROM (data flash), SFR	ROM (program ROM), RAM
Even address byte access		
Odd address byte access		
Even address word access		
Odd address word access		

5. System Control

5.1 Overview

This chapter describes system control functions, such as ID code checking, register access protection, and option functions.

5.2 Registers

Table 5.1 lists the Register Configuration for System Control.

Table 5.1 Register Configuration for System Control

Register Name	Symbol	After Reset	Address	Access Size
Processor Mode Register 0	PM0	00h	00010h	8
Module Standby Control Register	MSTCR	(Note 1)	00012h	8
Protect Register	PRCR	00h	00013h	8
Hardware Reset Protect Register	HRPR	00h	00016h	8
Reset Source Determination Register	RSTFR	(Note 2)	0005Fh	8
Option Function Select Register 2	OFS2	(Note 3)	0FFDBh	8
Option Function Select Register	OFS	(Note 4)	0FFFFh	8

Notes:
1. See the description of the individual registers.
2. The value of the RSTFR register after a reset differs depending on the reset source. For details, see **5.2.5 Reset Source Determination Register (RSTFR)**.
3. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.
4. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

5.2.1 Processor Mode Register 0 (PM0)

Address 00010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	SRST	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	SRST	Software reset bit	0: State is retained 1: Reset is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

SRST Bit (Software reset bit)

When the SRST bit is set to 1, the entire MCU is reset. The read value is 0. For details, see **6. Resets**.

5.2.2 Module Standby Control Register (MSTCR)

Address 00012h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTUART	MSTTRC	MSTAD	—	—	MSTTRB	MSTTRJ
After Reset	0	0	0	0	0	0	0	0

The above applies when the MSTINI bit in the OFS2 register is 0.

After Reset	0	1	1	1	0	1	1	1

The above applies when the MSTINI bit in the OFS2 register is 1.

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRJ	Timer RJ2 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB	Timer RB2 standby bit	0: Active 1: Standby (2)	R/W
b2	—	Reserved	Set to 0. The read value is undefined.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	MSTAD	A/D converter standby bit	0: Active 1: Standby (3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTUART	UART0 standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Notes:
1. When the MSTTRJ bit is set to 1 (standby), access to the registers associated with timer RJ2 (addresses 000D8h to 000DEh) is disabled.
2. When the MSTTRB bit is set to 1 (standby), access to the registers associated with timer RB2 (addresses 000E0h to 000E7h) is disabled.
3. When the MSTAD bit is set to 1 (standby), access to the registers associated with the A/D converter (addresses 00098h to 0009Fh) is disabled.
4. When the MSTTRC bit is set to 1 (standby), access to the registers associated with timer RC (addresses 000E8h to 000FCh) is disabled.
5. When the MSTUART bit is set to 1 (standby), access to the registers associated with UART0 (addresses 00080h to 00088h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand.

5.2.3 Protect Register (PRCR)

Address 00013h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	PRC4	PRC3	—	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2 0: Disabled 1: Enabled (1)	R/W
b1	PRC1	Protect bit 1	Writing to registers PM0 and RISR 0: Disabled 1: Enabled (1)	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	PRC3	Protect bit 3	Writing to registers VCA2, VD1LS, VW0C, and VW1C 0: Disabled 1: Enabled (1)	R/W
b4	PRC4	Protect bit 4	Writing to the PINSR register 0: Disabled 1: Enabled (1)	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

Note:
1. Once this bit is set to 1, writing remains enabled until it is set to 0 by a program.

5.2.4 Hardware Reset Protect Register (HRPR)

Address 00016h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PAMCRE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PAMCRE	PAMCR register write enable bit (1)	0: Write disabled 1: Write enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.

PAMCRE Bit (PAMCR register write enable bit)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When 0 and then 1 is written to this bit.

5.2.5 Reset Source Determination Register (RSTFR)

Address 0005Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDR	SWR	HWR	CWR
After Reset	0	0	0	0	X (1)	X (1)	X (1)	X (1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. The value after a reset differs depending on the reset source.

CWR Bit (Cold start-up/warm start-up determine flag)

This flag indicates whether a cold start-up or warm start-up has occurred. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The CWR bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.

[Condition for setting to 0]
• When a reset occurs after power-on or voltage detection 0.
[Condition for setting to 1]
• When 1 is written to this bit by a program.

HWR Bit (Hardware reset detect flag)

This flag indicates that a hardware reset has occurred.

[Condition for setting to 0]
• When a software reset, watchdog timer reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a hardware reset occurs.

SWR Bit (Software reset detect flag)

This flag indicates that a reset has been generated by software.

[Condition for setting to 0]
• When a watchdog timer reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a software reset occurs.

WDR Bit (Watchdog timer reset detect flag)

This flag indicates that a reset has been generated by the watchdog timer.

[Condition for setting to 0]
• When a software reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a watchdog timer reset occurs.

5.2.6 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTINI	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period setting bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period setting bits	b3 b2 0 0: 25 % 0 1: 50 % 1 0: 75 % 1 1: 100 %	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	MSTINI	MSTCR register initial value select bit	0: MSTCR register is set to 00h after reset 1: MSTCR register is set to 77h after reset	R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For an example of the OFS2 register settings, see **5.6.1 Option Function Select Area Setting Example**.

Bits WDTUFS0 to WDTUFS1 (Watchdog timer underflow period setting bits)

These bits are used to select the underflow period for the watchdog timer.

Bits WDTRCS0 to WDTRCS1 (Watchdog timer refresh acceptance period setting bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100 %.
For details, see **8.3.1.1 Refresh Acceptance Period**.

5.2.7 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer is automatically started after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) 1 0: 2.35 V (typ.) selected (Vdet0_1) 1 1: 1.90 V (typ.) selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Note:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

   For an example of the OFS register settings, see **5.6.1 Option Function Select Area Setting Example**.

WDTON Bit (Watchdog timer start select bit)

This bit is used to select whether the watchdog timer is automatically started after a reset is cleared.

Bits VDSEL0 to VDSEL1 (Voltage detection 0 level select bits)

These bits are used to select the detection level (Vdet0) for voltage monitor 0 reset. The same level of the voltage detection 0 level selected by bits VDSEL0 to VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.

LVDAS Bit (Voltage detection 0 circuit start bit)

This bit is used to select whether voltage monitor 0 reset is enabled. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset.

CSPROINI Bit (Count source protection mode after reset select bit)

This bit is used to select whether to protect the count source for the watchdog timer from being changed.

5.3 ID Code Check Function

The ID code check function prevents the flash memory from being read, rewritten, or erased when standard serial I/O mode is used. This function is realized by examination of the ID codes written in the ID code area.
For details, see **19.3 ID Code Check Function**.

5.4 Register Access Protect Function

The protection function protects important registers from being easily rewritten if a program runs out of control.
Table 5.2 lists the PRCR Register Bits and Registers Protected.
For details on each bit, see **5.2.3 Protect Register (PRCR)**.

Table 5.2 PRCR Register Bits and Registers Protected

Bit	Registers Protected
PRC0	Registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2
PRC1	Registers PM0 and RISR
PRC3	Registers VCA2, VD1LS, VW0C, and VW1C
PRC4	PINSR register

Table 5.3 lists the HRPR Register Bit and Register Protected.
For details on each bit, see **5.2.4 Hardware Reset Protect Register (HRPR)**.

Table 5.3 HRPR Register Bit and Register Protected

Bit	Registers Protected
PAMCRE	PAMCR register

5.5 Option Functions

The option functions allow the user to select the MCU state after a reset is cleared. Table 5.4 lists the Option Functions.

The option functions can be selected by registers OFS2 and OFS. These registers are allocated at the addresses 0FFFFh (highest of the reset vector) and 0FFDBh, as shown in Figure 5.1.

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

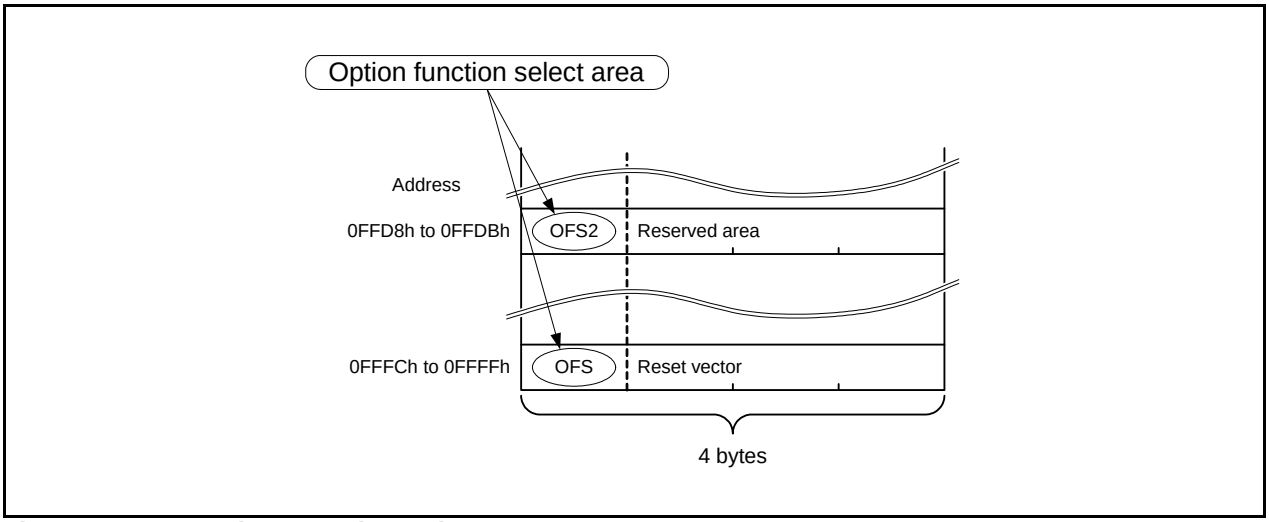


Figure 5.1 Option Function Select Area

Table 5.4 Option Functions

Option Function Name		Register Name	Bit Name	Reference
Watchdog timer	Start select function	OFS register	WDTON bit	8. Watchdog Timer
	Count source protection select function		CSPROINI bit	
	Underflow period select function	OFS2 register	Bits WDTUFS0 to WDTUFS1	
	Refresh acceptance period select function		Bits WDTRCS0 to WDTRCS1	
Voltage detection circuit	Voltage monitor 0 reset level function	OFS register	Bits VDSEL0 to VDSEL1	6. Resets 7. Voltage Detection Circuit
	Voltage monitor 0 reset start select function		LVDAS bit	
Flash memory	ROM code protection function		Bits ROMCR to ROMCP1	19. Flash Memory

5.6 Notes on System Control

5.6.1 Option Function Select Area Setting Example

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

Programming formats vary depending on the compiler. Check the compiler manual.

• To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)          ; RESET
```

Programming formats vary depending on the compiler. Check the compiler manual.

6. Resets

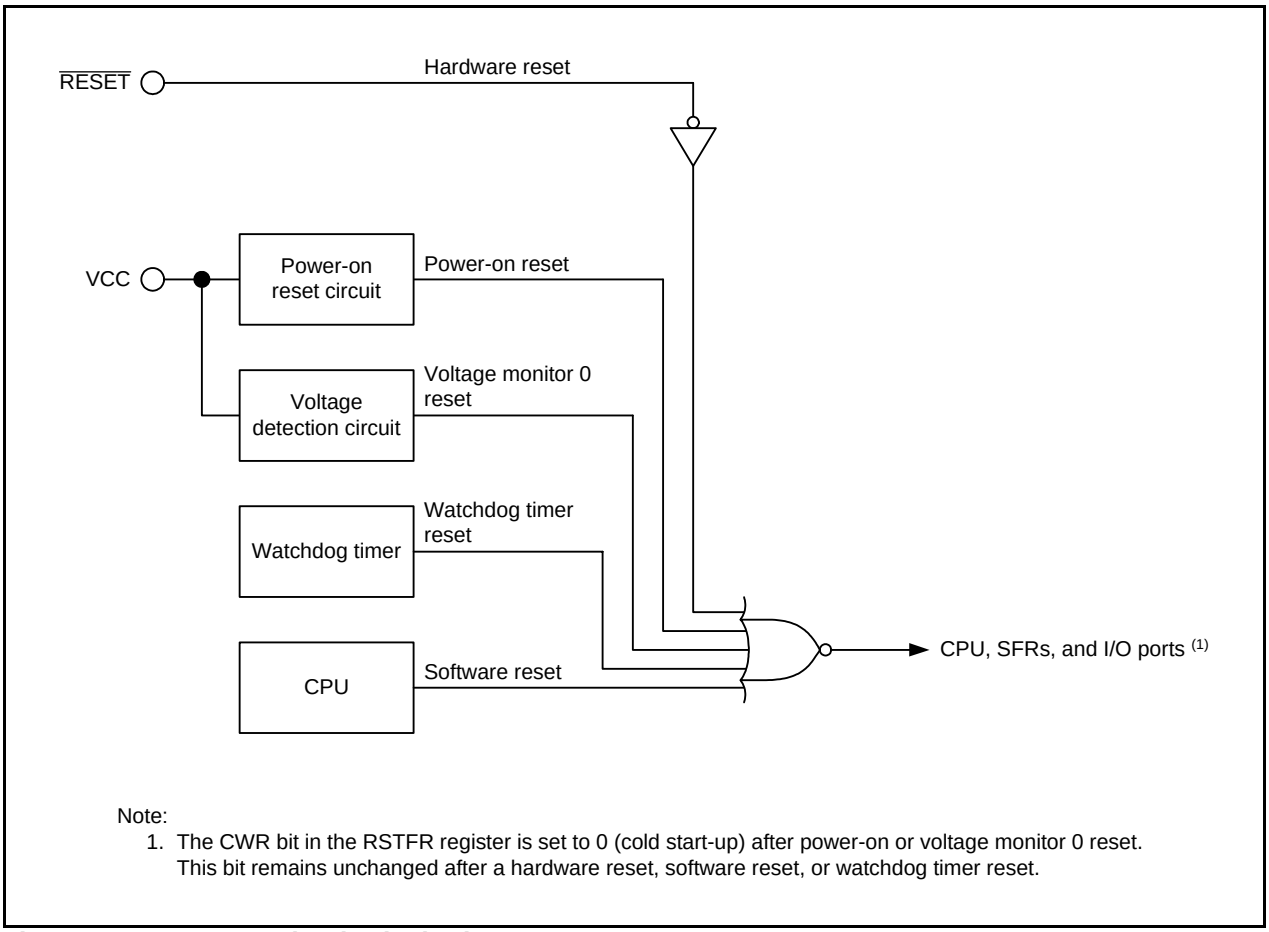
The following resets are provided: hardware reset, power-on reset, voltage monitor 0 reset triggered by the voltage detection circuit, watchdog timer reset, and software reset.

6.1 Overview

Table 6.1 lists the Reset Names and Sources. Figure 6.1 shows the Reset Circuit Block Diagram.

Table 6.1 Reset Names and Sources

Reset Name	Source
Hardware reset	When a low level is input to the $\overline{\text{RESET}}$ pin.
Power-on reset	When VCC is turned on.
Voltage monitor 0 reset	When VCC decreases below Vdet0, which is detected by voltage detection circuit 0.
Watchdog timer reset	When the watchdog timer underflows.
Software reset	When 1 is written to the SRST bit in the PM0 register by a program.



Note:
1. The CWR bit in the RSTFR register is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.

Figure 6.1 Reset Circuit Block Diagram

6.2 Registers

Table 6.2 lists the Register Configuration for Reset.

Table 6.2 Register Configuration for Reset

Register Name	Symbol	After Reset	Address	Access Size
Processor Mode Register 0	PM0	00h	00010h	8
Reset Source Determination Register	RSTFR	(Note 1)	0005Fh	8
Option Function Select Register 2	OFS2	(Note 2)	0FFDBh	8
Option Function Select Register	OFS	(Note 3)	0FFFFh	8

Notes:
1. The value of the RSTFR register after a reset differs depending on the reset source. For details, see **6.2.2 Reset Source Determination Register (RSTFR)**.
2. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.
3. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

6.2.1 Processor Mode Register 0 (PM0)

Address 00010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	SRST	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	SRST	Software reset bit	0: State is retained 1: Reset is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

SRST Bit (Software reset bit)

When the SRST bit is set to 1, the entire MCU is reset. The read value is 0. For details, see **6. Resets**.

6.2.2 Reset Source Determination Register (RSTFR)

Address 0005Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDR	SWR	HWR	CWR
After Reset	0	0	0	0	X (1)	X (1)	X (1)	X (1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. The value after a reset differs depending on the reset source.

CWR Bit (Cold start-up/warm start-up determine flag)

This flag indicates whether a cold start-up or warm start-up has occurred. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The CWR bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.

[Condition for setting to 0]
• When a reset occurs after power-on or voltage detection 0.
[Condition for setting to 1]
• When 1 is written to this bit by a program.

HWR Bit (Hardware reset detect flag)

This flag indicates that a hardware reset has occurred.

[Condition for setting to 0]
• When a software reset, watchdog timer reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a hardware reset occurs.

SWR Bit (Software reset detect flag)

This flag indicates that a reset has been generated by software.

[Condition for setting to 0]
• When a watchdog timer reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a software reset occurs.

WDR Bit (Watchdog timer reset detect flag)

This flag indicates that a reset has been generated by the watchdog timer.

[Condition for setting to 0]
• When a software reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a watchdog timer reset occurs.

6.2.3 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTINI	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period setting bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period setting bits	b3 b2 0 0: 25 % 0 1: 50 % 1 0: 75 % 1 1: 100 %	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	MSTINI	MSTCR register initial value select bit	0: MSTCR register is set to 00h after reset 1: MSTCR register is set to 77h after reset	R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For an example of the OFS2 register settings, see **5.6.1 Option Function Select Area Setting Example**.

Bits WDTUFS0 to WDTUFS1 (Watchdog timer underflow period setting bits)

These bits are used to select the underflow period for the watchdog timer.

Bits WDTRCS0 to WDTRCS1 (Watchdog timer refresh acceptance period setting bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100 %.
For details, see **8.3.1.1 Refresh Acceptance Period**.

6.2.4 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer is automatically started after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) 1 0: 2.35 V (typ.) selected (Vdet0_1) 1 1: 1.90 V (typ.) selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Note:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

   For an example of the OFS register settings, see **5.6.1 Option Function Select Area Setting Example**.

WDTON Bit (Watchdog timer start select bit)

This bit is used to select whether the watchdog timer is automatically started after a reset is cleared.

Bits VDSEL0 to VDSEL1 (Voltage detection 0 level select bits)

These bits are used to select the detection level (Vdet0) for voltage monitor 0 reset. The same level of the voltage detection 0 level selected by bits VDSEL0 to VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.

LVDAS Bit (Voltage detection 0 circuit start bit)

This bit is used to select whether voltage monitor 0 reset is enabled. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset.

CSPROINI Bit (Count source protection mode after reset select bit)

This bit is used to select whether to protect the count source for the watchdog timer from being changed.

6.3 Operation

6.3.1 Reset Sequence

Figure 6.2 shows the Reset Sequence using a hardware reset as an example. When the internal reset signal is cleared, the CPU starts operation from the reset vector (addresses 0FFFCh to 0FFFEh) after a predetermined time has elapsed.

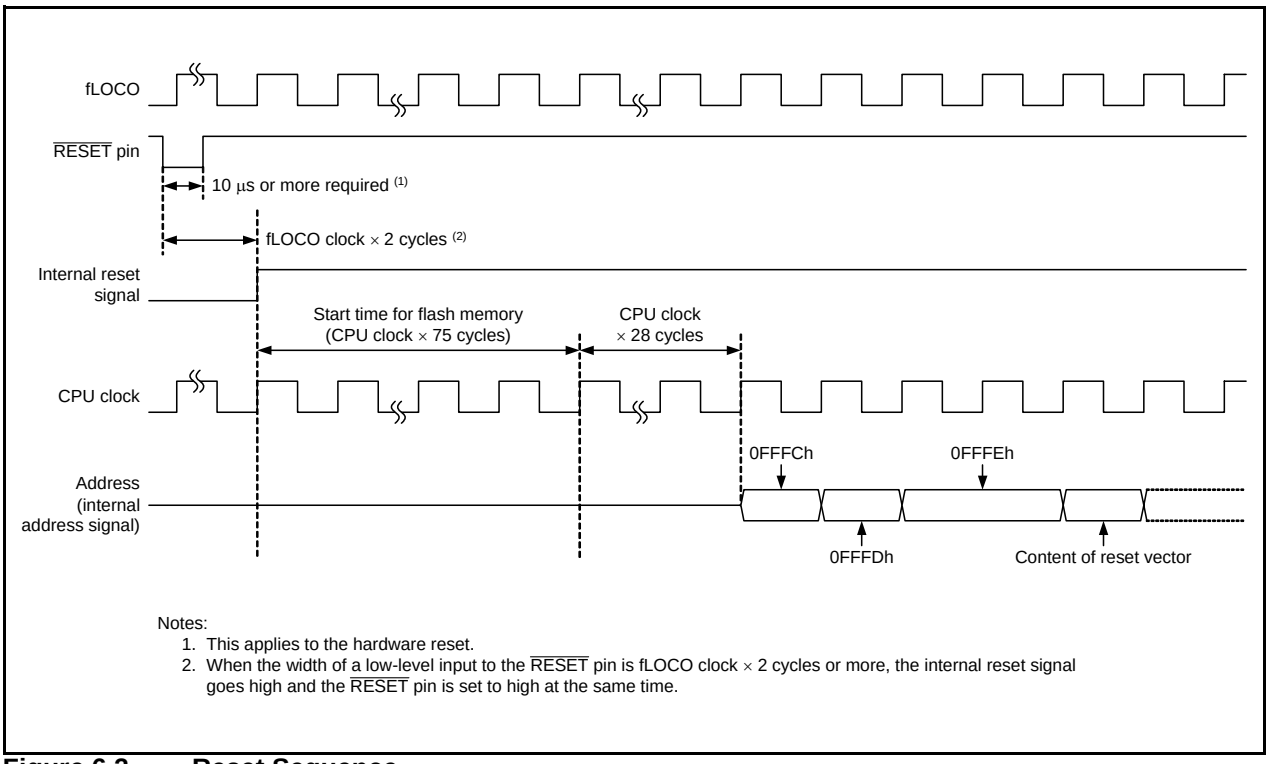


Figure 6.2 Reset Sequence

6.3.2 Hardware Reset

The hardware reset is the reset that is caused by the $\overline{\text{RESET}}$ pin. When a low level is input to the $\overline{\text{RESET}}$ pin under the condition that the power supply voltage meets the recommended operating conditions, the CPU, SFRs, and I/O ports are initialized. See **3.2 Special Function Registers (SFRs)** for the states of the SFRs after a reset, and **Tables 6.3** and **6.4 Pin States** for the states of I/O ports.

The internal RAM is not initialized. If the $\overline{\text{RESET}}$ pin is set to low while writing to the internal RAM, the RAM values will be undefined.

When the $\overline{\text{RESET}}$ pin is changed from low to high, a program is executed starting at the address indicated by the reset vector. The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.

Figure 6.3 shows the Hardware Reset Circuit Example (Using External Power Supply Voltage Detection Circuit) and Operation.

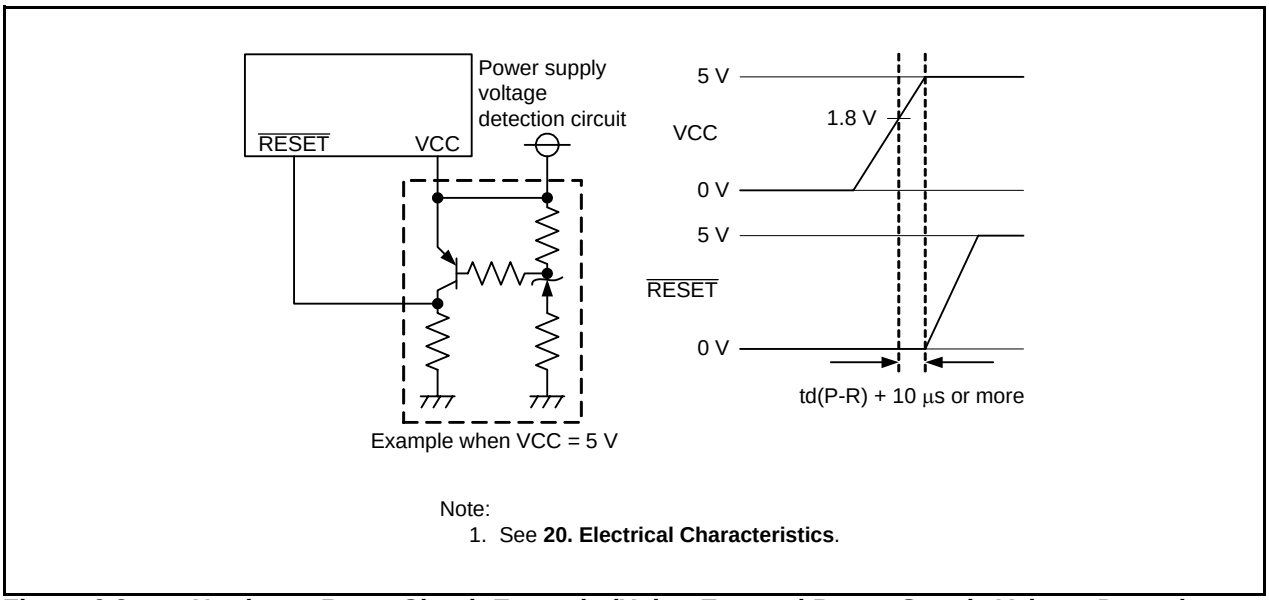
The $\overline{\text{RESET}}$ pin is multiplexed with port PA_0, so it can be used as general-purpose I/O ports when not used for a hardware reset. For details, see **12.11.1 Notes on PA_0 Pin**.

6.3.2.1 When Power Supply is Stable

(1) Input a low level to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Input a high level to the $\overline{\text{RESET}}$ pin.

6.3.2.2 When Power Supply is Turned on

(1) Input a low level to the $\overline{\text{RESET}}$ pin.
(2) Let the power supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) until the internal power supply is stabilized (see **20. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Input a high level to the $\overline{\text{RESET}}$ pin.



Note:
1. See **20. Electrical Characteristics**.

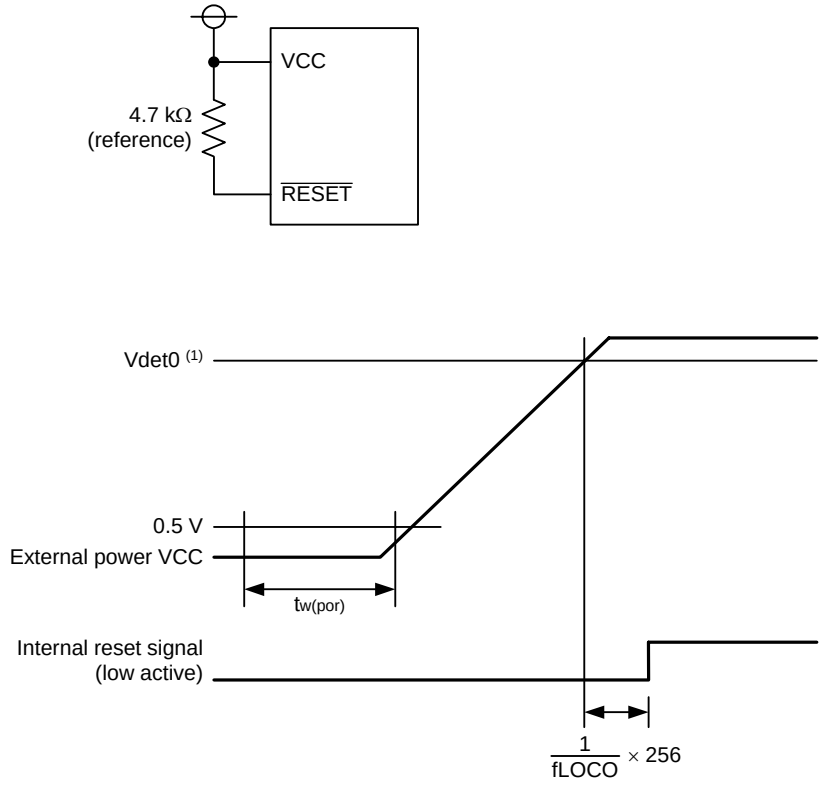
Figure 6.3 Hardware Reset Circuit Example (Using External Power Supply Voltage Detection Circuit) and Operation

6.3.3 Power-On Reset

When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a resistor and the VCC pin voltage level rises, the power-on reset is activated and the CPU, SFRs, and I/O ports are initialized. The internal RAM values will be undefined. In addition, when a capacitor is connected to the $\overline{\text{RESET}}$ pin, assure that the voltage applied to the $\overline{\text{RESET}}$ pin is always 0.8 VCC or more. When using the $\overline{\text{RESET}}$ pin as an I/O port, see **12.11.1 Notes on PA_0 Pin**.

When the input voltage to the VCC pin reaches Vdet0 or above, counting of the low-speed on-chip oscillator clock starts. When the low-speed on-chip oscillator clock count reaches 256, the internal reset signal goes high and the MCU proceeds to the reset sequence (see Figure 6.2). The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset. For the states of the SFRs after a power-on reset, see **3.2 Special Function Registers (SFRs)**. To use the power-on reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled) and enable the voltage monitor 0 reset.

Figure 6.4 shows the Power-On Reset Circuit Example and Operation.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. For details, see **7. Voltage Detection Circuit**.
2. For details on the electrical characteristics, see **20. Electrical Characteristics**.
3. To use the power-on reset, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 6.4 Power-On Reset Circuit Example and Operation

6.3.4 Voltage Monitor 0 Reset

The voltage monitor 0 reset is due to the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the voltage applied to the VCC pin. Vdet0 is the detection level. The Vdet0 level is set with bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin falls to the Vdet0 level or lower, the CPU, SFRs and I/O ports are initialized. The internal RAM is not initialized. If the supply voltage falls to Vdet0 or lower while writing to the internal RAM, the RAM values will be undefined.

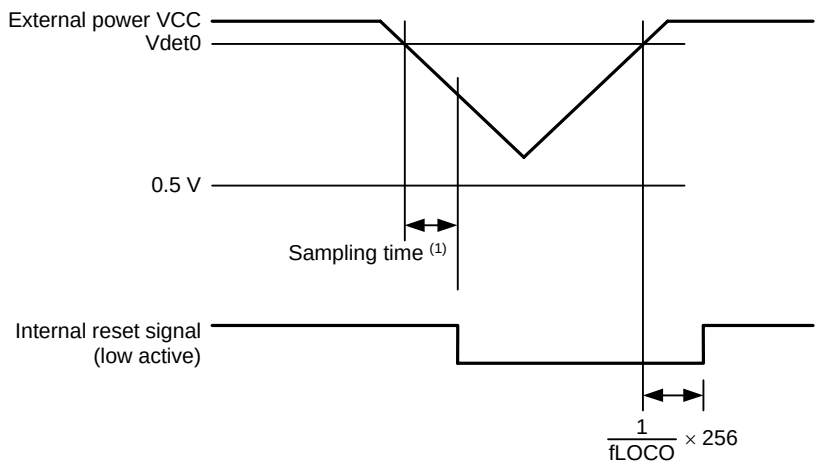
When the voltage applied to the VCC pin next rises to the Vdet0 level or higher, counting of the low-speed on-chip oscillator clock starts. When the low-speed on-chip oscillator clock count reaches 256, the internal reset signal goes high and the MCU proceeds to the reset sequence (see Figure 6.2). The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.

The LVDAS bit in the OFS register can be used to enable or disable the voltage monitor 0 reset after a reset. The setting of the LVDAS bit is valid at all resets.

Bits VDSEL0 to VDSEL1, and LVDAS cannot be changed by a program. To change these bits, write values to b4 to b6 at address 0FFFFh using a flash programmer. For details on the OFS register, see **6.2.4 Option Function Select Register (OFS)**.

For details on the voltage monitor 0 reset, see **7. Voltage Detection Circuit**.

Figure 6.5 shows an Example of Voltage Monitor 0 Reset Operation.



Note:
1. The voltage monitor 0 digital filter samples VCC to monitor the voltage. If VCC falls below the operating voltage range (1.8 V or more), the voltage cannot be correctly measured. This factor should be considered when selecting the sampling clock for the digital filter. For details, see **7. Voltage Detection Circuit**.

Figure 6.5 Example of Voltage Monitor 0 Reset Operation

6.3.5 Watchdog Timer Reset

When the RIS bit in the RISR register is 1 (watchdog timer reset enabled), if the watchdog timer underflows or if the WDTR register is written at a time other than the refresh acceptance period, a watchdog timer reset is generated. This reset initializes the CPU, SFRs, and I/O ports. The internal reset signal goes high and the watchdog timer reset is cleared at the same time. The MCU then proceeds to the reset sequence (see Figure 6.2).
The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.
The internal RAM is not initialized. When the watchdog timer underflows, the RAM values will be undefined.
The underflow period and refresh acceptance period for the watchdog timer are set by bits WDTUFS0 to WDTUFS1 and WDTRCS0 to WDTRCS1 in the OFS2 register, respectively.
For details on the watchdog timer, see **8. Watchdog Timer**.

6.3.6 Software Reset

When the SRST bit in the PM0 register is 1 (reset is generated), the CPU, SFRs, and I/O ports are initialized. Next, the program located at the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after the reset is cleared.
For the states of the SFRs after a software reset, see **3.2 Special Function Registers (SFRs)**.
The internal RAM is not initialized.

6.3.7 Cold Start-Up/Warm Start-Up Determination Function

The CWR bit in the RSTFR register is used to determine whether a cold start-up reset process was initiated at power-on, or whether a warm start-up reset process was initiated during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 by a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm stat-up determination function uses the voltage monitor 0 reset.
For the bit settings associated with the voltage monitor 0 reset, see **Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.
Figure 6.6 shows an Example of Cold Start-Up/Warm Start-Up Function Operation.

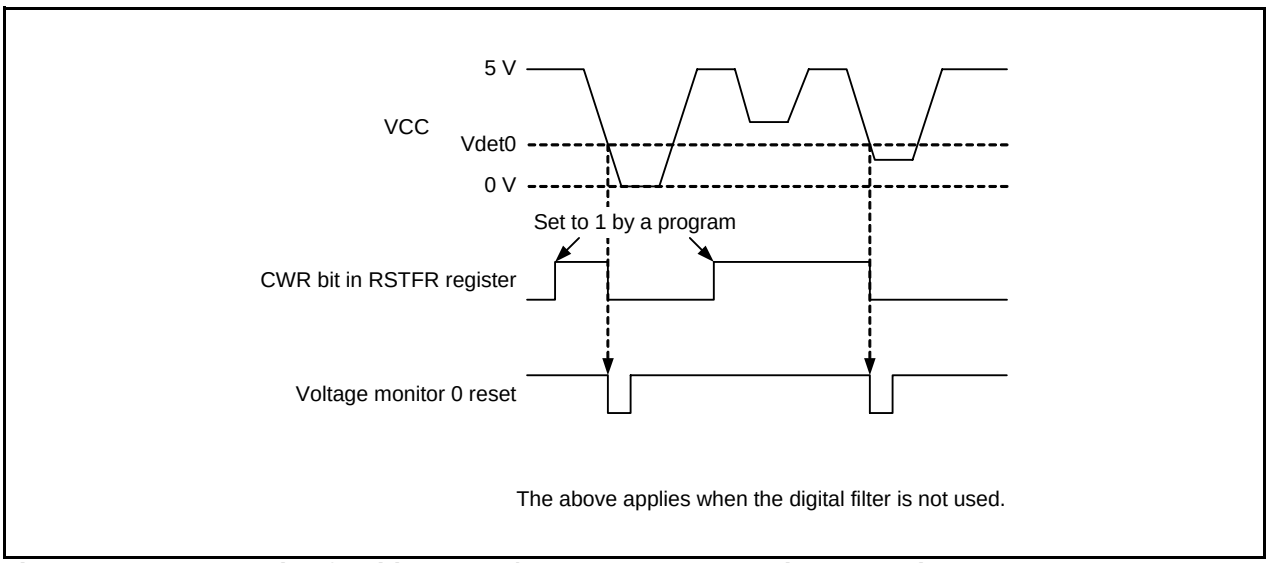


Figure 6.6 Example of Cold Start-Up/Warm Start-Up Function Operation

6.3.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit is set to 1 (detected). If a software reset occurs, the SWR bit is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6.4 States during Reset

6.4.1 Pin States While $\overline{\text{RESET}}$ Pin Level is Low

Tables 6.3 and 6.4 list the Pin States.

Table 6.3 Pin States (R8C/M11A Group)

Pin Name	Pin Function
P1_1 to P1_7	Input port
P3_7	Input port
P4_6, P4_7	Input port
PA_0	Input port

Table 6.4 Pin States (R8C/M12A Group)

Pin Name	Pin Function
P1_0 to P1_7	Input port
P3_3 to P3_5, P3_7	Input port
P4_2, P4_5 to P4_7	Input port
PA_0	Input port

6.4.2 CPU Register States After Reset

Figure 6.7 shows the CPU Register States After Reset.

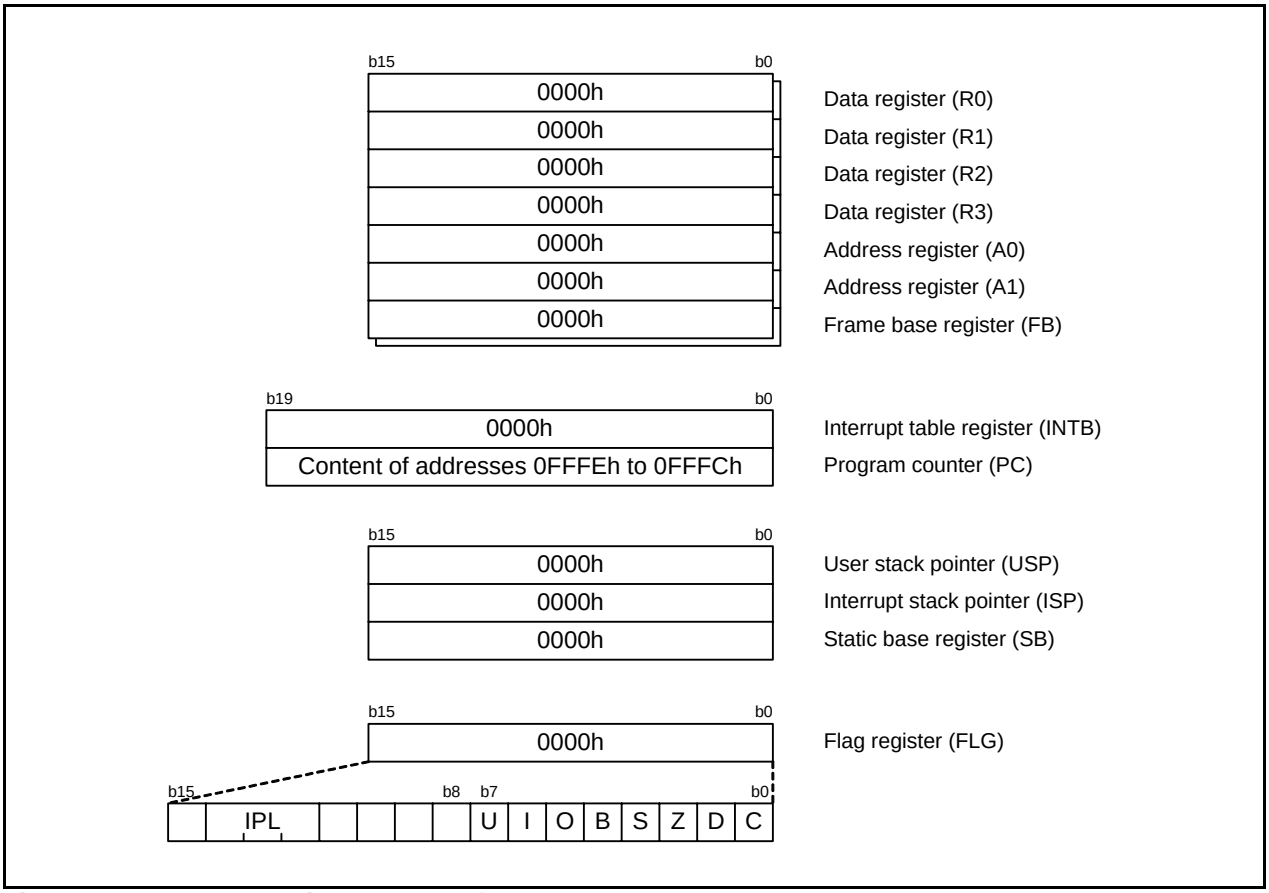


Figure 6.7 CPU Register States After Reset

7. Voltage Detection Circuit

The voltage detection circuit is used to monitor the voltage applied to the VCC pin. The VCC input voltage can be monitored by a program.

7.1 Overview

The detection voltage for voltage detection 0 can be selected from four levels with the OFS register. For details on the OFS register, see **5. System Control**.
The detection voltage for voltage detection 1 can be selected from eight levels with the VD1LS register.
The voltage monitor 0 reset, and voltage monitor 1 interrupt can be used.
Table 7.1 lists the Voltage Detection Circuit Specifications. Figure 7.1 shows the Voltage Detection Circuit Block Diagram. Figure 7.2 shows the Voltage Monitor 0 Reset Generation Circuit Block Diagram. Figure 7.3 shows the Voltage Monitor 1 Interrupt Generation Circuit Block Diagram.

Table 7.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1
VCC monitor	Voltage to be monitored	Vdet0	Vdet1
	Detection target	Detection by passing down through Vdet0	Detection by passing up or down through Vdet1
	Detection voltage	Selectable from 4 levels with the OFS register	Selectable from 8 levels with the VD1LS register
	Monitor	None	The VW1C3 bit in the VW1C register
			Higher or lower than Vdet1
Process at voltage detection	Reset	Voltage monitor 0 reset	None
		Reset at Vdet0 > VCC, CPU operation is restarted at VCC > Vdet0	
	Interrupts	None	Voltage monitor 1 interrupt
			Interrupt request at Vdet1 > VCC and/or VCC > Vdet1
Digital filter	Switching enable/disable	Available	Available
	Sampling time	(Division of fLOCO by n) × 2 n: 1, 2, 4, or 8	(Division of fLOCO by n) × 2 n: 1, 2, 4, or 8

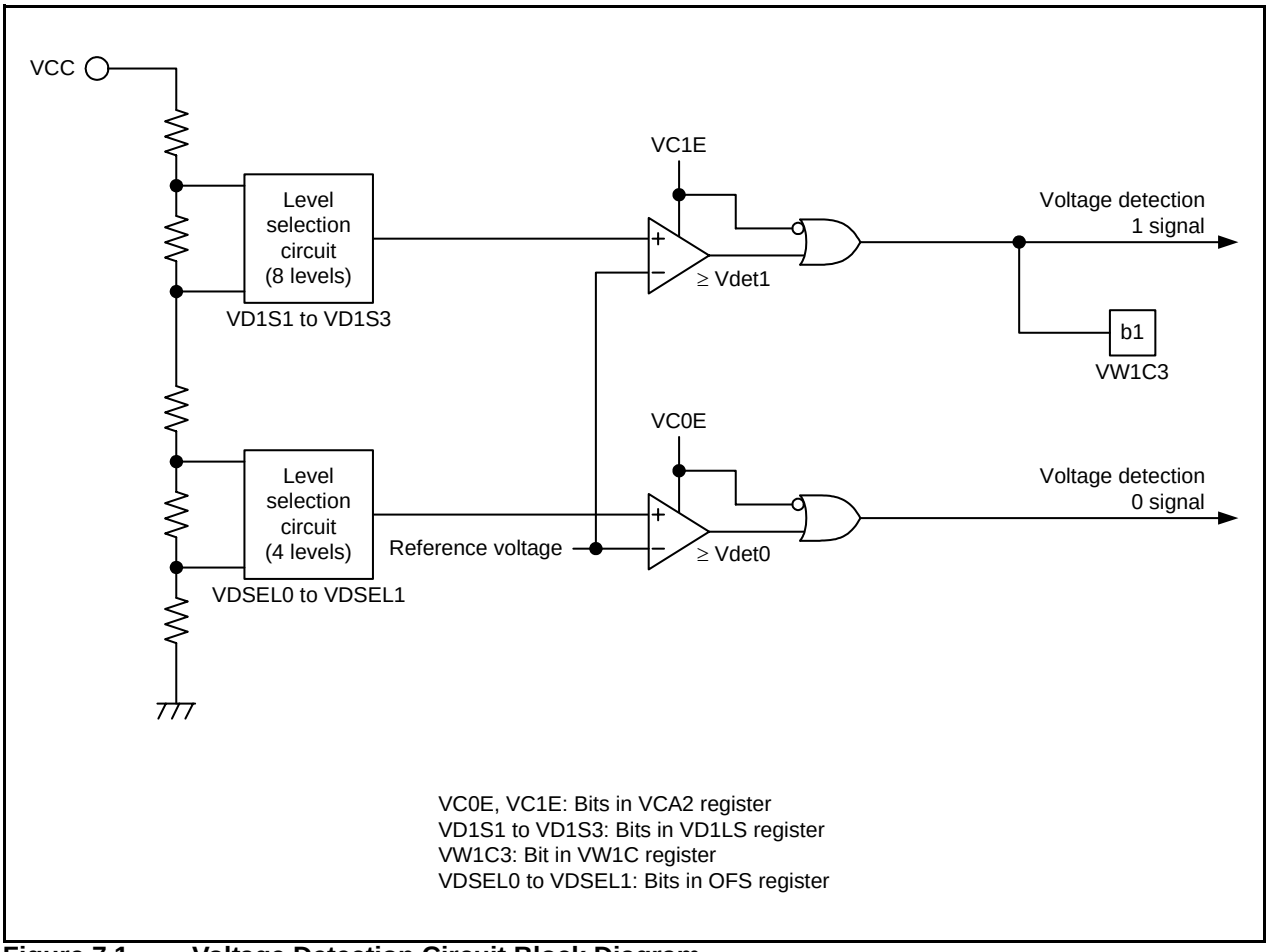
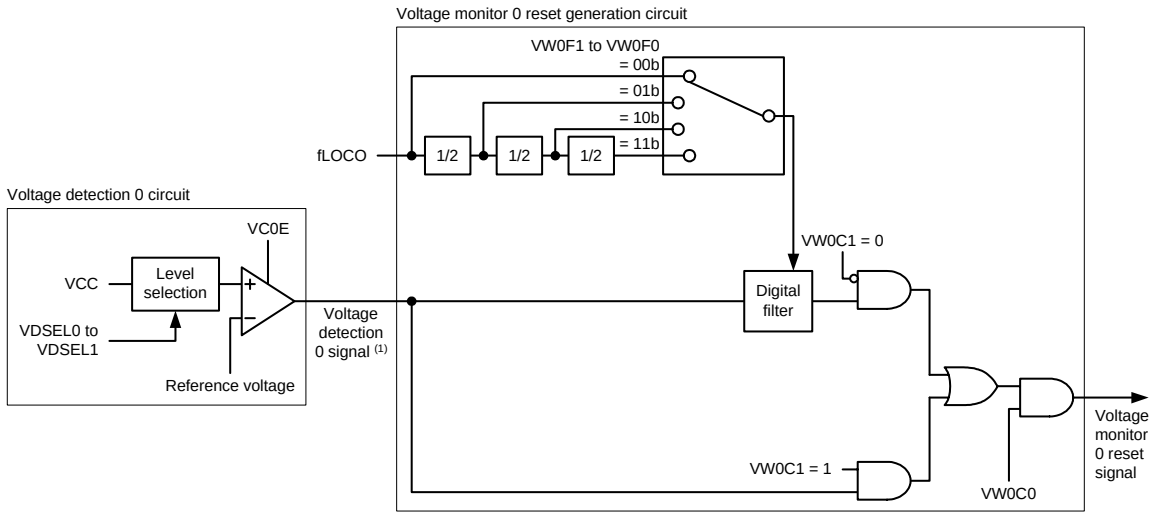


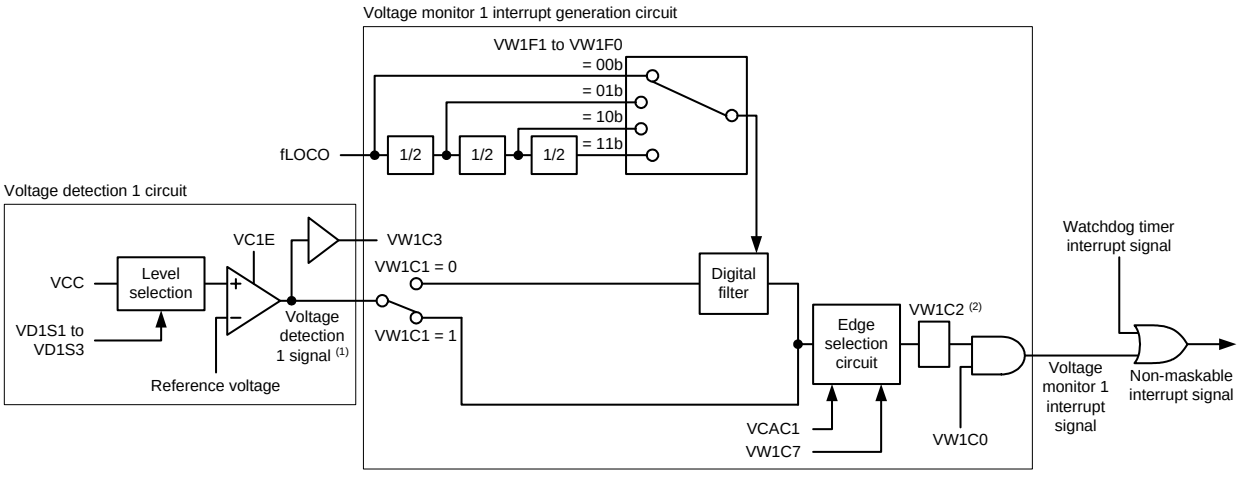
Figure 7.1 Voltage Detection Circuit Block Diagram



VC0E: Bit in VCA2 register
VW0C0, VW0C1, VW0F0 to VW0F1: Bits in VW0C register
VDSEL0 to VDSEL1: Bits in OFS register

Note:
1. When the VC0E bit is 0 (voltage detection 0 circuit disabled), the voltage detection 0 signal will be high.

Figure 7.2 Voltage Monitor 0 Reset Generation Circuit Block Diagram



VCAC1: Bit in VCAC register
VC1E: Bit in VCA2 register
VD1S1 to VD1S3: Bits in VD1LS register
VW1C0, VW1C1, VW1C2, VW1C3, VW1F0 to VW1F1, VW1C7: Bits in VW1C register

Notes:
1. When the VC1E bit is 0 (voltage detection 1 circuit disabled), the voltage detection 1 signal will be high.
2. The VW1C2 bit is set to 0 by writing 0 by a program. When the VC1E bit is 0 (voltage detection 1 circuit disabled), the VW1C2 bit will be 0 (not detected).

Figure 7.3 Voltage Monitor 1 Interrupt Generation Circuit Block Diagram

7.2 Registers

Table 7.2 lists the Voltage Detection Circuit Register Configuration.

Table 7.2 Voltage Detection Circuit Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Voltage Monitor Circuit Edge Select Register	VCAC	00h	00058h	8
Voltage Detect Register 2	VCA2	(Note 1)	0005Ah	8
Voltage Detection 1 Level Select Register	VD1LS	00000111b	0005Bh	8
Voltage Monitor 0 Circuit Control Register	VW0C	(Note 1)	0005Ch	8
Voltage Monitor 1 Circuit Control Register	VW1C	10001010b	0005Dh	8

Note:
1. See the description of the individual registers.

7.2.1 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 00058h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One-way edge 1: Two-way edge	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When the VCAC1 bit is 0 (one-way edge), the VW1C7 bit in the VW1C register can be used to select an interrupt generated when the voltage increases or decreases. Set the VCAC1 bit to 0 before setting the VW1C7 bit.

7.2.2 Voltage Detect Register 2 (VCA2)

Address 0005Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	VC1E	VC0E	—	—	—	—	LPE
After Reset	0	0	1	0	0	1	0	0
	The above applies when the LVDAS bit in the OFS register is 0.							
After Reset	0	0	0	0	0	1	0	0
	The above applies when the LVDAS bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	LPE	Internal low-power-consumption enable bit (1)	0: Low-power-consumption wait mode disabled 1: Low-power-consumption wait mode enabled	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—	Reserved	Set to 1.	R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	VC0E	Voltage detection 0 enable bit (2)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VC1E	Voltage detection 1 enable bit (3)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:

1. Use the LPE bit only when entering wait mode. To set the LPE bit, see **Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit**. When the LPE bit is 1 (low-power-consumption wait mode), do not set the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)).
2. When voltage monitor 0 reset is used, set the VC0E bit to 1 (voltage detection 0 circuit enabled). Set the VC0E bit from 0 to 1 and wait for td(E-A). After that, the voltage detection 0 circuit operates. For details on td(E-A), see **20. Electrical Characteristics**.
3. When a voltage detection 1 interrupt or the VW1C3 bit in the VW1C register is used, set the VC1E bit to 1 (voltage detection 1 circuit enabled). Set the VC1E bit from 0 to 1 and wait for td(E-A). After that, the voltage detection 1 circuit operates. For details on td(E-A), see **20. Electrical Characteristics**.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

7.2.3 Voltage Detection 1 Level Select Register (VD1LS)

Address 0005Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	—
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 1.	R/W
b1	VD1S1	Voltage detection 1 level select bits	b3 b2 b1 0 0 0: 2.35 V (Vdet1_1) 0 0 1: 2.65 V (Vdet1_3) 0 1 0: 2.95 V (Vdet1_5) 0 1 1: 3.25 V (Vdet1_7) 1 0 0: 3.55 V (Vdet1_9) 1 0 1: 3.85 V (Vdet1_B) 1 1 0: 4.15 V (Vdet1_D) 1 1 1: 4.45 V (Vdet1_F)	R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

7.2.4 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0005Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	VW0F1	VW0F0	—	—	VW0C1	VW0C0
After Reset	1	1	0	0	X	0	1	1
	The above applies when the LVDAS bit in the OFS register is 0.							
After Reset	1	1	0	0	X	0	1	0
	The above applies when the LVDAS bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Voltage monitor 0 reset disabled 1: Voltage monitor 0 reset enabled	R/W
b1	VW0C1	Voltage monitor 0 digital filter mode select bit (2, 3)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—	Reserved	The read value is undefined.	R
b4	VW0F0	Sampling clock select bits (3)	b5 b4 0 0: Division of fLOCO by 1 (no division) 0 1: Division of fLOCO by 2 1 0: Division of fLOCO by 4 1 1: Division of fLOCO by 8	R/W
b5	VW0F1			R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Notes:

1. The VW0C0 bit is enabled when the VC0E bit in the VCA2 register is 1 (voltage detection 0 circuit enabled). When the VC0E bit is 0 (voltage detection 0 circuit disabled), set the VW0C0 bit to 0 (voltage monitor 0 reset disabled). To set the VW0C0 bit to 1 (voltage monitor 0 reset enabled), see **Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.
2. When the digital filter is used (while the VW0C1 bit is 0), set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).
   When the voltage monitor 0 reset is used to return from stop mode, set the VW0C1 bit to 1 (digital filter disabled mode).
3. When the VW0C0 bit is 1 (voltage monitor 0 reset enabled), do not set bits VW0C1 and VW0F0 to VW0F1 at the same time (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW0C register.

7.2.5 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0005Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Voltage monitor 1 interrupt disabled 1: Voltage monitor 1 interrupt enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter mode select bit (2, 5)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Detected by passing through Vdet1	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bits (5)	b5 b4 0 0: Division of fLOCO by 1 (no division) 0 1: Division of fLOCO by 2 1 0: Division of fLOCO by 4 1 1: Division of fLOCO by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (6)	0: VCC reaches Vdet1 or above 1: VCC reaches Vdet1 or below	R/W

Notes:

1. The VW1C0 bit is enabled when the VC1E bit in the VCA2 register is 1 (voltage detection 1 circuit enabled). When the VC1E bit is 0 (voltage detection 1 circuit disabled), set the VW1C0 bit to 0 (voltage monitor 1 interrupt disabled). To set the VW1C0 bit to 1 (voltage monitor 1 interrupt enabled), see **Table 7.4 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When the digital filter is used (the VW1C1 bit is 0), set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).
   When the voltage monitor 1 interrupt is used to return from stop mode, set the VW1C1 bit to 1 (digital filter disabled mode).
3. Bits VW1C2 and VW1C3 are enabled when the VC1E bit in the VCA2 register is 1 (voltage detection 1 circuit enabled).
4. Set this bit to 0 by a program. The VW1C2 bit can be set to 0 by writing 0 by a program, but writing 1 to this bit has no effect.
5. When the VW1C0 bit is 1 (voltage monitor 1 interrupt enabled), do not set bits VW1C1 and VW1F0 to VW1F1 at the same time (with one instruction).
6. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is 0 (one-way edge). Set the VCAC1 bit to 0 before setting the VW1C7 bit.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW1C register. Rewriting the the VW1C register may set the VW1C2 bit to 1 (Vdet1 passing detected). Rewrite this register before setting the VW1C2 bit to 0 (not detected).

7.3 Monitoring VCC Input Voltage

7.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

7.3.2 Monitoring Vdet1

Make the following settings and wait for td(E-A) (see **20. Electrical Characteristics**). After that, the comparison result from voltage monitor 1 can be monitored with the VW1C3 bit in the VW1C register.

(1) Set bits VD1S1 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.
(2) Set the VC1E bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

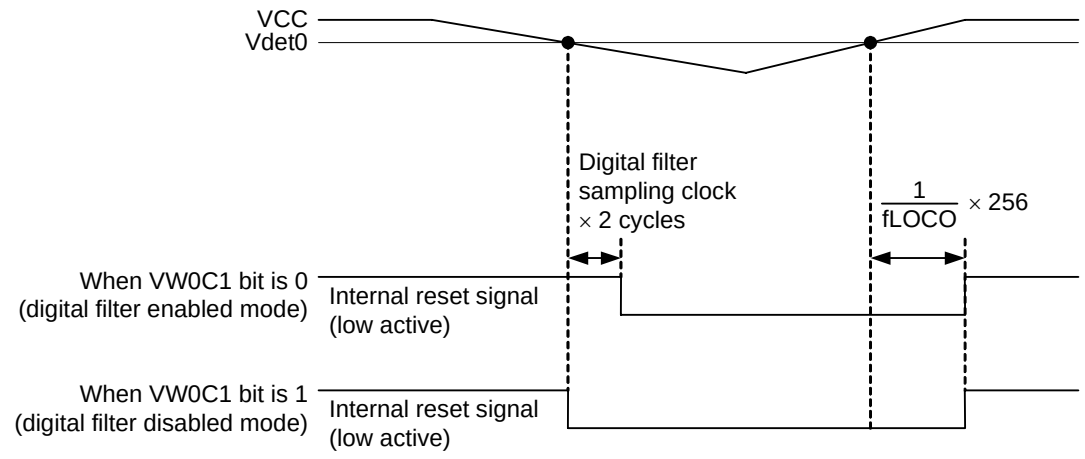
7.4 Voltage Monitor 0 Reset

Table 7.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 0 Reset. Figure 7.4 shows an Example of Voltage Monitor 0 Reset Operation.
Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled mode) to use the voltage monitor 0 interrupt to clear stop mode.

Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset

Step	When the Digital Filter is Used	When the Digital Filter is Not Used
1	Set bits VDSEL0 to VDSEL1 in the OFS register to select the detection voltage for voltage detection 0.	
2	Set the VC0E bit in the VCA2 register to 1 (voltage detection 0 circuit enabled).	
3	Wait for td(E-A).	
4 (1)	Set VW0F0 to VW0F1 in the VW0C register to select the sampling clock for the digital filter.	—
5 (1)	Set the VW0C1 bit in the VW0C register to 0 (digital filter enabled mode).	Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled mode).
6	Set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).	—
7	Wait for 2 cycles of the digital filter sampling clock.	No wait time
8	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).	

Note:
1. When the VW0C0 bit in the VW0C register is 0 (voltage monitor 0 reset disabled), steps 4 and 5 can be executed at the same time (with one instruction).



VW0C1: Bit in VW0C register

The above diagram applies under the following conditions:
- VC0E bit in VCA2 register = 1 (voltage detection 0 circuit enabled)
- VW0C0 bit in VW0C register = 1 (voltage monitor 0 reset enabled)

When the internal reset signal goes low, the CPU, SFRs, and I/O ports are initialized.
When the internal reset signal changes from low to high, program execution starts from the address indicated by the reset vector.
For the states of the SFRs, see **3.2 Special Function Registers (SFRs)**.

Figure 7.4 Example of Voltage Monitor 0 Reset Operation

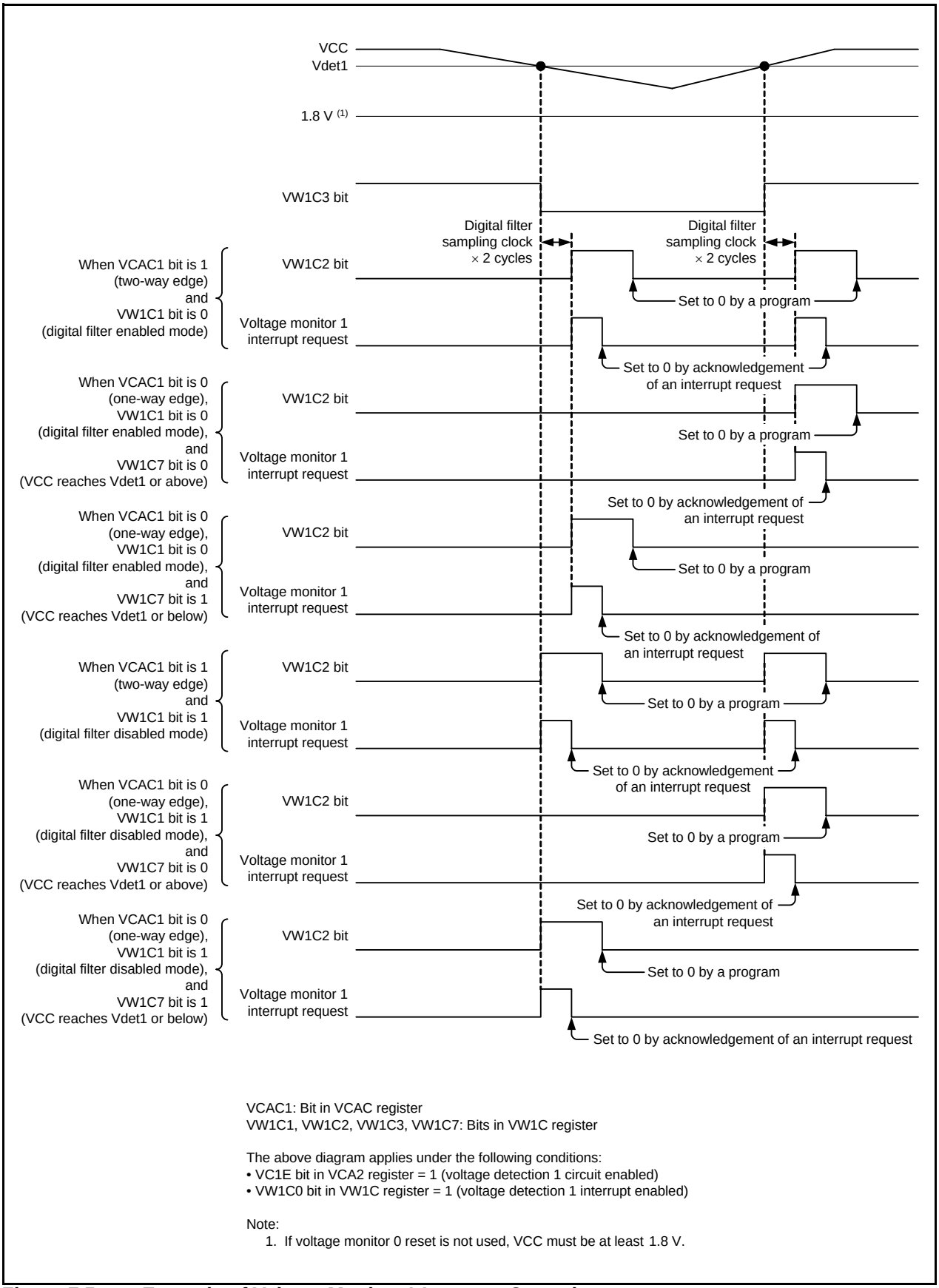
7.5 Voltage Monitor 1 Interrupt

Table 7.4 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 7.5 shows an Example of Voltage Monitor 1 Interrupt Operation.
Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled mode) to use the voltage monitor 1 interrupt to clear stop mode.

Table 7.4 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When the Digital Filter is Used	When the Digital Filter is Not Used
1	Set bits VD1S1 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.	
2	Set the VC1E bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td(E-A).	
4 (1)	Set bits VW1F0 to VW1F1 in the VW1C register to select the sampling clock for the digital filter.	—
5 (1)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled mode).	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled mode).
6	Set the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register to select the timing for an interrupt request.	
7	Set the VW1C2 bit in the VW1C register to 0 (not detected).	
8	Set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).	—
9	Wait for 2 cycles of the digital filter sampling clock.	No wait time
10	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled).	

Note:
1. When the VW1C0 bit in the VW1C register is 0 (voltage monitor 1 interrupt disabled), steps 4 and 5 can be executed at the same time (with one instruction).



VCAC1: Bit in VCAC register
VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register

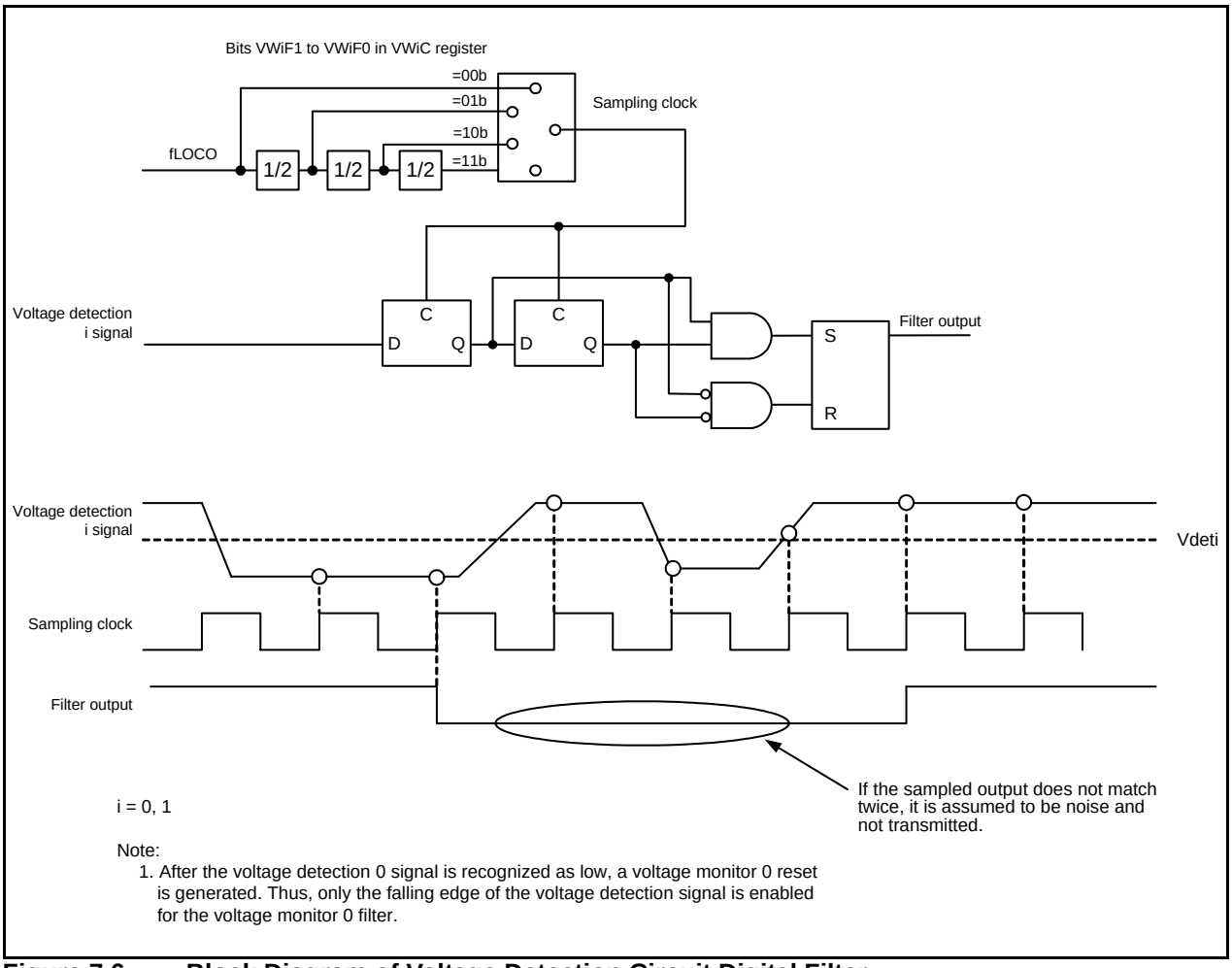
The above diagram applies under the following conditions:
- VC1E bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage detection 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, VCC must be at least 1.8 V.

Figure 7.5 Example of Voltage Monitor 1 Interrupt Operation

7.6 Digital Filter for Voltage Detection Circuits 0 and 1

Figure 7.6 shows a Block Diagram of Voltage Detection Circuit Digital Filter. In digital filter enabled mode, the voltage detection signal from the voltage detection circuit is used to generate a voltage monitor 0 reset signal and a voltage monitor 1 interrupt signal individually through the digital filter circuit. The filter width of the digital filter circuit is the sampling clock × 2.



Note:
1. After the voltage detection 0 signal is recognized as low, a voltage monitor 0 reset is generated. Thus, only the falling edge of the voltage detection signal is enabled for the voltage monitor 0 filter.

Figure 7.6 Block Diagram of Voltage Detection Circuit Digital Filter

8. Watchdog Timer

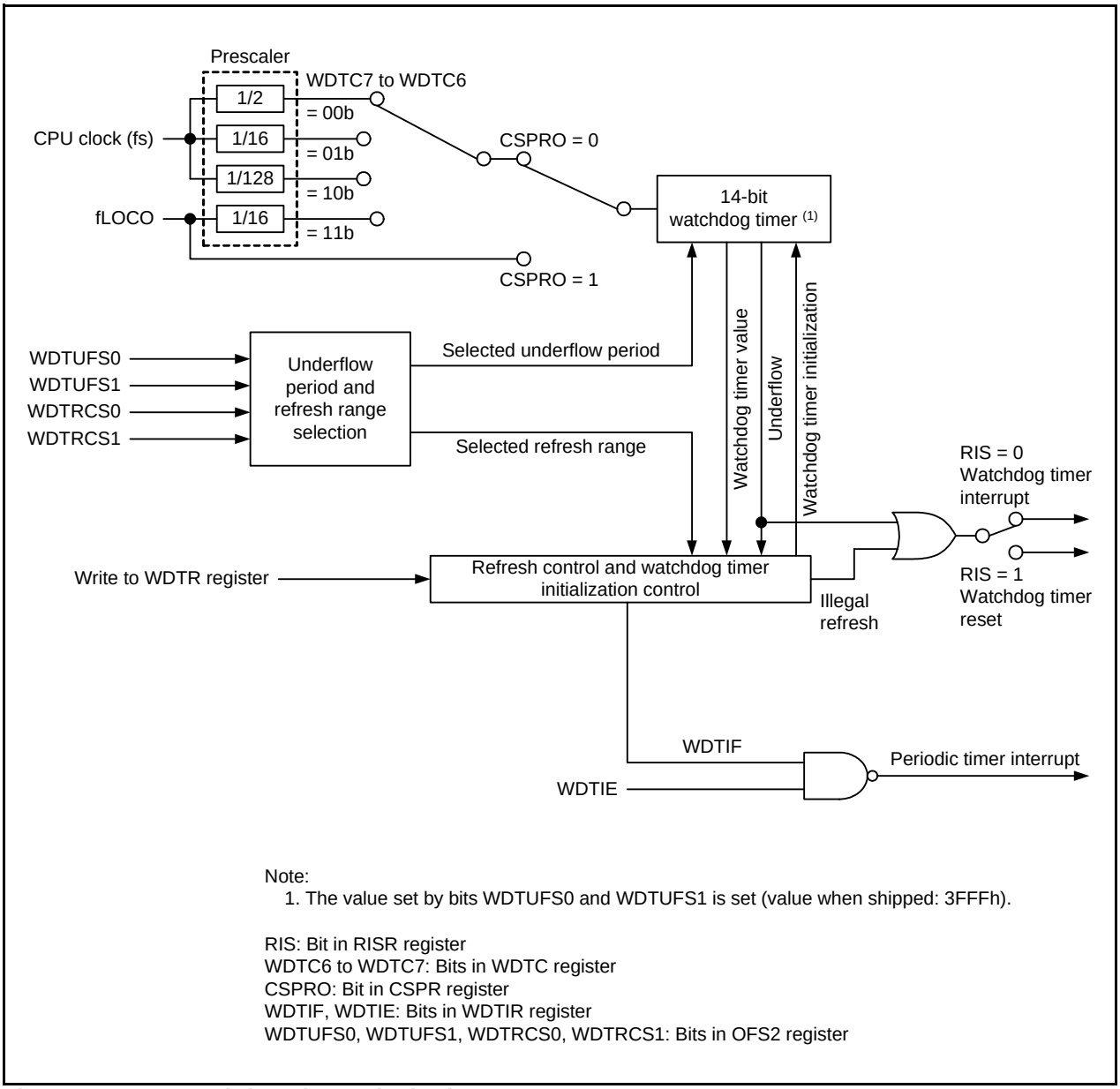
The watchdog timer is a function for detecting program malfunctions. Using this function is recommended, since it can improve system reliability.
The watchdog timer also has a function that can be used as a periodic timer.

8.1 Overview

The watchdog timer has a 14-bit down counter, and count source protection mode can be enabled or disabled.
Table 8.1 lists the Watchdog Timer Specifications.
For details on the watchdog timer reset, see **6.3.5 Watchdog Timer Reset**.
For details on the periodic timer, see **8.3.4 Periodic Timer Function**.
Figure 8.1 shows the Watchdog Timer Block Diagram.

Table 8.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock or low-speed on-chip oscillator clock (1/16)	Low-speed on-chip oscillator clock
Count operation	Decrement	
Count start condition	Either of the following can be selected: • The count is automatically started after a reset. • The count is started by writing to the WDTS register.	
Count stop conditions	When wait mode or stop mode is entered while the count source is the CPU clock	None
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register during the refresh acceptance period (when a refresh acceptance period is set) • Underflow	
Operation at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Selection of the count source Selected by bits WDTC6 to WDTC7 in the WDTC register. • Count source protection mode - Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register. - If count source protection mode is disabled, whether count source protection mode is enabled or disabled is selected by the CSPRO bit in the CSPR register. • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register. • Initial value of the watchdog timer (underflow period) Selected by bits WDTUFS0 to WDTUFS1 in the OFS2 register. • Refresh acceptance period for the watchdog timer Selected by bits WDTRCS0 to WDTRCS1 in the OFS2 register.	



Note:
1. The value set by bits WDTUFS0 and WDTUFS1 is set (value when shipped: 3FFFh).

RIS: Bit in RISR register
WDTC6 to WDTC7: Bits in WDTC register
CSPRO: Bit in CSPR register
WDTIF, WDTIE: Bits in WDTIR register
WDTUFS0, WDTUFS1, WDTRCS0, WDTRCS1: Bits in OFS2 register

Figure 8.1 Watchdog Timer Block Diagram

8.2 Registers

Table 8.2 lists the Watchdog Timer Register Configuration.

Table 8.2 Watchdog Timer Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Watchdog Timer Function Register	RISR	(Note 1)	00030h	8
Watchdog Timer Reset Register	WDTR	XXh	00031h	8
Watchdog Timer Start Register	WDTS	XXh	00032h	8
Watchdog Timer Control Register	WDTC	01XXXXXXb	00033h	8
Count Source Protection Mode Register	CSPR	(Note 1)	00034h	8
Periodic Timer Interrupt Control Register	WDTIR	00h	00035h	8

Note:
1. See the description of the individual registers.

8.2.1 Watchdog Timer Function Register (RISR)

Address 00030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RIS	UFIF	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 0.							
After Reset	0	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	UFIF	WDT underflow detection flag	0: No watchdog timer underflow 1: Watchdog timer underflow (1)	R/W
b7	RIS	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (2)	R/W

Notes:
1. After reading this bit as 1, wait at least one cycle of the count source before writing 0 to it.
2. The RIS bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.
   When the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the RIS bit is automatically set to 1.

   Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the RISR register.

UFIF Bit (WDT underflow detection flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Conditions for setting to 1]
• When the watchdog timer underflows while the RIS bit is 0 (watchdog timer interrupt).
• When a refresh is executed during the period other than the acceptance period (illegal refresh) while the RIS bit is 0 (watchdog timer interrupt).

8.2.2 Watchdog Timer Reset Register (WDTR)

Address 00031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	The watchdog timer is initialized by writing 00h and then writing FFh during the acceptance period. When 00h and then FFh is written during a period other than the acceptance period, a watchdog timer reset or watchdog timer interrupt is generated. If a watchdog timer interrupt is selected, the watchdog timer is not initialized. The initial value in the watchdog timer is specified by bits WDTUFS0 to WDTUFS1 in the OFS2 register. (1)	W

Note:
1. Only write to the WDTR register when the watchdog timer is counting.

8.2.3 Watchdog Timer Start Register (WDTS)

Address 00032h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	The watchdog timer is started by executing a write instruction to this register.	W

8.2.4 Watchdog Timer Control Register (WDTC)

Address 00033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	WDTC6	—	—	—	—	—	—
After Reset	0	1	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is undefined.	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	WDTC6	Watchdog timer count source select bits	b7 b6 0 0: Division of CPU clock by 2 0 1: Division of CPU clock by 16 1 0: Division of CPU clock by 128 1 1: Division of low-speed on-chip oscillator by 16	R/W
b7	WDTC7			R/W

8.2.5 Count Source Protection Mode Register (CSPR)

Address 00034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 0.							
After Reset	0	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, first write 0 and then write 1 to it. This bit cannot be set to 0 by a program. Do not write to any register other than the CSPR register between writing 0 and then writing 1.

8.2.6 Periodic Timer Interrupt Control Register (WDTIR)

Address 00035h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTIE	WDTIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	WDTIF	Periodic timer interrupt request flag	0: No periodic timer interrupt requested 1: Periodic timer interrupt requested	R/W
b7	WDTIE	Periodic timer interrupt enable bit (1)	0: Periodic timer interrupt disabled 1: Periodic timer interrupt enabled	R/W

Note:
1. When bits WDTRCS1 to WDTRCS0 in the OFS2 register is 11b (100 %), set the WDTIE bit to 0 (periodic timer interrupt disabled).

WDTIF Bit (Periodic timer interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• When the watchdog timer completes counting an illegal write range.

8.3 Operation

8.3.1 Items Common to Multiple Modes

8.3.1.1 Refresh Acceptance Period

The period for accepting a refresh operation to the watchdog timer (a write to the WDTR register) can be selected by bits WDTRCS0 to WDTRCS1 in the OFS2 register. Figure 8.2 shows the Watchdog Timer Refresh Acceptance Period.

When the period from the start of counting to underflow is 100 %, a refresh operation executed during the acceptance period is accepted as shown below. A refresh operation executed during a period other than the acceptance period is processed as an illegal refresh, generating a watchdog timer interrupt or watchdog timer reset (selected by the RIS bit in the RISR register). In addition, the UFIF bit in the RISR register is set to 1.

Do not perform a refresh operation when the watchdog timer is stopped.

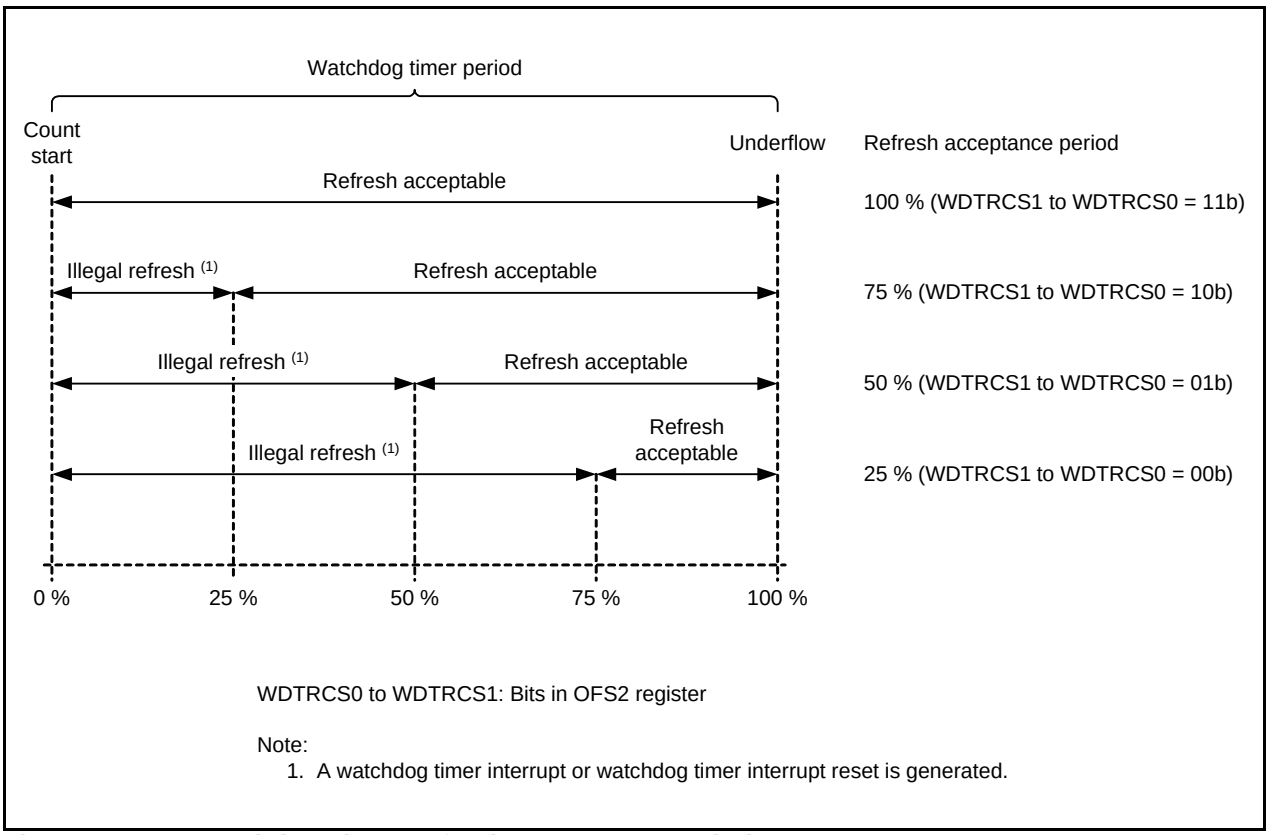


Figure 8.2 Watchdog Timer Refresh Acceptance Period

8.3.2 When Count Source Protection Mode is Disabled

When count source protection mode is disabled, the count source for the watchdog timer is the CPU clock or low-speed on-chip oscillator clock.
Table 8.3 lists the Watchdog Timer Specifications When Count Source Protection Mode is Disabled.

Table 8.3 Watchdog Timer Specifications When Count Source Protection Mode is Disabled

Item	Specification
Count source	CPU clock or low-speed on-chip oscillator clock (1/16)
Count operation	Decrement
Period	$\frac{\text{Prescaler division ratio (n)} \times \text{Count value in the watchdog timer (m)}}{\text{Count source}}$ (1) n: 2, 16, or 128 (selected by bits WDTC6 to WDTC7 in the WDTC register) However, when bits WDTC7 to WDTC6 are 11b (count source is low-speed on-chip oscillator), n is 16. m: Value set by bits WDTUFS0 to WDTUFS1 in the OFS2 register Ex.: When the prescaler divides a CPU clock of 20 MHz by 16, and bits WDTUFS1 to WDTUFS0 are 11b (3FFFh), the period is approx. 13.1 ms.
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit in the OFS register (address 0FFFFh). • When the WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer and the prescaler are stopped after a reset, and only start counting when the WDTS register is written. • When the WDTON bit is 0 (watchdog timer is automatically started after reset) The watchdog timer and the prescaler automatically start counting after a reset.
Count stop conditions	When wait mode or stop mode is entered while the count source is the CPU clock
Operation at underflow	• When the RIS bit in the RISR register is 0 Watchdog timer interrupt • When the RIS bit in the RISR register is 1 Watchdog timer reset (See **6.3.5 Watchdog Timer Reset**.)

Note:
1. The watchdog timer is initialized by writing 00h and then writing FFh to the WDTR register. The prescaler is initialized after a reset. This results in discrepancies in the watchdog timer period due to the prescaler.

8.3.3 When Count Source Protection Mode is Enabled

When count source protection mode is enabled, the count source for the watchdog timer is the low-speed on-chip oscillator clock. If the CPU clock is stopped when a program runs out of control, a clock will still be supplied to the watchdog timer.
Table 8.4 lists the Watchdog Timer Specifications When Count Source Protection Mode is Enabled.

Table 8.4 Watchdog Timer Specifications When Count Source Protection Mode is Enabled

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value in the watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock}}$ m: Value set by WDTUFS0 to WDTUFS1 in the OFS2 register Ex.: When the low-speed on-chip oscillator clock is 125 kHz and bits WDTUFS1 to WDTUFS0 are 00b (03FFh), the period is approx. 8.2 ms.
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit in the OFS register (address 0FFFFh). • When the WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer is stopped after a reset, and only starts counting when the WDTS register is written. • When the WDTON bit is 0 (watchdog timer is automatically started after reset) The watchdog timer automatically starts counting after a reset.
Count stop condition	None (The count is not stopped even in wait mode or stop mode once it is started.)
Operation at underflow	Watchdog timer reset (See **6.3.5 Watchdog Timer Reset**.)
Registers, bits	When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), the following are automatically set: • The low-speed on-chip oscillator oscillates. • The RIS bit in the RISR register is set to 1 (watchdog timer reset).

8.3.4 Periodic Timer Function

The count range is determined by the underflow period setting (bits WDTUFS0 to WDTUFS1 in the OFS2 register) and the refresh acceptance period setting (bits WDTRCS0 to WDTRCS1 in the OFS2 register). The periodic timer cannot be used in stop mode.
Table 8.5 lists the Periodic Timer Settings. Figure 8.3 shows the Timing of Periodic Timer Function.
When the periodic timer runs beyond the count range in Table 8.5, the WDTIF bit in the WDTIR register is set to 1 (periodic timer interrupt requested).

Table 8.5 Periodic Timer Settings

Initial Value Set by Bits WDTUFS1 to WDTUFS0 in OFS2 Register	Refresh Range Set by Bits WDTRCS1 to WDTRCS0 in OFS2 Register (1)	Range Counted by Periodic Timer
11b	10b	3FFFh → 2FFFh
	01b	3FFFh → 1FFFh
	00b	3FFFh → 0FFFh
10b	10b	1FFFh → 17FFh
	01b	1FFFh → 0FFFh
	00b	1FFFh → 07FFh
01b	10b	0FFFh → 0BFFh
	01b	0FFFh → 07FFh
	00b	0FFFh → 03FFh
00b	10b	03FFh → 02FFh
	01b	03FFh → 01FFh
	00b	03FFh → 00FFh

Note:
1. When bits WDTRCS1 to WDTRCS0 in the OFS2 register is 11b (100 %), set the WDTIE bit to 0 (periodic timer interrupt disabled).

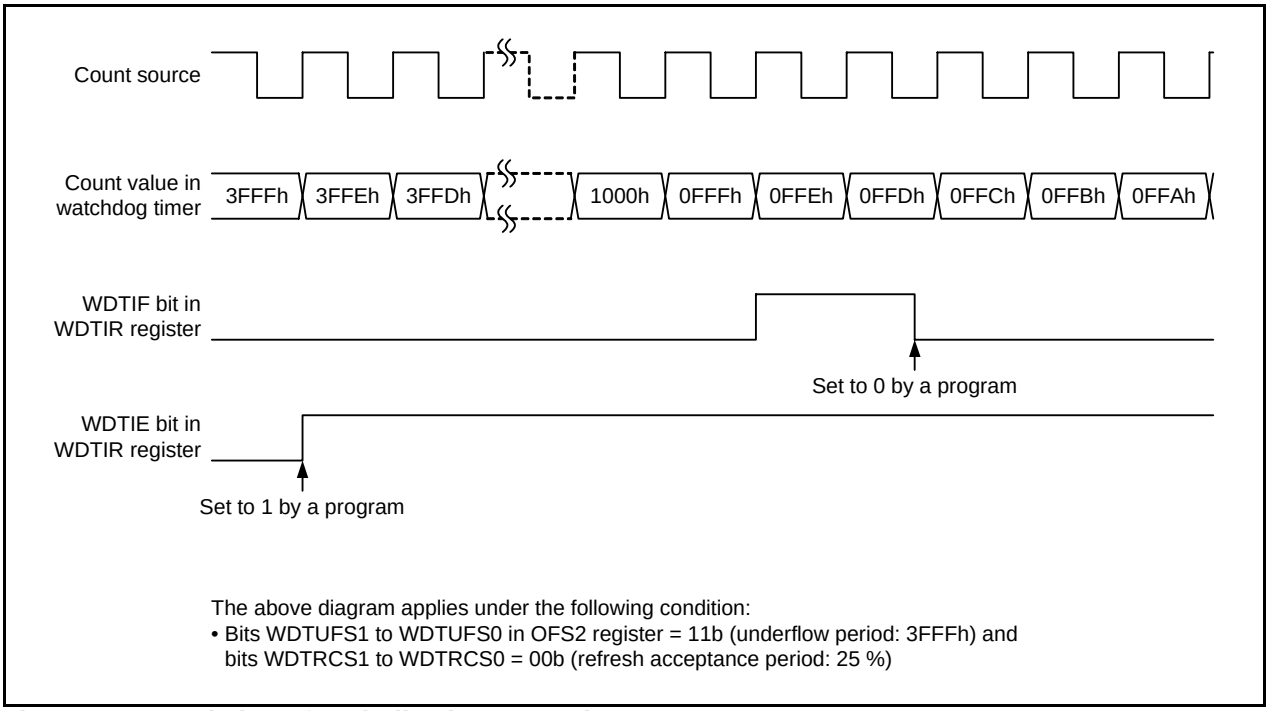


Figure 8.3 Timing of Periodic Timer Function

8.4 Notes on Watchdog Timer

- Do not switch the count sources during watchdog timer operation.
- There is a delay of two cycles of the count source from a write to the WDTR register until the initialization of the watchdog timer.
- Allow at least three cycles of the count source between the previous and the next initialization of the watchdog timer.

9. Clock Generation Circuit

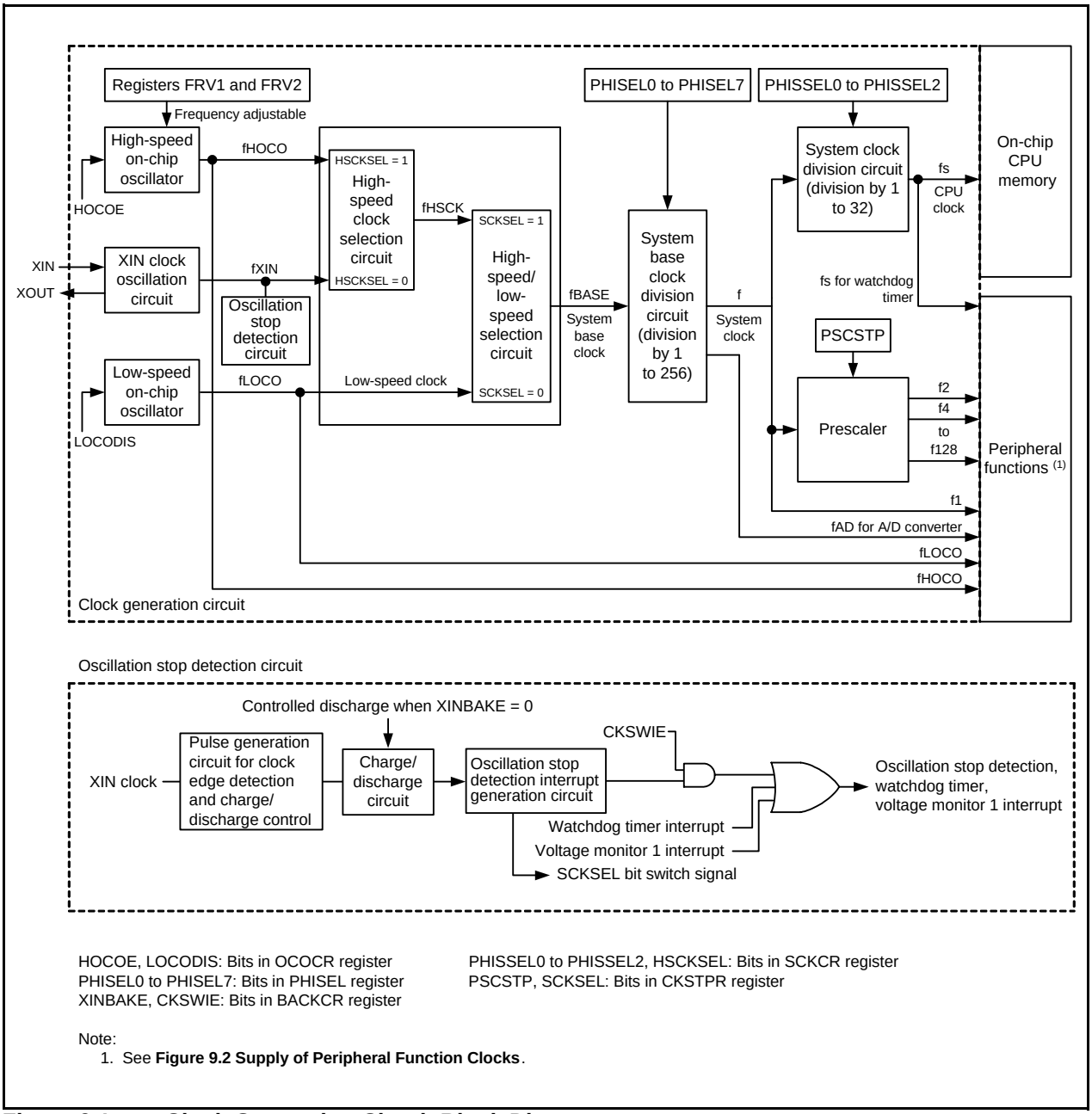
9.1 Overview

The following three circuits are included in the clock generation circuit:
• XIN clock oscillation circuit
• High-speed on-chip oscillator
• Low-speed on-chip oscillator
Table 9.1 lists the Clock Generation Circuit Specifications. Figure 9.1 shows the Clock Generation Circuit Block Diagram. Figure 9.2 shows the Supply of Peripheral Function Clocks. Table 9.2 lists the Clock Generation Circuit Pin Configuration.

Table 9.1 Clock Generation Circuit Specifications

Item	XIN Clock Oscillation Circuit	High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator
Clock frequency	0 MHz to 20 MHz (2 MHz to 20 MHz when an oscillator is used)	Approx. 20 MHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	—	—
Oscillator connect pins	XIN, XOUT (1)	—	—
Oscillation start and stop	Usable	Usable	Usable
State after reset	Stopped	Stopped	Oscillates
Others	• An externally generated clock can be input. • A feed-back resistor is included (connected or not connected can be selected).	The system clock can be output from P4_7.	The system clock can be output from P4_7.

Note:
1. When the on-chip oscillator clock instead of the XIN clock oscillation circuit is used as the CPU clock, these pins can be used as P4_6 and P4_7.



HOCOE, LOCODIS: Bits in OCOCR register
PHISEL0 to PHISEL7: Bits in PHISEL register
XINBAKE, CKSWIE: Bits in BACKCR register

PHISSEL0 to PHISSEL2, HSCKSEL: Bits in SCKCR register
PSCSTP, SCKSEL: Bits in CKSTPR register

Note:
1. See **Figure 9.2 Supply of Peripheral Function Clocks**.

Figure 9.1 Clock Generation Circuit Block Diagram

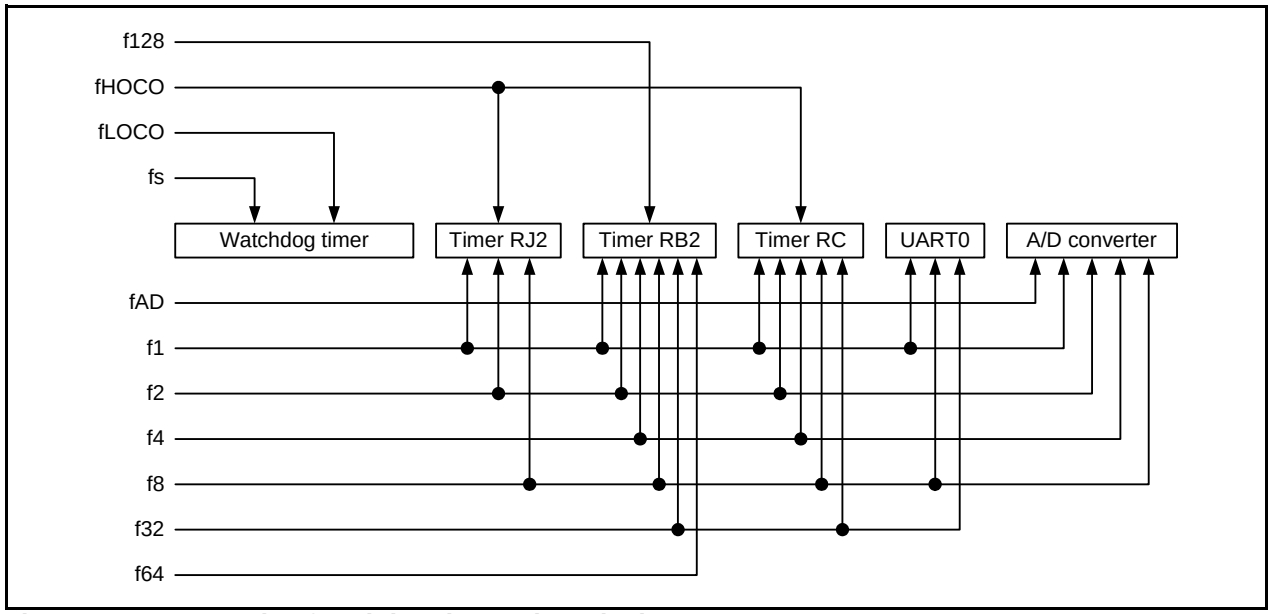


Figure 9.2 Supply of Peripheral Function Clocks

Table 9.2 Clock Generation Circuit Pin Configuration

Pin Name	I/O	Function
XIN	I	XIN clock input/external clock input
XOUT	O	XIN clock output

9.2 Registers

Table 9.3 lists the Clock Generation Circuit Register Configuration.

Table 9.3 Clock Generation Circuit Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
External Clock Control Register	EXCKCR	00h	00020h	8
High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h	00021h	8
System Clock f Control Register	SCKCR	00h	00022h	8
System Clock f Select Register	PHISEL	00h	00023h	8
Clock Stop Control Register	CKSTPR	00h	00024h	8
Clock Control Register When Returning from Modes	CKRSCR	00h	00025h	8
Oscillation Stop Detection Register	BAKCR	00h	00026h	8
High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	Value when shipped	00064h	8
High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	Value when shipped	00065h	8
High-Speed On-Chip Oscillator Control Register 1	FRV1	Value when shipped	00067h	8
High-Speed On-Chip Oscillator Control Register 2	FRV2	Value when shipped	00068h	8

9.2.1 External Clock Control Register (EXCKCR)

Address 00020h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	XRCUT	—	—	—	—	CKPT1	CKPT0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKPT0	Port P4_6 and P4_7 pin function select bits	See table below	R/W
b1	CKPT1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	XRCUT	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Register Setting		Pin Function	
CKPT1	CKPT0	P4_6	P4_7
0	0	I/O port	I/O port
0	1	XIN clock input (External clock input)	I/O port
1	0	I/O port	System clock output
1	1	XIN	XOUT

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the EXCKCR register.

Bits CKPT0 to CKPT1 (Port P4_6 and P4_7 pin function select bits)

When stopping oscillation with an oscillator attached, set bits CKPT1 to CKPT0 to 00b and set P4_6 and P4_7 to input ports according to Tables 12.18 and 12.19.
While the high-speed on-chip oscillator clock or the low-speed on-chip oscillator clock is selected as the system base clock, the system clock can be output from P4_7 by setting bits CKPT1 to CKPT0 to 10b and bits P47SEL1 to P47SEL0 in the PMH4 register to 00b.

XRCUT Bit (XIN-XOUT on-chip feedback resistor select bit)

The XRCUT bit is enabled only when bits CKPT1 to CKPT0 are 11b.
When the STPM bit in the CKSTPR register is set to 1 (stop mode), the on-chip feedback resistor is disabled.

9.2.2 High-Speed/Low-Speed On-Chip Oscillator Control Register (OCOCR)

Address 00021h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	LOCODIS	HOCOE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	HOCOE	High-speed on-chip oscillator oscillation enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	LOCODIS	Low-speed on-chip oscillator oscillation stop bit	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCOCR register.

HOCOE Bit (High-speed on-chip oscillator oscillation enable bit)

The high-speed on-chip oscillator clock generated by the high-speed on-chip oscillator is stopped after a reset. Table 9.4 lists the Register Settings and High-Speed On-Chip Oscillator States. When selecting the high-speed on-chip oscillator clock as the system base clock, switch the clock according to **9.4.6 Procedure for Switching System Base Clock**.

Table 9.4 Register Settings and High-Speed On-Chip Oscillator States

Register	CKSTPR	SCKCR	CKSTPR	OCOCR	High-Speed On-Chip Oscillator State
Bit	STPM	HSCKSEL	SCKSEL	HOCOE	
Setting value	0	Other than 11b		0	Oscillation off
	0	Other than 11b		1	Oscillation on
	0	11b		X	Oscillation on
	1	X		X	Oscillation off

X: 0 or 1

LOCODIS Bit (Low-speed on-chip oscillator oscillation stop bit)

Table 9.5 lists the Register Settings and Low-Speed On-Chip Oscillator States. If the XINBAKE bit in the BAKCR register is 1 (oscillation stop detection function enabled), when the XIN clock is stopped, the low-speed on-chip oscillator starts operation and supplies the system base clock.

Table 9.5 Register Settings and Low-Speed On-Chip Oscillator States

Register	CSPR	WDTC		CKSTPR		OCOCR	Low-Speed On-Chip Oscillator State
Bit	CSPRO	WDTC7	WDTC6	STPM	SCKSEL	LOCODIS	
Setting value	0	Other than 11b		0	1	0	Oscillation on
	0	Other than 11b		0	1	1	Oscillation off
	0	Other than 11b		0	0	X	Oscillation on
	0	Other than 11b		1	X	X	Oscillation off
	0	11b		X	X	X	Oscillation on
	1	X		X	X	X	Oscillation on

X: 0 or 1

9.2.3 System Clock f Control Register (SCKCR)

Address 00022h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	HSCKSEL	WAITM	—	—	PHISSEL2	PHISSEL1	PHISSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PHISSEL0	CPU clock division ratio select bits	These bits are used to select the division ratio of the system clock (f) to generate the CPU clock (fs). b2 b1 b0 0 0 0: fs = System clock with no division 0 0 1: fs = System clock divided by 2 0 1 0: fs = System clock divided by 4 0 1 1: fs = System clock divided by 8 1 0 0: fs = System clock divided by 16 1 0 1: fs = System clock divided by 32 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	PHISSEL1			R/W
b2	PHISSEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	WAITM	Wait control bit	0: Not in wait mode 1: Wait mode is entered	R/W
b6	HSCKSEL	High-speed on-chip oscillator/XIN clock select bit	0: XIN clock 1: High-speed on-chip oscillator clock	R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the SCKCR register.

Bits PHISSEL0 to PHISSEL2 (CPU clock division ratio select bits)

Bits PHISSEL2 to PHISSEL0 are set to 000b (system clock with no division) if the PHISRS bit in the CKRSCR register is 1 (no division) when the MCU returns from wait mode or stop mode.

WAITM Bit (Wait control bit)

[Condition for setting to 0]
• When a peripheral function interrupt is used to return from wait mode.
[Condition for setting to 1]
• When 1 is written to the WAITM bit after the PRC0 bit in the PRCR register is set to 1 (write enabled).

9.2.4 System Clock f Select Register (PHISEL)

Address 00023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PHISEL7	PHISEL6	PHISEL5	PHISEL4	PHISEL3	PHISEL2	PHISEL1	PHISEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b7 to b0	PHISEL7 to PHISEL0	System clock division ratio select bits	These bits used to set the division ratio of the system base clock (fBASE) to generate the system clock (f) and the A/D converter clock (fAD). • System clock (f) f = fBASE/(n + 1) • Clock for A/D converter (fAD) fAD = fBASE/(n + 1).....when (n + 1) is not a multiple of 4 fAD = 4 × fBASE/(n + 1)...when (n + 1) is a multiple of 4 n: Binary value set by the PHISEL register	00h to FFh	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the PHISEL register.
Table 9.6 lists the PHISEL Register Setting Example.

Table 9.6 PHISEL Register Setting Example

Value Set in PHISEL Register (n)	System Clock (f)	A/D Converter Clock (fAD)
00h	fBASE	fBASE
01h	Division of fBASE by 2	Division of fBASE by 2
02h	Division of fBASE by 3	Division of fBASE by 3
03h	Division of fBASE by 4	fBASE
04h	Division of fBASE by 5	Division of fBASE by 5
05h	Division of fBASE by 6	Division of fBASE by 6
06h	Division of fBASE by 7	Division of fBASE by 7
07h	Division of fBASE by 8	Division of fBASE by 2

9.2.5 Clock Stop Control Register (CKSTPR)

Address 00024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCKSEL	—	—	—	—	PSCSTP	WCKSTP	STPM
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	STPM	All clock stop control bit	0: Clocks oscillate 1: All clocks are stopped (stop mode)	R/W
b1	WCKSTP	fBASE stop bit in wait mode	0: System clock supplied in wait mode 1: System clock stopped in wait mode	R/W
b2	PSCSTP	Prescaler stop bit	0: Prescaler operates 1: Prescaler is stopped	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	SCKSEL	System base clock select bit	0: fLOCO 1: fHSCK	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CKSTPR register.

STPM Bit (All clock stop control bit)

The low-speed on-chip oscillator clock is not stopped when:
- The count source protection mode for the watchdog timer is enabled.
- A clock obtained by dividing the low-speed on-chip oscillator by 16 is selected as the count source for the watchdog timer.

WCKSTP Bit (fBASE stop bit in wait mode)

This bit is used to control supply and stop of the system clock in wait mode.

PSCSTP Bit (Prescaler stop bit)

Setting the PSCSTP bit to 1 stops the prescaler. The peripheral functions that use f2 to f128 are stopped operating. However, the values of corresponding registers are retained.

SCKSEL Bit (System base clock select bit)

[Conditions for setting to 0]
- When 0 is written to this bit.
- When the XIN clock oscillation stop is detected and the system clock is switched to fLOCO if the XIN clock is selected as the system clock and the XINBAKE bit in the BAKCR register is 1 (oscillation stop detection function enabled).

[Conditions for setting to 1]
- When 1 is written to this bit.
- When the MCU returns from wait mode when the WAITRS bit in the CKRSCR register is 1 (fHSCK).
- When the MCU returns from stop mode when the STOPRS bit in the CKRSCR register is 1 (fHSCK).

9.2.6 Clock Control Register When Returning from Modes (CKRSCR)

Address 00025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	STOPRS	WAITRS	PHISRS	—	CKST3	CKST2	CKST1	CKST0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKST0	Clock oscillator circuit oscillation stabilization state select bits	Number of wait states b3 b2 b1 b0 0 0 0 0: 4 0 0 0 1: 16 0 0 1 0: 32 0 0 1 1: 64 0 1 0 0: 128 0 1 0 1: 256 0 1 1 0: 512 0 1 1 1: 1024 1 0 0 0: 2048 1 0 0 1: 4096 1 0 1 0: 8192 1 0 1 1: 16384 1 1 0 0: 32768 1 1 0 1: 65536 1 1 1 0: 131072 1 1 1 1: 262144	R/W
b1	CKST1			R/W
b2	CKST2			R/W
b3	CKST3			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	PHISRS	CPU clock division select bit when returning from wait mode or stop mode	0: The value set in bits PHISSEL0 to PHISSEL2 in the SCKCR register is valid 1: No division	R/W
b6	WAITRS	System base clock select bit when returning from wait mode	0: Return using the system base clock used immediately before entering wait mode 1: fHSCK (1, 2)	R/W
b7	STOPRS	System base clock select bit when returning from stop mode	0: Return using the system base clock used immediately before entering stop mode 1: fHSCK (1, 2)	R/W

Notes:
1. When the HSCKSEL bit in the SCKCR register is 0 (XIN clock), set pins P4_6 and P4_7 to XIN oscillation by a program before entering wait mode or stop mode.
2. Set this bit to 0 before entering wait mode or stop mode if the FMR27 bit in the FMR2 register is set to 1 (low-current-consumption read mode enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CKRSCR register.

Bits CKST0 to CKST3 (Clock oscillator circuit oscillation stabilization state select bits)

These bits are used to set the oscillation stabilization time of the oscillator circuit for the system base clock when returning wait mode or stop mode. Set appropriate values according to Table 9.7.

Table 9.7 Oscillation Stabilization Time When Returning Wait Mode or Stop Mode

System Base Clock after Returning	Stabilization Time (Automatic Generation)	Setting Value for Number of Wait States (Bits CKST0 to CKST3)
XIN clock	XIN clock period × system clock division ratio × number of wait states	Contact the oscillator manufacturer.
High-speed on-chip oscillator clock	High-speed on-chip oscillator clock period × system clock division ratio × number of wait states	See **Table 20.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
Low-speed on-chip oscillator clock	Low-speed on-chip oscillator clock period × system clock division ratio × 2 wait states	— (Value set in CKST0 to CKST3 is invalid)

When the oscillation stop detection function is disabled, the system base clock used after returning from stop mode is the XIN clock. The stabilization time generated by the hardware is expressed as follows:
Stabilization time = XIN clock period × System clock division ratio × Number of steps for stabilization

When the oscillation stop detection function is enabled, the system base clock used after returning from stop mode is the low-speed on-chip oscillator clock. The stabilization time generated by the hardware is expressed as follows:
Stabilization time = Low-speed on-chip oscillator clock cycle × System clock division ratio × Number of steps for stabilization

9.2.7 Oscillation Stop Detection Register (BAKCR)

Address 00026h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CKSWIF	XINHALT	CKSWIE	XINBAKE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	XINBAKE	Oscillation stop detection enable bit	0: Oscillation stop detection function disabled 1: Oscillation stop detection function enabled	R/W
b1	CKSWIE	Oscillation stop detection interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b2	XINHALT	Clock monitor bit (1)	0: XIN clock oscillating 1: XIN clock halted	R
b3	CKSWIF	Oscillation stop detection interrupt request flag (1)	0: No oscillation stop detection interrupt request is generated 1: Oscillation stop detection interrupt request is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Bits XINHALT and CKSWIF are enabled when the XINBAKE bit is 1 (oscillation stop detection function enabled). When the XINHALT bit is 0 (XIN clock oscillating), it indicates that the XIN clock is oscillating. It does not indicate oscillation is stable.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the BAKCR register.

CKSWIF Bit (Oscillation stop detection interrupt request flag)

[Condition for setting to 0]
- When 0 is written to this bit.

[Condition for setting to 1]
- When oscillation stop is detected while the XIN clock is selected as the system base clock and the XINBAKE bit in the BAKCR register is 1 (oscillation stop detection function enabled).

9.2.8 High-Speed On-Chip Oscillator 18.432 MHz Control Register 0 (FR18S0)

Address 00064h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	Frequency adjustment data for 18.432 MHz is stored. The frequency of the high-speed on-chip oscillator can be adjusted to 18.432 MHz by transferring this value to the FRV1 register and the adjustment value in the FR18S1 register to the FRV2 register.	R/W

9.2.9 High-Speed On-Chip Oscillator 18.432 MHz Control Register 1 (FR18S1)

Address 00065h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	Frequency adjustment data for 18.432 MHz is stored. The frequency of the high-speed on-chip oscillator can be adjusted to 18.432 MHz by transferring this value to the FRV2 register and the adjustment value in the FR18S0 register to the FRV1 register.	R/W

9.2.10 High-Speed On-Chip Oscillator Control Register 1 (FRV1)

Address 00067h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 20 MHz: FRV1 = Value after reset, FRV2 = Value after reset 18.432 MHz: Transfer the value in the FR18S0 register to the FRV1 register and the value in the FR18S1 register to the FRV2 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRV1 register.

9.2.11 High-Speed On-Chip Oscillator Control Register 2 (FRV2)

Address 00068h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

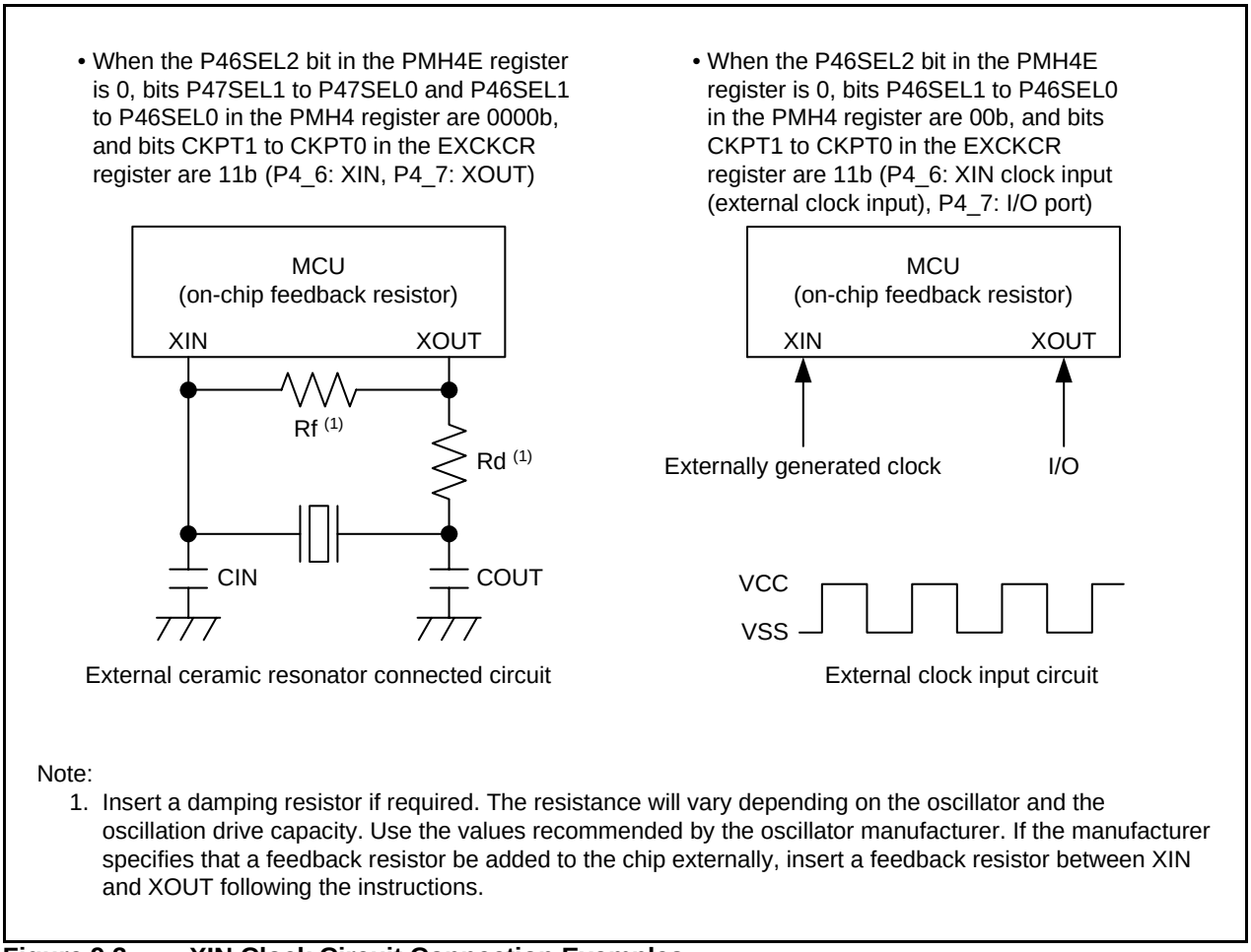
Bit	Function	R/W
b7 to b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 20 MHz: FRV1 = Value after reset, FRV2 = Value after reset 18.432 MHz: Transfer the value in the FR18S0 register to the FRV1 register and the value in the FR18S1 register to the FRV2 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRV2 register.

9.3 Clock Oscillation Circuit

9.3.1 XIN Clock Oscillation Circuit

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU clock and the peripheral function clock. The XIN clock oscillation circuit is configured by connecting an oscillator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode to reduce power consumption. To input an externally generated clock to the XIN pin, set the P46SEL2 bit in the PMH4E register to 0, bits P46SEL1 to P46SEL0 in the PMH4 register to 00b (I/O port or XIN input), and bits CKPT1 to CKPT0 in the EXCKCR register to 01b (XIN clock input).
Figure 9.3 shows the XIN Clock Circuit Connection Examples.
The XIN clock is stopped during and after a reset.
The XIN clock starts oscillating when the P46SEL2 bit in the PMH4E register is set to 0, bits P47SEL1 to P47SEL0 and P46SEL1 to P46SEL0 in the PMH4 register are set to 0000b, and bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b (P4_6: XIN, P4_7: XOUT). After the XIN clock oscillation stabilizes, when the HSCKSEL bit in the SCKCR register is set to 0 (XIN clock) and the SCKSEL bit in the CKSTPR register is set to 1 (fHSCK), the XIN clock is selected to be used as the clock source for the CPU clock and the peripheral function clock.
When the high-speed on-chip oscillator or the low-speed on-chip oscillator is used as the system base clock, the XIN clock oscillation is stopped by setting bits CKPT1 to CKPT0 in the EXCKCR register to 00b. This reduces power consumption.
The XIN clock is stopped in stop mode. When inputting an externally generated clock to the XIN clock, do not use stop mode. See **10. Power Control** for details.



Note:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity. Use the values recommended by the oscillator manufacturer. If the manufacturer specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.

Figure 9.3 XIN Clock Circuit Connection Examples

9.3.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral function clock.

After the HOCOE bit in the OCOCR register is set to 1 (high-speed on-chip oscillator on) and the wait time for oscillation stabilization has elapsed, when the HSCKSEL bit in the SCKCR register is set to 1 (high-speed on-chip oscillator clock) and the SCKSEL bit in the CKSTPR register is set to 1 (fHSCK), the high-speed on-chip oscillator clock is the system base clock (fBASE).

Frequency adjustment data is stored in registers FRV1, FRV2, FR18S0, and FR18S1.

To adjust the frequency of the high-speed on-chip oscillator clock to 18.432 MHz, transfer the adjustment values in registers FR18S0 and FR18S1 to registers FRV1 and FRV2 respectively before use.

This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode. (See **Table 16.8 Setting Example for Clock Asynchronous Serial I/O Mode (Internal Clock Selected)**).

9.3.3 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral function clock.

After the LOCODIS bit in the OCOCR register is set to 0 (low-speed on-chip oscillator on) and the wait time for oscillation stabilization has elapsed, when the LSCKSEL bit in the SCKCR register is set to 0 (low-speed on-chip oscillator clock) and the SCKSEL bit in the CKSTPR register is set to 0 (fLOCO), the low-speed on-chip oscillator clock is the system base clock (fBASE).

After a reset, the on-chip oscillator clock (with no division) is the CPU clock.

The frequency of the on-chip oscillator clock will vary greatly depending on the power supply voltage and operating ambient temperature. Application products must be designed with sufficient margin to allow for these variations in frequency.

9.4 Clocks

9.4.1 System Base Clock (fBASE)

The system base clock is selected from the XIN clock oscillation circuit, high-speed on-chip oscillator, or low-speed on-chip oscillator to operate the MCU.
After a reset, the MCU operates using the on-chip oscillator clock in standard mode.

9.4.2 System Clock (f)

The system clock is obtained by dividing the system base clock by any value from 1 to 256, set by bits PHISEL0 to PHISEL7 in the PHISEL register. After a reset is cleared, the low-speed on-chip oscillator clock (no division) is used as the system clock.

9.4.3 CPU Clock (fs)

The CPU clock can be obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32 for CPU operation. The frequency division ratio for the system clock is set by bits PHISSEL0 to PHISSEL2 in the SCKCR register. After a reset is cleared, the low-speed on-chip oscillator clock (no division) will be the CPU clock.

9.4.4 Various Clocks

Table 9.8 lists the Names and Descriptions of Various Clocks that can be generated in the clock generation circuit.

Table 9.8 Names and Descriptions of Various Clocks

Clock Name	Description
Peripheral function clocks f1 to f128	Clocks for the peripheral functions. These clocks are generated by dividing the system clock. They are used in timer RJ2, timer RB2, timer RC, UART0, or the A/D converter. The peripheral function clocks are stopped when wait mode is entered after the WCKSTP bit in the CKSTPR register is set to 1 (system clock stopped in wait mode).
fHOCO	fHOCO is generated by the high-speed on-chip oscillator, and oscillates when the HOCOE bit in the OCOCR register is set to 1. fHOCO is not stopped in wait mode.
fLOCO	fLOCO is generated by the low-speed on-chip oscillator, and oscillates when the LOCODIS bit in the OCOCR register is set to 0. fLOCO is not stopped in wait mode.
fHSCK	fHSCK is selected from the XIN clock or high-speed on-chip oscillator clock using the HSCKSEL bit in the SCKCR register.
fAD	A clock for the A/D converter. This clock is obtained by dividing the system clock. fAD is not stopped in wait mode.

9.4.5 Prescaler

The prescaler is a 13-bit counter that uses the system clock as an input clock. The divided output is used as the internal clock for the on-chip peripheral functions. The prescaler starts operating when the PSCSTP bit in the CKSTPR register is set to 0 (prescaler operates).
The prescaler is stopped when wait mode is entered after the WCKSTP bit in the CKSTPR register is set to 1 (system clock stopped in wait mode). If the clock is switched by the WAITRS bit in the CKRSCR register when a transition is made from wait mode to standard mode, the prescaler is initialized. When a transition is made from stop mode to standard mode, the prescaler is initialized. The prescaler cannot be read or written.

9.4.6 Procedure for Switching System Base Clock

Figure 9.4 shows the Flowchart for Clock Switching between XIN Clock Oscillation Circuit, Low-Speed On-Chip Oscillator, and High-Speed On-Chip Oscillator.

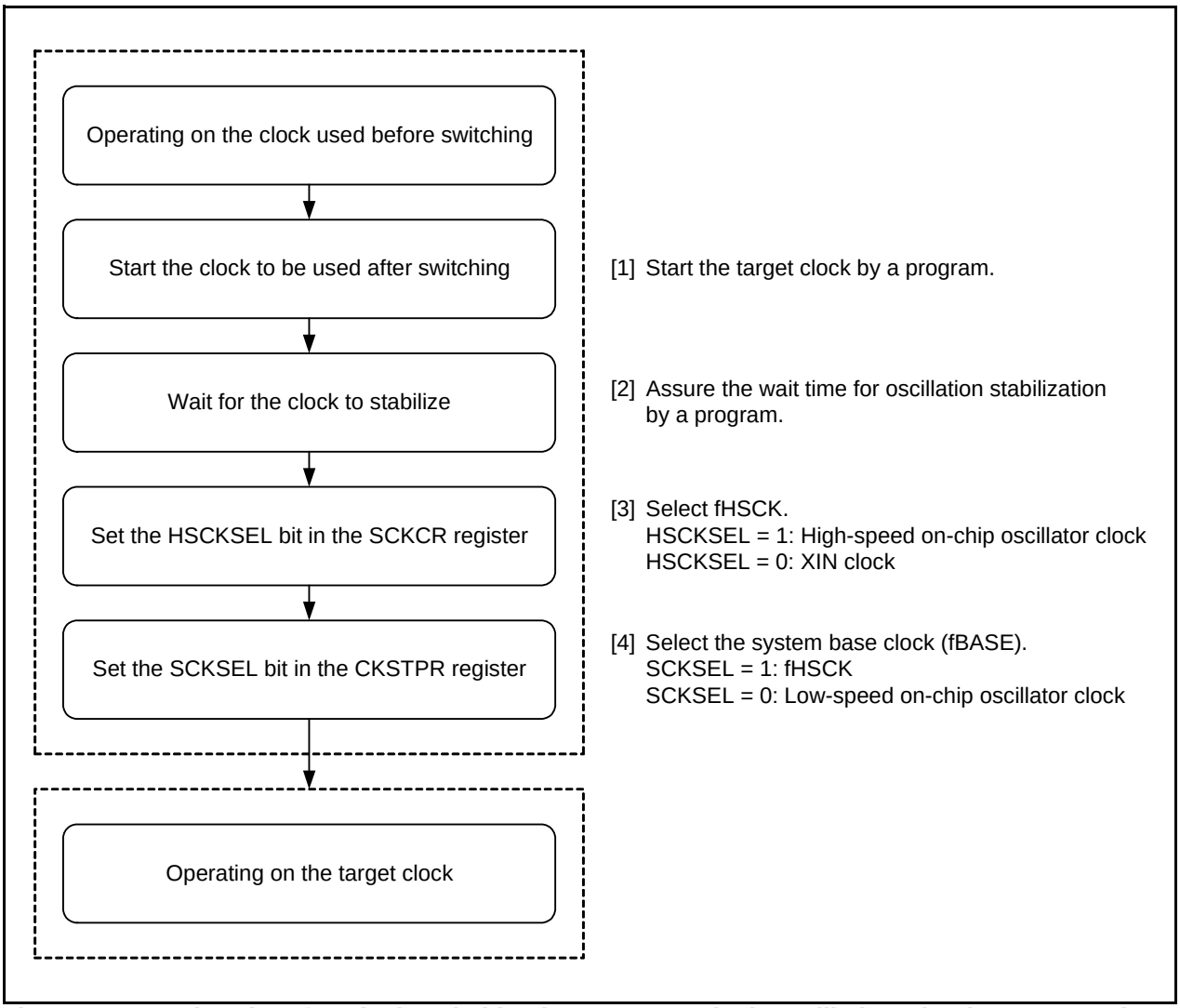


Figure 9.4 Flowchart for Clock Switching between XIN Clock Oscillation Circuit, Low-Speed On-Chip Oscillator, and High-Speed On-Chip Oscillator

9.4.6.1 Procedure for Switching System Base Clock to High-Speed On-Chip Oscillator

Figure 9.5 shows the Flowchart for Switching from Low-Speed On-Chip Oscillator to High-Speed On-Chip Oscillator Clock.

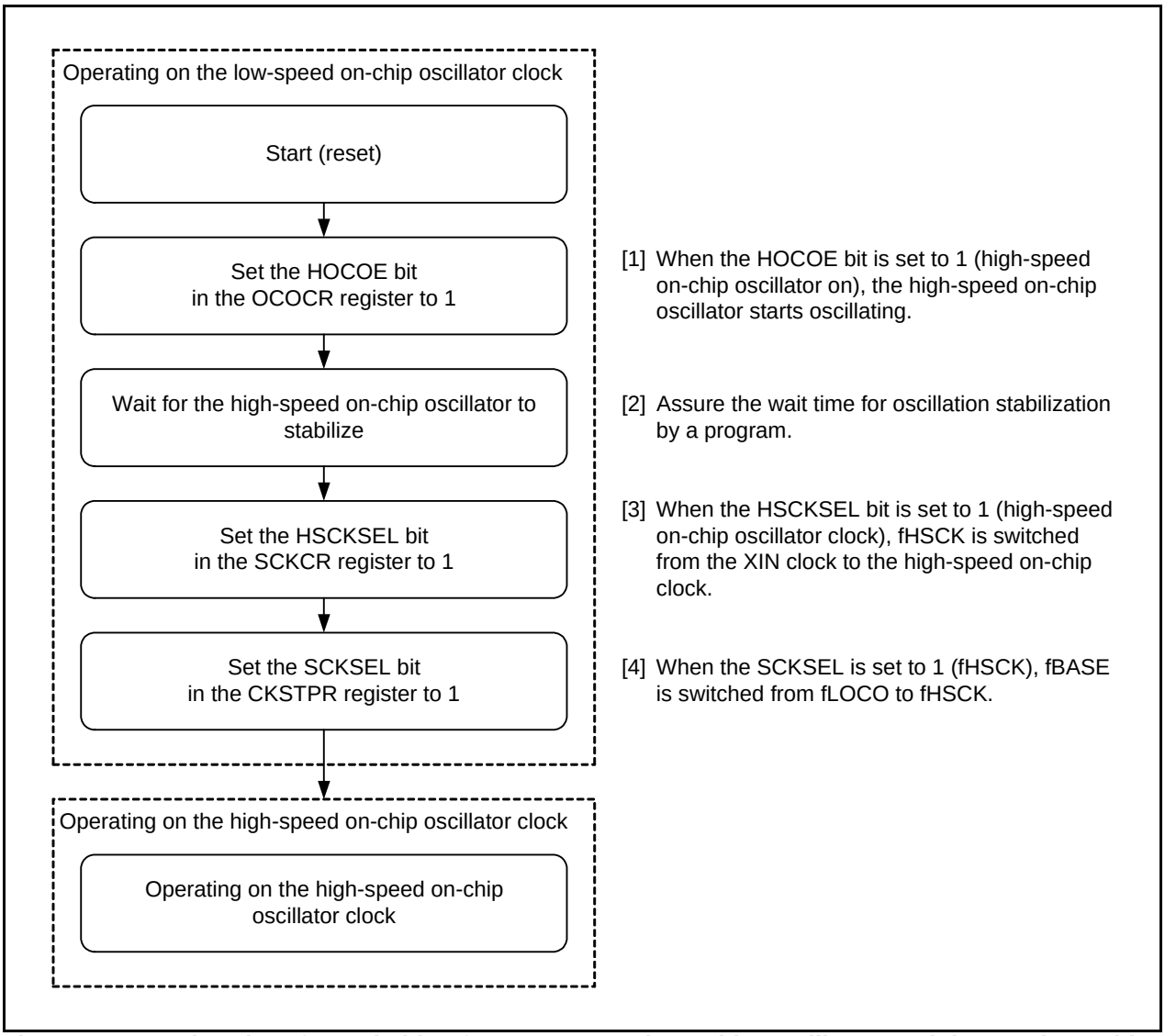


Figure 9.5 Flowchart for Switching from Low-Speed On-Chip Oscillator to High-Speed On-Chip Oscillator Clock

9.4.6.2 Procedure for Switching System Base Clock to XIN Clock

Figure 9.6 shows the Flowchart for Switching from Low-Speed On-Chip Oscillator to XIN Clock.

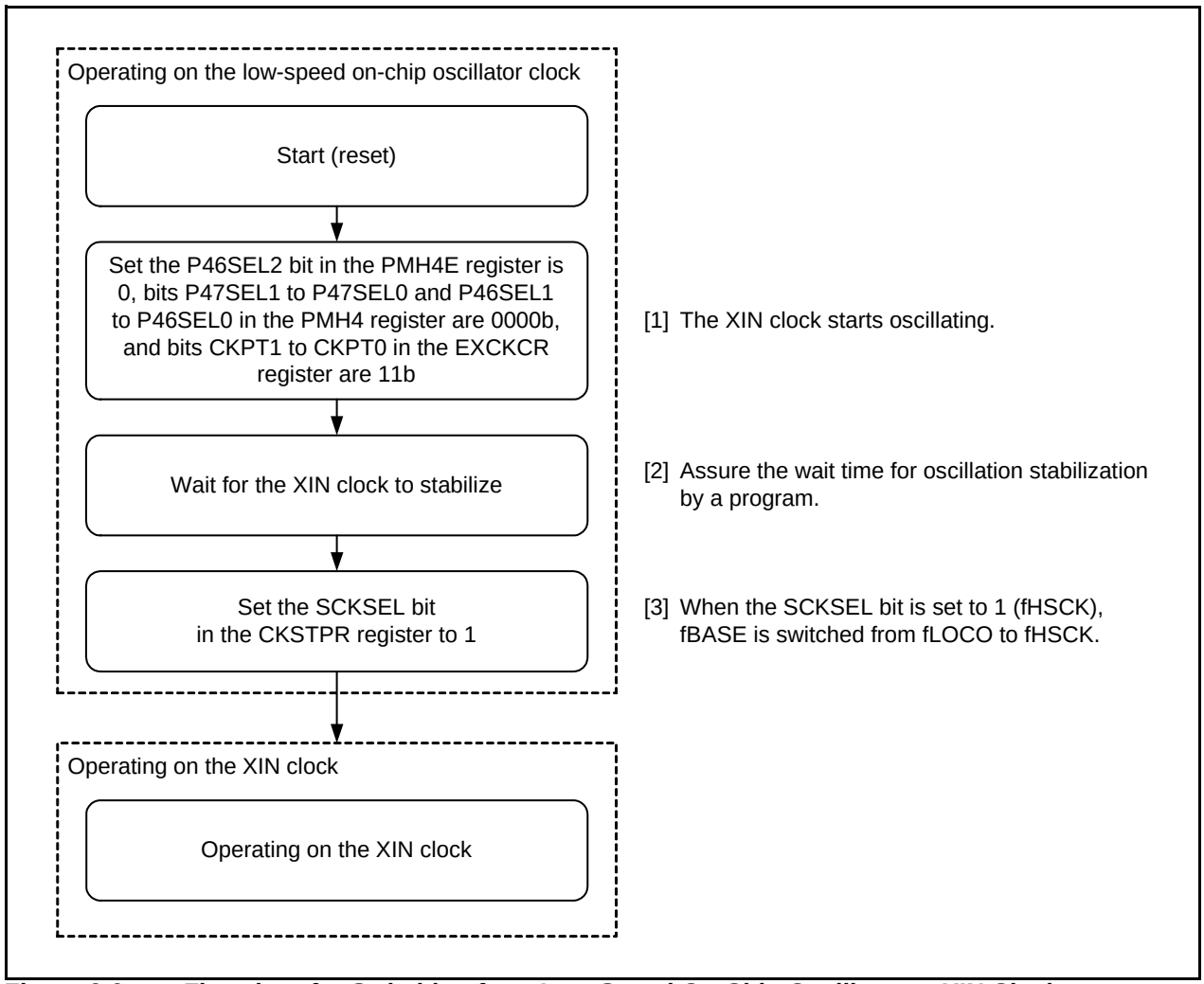


Figure 9.6 Flowchart for Switching from Low-Speed On-Chip Oscillator to XIN Clock

9.5 Oscillation Stop Detection Function

The oscillation stop detection function is used to detect whether the XIN clock oscillation is stopped.
Whether this function is enabled can be selected by the XINBAKE bit in the BAKCR register.
Table 9.9 lists the Oscillation Stop Detection Function Specifications.
When the XIN clock is selected as the system base clock and bits CKSWIE to XINBAKE in the BAKCR register are set to 11b (interrupt enabled, oscillation stop detection function enabled), if the XIN clock is stopped, the states will change as follows:

- The low-speed on-chip oscillator oscillates. However, the value in the LOCODIS bit in the OCOCR register does not change.
- The SCKSEL bit in the CKSTPR register = 0 (fLOCO)
- The XINHALT bit in the BAKCR register = 0 (XIN clock halted)
- An oscillation stop detection interrupt is generated.

Table 9.9 Oscillation Stop Detection Function Specifications

Item	Specification
Clock frequency range for oscillation stop detection	f(XIN) ≥ 2 MHz
Condition for enabling the oscillation stop detection function	Set bits CKSWIE through XINBAKE to 11b (interrupt enabled, oscillation stop detection function enabled).
Operation at oscillation stop detection	An oscillation stop detection interrupt is generated.

9.5.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the watchdog timer and voltage monitor 1 interrupts. To use both the oscillation stop detection and watchdog timer interrupts, the interrupt source needs to be determined. See **11.8 How to Determine Interrupt Sources** for how to determine interrupt sources.
- When the XIN clock starts oscillating after oscillation is stopped, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.6 shows the Flowchart for Switching from Low-Speed On-Chip Oscillator to XIN Clock.
- The oscillation stop detection function can stop the XIN clock by an external cause. In that case, set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt disabled, oscillation stop detection function disabled) to stop or oscillate the XIN clock by a program (to select stop mode or change bits CKPT0 to CKPT1 in the EXCKCR register).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt disabled, oscillation stop detection function disabled).
- After the oscillation stop is detected, the low-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral functions. To reduce power consumption, the low-speed on-chip oscillator can be set to stop while the oscillation stop detection function is enabled. In that case, allow the low-speed on-chip oscillator to automatically oscillate when the stop of the XIN clock is detected, then switch the system clock after the wait time for oscillation stabilization.

9.6 Notes on Clock Generation Circuit

9.6.1 Oscillation Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, so set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt disabled, oscillation stop detection function disabled).

9.6.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Power Control

Power control refers to controlling power consumption by selecting or stopping the CPU clock and the peripheral function clocks.

10.1 Overview

There are three power control modes. Standard operating mode is further divided into three modes depending on the system base clock (fBASE).

Table 10.1 Types of Modes

Item		Description	
Standard operating mode		The CPU and the peripheral functions operate.	
	High-speed clock mode	System base clock (fBASE)	XIN clock
	High-speed on-chip oscillator mode		High-speed on-chip oscillator clock
	Low-speed on-chip oscillator mode		Low-speed on-chip oscillator clock
Wait mode		The CPU is stopped and the peripheral functions operate.	
Stop mode		The CPU and the peripheral functions are stopped, and power consumption is lowest.	

Figure 10.1 shows the Power Control State Transition Diagram.

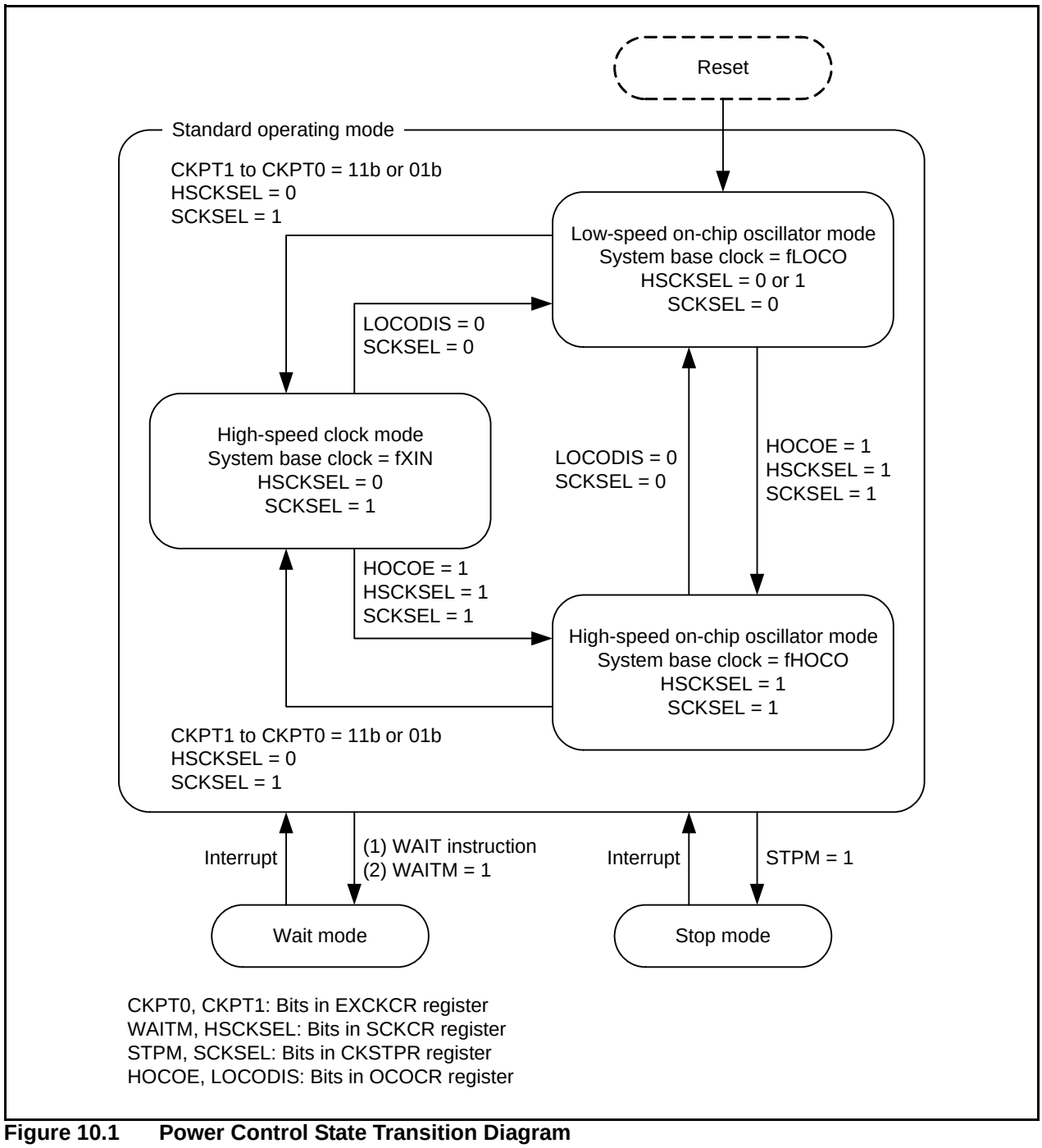


Figure 10.1 Power Control State Transition Diagram

10.2 Standard Operating Mode

In standard operating mode, the system clock is supplied to operate the CPU and the peripheral functions. Power consumption control is implemented by controlling the frequency of the system clock or CPU clock.
The higher the CPU clock frequency, the higher processing power. The lower the CPU clock frequency, the lower the power consumption. Stopping unnecessary oscillation circuits will further reduce power consumption.
When the clock sources for the CPU clock are switched, the new clock needs to be oscillating and stable. Assure the wait time for the new clock oscillation to stabilize by a program before switching the clocks.
Table 10.2 lists the Register Settings in Standard Operating Mode.

Table 10.2 Register Settings in Standard Operating Mode

Mode	Register	OCOCR		SCKCR	CKSTPR	EXCKCR	
	Bit	HOCOE	LOCODIS	HSCKSEL	SCKSEL	CKPT1	CKPT0
	Content to be Switched	fHOCO Oscillate/Stop	fLOCO Oscillate/Stop	XIN/fHOCO	fLOCO/ fHSCK	P4_6 and P4_7 Pin Function	
High-speed clock mode		—	—	0 (XIN)	1 (fHSCK)	1	1
High-speed on-chip oscillator mode		1 (oscillate)	—	1 (fHOCO)	1 (fHSCK)	—	—
Low-speed on-chip oscillator mode		—	0 (oscillate)	—	0 (fLOCO)	—	—

—: Indicates that either 0 or 1 can be set.
The setting in ( ) is selected.

10.2.1 High-Speed Clock Mode

When the HSCKSEL bit in the SCKCR register is 0 (XIN clock) and the SCKSEL bit in the CKSTPR register is 1 (fHSCK), the XIN clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the XIN clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fHOCO can be used as the peripheral function clock when the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on), and fLOCO when the LOCODIS bit is 0 (low-speed on-chip oscillator on).

10.2.2 High-Speed On-Chip Oscillator Mode

When the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on), the HSCKSEL bit in the SCKCR register is 1 (high-speed on-chip oscillator clock), and the SCKSEL bit in the CKSTPR register is 1 (fHSCK), the high-speed on-chip oscillator clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the high-speed on-chip oscillator clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fLOCO can be used as the peripheral function clock when the LOCODIS bit is 0 (low-speed on-chip oscillator on).

10.2.3 Low-Speed On-Chip Oscillator Mode

When the LOCODIS bit in the OCOCR register is 0 (low-speed on-chip oscillator on) and the SCKSEL bit in the CKSTPR register is 0 (fLOCO), the low-speed on-chip oscillator clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the low-speed on-chip oscillator clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fHOCO can be used as the peripheral function clock when the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on).

In this mode, low-power operation can be enabled by stopping the XIN clock and the high-speed on-chip oscillator and setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). Furthermore, if wait mode is entered from this mode, power consumption in wait mode can be reduced even further by setting the VCA2 register LPE bit to 1 (low-power-consumption wait mode enabled).

For details on how to reduce power consumption, see **10.5 Reducing Power Consumption**.

10.3 Wait Mode

The watchdog timer is stopped when count source protection mode is disabled and the CPU clock is used. The XIN clock and the high-speed/low-speed on-chip oscillator clock are not stopped, so the peripheral functions that use these clocks continue operating. The system clock can be stopped with WCKSTP bit in the CKSTPR register. At this time, the peripheral functions that use the system clock and a divided system clock generated by the prescaler are stopped.

10.3.1 Peripheral Function Clock Stop Function

When the WCKSTP bit in the CKSTPR register is 1 (peripheral function clock stopped in wait mode), the system clock and the prescaler are stopped in wait mode to reduce power consumption. At this time, the peripheral functions that use the system clock and a divided system clock generated by the prescaler are stopped.

10.3.2 Entering Wait Mode

Wait mode is entered when the WAIT instruction is executed or the WAITM bit in the SCKCR register is set to 1 (wait mode is entered).

10.3.3 Pin States in Wait Mode

The I/O ports retain the states immediately before wait mode is entered.

10.3.4 Returning from Wait Mode

A reset or a peripheral function interrupt is used to return from wait mode.
Peripheral function interrupts are affected by the WCKSTP bit in the CKSTPR register. When the WCKSTP bit is 0 (system clock is supplied in wait mode), the peripheral function interrupts can be used to return from wait mode. When the WCKSTP bit is 1 (system clock is stopped in wait mode), the peripheral functions that use the peripheral function clock are stopped. Only the peripheral function interrupts that operate using external signals, fAD, the high-speed on-chip oscillator clock, or the low-speed on-chip clock (oscillation of each oscillator is necessary) can be used to return from wait mode.
Table 10.3 lists the Interrupts Used to Return from Wait Mode and Usage Conditions.

Table 10.3 Interrupts Used to Return from Wait Mode and Usage Conditions

Interrupt	CKSTPR Register	
	When WCKSTP Bit = 0	When WCKSTP Bit = 1
Oscillation stop detection interrupt	Usable	Not usable.
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ interrupts	Usable	Usable without a filter.
Key input interrupt	Usable	Usable
Periodic timer interrupt	Usable when fLOCO/16 is selected as the count source.	Not usable.
Timer RJ2 interrupt	Usable in all modes.	• Usable without a filter in event counter mode. • Usable when fHOCO is selected as the count source.
Timer RB2 interrupt	Usable in all modes.	Usable when timer RJ2 is used without a filter in event mode and timer RJ2 is selected as the count source for timer RB2.
Timer RC interrupt	Usable in all modes.	Not usable.
Serial interface interrupt	Usable with an internal clock or external clock supplied.	Usable with an external clock supplied.
A/D conversion interrupt	Usable	Usable when the flash memory operates and fAD is selected as the A/D conversion clock.
Voltage monitor 1 interrupt	Usable	Usable
Comparator B1 interrupt	Usable	Usable without a filter.
Comparator B3 interrupt	Usable	Usable without a filter.

Figure 10.2 shows the Sequence from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed.
When a peripheral function interrupt is used to return from wait mode, the following items must be set before executing the WAIT instruction:

(1) Set the interrupt priority level in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in the interrupt priority level registers for the peripheral function interrupts that are used to return from wait mode. Also, set 00b (level 0 (interrupt disabled)) in bits ILVLi1 to ILVLi0 or bits ILVLi5 to ILVLi4 for the peripheral function interrupts that are not to be used to return from wait mode.
(2) Set the I flag to 1 (maskable interrupts enabled).
(3) Operate the peripheral functions to be used to return from wait mode.

The system base clock when returning from wait mode by a peripheral interrupt is the clock set by the WAITRS bit in the CKRSCR register. At this time, bits PHISSEL0 to PHISSEL2 in the SCKCR register and the SCKSEL bit in the CKSTPR register are automatically changed according to bits PHISRS and WAITRS.
If the system base clock when returning is different from the clock used immediately before entering wait mode, a period until the clock supply (oscillation stabilization time) is generated automatically. If the system base clock when returning is the high-speed on-chip oscillator clock, oscillation is started when an interrupt request is generated. If the system base clock is the XIN clock, set pins P4_6 and P4_7 to XIN oscillation by a program to start oscillation before entering wait mode.
Depending on the clock to be used, set appropriate values for oscillation stabilization time using bits CKST0 to CKST3 in the CKRSCR register. It is unnecessary to generate a wait time by a program. When returning from wait mode using the same clock as the one used immediately before entering the mode, no oscillation stabilization time is generated.

FMR0 Register FMSTP Bit	FMR1 Register WTFMSTP Bit	VCA2 Register LPE Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Clock Stabilization Time (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	1 (flash memory is stopped in wait mode)	0 (low-power-consumption wait mode disabled)	0 µs	60 µs (max.)	Set by bits CKST0 to CKST3 in the CKRSCR register if the clocks are switched when returning from wait mode 0 if the clocks are not switched when returning from wait mode	CPU clock period × 2 cycles	CPU clock period × 20 cycles	The total on the left amounts to the time from wait mode until execution of an interrupt routine.
		1 (low-power-consumption wait mode enabled)	100 µs (max.)					
1 (flash memory is stopped)	—	0 (low-power-consumption wait mode disabled)	0 µs	— (Flash memory is not activated)				
		1 (low-power-consumption wait mode enabled)	100 µs (max.)					
0 (flash memory operates)	0 (flash memory operates in wait mode)	0 (low-power-consumption wait mode disabled)	0 µs					
		1 (low-power-consumption wait mode enabled)	—					Setting prohibited

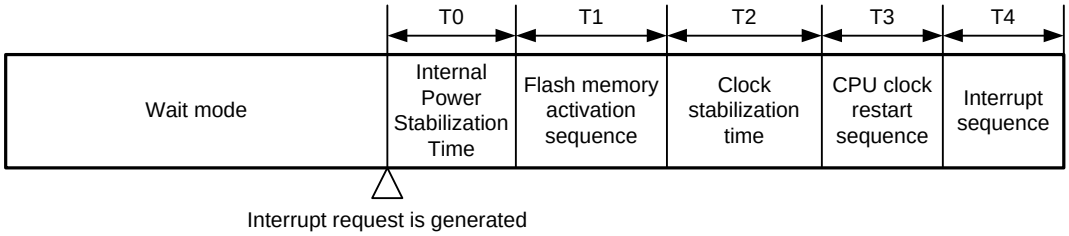


Figure 10.2 Sequence from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

Figure 10.3 shows the Time from Wait Mode to First Instruction Execution after Exit after WAITM Bit in SCKCR Register is Set to 1 (Wait Mode is Entered).
When a peripheral function interrupt is used to return from wait mode, the following items must be set before setting the WAITM bit to 1:

(1) Set the I flag to 0 (maskable interrupt disabled).
(2) Set the interrupt priority level in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in the interrupt priority level registers for the peripheral function interrupts that are used to return from wait mode. Also, set 00b (level 0 (interrupt disabled)) in bits ILVLi1 to ILVLi0 or bits ILVLi5 to ILVLi4 for the peripheral function interrupts that are not to be used to return from wait mode.
(3) Operate the peripheral functions to be used to return from wait mode.

If the MCU returns from wait mode without executing any interrupt for external interrupts ($\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$), bits IRI0 to IRI3 and IRKI in the IRR3 register are not changed automatically. Set these bits to 0 by a program.

The system base clock when returning from wait mode by a peripheral interrupt is the clock set by the WAITRS bit in the CKRSCR register. At this time, bits PHISSEL0 to PHISSEL2 in the SCKCR register and the SCKSEL bit in the CKSTPR register are automatically changed according to bits PHISRS and WAITRS.
If the system base clock when returning is different from the clock used immediately before entering wait mode, a period until the clock supply (oscillation stabilization time) is generated automatically. If the system base clock when returning is the high-speed on-chip oscillator clock, oscillation is started when an interrupt request is generated. If the system base clock is the XIN clock, set pins P4_6 and P4_7 to XIN oscillation by a program to start oscillation before entering wait mode.
Depending on the clock to be used, set appropriate values for oscillation stabilization time using bits CKST0 to CKST3 in the CKRSCR register. It is unnecessary to generate a wait time by a program. When returning from wait mode using the same clock as the one used immediately before entering the mode, no oscillation stabilization time is generated.

FMR0 Register	FMR1 Register	VCA2 Register	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Clock Stabilization Time (T2)	Time until CPU Clock Supply (T3)	Remarks
FMSTP Bit	WTFMSTP Bit	LPE Bit					
0 (flash memory operates)	1 (flash memory is stopped in wait mode)	0 (low-power-consumption wait mode disabled)	0 μs	60 μs (max.)	Set by bits CKST0 to CKST3 in the CKRSCR register if the clocks are switched when returning from wait mode 0 if the clocks are not switched when returning from wait mode	CPU clock period × 2 cycles	The total on the left amounts to the time from wait mode until execution of an interrupt routine.
		1 (low-power-consumption wait mode enabled)	100 μs (max.)				
1 (flash memory is stopped)	—	0 (low-power-consumption wait mode disabled)	0 μs	— (Flash memory is not activated)			
		1 (low-power-consumption wait mode enabled)	100 μs (max.)				
0 (flash memory operates)	0 (flash memory operates in wait mode)	0 (low-power-consumption wait mode disabled)	0 μs				
		1 (low-power-consumption wait mode enabled)	—				Setting prohibited

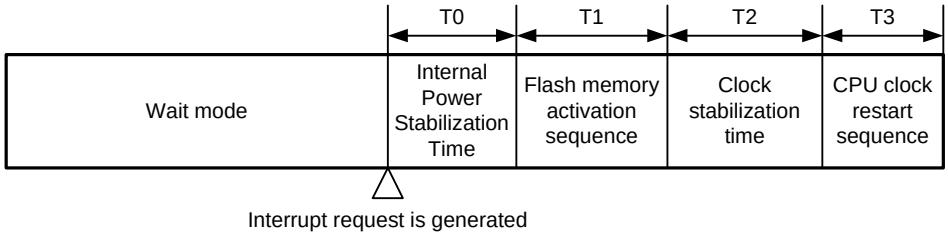


Figure 10.3 Time from Wait Mode to First Instruction Execution after Exit after WAITM Bit in SCKCR Register is Set to 1 (Wait Mode is Entered)

10.4 Stop Mode

All oscillations are stopped in stop mode. Thus, the CPU clock and the peripheral function clock are stopped and the CPU and the peripheral functions that operate using these clocks are stopped. However, when the low-speed on-chip oscillator is selected as the count source for the watchdog timer (in count source protection mode or when bits WDTC7 to WDTC6 in the WDTC register are set to 11b (division of low-speed on-chip oscillator by 16)), the low-speed on-chip oscillator oscillates.
Power consumption is lowest compared to other modes. When the voltage applied to the VCC pin is VRAM or above, the content of the internal RAM is retained.

10.4.1 Entering Stop Mode

Stop mode is entered when the STPM bit in the CKSTPR register is set to 1 (all clocks are stopped (stop mode)).

10.4.2 Pin States in Stop Mode

The I/O ports retain the states immediately before stop mode is entered.
If bits CKPT1 to CKPT0 in the EXCKCR register are 11b (P4_6: XIN and P4_7: XOUT), pins XIN (P4_6) and XOUT (P4_7) become the high-impedance state. If bits CKPT1 to CKPT0 in the EXCKCR register are 01b (XIN clock input), do not use stop mode.

10.4.3 Returning from Stop Mode

A reset or a peripheral function interrupt is used to return from stop mode.
Table 10.4 lists the Interrupts Used to Return from Stop Mode and Usage Conditions.

Table 10.4 Interrupts Used to Return from Stop Mode and Usage Conditions

Interrupt	Usage Condition
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ interrupts	Usable without a filter.
Key input interrupt	Usable
Timer RJ2 interrupt	Usable when an external pulse is counted without a filter in event counter mode.
Timer RB2 interrupt	Usable when timer RJ2 is used without a filter in event counter mode and timer RJ2 underflow is selected as the count source for timer RB2.
Serial interface interrupt	Usable with an external clock supplied.
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (when the VW1C1 bit in the VW1C register is 1).
Comparator B1 interrupt	Usable without a filter.
Comparator B3 interrupt	Usable without a filter.

Figure 10.4 shows the Sequence from Stop Mode to Interrupt Routine Execution.
When a peripheral function interrupt is used to return from stop mode, the following items must be set before setting the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)):

(1) Set the interrupt priority level in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in the interrupt priority level registers for the peripheral function interrupts that are used to return from stop mode. Also, set 00b (level 0 (interrupt disabled)) in bits ILVLi1 to ILVLi0 or bits ILVLi5 to ILVLi4 for the peripheral function interrupts that are not to be used to return from stop mode.
(2) Set the I flag to 1 (maskable interrupt enabled).
(3) Operate the peripheral function to be used to return from stop mode.

The system base clock when returning from stop mode by a peripheral interrupt is the clock set by the STOPRS bit in the CKRSCR register. At this time, bits PHISSEL0 to PHISSEL2 in the SCKCR register and the SCKSEL bit in the CKSTPR register are automatically changed according to bits PHISRS and STOPRS.
When an interrupt is generated, oscillation is started, and a period until the clock supply (oscillation stabilization time) is generated automatically. If the system base clock when returning is the XIN clock, set pins P4_6 and P4_7 to XIN oscillation by a program before entering stop mode.
Depending on the clock to be used, set appropriate values for oscillation stabilization time using bits CKST0 to CKST3 in the CKRSCR register. It is unnecessary to generate a wait time by a program.

FMR0 Register FMSTP bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Clock Stabilization Time (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 μs (max.)	60 μs (max.)	Set by bits CKST0 to CKST3 in the CKRSCR register	CPU clock period × 2 cycles	CPU clock period × 20 cycles	The total on the left amounts to the time from stop mode to execution of an interrupt routine.
1 (flash memory is stopped)	100 μs (max.)	— (Flash memory is not activated)				

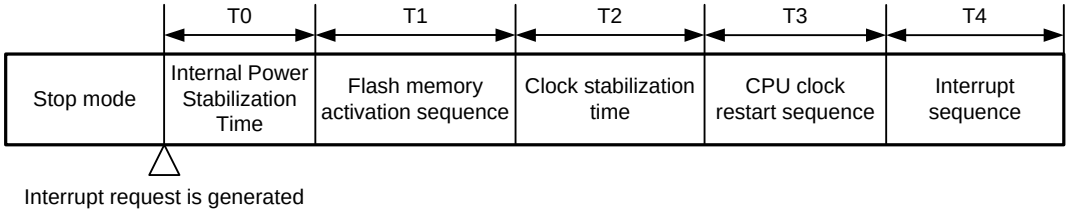


Figure 10.4 Sequence from Stop Mode to Interrupt Routine Execution

10.5 Reducing Power Consumption

The following describes key points and processing methods for reducing power consumption. They should be referred to when designing a system or creating a program.

10.5.1 Voltage Detection Circuit

When voltage monitor 1 is not used, set the VC1E bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). When power-on reset or voltage monitor 0 reset is not used, set the VC0E bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

10.5.2 Ports

Even after entering wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state. Shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before entering wait mode or stop mode.

10.5.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases. Unnecessary clocks should be stopped accordingly.

Stopping low-speed on-chip oscillator oscillation: LOCODIS bit in OCOCR register
Stopping high-speed on-chip oscillator oscillation: HOCOE bit in OCOCR register

10.5.4 Wait Mode and Stop Mode

Power consumption can be reduced in wait mode and stop mode.

10.5.5 Stopping Peripheral Function Clocks

If the peripheral function clocks f1 to f128 are not necessary, set the PSCSTP bit in the CKSTPR register to 1 to stop these peripheral function clocks. If the peripheral function clocks f1 to f128 are not necessary in wait mode, set the WCKSTP bit in the CKSTPR register to 1 to stop the system clock in wait mode.

10.5.6 Timers

When timer RJ2 is not used, set the TCKCUT bit in the TRJMR register to 1 (count source cutoff). Or set the MSTTRJ bit in the MSTCR register to 1 (standby).
When timer RB2 is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff). Or set the MSTTRB bit in the MSTCR register to 1 (standby).
When timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).

10.5.7 A/D Converter

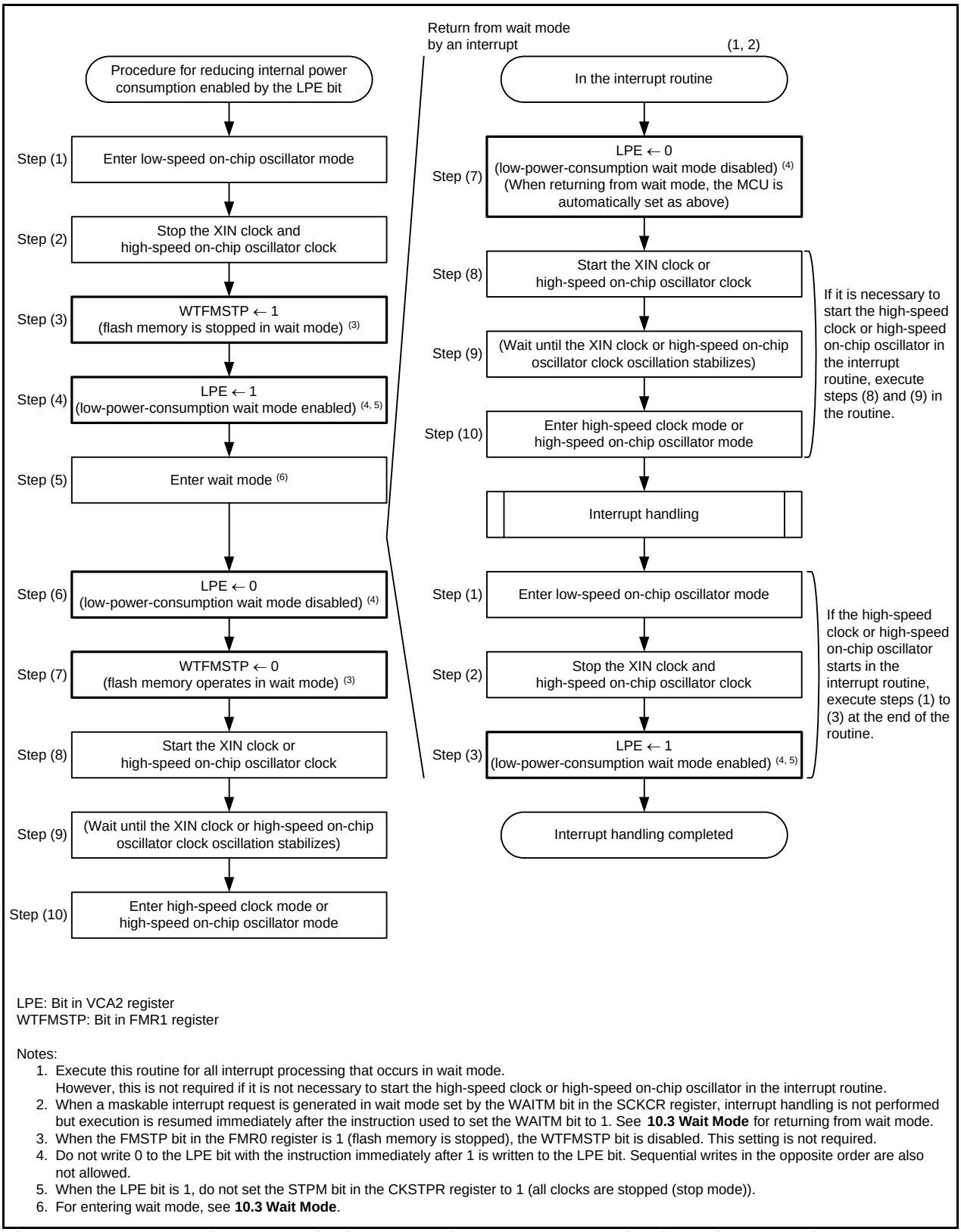
When the A/D converter is not used, set the MSTAD bit in the MSTCR register to 1 (standby).

10.5.8 Serial Interface (UART0)

When the serial interface (UART0) is not used, set the MSTUART bit in the MSTCR register to 1 (standby).

10.5.9 Reducing Internal Power Consumption

When entering wait mode using low-speed on-chip clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced using the LPE bit in the VCA2 register. To enable low internal power consumption using the LPE bit, follow **Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit**.



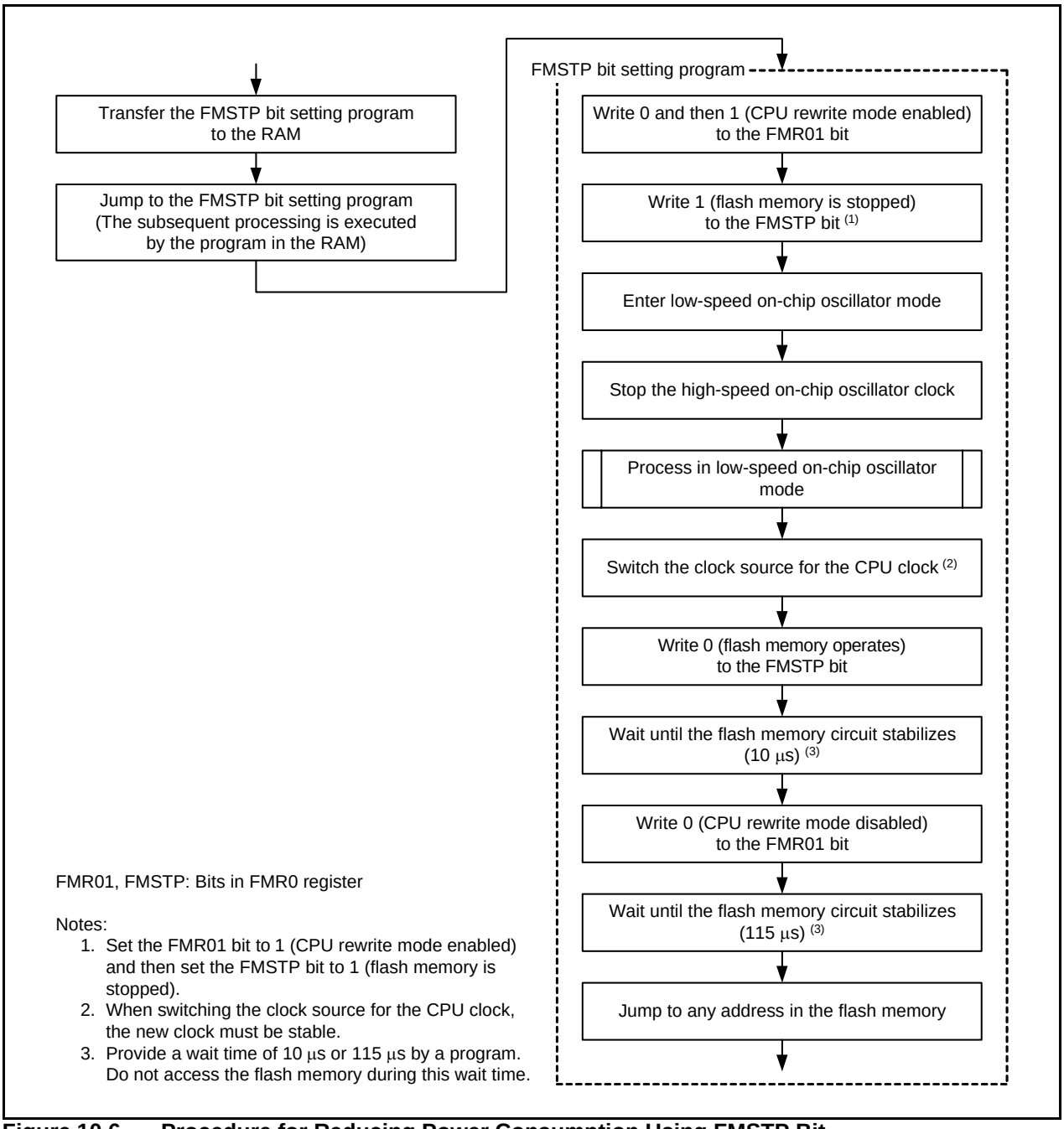
LPE: Bit in VCA2 register
WTFMSTP: Bit in FMR1 register

Notes:
1. Execute this routine for all interrupt processing that occurs in wait mode.
   However, this is not required if it is not necessary to start the high-speed clock or high-speed on-chip oscillator in the interrupt routine.
2. When a maskable interrupt request is generated in wait mode set by the WAITM bit in the SCKCR register, interrupt handling is not performed but execution is resumed immediately after the instruction used to set the WAITM bit to 1. See **10.3 Wait Mode** for returning from wait mode.
3. When the FMSTP bit in the FMR0 register is 1 (flash memory is stopped), the WTFMSTP bit is disabled. This setting is not required.
4. Do not write 0 to the LPE bit with the instruction immediately after 1 is written to the LPE bit. Sequential writes in the opposite order are also not allowed.
5. When the LPE bit is 1, do not set the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)).
6. For entering wait mode, see **10.3 Wait Mode**.

Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit

10.5.10 Stopping Flash Memory

In low-speed on-chip oscillator mode, the flash memory can be stopped using the FMSTP bit in the FMR0 register to further reduce the power consumption.
When the FMSTP bit is set to 1 (flash memory is stopped), the flash memory cannot be accessed. The FMSTP bit must be written by a program that has been transferred to the RAM.
When the MCU enters stop mode or wait mode with CPU rewrite mode disabled, the power supply for the flash memory is automatically turned off. It is turned on again when MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.
Figure 10.6 shows the Procedure for Reducing Power Consumption Using FMSTP Bit.



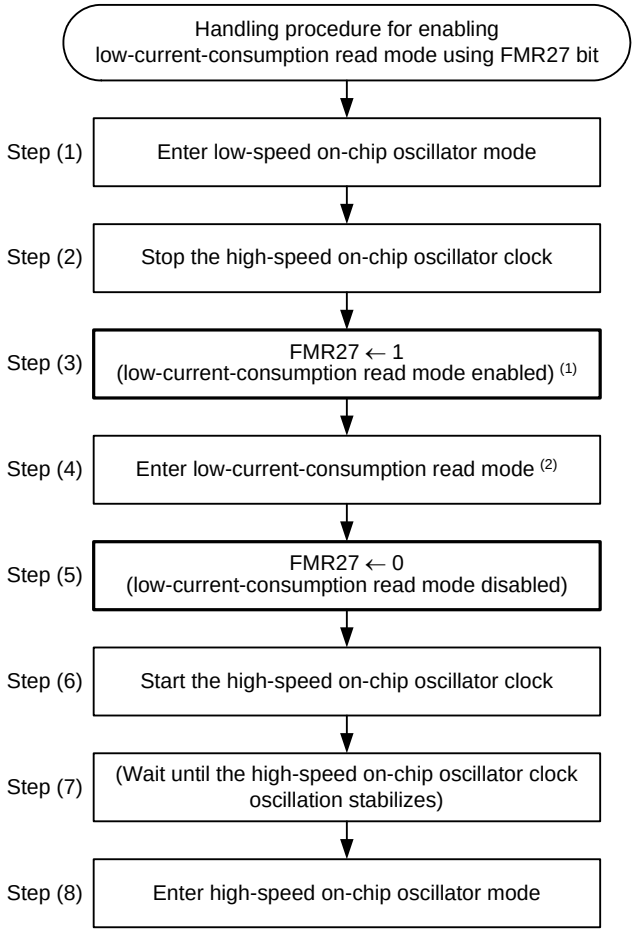
FMR01, FMSTP: Bits in FMR0 register

Notes:
1. Set the FMR01 bit to 1 (CPU rewrite mode enabled) and then set the FMSTP bit to 1 (flash memory is stopped).
2. When switching the clock source for the CPU clock, the new clock must be stable.
3. Provide a wait time of 10 µs or 115 µs by a program. Do not access the flash memory during this wait time.

Figure 10.6 Procedure for Reducing Power Consumption Using FMSTP Bit

10.5.11 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Set the CPU clock (fs) to a frequency in the range of 3 kHz to 50 kHz.
Figure 10.7 shows the Procedure for Using Low-Current-Consumption Read Mode.



FMR27: Bit in FMR2 register

Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

Figure 10.7 Procedure for Using Low-Current-Consumption Read Mode

10.6 Notes on Power Control

10.6.1 Program Restrictions When Entering Wait Mode

To enter wait mode by setting the WAITM bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the WAITM bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction. The 4 bytes of instruction data following the instruction that sets the WAITM bit to 1 (wait mode is entered) or the WAIT instruction are prefetched from the instruction queue and then the program stops. Insert at least four NOP instructions after the instruction that sets the WAITM bit to 1 (wait mode is entered) or after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        FSET    I               ; Interrupt enabled
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to set the WAITM bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to the SCKCR register enabled
        FCLR    I               ; Interrupt disabled
        BSET    5, SCKCR        ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to the SCKCR register disabled
        FSET    I               ; Interrupt enabled
```

10.6.2 Program Restrictions When Entering Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)). The 4 bytes of instruction data following the instruction that sets the STPM bit to 1 are prefetched from the instruction queue and then the program stops.
Insert at least four NOP instructions following the JMP.B instruction immediately after the instruction that sets the STPM bit to 1.

• Program example to enter stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CKSTPR register enabled
        FSET    I               ; Interrupt enabled
        BSET    0, CKSTPR       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

11. Interrupts

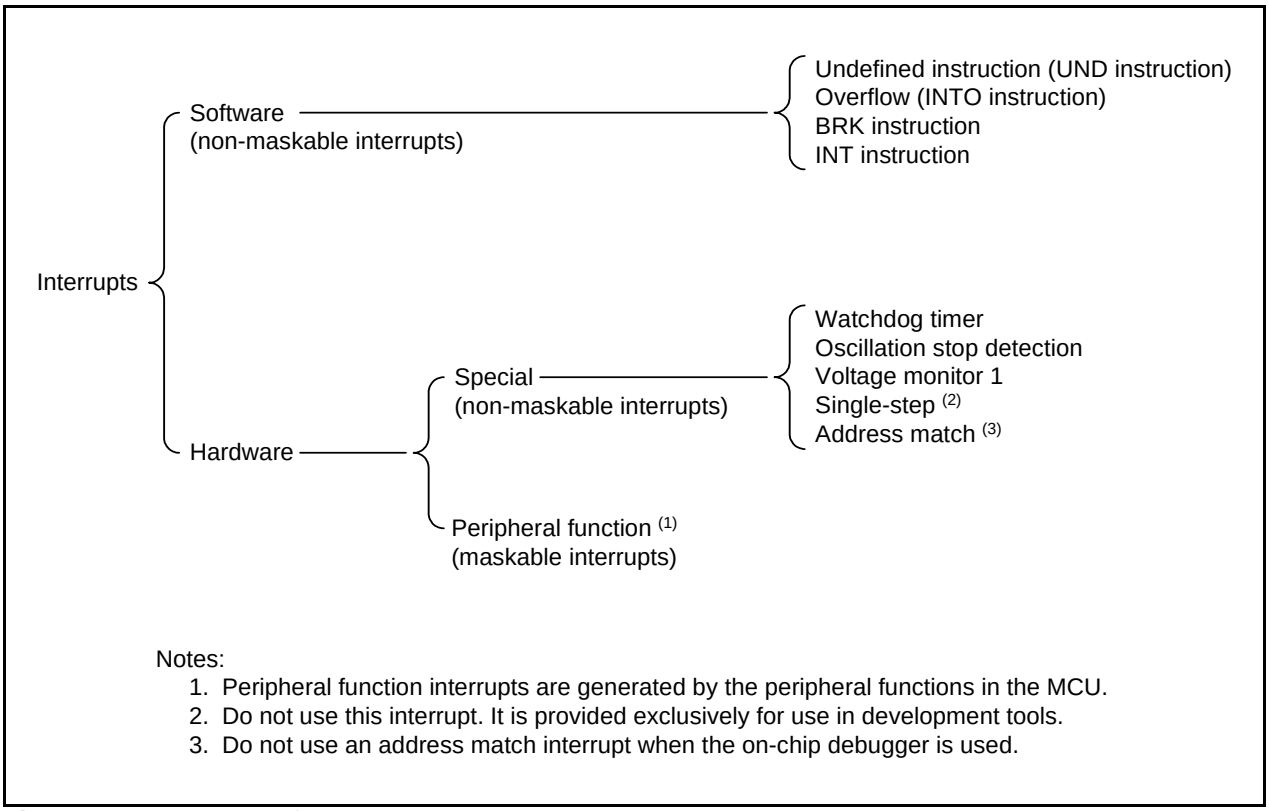
11.1 Overview

Interrupts are classified into non-maskable and maskable interrupts. These differ in whether or not the interrupt can be enabled or disabled by an interrupt enable flag (I flag) and in whether or not the interrupt priority level can be changed as listed in Table 11.1.

Table 11.1 Maskable/Non-Maskable Interrupts

	Disabling Interrupt by Interrupt Enable Flag (I Flag)	Changing Priority by Setting Interrupt Priority Level
Non-maskable interrupts	Not possible	Not possible
Maskable interrupts	Possible	Possible

Figure 11.1 shows the Types of Interrupts. Table 11.2 lists the Descriptions of Interrupts.



Notes:
1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. Do not use this interrupt. It is provided exclusively for use in development tools.
3. Do not use an address match interrupt when the on-chip debugger is used.

Figure 11.1 Types of Interrupts

Table 11.2 Descriptions of Interrupts

Interrupt	Description
Undefined instruction interrupt	An unidentified instruction interrupt is generated when the UND instruction is executed.
Overflow interrupt	An overflow interrupt is generated when the O flag is 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that change the O flag are as follows: ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.
BRK instruction interrupt	A BRK interrupt is generated when the BRK instruction is executed.
INT instruction interrupt	An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers the INT instruction can specify are 0 to 63. The number is assigned to each peripheral function interrupt. When the INT instruction is executed specifying the number, the peripheral function interrupt with the same number can be executed. For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution, and the U flag is set to 0 (ISP) before the interrupt sequence is executed. The U flag is restored from the stack when the MCU returns from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.
Watchdog timer interrupt	This interrupt is generated by the watchdog timer. For details, see **8. Watchdog Timer**.
Oscillation stop detection interrupt	This interrupt is generated by the oscillation stop detection function. For details on the oscillation stop detection function, see **9. Clock Generation Circuit**.
Voltage monitor 1 interrupt	This interrupt is generated by the voltage detection circuit. For details on the voltage detection circuit, see **7. Voltage Detection Circuit**.
Single-step interrupt	Do not use this interrupt. It is provided exclusively for use in development tools.
Address match interrupt	When one of the AIENi0 bit (i = 0 or 1) in the AIENi register is 1 (enabled), an address match interrupt is generated immediately before executing the instruction that is stored at an address indicated by the corresponding AIADRi register (i = 0 or 1). For details on the address match interrupt, see **11.7 Address Match Interrupt**.
Peripheral function interrupt	A peripheral function interrupt is generated by a peripheral function in the MCU. For the interrupt sources for the corresponding peripheral function interrupt, see the interrupts and the vector table addresses as listed in **Table 11.6 Relocatable Vector Table**. For details on the peripheral functions, see the descriptions of individual peripheral functions.

11.2 Registers

Table 11.3 lists the Register Configuration for Interrupts.

Table 11.3 Register Configuration for Interrupts

Register Name	Symbol	After Reset	Address	Access Size
External Input Enable Register	INTEN	00h	00038h	8
INT Input Filter Select Register 0	INTF0	00h	0003Ah	8
INT Input Edge Select Register 0	ISCR0	00h	0003Ch	8
Key Input Enable Register	KIEN	00h	0003Eh	8
Interrupt Priority Level Register 0	ILVL0	00h	00040h	8
Interrupt Priority Level Register 2	ILVL2	00h	00042h	8
Interrupt Priority Level Register 3	ILVL3	00h	00043h	8
Interrupt Priority Level Register 4	ILVL4	00h	00044h	8
Interrupt Priority Level Register 5	ILVL5	00h	00045h	8
Interrupt Priority Level Register 6	ILVL6	00h	00046h	8
Interrupt Priority Level Register 7	ILVL7	00h	00047h	8
Interrupt Priority Level Register 8	ILVL8	00h	00048h	8
Interrupt Priority Level Register 9	ILVL9	00h	00049h	8
Interrupt Priority Level Register A	ILVLA	00h	0004Ah	8
Interrupt Priority Level Register B	ILVLB	00h	0004Bh	8
Interrupt Priority Level Register C	ILVLC	00h	0004Ch	8
Interrupt Priority Level Register D	ILVLD	00h	0004Dh	8
Interrupt Priority Level Register E	ILVLE	00h	0004Eh	8
Interrupt Monitor Flag Register 0	IRR0	00h	00050h	8
Interrupt Monitor Flag Register 1	IRR1	00h	00051h	8
Interrupt Monitor Flag Register 2	IRR2	00h	00052h	8
External Interrupt Flag Register	IRR3	00h	00053h	8
Address Match Interrupt Register 0	AIADR0L	00h	001C0h	8
	AIADR0M	00h	001C1h	8
	AIADR0H	00h	001C2h	8
Address Match Interrupt Enable Register 0	AIEN0	00h	001C3h	8
Address Match Interrupt Register 1	AIADR1L	00h	001C4h	8
	AIADR1M	00h	001C5h	8
	AIADR1H	00h	001C6h	8
Address Match Interrupt Enable Register 1	AIEN1	00h	001C7h	8

11.2.1 External Input Enable Register (INTEN)

Address 00038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INT3EN	INT2EN	INT1EN	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit (1)	0: Disabled 1: Enabled	R/W
b1	INT1EN	$\overline{\text{INT1}}$ input enable bit (1)		R/W
b2	INT2EN	$\overline{\text{INT2}}$ input enable bit (1)		R/W
b3	INT3EN	$\overline{\text{INT3}}$ input enable bit (1)		R/W
b4	—	Reserved	Set to 0.	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—	Reserved	Set to 0.	R/W

Notes:
1. Changing the INTiEN bit (i = 0 to 3) may set the IRIi bit (i = 0 to 3) in the IRR3 register to 1 (interrupt requested). See **11.9.4 Rewriting Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN**.

11.2.2 INT Input Filter Select Register 0 (INTF0)

Address 0003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bits	b1 b0 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bits	b3 b2 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bits	b5 b4 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bits	b7 b6 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b7	INT3F1			R/W

11.2.3 INT Input Edge Select Register 0 (ISCR0)

Address 0003Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3SB	INT3SA	INT2SB	INT2SA	INT1SB	INT1SA	INT0SB	INT0SA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0SA	$\overline{\text{INT0}}$ input edge select bits (1)	b1 b0 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT0}}$ input 0 1: Interrupt request is generated on the rising edge of $\overline{\text{INT0}}$ input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT0}}$ input	R/W
b1	INT0SB			R/W
b2	INT1SA	$\overline{\text{INT1}}$ input edge select bits (1)	b3 b2 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT1}}$ input 0 1: Interrupt request is generated on the rising edge of INT1 input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT1}}$ input	R/W
b3	INT1SB			R/W
b4	INT2SA	$\overline{\text{INT2}}$ input edge select bits (1)	b5 b4 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT2}}$ input 0 1: Interrupt request is generated on the rising edge of INT2 input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT2}}$ input	R/W
b5	INT2SB			R/W
b6	INT3SA	$\overline{\text{INT3}}$ input edge select bits (1)	b7 b6 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT3}}$ input 0 1: Interrupt request is generated on the rising edge of $\overline{\text{INT3}}$ input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT3}}$ input	R/W
b7	INT3SB			R/W

Note:
1. Changing bits INTiSA to INTiSB (i = 0 to 3) may set the IRIi bit (i = 0 to 3) in the IRR3 register to 1 (interrupt requested). See **11.9.4 Rewriting Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN**.

11.2.4 Key Input Enable Register (KIEN)

Address 0003Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	$\overline{KI0}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	$\overline{KI0}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	$\overline{KI1}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	$\overline{KI1}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	$\overline{KI2}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	$\overline{KI2}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	$\overline{KI3}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	$\overline{KI3}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W

Note:
1. Changing the bits KIiPL or KIiEN (i = 0 to 3) may set the IRKI bit in the IRR3 register to 1 (interrupt requested). See **11.9.4 Rewriting Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN**.

11.2.5 Interrupt Priority Level Register i (ILVLi) (i = 0, or 2 to E)

Address 00040h (ILVL0), 00042h to 0004Eh (ILVL2 to ILVLE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	ILVLi5	ILVLi4	—	—	ILVLi1	ILVLi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVLi0	Interrupt priority level setting bits	b1 b0 0 0: Level 0 (interrupt disabled) 0 1: Level 1 1 0: Level 2 1 1: Level 2	R/W
b1	ILVLi1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	ILVLi4	Interrupt priority level setting bits	b5 b4 0 0: Level 0 (interrupt disabled) 0 1: Level 1 1 0: Level 2 1 1: Level 2	R/W
b5	ILVLi5			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The ILVLi register (i = 0, or 2 to E) is used to set the priority levels (levels 0 to 2) of the maskable interrupts. The settings in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in each register are used to decide the priority of the corresponding interrupt request.

See **Table 11.4 Correspondence between Interrupt Requests and ILVLi (i = 0, or 2 to E)** for the interrupt setting bits.

The interrupt priority level register must be rewritten only while no interrupt requests corresponding to that register are generated. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers**.

Table 11.4 Correspondence between Interrupt Requests and ILVLi (i = 0, or 2 to E)

ILVLi Register	Bit							
	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	ILVLi5	ILVLi4	—	—	ILVLi1	ILVLi0
ILVL0	—	—	Flash ready		—	—	—	
ILVL2	—	—	Comparator B3		—	—	Comparator B1	
ILVL3	—	—	Timer RC		—	—	—	
ILVL4	—	—	—		—	—	—	
ILVL5	—	—	—		—	—	—	
ILVL6	—	—	Key input		—	—	—	
ILVL7	—	—	—		—	—	A/D conversion	
ILVL8	—	—	UART0 transmission		—	—	—	
ILVL9	—	—	—		—	—	UART0 reception	
ILVLA	—	—	$\overline{\text{INT2}}$		—	—	—	
ILVLB	—	—	Periodic timer		—	—	Timer RJ2	
ILVLC	—	—	$\overline{\text{INT1}}$		—	—	Timer RB2	
ILVLD	—	—	—		—	—	$\overline{\text{INT3}}$	
ILVLE	—	—	$\overline{\text{INT0}}$		—	—	—	

—: Not used. The write value must be 0.
i = 0, or 2 to E

11.2.6 Interrupt Monitor Flag Register 0 (IRR0)

Address 00050h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	IRS0R	IRS0T	—	IRTC	IRTB	IRTJ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IRTJ	Timer RJ2 interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b1	IRTB	Timer RB2 interrupt request monitor flag		R
b2	IRTC	Timer RC interrupt request monitor flag		R
b3	—	Reserved	The read value is 0.	R
b4	IRS0T	UART0 transmit interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b5	IRS0R	UART0 receive interrupt request monitor flag		R
b6	—	Reserved	The read value is 0.	R
b7	—			

The IRR0 register is the monitor flag register for timer RJ2, timer RB2, timer RC, UART0 transmit, and UART0 receive interrupt requests. See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

11.2.7 Interrupt Monitor Flag Register 1 (IRR1)

Address 00051h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	IRWD	IRFM	—	IRAD	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0.	R
b1	—			
b2	IRAD	A/D conversion interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b3	—	Reserved	The read value is 0.	R
b4	IRFM	Flash ready interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b5	IRWD	Periodic timer interrupt request monitor flag		R
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The IRR1 register is the monitor flag register for A/D conversion, flash ready, and periodic timer interrupt requests. See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

11.2.8 Interrupt Monitor Flag Register 2 (IRR2)

Address 00052h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IRCMP3	IRCMP1	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0.	R
b1	—			
b2	IRCMP1	Comparator B1 interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b3	IRCMP3	Comparator B3 interrupt request monitor flag		R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

The IRR2 register is the monitor flag register for comparator B1 and comparator B3 interrupt requests. See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

11.2.9 External Interrupt Flag Register (IRR3)

Address 00053h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	IRKI	—	IRI3	IRI2	IRI1	IRI0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IRI0	$\overline{\text{INT0}}$ interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	IRI1	$\overline{\text{INT1}}$ interrupt request flag		R/W
b2	IRI2	$\overline{\text{INT2}}$ interrupt request flag		R/W
b3	IRI3	$\overline{\text{INT3}}$ interrupt request flag		R/W
b4	—	Reserved	Set to 0.	R/W
b5	IRKI	Key input interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

IRI0 Bit ($\overline{\text{INT0}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI0 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT0}}$) is acknowledged.

IRI1 Bit ($\overline{\text{INT1}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI1 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT1}}$) is acknowledged.

IRI2 Bit ($\overline{\text{INT2}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI2 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT2}}$) is acknowledged.

IRI3 Bit ($\overline{\text{INT3}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI3 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT3}}$) is acknowledged.

IRKI Bit (Key input interrupt request flag)

Writing 0 after reading the value 1 sets the IRKI bit to 0. This bit is also automatically set to 0 when the corresponding interrupt (key input) is acknowledged.

The interrupt priority level register must be rewritten only while no interrupt requests corresponding to that register are generated. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers**.

11.2.10 Address Match Interrupt Register i (AIADRi) (i = 0 or 1)

Address 001C0h (AIADR0L), 001C4h (AIADR1L)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Address 001C1h (AIADR0M), 001C5h (AIADR1M)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Address 001C2h (AIADR0H), 001C6h (AIADR1H)

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Setting for the addresses to be matched	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b21	—			
b22	—			
b23	—			

The AIADRi register (i = 0 or 1) is initialized after a voltage monitor 0 reset, power-on reset, or hardware reset. This register remains unchanged after a watchdog timer reset or software reset.

11.2.11 Address Match Interrupt Enable Register i (AIENi) (i = 0 or 1)

Address 001C3h (AIEN0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	AIEN00
After Reset	0	0	0	0	0	0	0	0

Address 001C7h (AIEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	AIEN10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	AIENi0	Address match interrupt enable i bit (i = 0 or 1)	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The AIENi register (i = 0 or 1) is initialized after a voltage monitor 0 reset, power-on reset, or hardware reset. This register remains unchanged after a watchdog timer reset or software reset.

11.3 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the start address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

Figure 11.2 Interrupt Vector

11.3.1 Fixed Vector Table

The fixed vector table is allocated to addresses 0FFDCh to 0FFFFh.
Table 11.5 lists the Fixed Vector Table. The vector addresses (H) of the fixed vectors are used by the ID code check function. For details, see **19.3 ID Code Check Function**.

Table 11.5 Fixed Vector Table

Interrupt Source	Vector Address Address (L) to Address (H)	Remarks
Undefined instruction	0FFDCh to 0FFDFh	Interrupt by the UND instruction
Overflow	0FFE0h to 0FFE3h	Interrupt by the INTO instruction
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address indicated by the vector in the relocatable vector table.
Address match	0FFE8h to 0FFEBh	
Single-step (1)	0FFECh to 0FFEFh	
Watchdog timer, oscillation stop detection, voltage monitor 1	0FFF0h to 0FFF3h	
Reserved	0FFF4h to 0FFF7h	
Reserved	0FFF8h to 0FFFBh	
Reset	0FFFCh to 0FFFFh	

Note:
1. Do not use this interrupt. It is provided exclusively for use in development tools.

11.3.2 Relocatable Vector Table

The relocatable vector table occupies 256 bytes beginning from the start address set in the INTB register. Table 11.6 lists the Relocatable Vector Table.

Table 11.6 Relocatable Vector Table

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Priority Level Setting (ILVL0 or ILVL2 to ILVLE)
BRK instruction (2)	+0 to +3 (+00000h to +00003h)	0	—
Flash ready	+4 to +7 (+00004h to +00007h)	1	ILVL05 to ILVL04
Reserved		2 to 3	—
Comparator B1	+16 to +19 (+00010h to +00013h)	4	ILVL21 to ILVL20
Comparator B3	+20 to +23 (+00014h to +00017h)	5	ILVL25 to ILVL24
Reserved	+24 to +27 (+00018h to +0001Bh)	6	—
Timer RC	+28 to +31 (+0001Ch to +0001Fh)	7	ILVL35 to ILVL34
Reserved	+32 to +35 (+00020h to +00023h)	8	—
Reserved	+36 to +39 (+00024h to +00027h)	9	—
Reserved	+40 to +43 (+00028h to +0002Bh)	10	—
Reserved	+44 to +47 (+0002Ch to +0002Fh)	11	—
Reserved	+48 to +51 (+00030h to +00033h)	12	—
Key input	+52 to +55 (+00034h to +00037h)	13	ILVL65 to ILVL64
A/D conversion	+56 to +59 (+00038h to +0003Bh)	14	ILVL71 to ILVL70
Reserved	+60 to +63 (+0003Ch to +0003Fh)	15	—
Reserved		16	—
UART0 transmission	+68 to +71 (+00044h to +00047h)	17	ILVL85 to ILVL84
UART0 reception	+72 to +75 (+00048h to +0004Bh)	18	ILVL91 to ILVL90
Reserved	+76 to +79 (+0004Ch to +0004Fh)	19	—
Reserved	+80 to +83 (+00050h to +00053h)	20	—
$\overline{\text{INT2}}$	+84 to +87 (+00054h to +00057h)	21	ILVLA5 to ILVLA4
Timer RJ2	+88 to +91 (+00058h to +0005Bh)	22	ILVLB1 to ILVLB0
Periodic timer	+92 to +95 (+0005Ch to +0005Fh)	23	ILVLB5 to ILVLB4
Timer RB2	+96 to +99 (+00060h to +00063h)	24	ILVLC1 to ILVLC0
$\overline{\text{INT1}}$	+100 to +103 (+00064h to +00067h)	25	ILVLC5 to ILVLC4
$\overline{\text{INT3}}$	+104 to +107 (+00068h to +0006Bh)	26	ILVLD1 to ILVLD0
Reserved		27 to 28	—
$\overline{\text{INT0}}$	+116 to +119 (+00074h to +00077h)	29	ILVLE5 to ILVLE4
Reserved		30	—
Reserved		31	—
Software (2)	+128 to +131 (+00080h to +00083h) to +252 to +255 (+000FCh to +000FFh)	32 to 63	—

Notes:
1. These addresses are relative to those indicated by the INTB register.
2. These interrupts are not disabled by the I flag.

11.4 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the priority for acknowledgement. This description does not apply to non-maskable interrupts.

11.4.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

11.4.2 Registers IRR0 to IRR3

11.4.2.1 Registers IRR0 to IRR2

Registers IRR0 to IRR2 are the monitor flag registers for peripheral function interrupts. These registers can only be read and cannot be written. Table 11.7 lists the Relation between Registers IRR0 to IRR2 and Registers Associated with Peripheral Function Interrupts.

Peripheral functions have individual interrupt request flags and interrupt enable registers. When both of the interrupt request flag and interrupt enable bit for a peripheral function are set to 1, the monitor flag in the corresponding IRR0 to IRR2 registers is set to 1 (interrupt requested). When either or both of the interrupt request flag and interrupt enable bit for a peripheral function are set to 1, the monitor flag in the corresponding IRR0 to IRR2 registers is set to 0 (no interrupt requested).

Table 11.7 Relation between Registers IRR0 to IRR2 and Registers Associated with Peripheral Function Interrupts

	Peripheral Function Interrupt Request Flag		Peripheral Function Interrupt Enable		Corresponding Interrupt Monitor Flag	
	Register	Bit	Register	Bit	Register	Bit
Timer RJ2	TRJIR	TRJIF	TRJIR	TRJIE	IRR0	IRTJ
Timer RB2	TRBIR	TRBIF	TRBIR	TRBIE	IRR0	IRTB
Timer RC (1)	TRCSR	IMFA	TRCIER	IMIEA	IRR0	IRTC
		IMFB		IMIEB		
		IMFC		IMIEC		
		IMFD		IMIED		
		OVF		OVIE		
Serial interface (UART0)	U0IR	U0TIF	U0IR	U0TIE	IRR0	IRS0T
		U0RIF		U0RIE		IRS0R
A/D converter	ADICSR	ADF	ADICSR	ADIE	IRR1	IRAD
Flash memory (1)	FST	RDYSTI	FMR0	RDYSTIE	IRR1	IRFM
		BSYAEI		BSYAEIE		
				CMDERIE		
Periodic timer	WDTIR	WDTIF	WDTIR	WDTIE	IRR1	IRWD
Comparator B	WCB1INTR	WCB1F	WCB1INTR	WCB1INTEN	IRR2	IRCMP1
	WCB3INTR	WCB3F	WCB3INTR	WCB3INTEN		IRCMP3

Note:
1. Timer RC and the flash memory each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the monitor flag (the IRTC bit in the IRR0 register or the IRFM bit in the IRR1 register).

11.4.2.2 IRR3 Register

The IRR3 register is the flag register for external interrupts ($\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$). When external input is enabled and an active edge is detected, the interrupt request flag in the IRR3 register is set to 1. When an interrupt request is acknowledged, the flag for this interrupt request is automatically set to 0 after the CPU branches to the corresponding interrupt vector. Writing 0 after reading the value 1 also sets the interrupt request flag to 0.

11.4.3 Interrupt Priority Levels in ILVLi Register (i = 0, or 2 to E) and IPL

Interrupt priority levels can be set by the ILVLi register (i = 0, or 2 to E).
Table 11.8 lists the Interrupt Priority Level Settings. Table 11.9 lists the Interrupt Priority Levels Enabled by IPL.
The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- The interrupt request flag and interrupt enable bit for each peripheral function = 1 or external interrupt request flag (IRR3) = 1
- Interrupt priority level > IPL

The I flag, registers IRR0 to IRR3, the ILVLi register (i = 0, or 2 to E), and IPL are independent of each other. They do not affect one another.

Table 11.8 Interrupt Priority Level Settings

Bits ILVLi1 to ILVLi0 or Bits ILVLi5 to ILVLi4 (1)	Interrupt Priority Level	Priority Level
00b	Level 0 (interrupt disabled)	—
01b	Level 1	Low ↓ High
10b	Level 2	
11b	Level 2	

Note:
1. Values to be set in interrupt priority level register i (ILVLi) (i = 0, or 2 to E).

Table 11.9 Interrupt Priority Levels Enabled by IPL

IPL	Interrupt Priority Level to be Enabled
000b	Levels 1 and 2
001b	Level 2
010b to 111b	None (all maskable interrupts are disabled)

11.4.4 Interrupt Sequence

The following describes the interrupt sequence performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction has completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, and RMPA instructions, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence.
The interrupt sequence is performed as described below.
Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. Then, for an $\overline{\text{INT}}$ interrupt and a key input interrupt, the corresponding interrupt request flag is set to 0 (no interrupt requested). For any other peripheral interrupts, the corresponding interrupt request flag remains 1 (interrupt requested) and does not change.
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before the interrupt sequence is entered.
(3) Flags I, D, and U in the FLG register are set as follows:
• The I flag is 0 (interrupt disabled).
• The D flag is 0 (single-step interrupt disabled).
• The U flag is set to 0 (ISP selected).
However, the U flag does not change if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The start address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the start address of the interrupt routine.

Note:
1. Temporary registers cannot be used by the user.

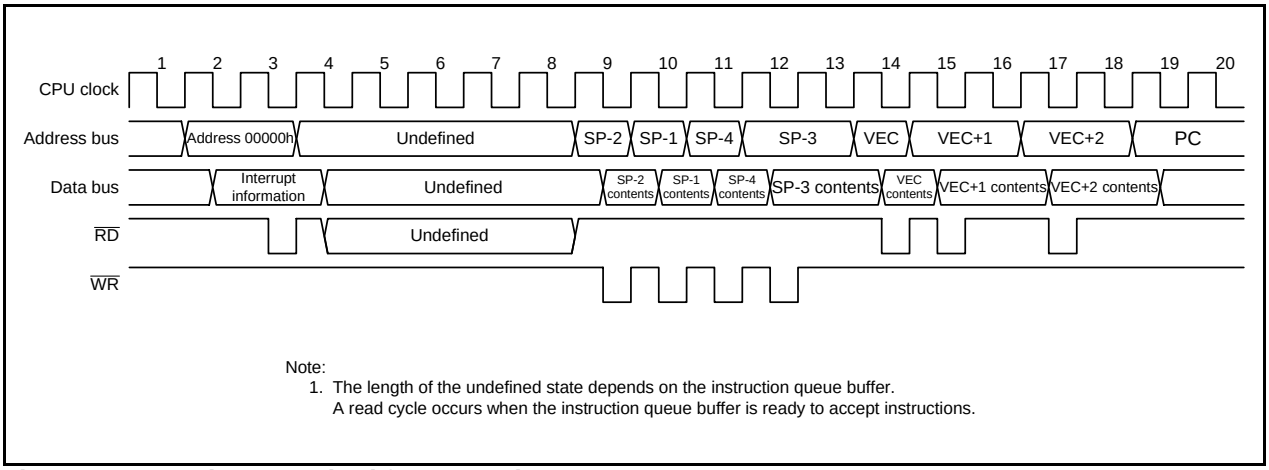
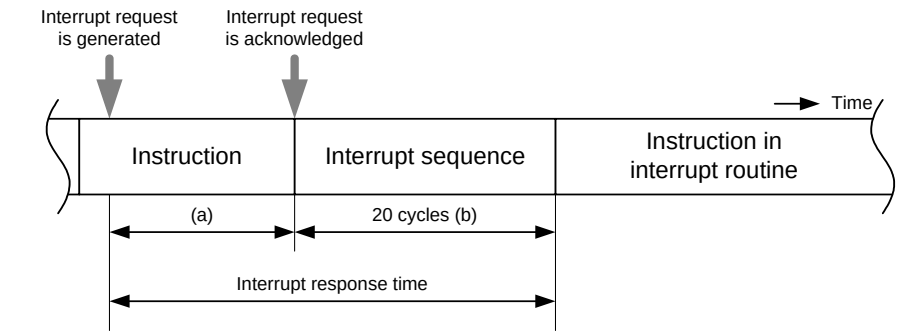


Figure 11.3 Time Required for Executing Interrupt Sequence

11.4.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. This time consists of two periods: the first period ranges from when an interrupt request is generated until the currently executing instruction is completed ((a) in Figure 11.4) and the second from when an interrupt request is acknowledged until the interrupt sequence is executed (20 cycles (b)).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of this time varies with the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states, and the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 11.4 Interrupt Response Time

11.4.6 IPL Change When Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.

For a software interrupt or special interrupt request, the level listed in Table 11.10 is set in the IPL.

Table 11.10 IPL Value When Software Interrupt or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1	7
Software, address match, single-step	Not changed

11.4.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After a total of 16 bits: higher 4 bits in the PC, higher 4 (IPL) and lower 8 bits in the FLG register, are saved on the stack, the lower 16 bits in the PC are saved.
Figure 11.5 shows the Stack State Before and After Interrupt Request is Acknowledged.
Any other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being used (1) with a single instruction.

Note:
1. Selectable from among registers R0, R1, R2, R3, A0, A1, SB, and FB.

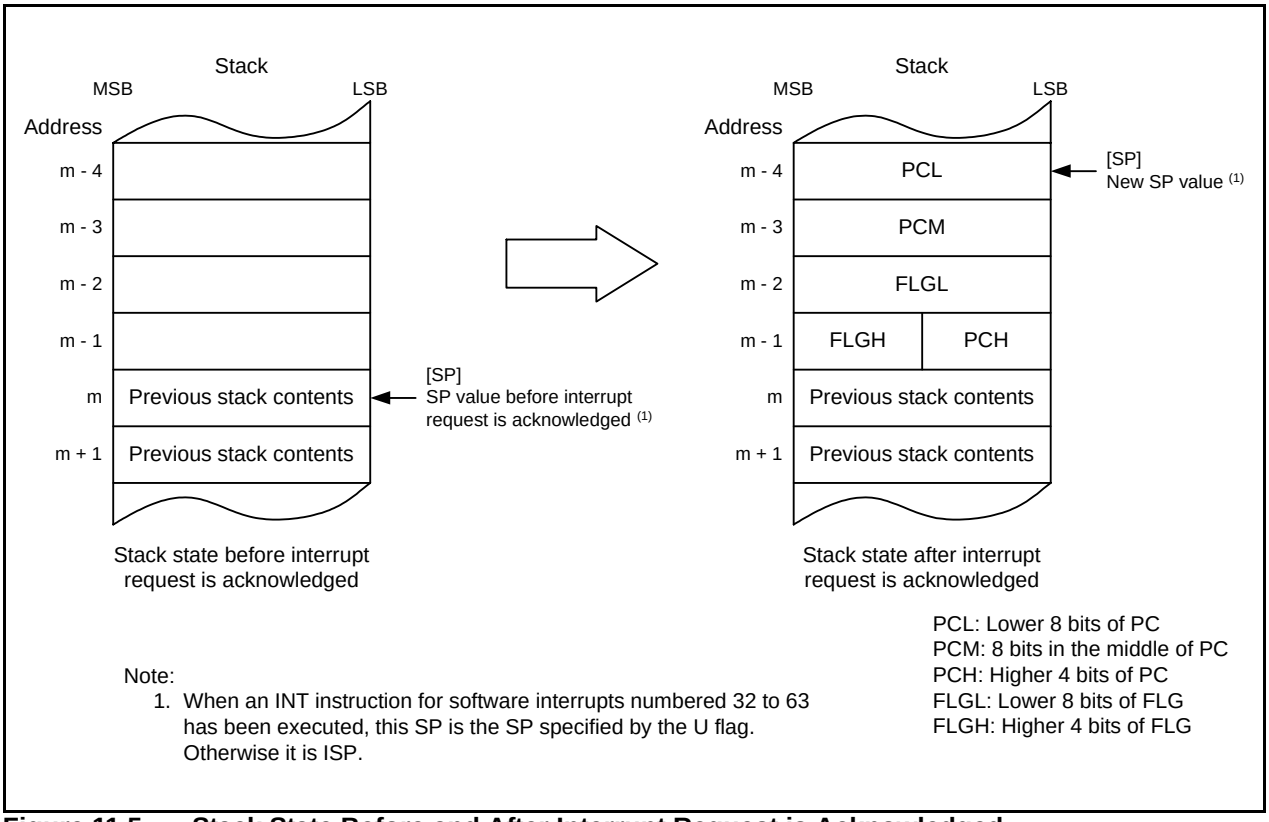
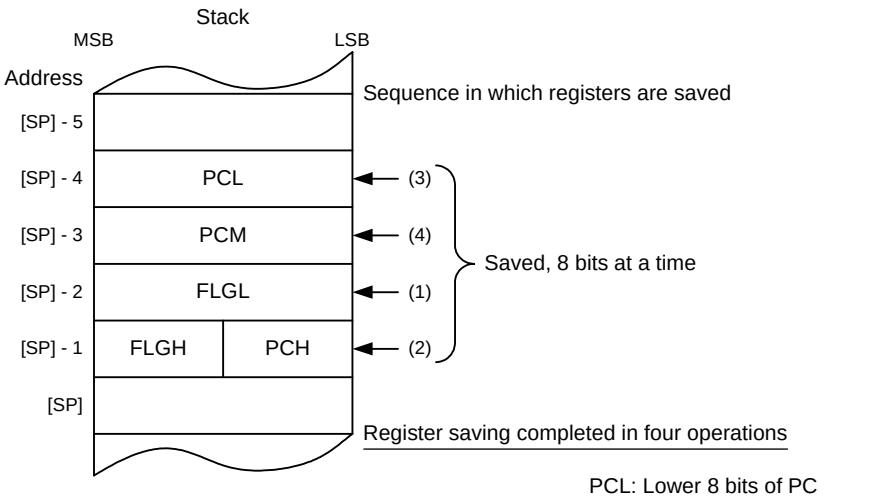


Figure 11.5 Stack State Before and After Interrupt Request is Acknowledged

The register saving operation in the interrupt sequence uses four operations, each one of which saves 8 bits. Figure 11.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged. After registers are saved, the SP content becomes [SP] minus 4. When an INT instruction for software interrupts numbered 32 to 63 has been executed, this SP is the SP specified by the U flag. Otherwise it is ISP.

Figure 11.6 Register Saving Operation

11.4.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are restored. The program that was running before the interrupt request was acknowledged starts running again.

The registers saved by a program in the interrupt routine should be restored using the POPM or similar instruction before executing the REIT instruction.

11.4.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Any maskable interrupt (peripheral function) priority level can be selected by bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5. However, if two or more maskable interrupts have the same priority level, the interrupt with higher priority given by hardware is acknowledged.

The priority of special interrupts such as the watchdog timer interrupt is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If a software interrupt instruction is executed, the MCU will execute the corresponding interrupt routine.

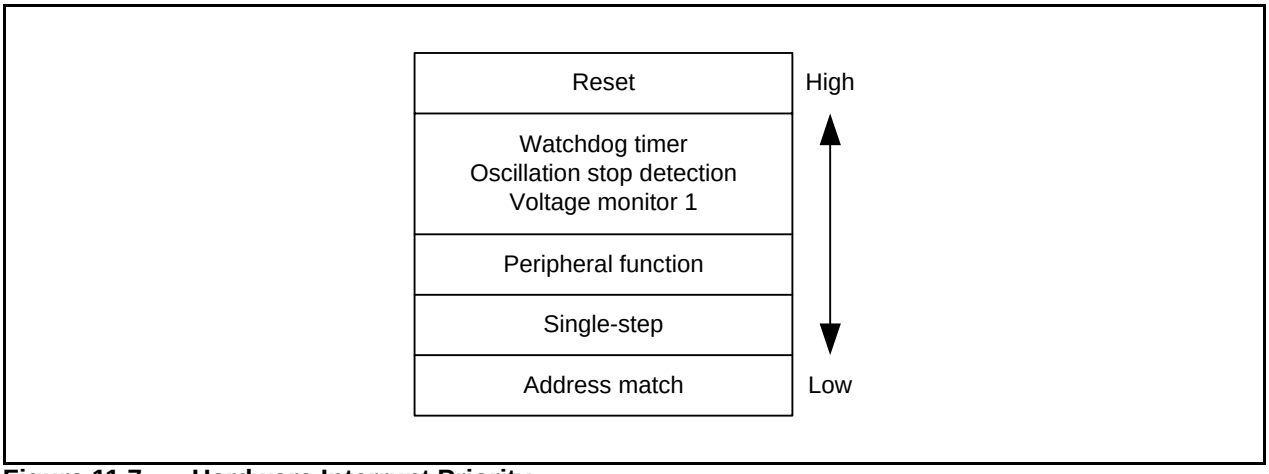


Figure 11.7 Hardware Interrupt Priority

11.4.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt.
Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

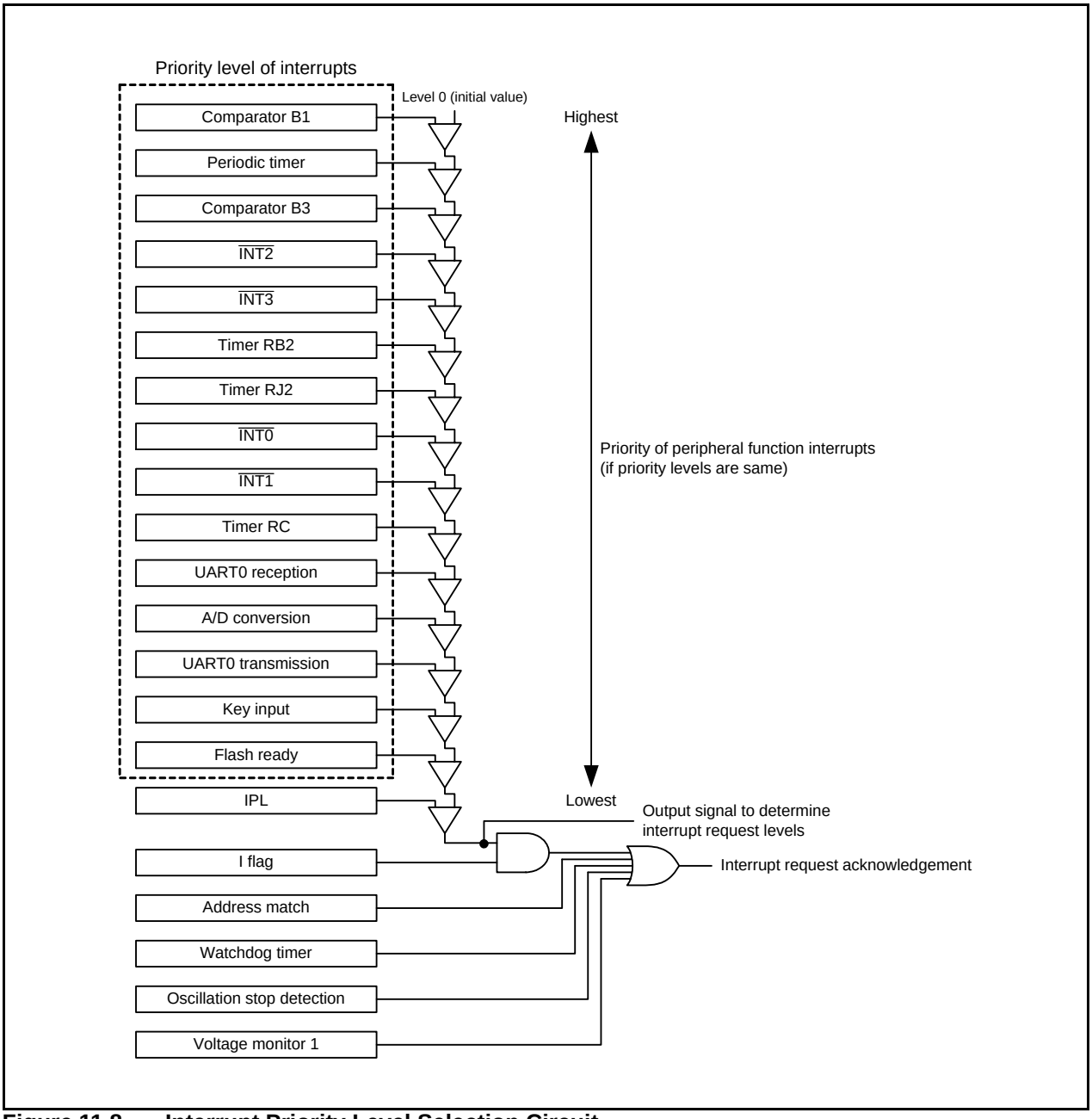


Figure 11.8 Interrupt Priority Level Selection Circuit

11.5 $\overline{\text{INT}}$ Interrupt

11.5.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity can be selected by bits INTiSA to INTiSB in the ISCR0 register. The input pins used as the $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ input can be selected.
Inputs can be passed through a digital filter with three different sampling clocks.
The interrupt by the $\overline{\text{INTi}}$ input can be used as a wakeup function to cancel wait mode or stop mode.
Table 11.11 lists the Pin Configuration for $\overline{\text{INTi}}$ Interrupt.

Table 11.11 Pin Configuration for $\overline{\text{INTi}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P1_4, P4_5	I	$\overline{\text{INT0}}$ interrupt input
$\overline{\text{INT1}}$	P1_5, P1_7, P4_6	I	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_4, P4_7	I	$\overline{\text{INT2}}$ interrupt input
$\overline{\text{INT3}}$	P3_3	I	$\overline{\text{INT3}}$ interrupt input

11.5.2 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3)

The $\overline{\text{INTi}}$ input has a digital filter. The sampling clock can be selected by bits INTiF0 to INTiF1 in the INTF0 register. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle, and the corresponding IRIi bit in the IRR3 register is set to 1 (interrupt requested) when the sampled input level matches three successive times.
Figure 11.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 11.10 shows an Example of $\overline{\text{INTi}}$ Input Filter Operation.

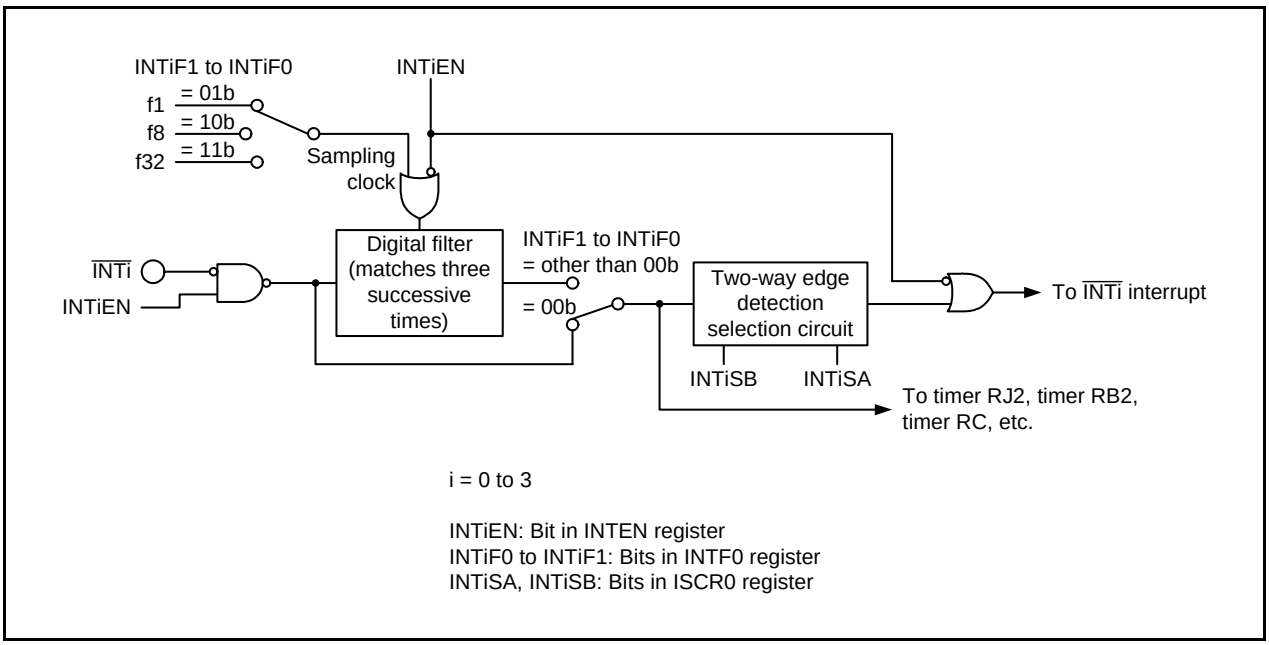


Figure 11.9 $\overline{\text{INTi}}$ Input Filter Configuration

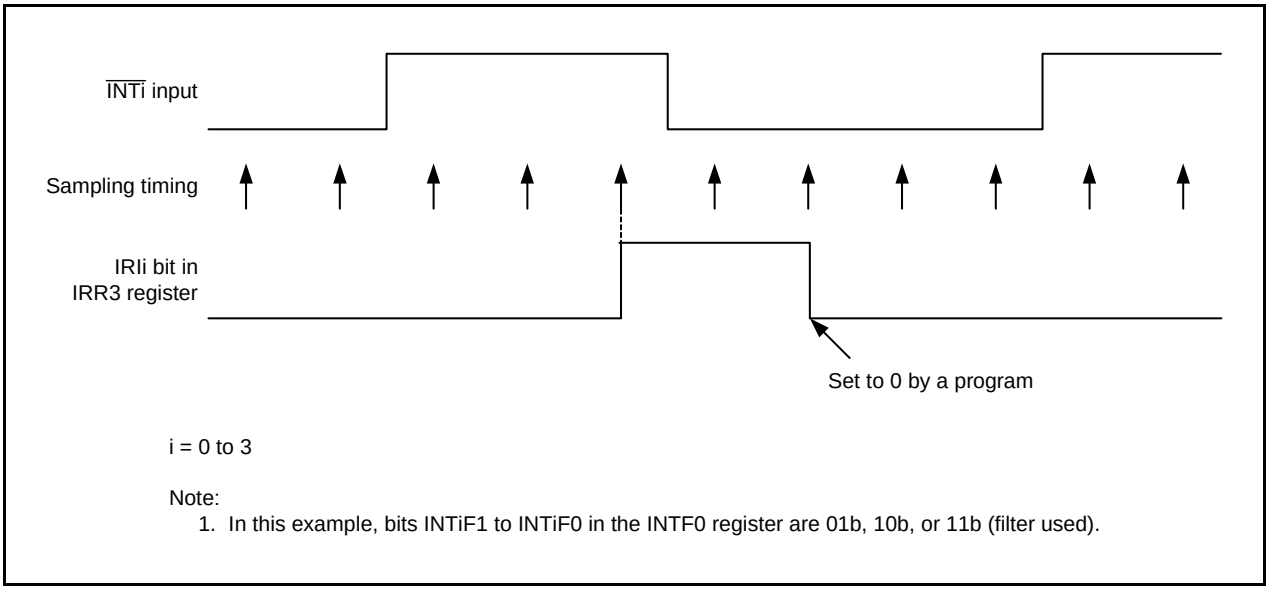


Figure 11.10 Example of $\overline{\text{INTi}}$ Input Filter Operation

11.6 Key Input Interrupt

A key input interrupt request is generated by one of the input edges on pins $\overline{KI0}$ to $\overline{KI3}$. The key input interrupt can be used as a key-on wakeup function to cancel wait mode or stop mode.

The KIiEN bit (i = 0 to 3) in the KIEN register is be used to select whether the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is be used to select the input polarity.

When a low level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts. Likewise, when a high level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts.

Figure 11.11 shows the Block Diagram for Key Input Interrupts. Table 11.12 lists the Pin Configuration for Key Input Interrupts.

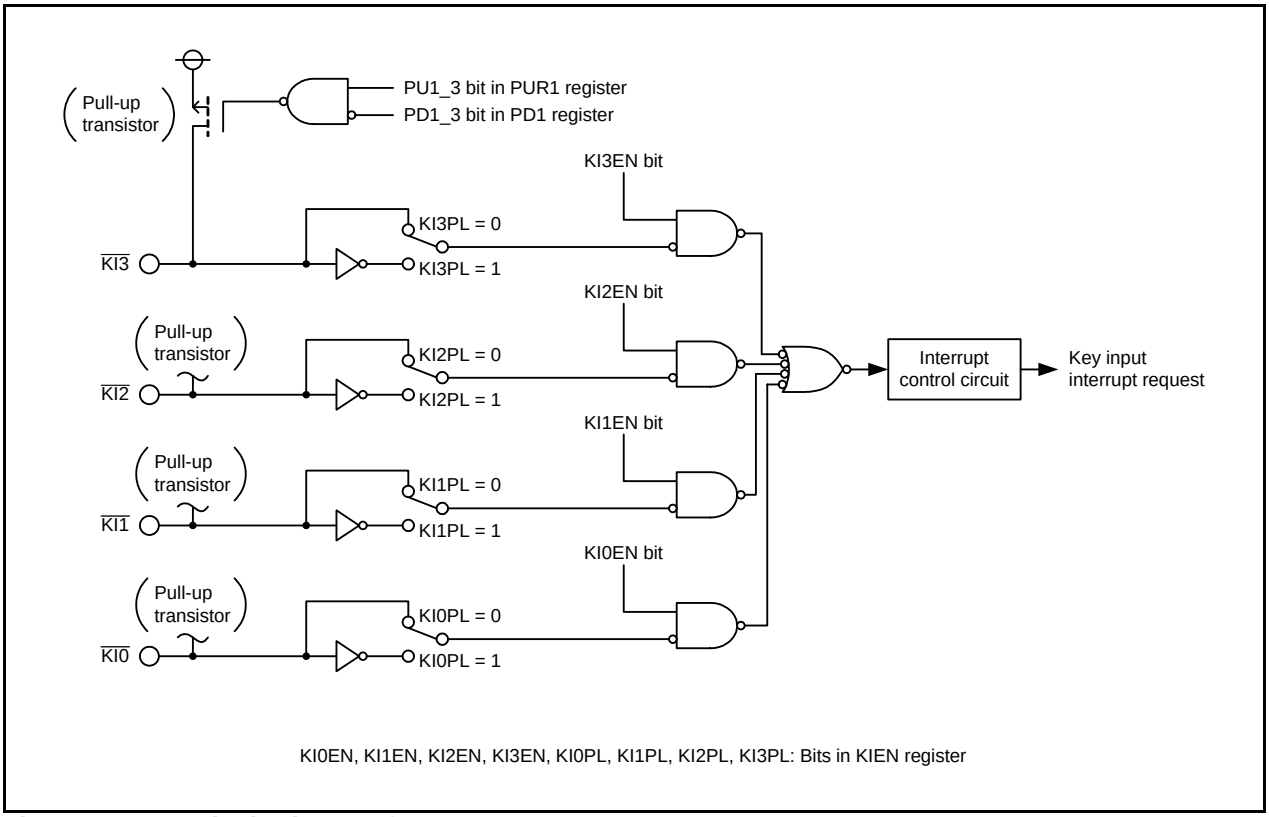


Figure 11.11 Block Diagram for Key Input Interrupts

Table 11.12 Pin Configuration for Key Input Interrupts

Pin Name	I/O	Function
$\overline{KI0}$	I	$\overline{KI0}$ interrupt input
$\overline{KI1}$	I	$\overline{KI1}$ interrupt input
$\overline{KI2}$	I	$\overline{KI2}$ interrupt input
$\overline{KI3}$	I	$\overline{KI3}$ interrupt input

11.7 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the AIADRi register (i = 0 or 1). This interrupt is used as a break function for the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIENi and AIADRi, and fixed vector table) in the user system.

Set the start address of any instruction in these registers. The AIENi0 bit (i = 0 or 1) in the AIENi register can be used to enable or disable the interrupt. The address match interrupt is not affected by the I flag and IPL.

The PC value (see **11.4.7 Saving Registers**), which is saved on the stack when an address match interrupt request is acknowledged, will differ depending on the instruction at the address indicated by the AIADRi register. The appropriate return address is not saved on the stack. When the MCU returns from the address match interrupt, use one of the following methods:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state where the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.13 lists the PC Value Saved When Address Match Interrupt Request is Acknowledged. Table 11.14 lists the Correspondence between Address Match Interrupt Sources and Associated Registers.

Table 11.13 PC Value Saved When Address Match Interrupt Request is Acknowledged

Instruction at Address Indicated by AIADRi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 16-bit operation code • Instruction shown below among the instructions with 8-bit operation code: ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ.B:S #IMM8,dest STNZ.B:S #IMM8,dest STZX.B:S #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by AIADRi register + 2
Instructions other than the above	Address indicated by AIADRi register + 1

Note:
1. PC value saved: See **11.4.7 Saving Registers**.

Table 11.14 Correspondence between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIEN00	AIADR0
Address match interrupt 1	AIEN10	AIADR1

11.8 How to Determine Interrupt Sources

Table 11.15 lists How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt. Figure 11.12 shows Example of How to Determine Interrupt Sources for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt.

Table 11.15 How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection	CKSWIF bit in BAKCR register = 1
Watchdog timer	UFIF bit in RISR register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1

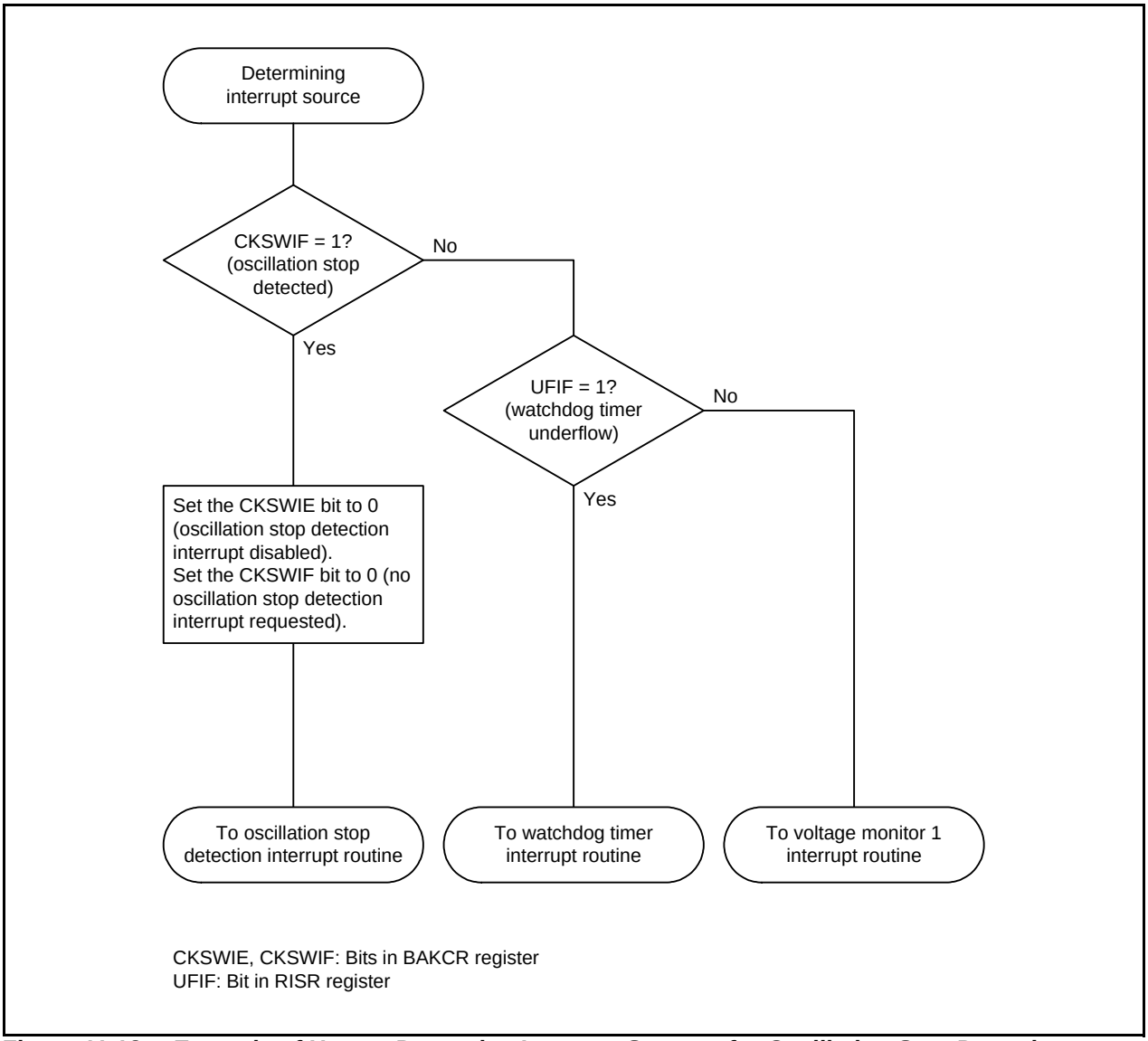


Figure 11.12 Example of How to Determine Interrupt Sources for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt

11.9 Notes on Interrupts

11.9.1 Reading Address 00000h

Do not read address 00000h by a program. When an external interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from address 00000h in the interrupt sequence. At this time, the corresponding bit in the IRR3 register for the acknowledged interrupt is set to 0.
If a program is used to read address 00000h, the corresponding bit in the IRR3 register for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

11.9.2 SP Setting

Set a value in the SP before any interrupt is acknowledged. The SP is 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

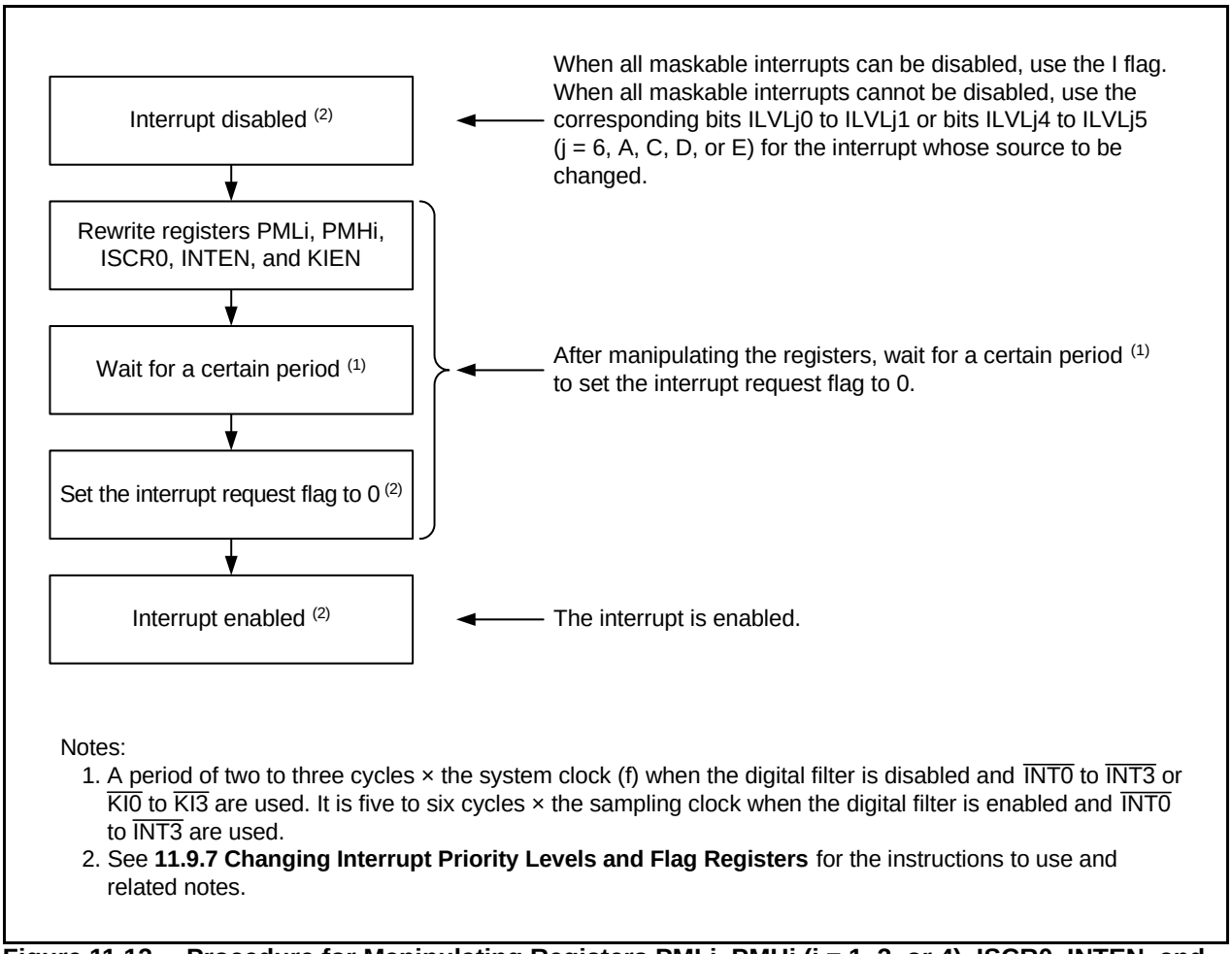
11.9.3 External Interrupt and Key Input Interrupt

Signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ must meet either the low-level width or the high-level width requirements shown in External Interrupt $\overline{\text{INTi}}$ Input (i = 0 to 3) in the Electrical Characteristics, regardless of the CPU operating clock. For details, see **Table 20.18** (Vcc = 5 V), **Table 20.24** (Vcc = 3 V), and **Table 20.30** (Vcc = 2.2 V) **External Interrupt $\overline{\text{INTi}}$ Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)**.

11.9.4 Rewriting Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN

When changing the functions of the $\overline{INT0}$ to $\overline{INT3}$ and $\overline{KI0}$ to $\overline{KI3}$ interrupts, an interrupt request flag may be set to 1 by rewriting registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN. When an interrupt function is switched, rewrite these registers with interrupt requests disabled, and wait for a certain period (1) before setting the interrupt request flag to 0.
Figure 11.13 shows the Procedure for Manipulating Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0.

Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.



Notes:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.
2. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers** for the instructions to use and related notes.

Figure 11.13 Procedure for Manipulating Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0

11.9.5 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) When Returning from Wait Mode or Stop Mode to Standard Mode

When a transition is made to wait mode or stop mode with the WCKSTP bit in the CKSTPR register set to 1 (system clock stopped in wait mode) while in use of the $\overline{\text{INTi}}$ input filter, the $\overline{\text{INTi}}$ interrupt cannot be used to return to standard operating mode.

When the $\overline{\text{INTi}}$ interrupt is used to return, set the WCKSTP bit to 1 and bits INTiF1 to INTiF0 in the INTF0 register to 00b (no filter) before a transition is made to wait mode or stop mode. When the $\overline{\text{INTi}}$ input filter is used again, select the sampling clock with bits INTiF0 to INTiF1 to enable the INTiEN bit in the INTEN register.

Figure 11.14 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used.

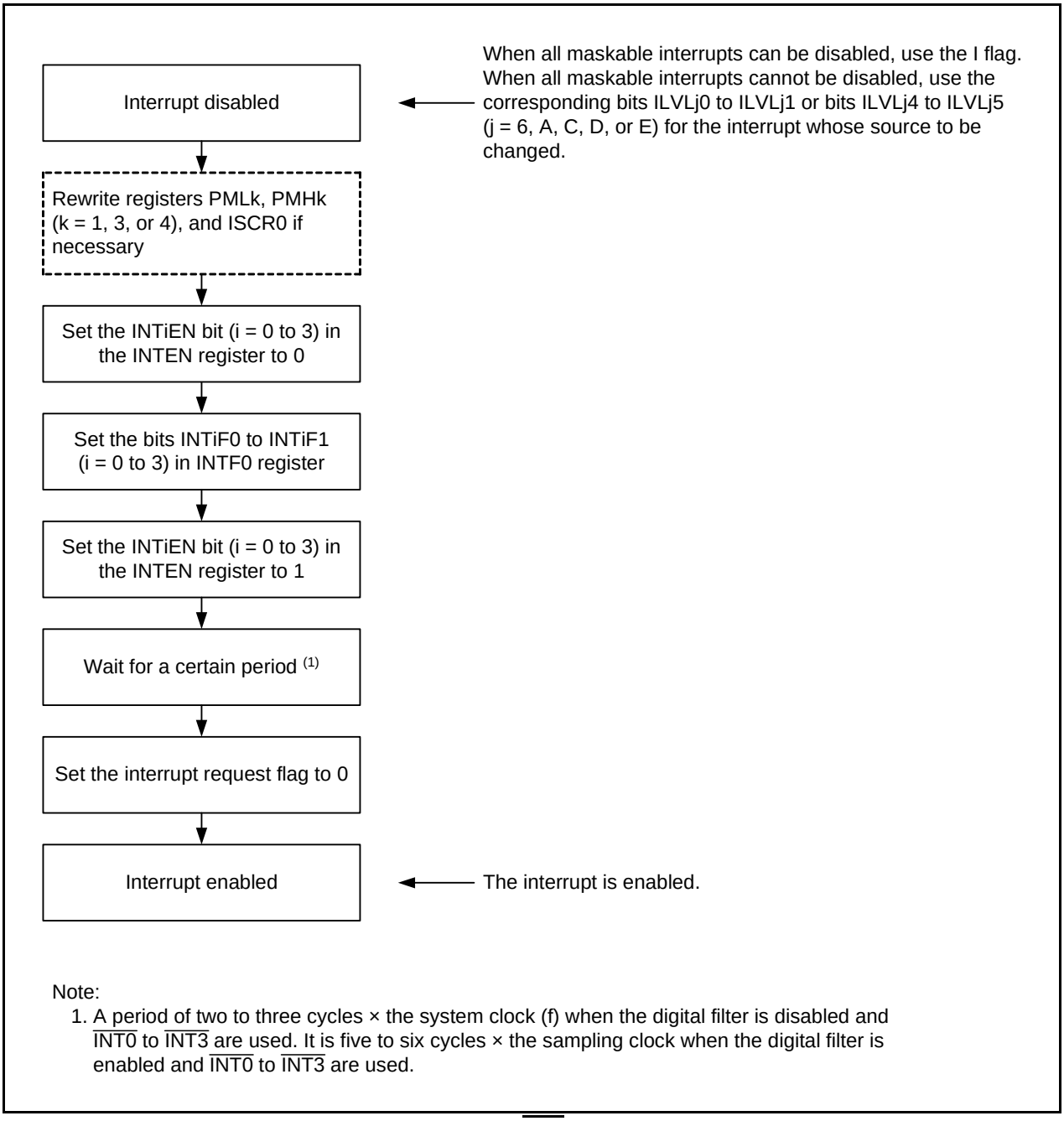
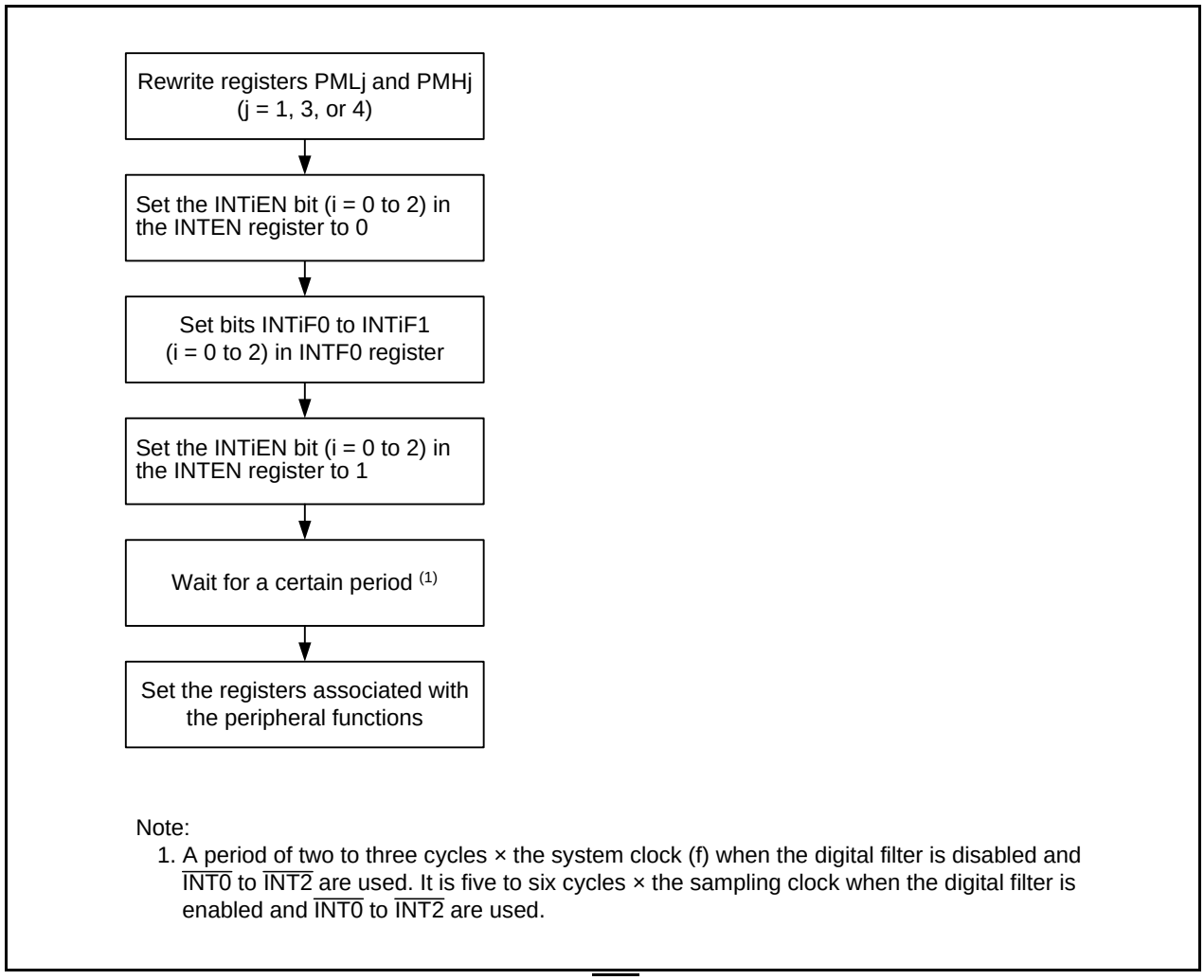


Figure 11.14 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used

11.9.6 Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions

Figure 11.15 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC).



Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used.

Figure 11.15 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC)

11.9.7 Changing Interrupt Priority Levels and Flag Registers

(a) The interrupt priority level and the flag register must be changed only while no interrupt requests are generated. If an interrupt may be generated, using the I flag to disable the interrupt before changing the interrupt priority level and the flag register.

(b) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the interrupt priority level and the flag register are changed due to effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instruction to separate the interrupt priority level and the flag register operation, and I flag operation.

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    POPC    FLG             ; Enable interrupts
```

12. I/O Ports

There are 17 I/O ports. P4_6 and P4_7 can be used as I/O ports when the XIN clock oscillation circuit is not used. PA_0 can be used as an I/O port when a hardware reset is not used. In addition, all the ports are multiplexed with multiple peripheral functions.

12.1 Overview

The functions of the ports are selected by the peripheral function mapping registers (PMLi/PMHi, i = 1, 3, or 4) and the peripheral function mapping expansion registers (PMH1E and PMH4E). The functions of the I/O ports are selected by the port direction registers (PDi, i = 1, 3, 4, or A). In addition, the drive capacity of some ports can be switched. Table 12.1 shows the I/O Port Overview. Table 12.2 lists the Port Functions by Pin (R8C/M12A Group). Table 12.3 lists the I/O Port Register Configuration.

Table 12.1 I/O Port Overview

Ports	I/O	Output Type	I/O Setting	Internal Pull-Up Resistor	Drive Capacity Switching
P1_0 to P1_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	Set in 1-bit units. (4)
P3_3, P3_4, P3_5, P3_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	Set in 1-bit units. (4)
PA_0 (1)	I/O	3-state CMOS	Set in 1-bit units.	None	None
P4_2, P4_5, P4_6, P4_7 (2)	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (3)	None

Notes:
1. When the hardware reset is not used, this port can be used as an I/O port.
2. When the XIN clock oscillation circuit or direct input of the XIN clock is not used, these can be used as I/O ports.
3. In input mode, whether an internal pull-up resistor is connected or not can be selected by the PURi register (i = 1, 3, or 4).
4. The drive capacity of the output transistors (low or high) can be selected by the DRRi register (i = 1 or 3).

Table 12.2 Port Functions by Pin (R8C/M12A Group)

Pin Number	R8C/M12A Group	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function Select Bit		
		PM2 to PM0 = 000b	PM2 to PM0 = 001b	PM2 to PM0 = 010b	PM2 to PM0 = 011b	PM2 to PM0 = 100b	PM2 to PM0 = 101b	PM2	PM1	PM0
1	P4_2	P4_2	TRBO	TXD0	$\overline{KI3}$	—	—	—	P42SEL1	P42SEL0
2	P3_7	P3_7	$\overline{ADTRG}$	TRJO	TRCIOD	—	—	—	P37SEL1	P37SEL0
3	$\overline{RESET}$	PA_0	—	—	—	—	—	—	—	—
4	P4_7/XOUT	P4_7/XOUT	$\overline{INT2}$	—	—	—	—	—	P47SEL1	P47SEL0
5	VSS/AVSS	—	—	—	—	—	—	—	—	—
6	P4_6/XIN	P4_6/XIN	RXD0	TXD0	$\overline{INT1}$	VCOUT1	TRJIO	P46SEL2	P46SEL1	P46SEL0
7	VCC/AVCC	—	—	—	—	—	—	—	—	—
8	MODE	—	—	—	—	—	—	—	—	—
9	P3_5	P3_5	TRCIOD	$\overline{KI2}$	VCOUT3	—	—	—	P35SEL1	P35SEL0
10	P3_4	P3_4/IVREF3	TRCIOC	$\overline{INT2}$	—	—	—	—	P34SEL1	P34SEL0
11	P3_3	P3_3/IVCMP3	TRCCLK	$\overline{INT3}$	—	—	—	—	P33SEL1	P33SEL0
12	P4_5	P4_5	$\overline{INT0}$	$\overline{ADTRG}$	—	—	—	—	P45SEL1	P45SEL0
13	P1_7	P1_7/AN7/ IVCMP1	$\overline{INT1}$	TRJIO	TRCCLK	—	—	—	P17SEL1	P17SEL0
14	P1_6	P1_6/IVREF1	CLK0	TRJO	TRCIOB	—	—	—	P16SEL1	P16SEL0
15	P1_5	P1_5	RXD0	TRJIO	$\overline{INT1}$	VCOUT1	—	P15SEL2	P15SEL1	P15SEL0
16	P1_4	P1_4/AN4	TXD0	RXD0	$\overline{INT0}$	TRCIOB	—	P14SEL2	P14SEL1	P14SEL0
17	P1_3	P1_3/AN3	TRCIOC	$\overline{KI3}$	TRBO	—	—	—	P13SEL1	P13SEL0
18	P1_2	P1_2/AN2	TRCIOB	$\overline{KI2}$	—	—	—	—	P12SEL1	P12SEL0
19	P1_1	P1_1/AN1	TRCIOA/ TRCTRG	$\overline{KI1}$	—	—	—	—	P11SEL1	P11SEL0
20	P1_0	P1_0/AN0	TRCIOD	$\overline{KI0}$	—	—	—	—	P10SEL1	P10SEL0

Table 12.3 I/O Port Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Port P1 Direction Register	PD1	00h	000A9h	8
Port P3 Direction Register	PD3	00h	000ABh	8
Port P4 Direction Register	PD4	00h	000ACh	8
Port PA Direction Register	PDA	00h	000ADh	8
Port P1 Register	P1	00h	000AFh	8
Port P3 Register	P3	00h	000B1h	8
Port P4 Register	P4	00h	000B2h	8
Port PA Register	PA	00h	000B3h	8
Pull-Up Control Register 1	PUR1	00h	000B5h	8
Pull-Up Control Register 3	PUR3	00h	000B7h	8
Pull-Up Control Register 4	PUR4	00h	000B8h	8
Port I/O Function Control Register	PINSR	00h	000B9h	8
Drive Capacity Control Register 1	DRR1	00h	000BBh	8
Drive Capacity Control Register 3	DRR3	00h	000BDh	8
Open-Drain Control Register 1	POD1	00h	000C1h	8
Open-Drain Control Register 3	POD3	00h	000C3h	8
Open-Drain Control Register 4	POD4	00h	000C4h	8
Port PA Mode Control Register	PAMCR	00010001b	000C5h	8
Port 1 Function Mapping Register 0	PML1	00h	000C8h	8
Port 1 Function Mapping Register 1	PMH1	00h	000C9h	8
Port 3 Function Mapping Register 0	PML3	00h	000CCh	8
Port 3 Function Mapping Register 1	PMH3	00h	000CDh	8
Port 4 Function Mapping Register 0	PML4	00h	000CEh	8
Port 4 Function Mapping Register 1	PMH4	00h	000CFh	8
Port 1 Function Mapping Expansion Register	PMH1E	00h	000D1h	8
Port 4 Function Mapping Expansion Register	PMH4E	00h	000D5h	8

12.2 Reading of Port Input Level

Regardless of the mapping settings for port functions, whether to read the port latch or the pin level can be selected when reading the Pi register (i = 1, 3, 4, or A).

12.2.1 Port I/O Function Control Register (PINSR)

Address 000B9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOINSEL	TRJIOSEL	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The write value is invalid. The read value is undefined.	—
b1	—	Reserved	Set to 0. The read value is 0.	—
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	TRJIOSEL	TRJIO input signal select bit	0: Input from external TRJIO pin 1: Internal input from VCOUT1 of comparator B	R/W
b7	IOINSEL	Pin level forced read-out bit	0: Disabled (control by PDi Register) 1: Enabled (read of pin input level)	R/W

Set the PRC4 bit in the PRCR register to 1 (write enabled) before rewriting the PINSR register.

[When the IOINSEL bit in the PINSR register is 0]
When the PDi_j bit (j = 0 to 7) in the PDi register (i = 1, 3, 4, or A) is 0 (input mode), if the Pi_j bit in the Pi register is read, the input level of the corresponding pin is read.
If the Pi_j bit in the Pi register is read when the PDi_j bit is 1 (output mode), the port latch is read.

[When the IOINSEL bit in the PINSR register is 1]
If the Pi register is read, the input level of the corresponding pin is read regardless of the setting of the PDi register.

12.3 Port 1

Figure 12.1 shows the Port 1 Pin Configuration.

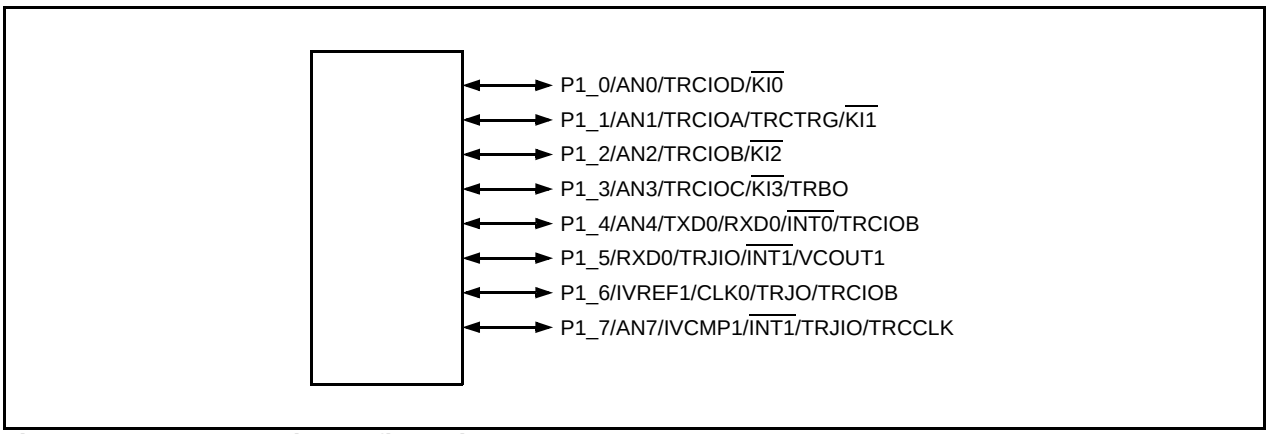


Figure 12.1 Port 1 Pin Configuration

12.3.1 Port P1 Direction Register (PD1)

Address 000A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD1_0	Port P1_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PD1_1	Port P1_1 direction bit		R/W
b2	PD1_2	Port P1_2 direction bit		R/W
b3	PD1_3	Port P1_3 direction bit		R/W
b4	PD1_4	Port P1_4 direction bit		R/W
b5	PD1_5	Port P1_5 direction bit		R/W
b6	PD1_6	Port P1_6 direction bit		R/W
b7	PD1_7	Port P1_7 direction bit		R/W

The PD1 register is used to select whether I/O ports are used as input or output.
Each bit in the PD1 register corresponds to individual ports.

12.3.2 Port P1 Register (P1)

Address 000AFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1_0	Port P1_0 bit	0: Low level 1: High level	R/W
b1	P1_1	Port P1_1 bit		R/W
b2	P1_2	Port P1_2 bit		R/W
b3	P1_3	Port P1_3 bit		R/W
b4	P1_4	Port P1_4 bit		R/W
b5	P1_5	Port P1_5 bit		R/W
b6	P1_6	Port P1_6 bit		R/W
b7	P1_7	Port P1_7 bit		R/W

The P1 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P1 register. The P1 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P1 register corresponds to individual ports.

12.3.3 Pull-Up Control Register 1 (PUR1)

Address 000B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU1_7	PU1_6	PU1_5	PU1_4	PU1_3	PU1_2	PU1_1	PU1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU1_0	Port P1_0 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b1	PU1_1	Port P1_1 pull-up control bit		R/W
b2	PU1_2	Port P1_2 pull-up control bit		R/W
b3	PU1_3	Port P1_3 pull-up control bit		R/W
b4	PU1_4	Port P1_4 pull-up control bit		R/W
b5	PU1_5	Port P1_5 pull-up control bit		R/W
b6	PU1_6	Port P1_6 pull-up control bit		R/W
b7	PU1_7	Port P1_7 pull-up control bit		R/W

The PUR1 register is used to control the port P1 pull-up resistors. I/O ports are pulled up when the corresponding PD1_j bit (j = 0 to 7) in the PD1 register is set to 0 (input mode (functions as an I/O port)) and the PU1_j bit (j = 0 to 7) in the PUR1 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD1_j bit is set to 0 and the PU1_j bit is set to 1.
Do not set the corresponding PU1_j bit to 1 for the output pins for peripheral functions.

12.3.4 Drive Capacity Control Register 1 (DRR1)

Address 000BBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	DRR1_5	DRR1_4	DRR1_3	DRR1_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	—
b1	—			
b2	DRR1_2	Port P1_2 drive capacity control bit	0: Low drive capacity 1: High drive capacity (1)	R/W
b3	DRR1_3	Port P1_3 drive capacity control bit		R/W
b4	DRR1_4	Port P1_4 drive capacity control bit		R/W
b5	DRR1_5	Port P1_5 drive capacity control bit		R/W
b6	—	Reserved	Set to 0.	—
b7	—			

Note:
1. Both H and L output are set to high drive capacity.

The DRR1 register is used to select the drive capacity of the output transistors (low or high) when P1 is set to output (an output port or a peripheral function output pin). The drive capacity of the corresponding output transistors is high when the DRR1_j bit (j = 2 to 5) in the DRR1 register is set to 1.

12.3.5 Open-Drain Control Register 1 (POD1)

Address 000C1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD1_7	POD1_6	POD1_5	POD1_4	POD1_3	POD1_2	POD1_1	POD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POD1_0	Port P1_0 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b1	POD1_1	Port P1_1 open-drain control bit		R/W
b2	POD1_2	Port P1_2 open-drain control bit		R/W
b3	POD1_3	Port P1_3 open-drain control bit		R/W
b4	POD1_4	Port P1_4 open-drain control bit		R/W
b5	POD1_5	Port P1_5 open-drain control bit		R/W
b6	POD1_6	Port P1_6 open-drain control bit		R/W
b7	POD1_7	Port P1_7 open-drain control bit		R/W

The POD1 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD1_j bit (j = 0 to 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.3.6 Port 1 Function Mapping Register 0 (PML1)

Address 000C8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P13SEL1	P13SEL0	P12SEL1	P12SEL0	P11SEL1	P11SEL0	P10SEL1	P10SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P10SEL0	Port P1_0 function select bits	b1 b0 0 0: I/O port or AN0 input 0 1: TRCIOD 1 0: $\overline{KI0}$ 1 1: Do not set.	R/W
b1	P10SEL1			R/W
b2	P11SEL0	Port P1_1 function select bits	b3 b2 0 0: I/O port or AN1 input 0 1: TRCIOA/TRCTRG 1 0: $\overline{KI1}$ 1 1: Do not set.	R/W
b3	P11SEL1			R/W
b4	P12SEL0	Port P1_2 function select bits	b5 b4 0 0: I/O port or AN2 input 0 1: TRCIOB 1 0: $\overline{KI2}$ 1 1: Do not set.	R/W
b5	P12SEL1			R/W
b6	P13SEL0	Port P1_3 function select bits	b7 b6 0 0: I/O port or AN3 input 0 1: TRCIOC 1 0: $\overline{KI3}$ 1 1: TRBO	R/W
b7	P13SEL1			R/W

The PML1 register is used to select the functions of pins P1_0 to P1_3.

12.3.7 Port 1 Function Mapping Register 1 (PMH1)

Address 000C9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P17SEL1	P17SEL0	P16SEL1	P16SEL0	P15SEL1	P15SEL0	P14SEL1	P14SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P14SEL0	Port P1_4 function select bits	bx b1 b0 0 0 0: I/O port or AN4 input 0 0 1: TXD0 0 1 0: RXD0 0 1 1: INT0 1 0 0: TRCIOB Other than the above: Do not set. (bx: P14SEL2 bit in the PMH1E register)	R/W
b1	P14SEL1			R/W
b2	P15SEL0	Port P1_5 function select bits	bx b3 b2 0 0 0: I/O port 0 0 1: RXD0 0 1 0: TRJIO 0 1 1: INT1 1 0 0: VCOUT1 Other than the above: Do not set. (bx: P15SEL2 bit in the PMH1E register)	R/W
b3	P15SEL1			R/W
b4	P16SEL0	Port P1_6 function select bits	b5 b4 0 0: I/O port or IVREF1 input 0 1: CLK0 1 0: TRJO 1 1: TRCIOB	R/W
b5	P16SEL1			R/W
b6	P17SEL0	Port P1_7 function select bits	b7 b6 0 0: I/O port or AN7 input or IVCMP1 input 0 1: INT1 1 0: TRJIO 1 1: TRCCLK	R/W
b7	P17SEL1			R/W

The PMH1 register is used to select the functions of pins P1_4 to P1_7.

12.3.8 Port 1 Function Mapping Expansion Register (PMH1E)

Address 000D1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	P15SEL2	—	P14SEL2
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P14SEL2	The P1_4 pin function is selected in conjunction with bits P14SEL0 to P14SEL1 in the PMH1 register. For details, see **12.3.7 Port 1 Function Mapping Register 1 (PMH1)**.		R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	P15SEL2	The P1_5 pin function is selected in conjunction with bits P15SEL0 to P15SEL1 in the PMH1 register. For details, see **12.3.7 Port 1 Function Mapping Register 1 (PMH1)**.		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

The PMH1E register is used to select the port 1 function in conjunction with registers PML1 and PMH1.

12.3.9 Pin Settings for Port 1

Tables 12.4 to 12.11 list the pin settings for port 1.

Table 12.4 Port P1_0/AN0/TRCIOD/$\overline{KI0}$

Register	PD1	ADINSEL			PML1		Timer RC Setting	Function
Bit	PD1_0	ADGSEL		CH0	P10SEL			
		1	0		1	0		
Setting value	0	X	X	X	0	0	X	Input port
	1	X	X	X	0	0	X	Output port
	0	0	0	0	0	0	X	A/D converter input (AN0)
	X	X	X	X	0	1	See **Table 12.24 TRCIOD Pin Settings**.	TRCIOD input
	X	X	X	X	0	1	See **Table 12.24 TRCIOD Pin Settings**.	TRCIOD output
	X	X	X	X	1	0	X	$\overline{KI0}$ input

X: 0 or 1

Table 12.5 Port P1_1/AN1/TRCIOA/TRCTRG/$\overline{KI1}$

Register	PD1	ADINSEL			PML1		Timer RC Setting	Function
Bit	PD1_1	ADGSEL		CH0	P11SEL			
		1	0		1	0		
Setting value	0	X	X	X	0	0	X	Input port
	1	X	X	X	0	0	X	Output port
	0	0	0	1	0	0	X	A/D converter input (AN1)
	X	X	X	X	0	1	See **Table 12.21 TRCIOA Pin Settings**.	TRCIOA input or TRCTRG input
	X	X	X	X	0	1	See **Table 12.21 TRCIOA Pin Settings**.	TRCIOA output
	X	X	X	X	1	0	X	$\overline{KI1}$ input

X: 0 or 1

Table 12.6 Port P1_2/AN2/TRCIOB/$\overline{KI2}$

Register	PD1	ADINSEL			PML1		Timer RC Setting	Function
Bit	PD1_2	ADGSEL		CH0	P12SEL			
		1	0		1	0		
Setting value	0	X	X	X	0	0	X	Input port
	1	X	X	X	0	0	X	Output port
	0	0	1	0	0	0	X	A/D converter input (AN2)
	X	X	X	X	0	1	See **Table 12.22 TRCIOB Pin Settings**.	TRCIOB input
	X	X	X	X	0	1	See **Table 12.22 TRCIOB Pin Settings**.	TRCIOB output
	X	X	X	X	1	0	X	$\overline{KI2}$ input

X: 0 or 1

Table 12.7 Port P1_3/AN3/TRCIOC/$\overline{KI3}$/TRBO

Register	PD1	ADINSEL			PML1		Timer RC Setting	Timer RB2 Setting	Function
Bit	PD1_3	ADGSEL		CH0	P13SEL				
		1	0		1	0			
Setting value	0	X	X	X	0	0	X	X	Input port
	1	X	X	X	0	0	X	X	Output port
	0	0	1	1	0	0	X	X	A/D converter input (AN3)
	X	X	X	X	0	1	See **Table 12.23 TRCIOC Pin Settings**.	X	TRCIOC input
	X	X	X	X	0	1	See **Table 12.23 TRCIOC Pin Settings**.	X	TRCIOC output
	X	X	X	X	1	0	X	X	$\overline{KI3}$ input
	X	X	X	X	1	1	X	X	TRBO output

X: 0 or 1

Table 12.8 Port P1_4/AN4/TXD0/RXD0/$\overline{\text{INT0}}$/TRCIOB

Register	PD1	ADINSEL			PMH1E	PMH1		Timer RC Setting	Function
Bit	PD1_4	ADGSEL		CH0	P14SEL2	P14SEL			
		1	0			1	0		
Setting value	0	X	X	X	0	0	0	X	Input port
	1	X	X	X	0	0	0	X	Output port
	0	1	0	0	0	0	0	X	A/D converter input (AN4)
	X	X	X	X	0	0	1	X	TXD0 output
	X	X	X	X	0	1	0	X	RXD0 input
	X	X	X	X	0	1	1	X	$\overline{\text{INT0}}$ input
	X	X	X	X	1	0	0	See **Table 12.22 TRCIOB Pin Settings**.	TRCIOB input
	X	X	X	X	1	0	0	See **Table 12.22 TRCIOB Pin Settings**.	TRCIOB output

X: 0 or 1

Table 12.9 Port P1_5/RXD0/TRJIO/$\overline{\text{INT1}}$/VCOUT1

Register	PD1	PMH1E	PMH1		TRJIOC	TRJMR			Function
Bit	PD1_5	P15SEL2	P15SEL		TOPCR	TMOD			
			1	0		2	1	0	
Setting value	0	0	0	0	X	X	X	X	Input port
	1	0	0	0	X	X	X	X	Output port
	X	0	0	1	X	X	X	X	RXD0 input
	X	0	1	0	0	Other than 000b, 001b			TRJIO input
	X	0	1	0	0	001b			TRJIO pulse output
	X	0	1	1	X	X	X	X	$\overline{\text{INT1}}$ input
	X	1	0	0	X	X	X	X	VCOUT1 output

X: 0 or 1

Table 12.10 Port P1_6/IVREF1/CLK0/TRJO/TRCIOB

Register	PD1	PMH1		U0MR				Timer RC Setting	Function
Bit	PD1_6	P16SEL		SMD			CKDIR		
		1	0	2	1	0			
Setting value	0	0	0	X	X	X	X	X	Input port/IVREF1
	1	0	0	X	X	X	X	X	Output port
	X	0	1	X	X	X	1	X	CLK0 (external clock) input
	X	0	1	0	0	1	0	X	CLK0 (internal clock) output
	X	1	0	X	X	X	X	X	TRJO output
	X	1	1	X	X	X	X	See **Table 12.22 TRCIOB Pin Settings**.	TRCIOB input
	X	1	1	X	X	X	X	See **Table 12.22 TRCIOB Pin Settings**.	TRCIOB output

X: 0 or 1

Table 12.11 Port P1_7/AN7/IVCMP1/$\overline{\text{INT1}}$/TRJIO/TRCCLK

Register	PD1	ADINSEL			PML1		TRJIOC	TRJMR			Function
Bit	PD1_7	ADGSEL		CH0	P17SEL		TOPCR	TMOD			
		1	0		1	0		2	1	0	
Setting value	0	X	X	X	0	0	X	X	X	X	Input port
	1	X	X	X	0	0	X	X	X	X	Output port
	0	1	0	1	0	0	X	X	X	X	A/D converter input (AN7)
	X	X	X	X	0	1	0	1	X	X	$\overline{\text{INT1}}$ input
	X	X	X	X	1	0	0	Other than 000b, 001b			TRJIO input
	X	X	X	X	1	0	0	001b			TRJIO pulse output
	X	X	X	X	1	1	1	1	X	X	TRCCLK input

X: 0 or 1

12.4 Port 3

Figure 12.2 shows the Port 3 Pin Configuration.

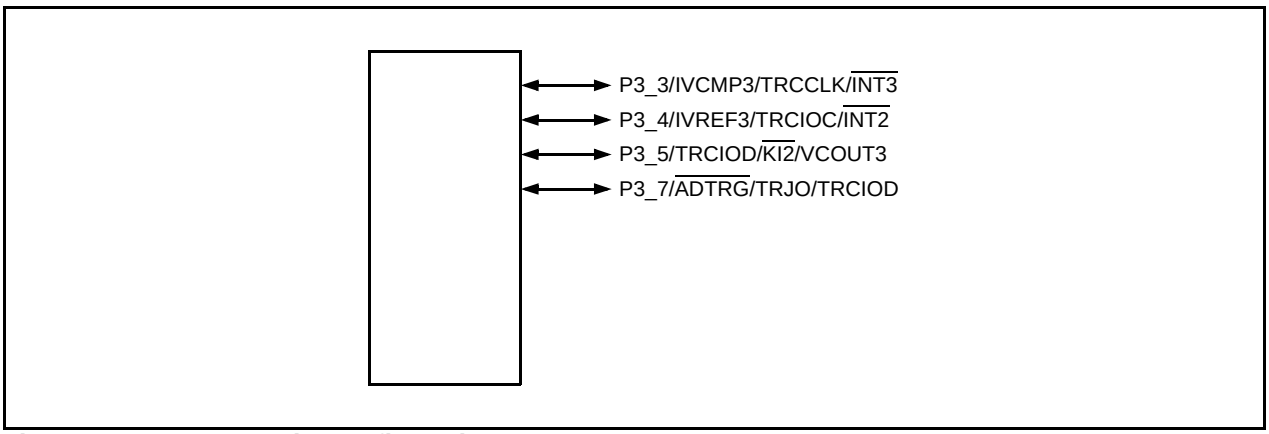


Figure 12.2 Port 3 Pin Configuration

12.4.1 Port P3 Direction Register (PD3)

Address 000ABh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD3_7	—	PD3_5	PD3_4	PD3_3	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	PD3_3	Port P3_3 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b4	PD3_4	Port P3_4 direction bit		R/W
b5	PD3_5	Port P3_5 direction bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	PD3_7	Port P3_7 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W

The PD3 register is used to select whether I/O ports are used as input or output.
Each bit in the PD3 register corresponds to individual ports.

12.4.2 Port P3 Register (P3)

Address 000B1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P3_7	—	P3_5	P3_4	P3_3	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	P3_3	Port P3_3 bit	0: Low level 1: High level	R/W
b4	P3_4	Port P3_4 bit		R/W
b5	P3_5	Port P3_5 bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	P3_7	Port P3_7 bit	0: Low level 1: High level	R/W

The P3 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P3 register. The P3 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P3 register corresponds to individual ports.

12.4.3 Pull-Up Control Register 3 (PUR3)

Address 000B7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU3_7	—	PU3_5	PU3_4	PU3_3	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	PU3_3	Port P3_3 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b4	PU3_4	Port P3_4 pull-up control bit		R/W
b5	PU3_5	Port P3_5 pull-up control bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	PU3_7	Port P3_7 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W

The PUR3 register is used to control the port P3 pull-up resistors. I/O ports are pulled up when the corresponding PD3_j bit (j = 3 to 5, or 7) in the PD3 register is set to 0 (input mode (functions as an I/O port)) and the PU3_j bit (j = 3 to 5, or 7) in the PUR3 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD3_j bit is set to 0 and the PU3_j bit is set to 1.
Do not set the corresponding PU3_j bit to 1 for the output pins for peripheral functions.

12.4.4 Drive Capacity Control Register 3 (DRR3)

Address 000BDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DRR3_7	—	DRR3_5	DRR3_4	DRR3_3	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	DRR3_3	Port P3_3 drive capacity control bit	0: Low drive capacity 1: High drive capacity (1)	R/W
b4	DRR3_4	Port P3_4 drive capacity control bit		R/W
b5	DRR3_5	Port P3_5 drive capacity control bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	DRR3_7	Port P3_7 drive capacity control bit	0: Low drive capacity 1: High drive capacity (1)	R/W

Note:
1. Both H and L output are set to high drive capacity.

The DRR3 register is used to select the drive capacity of the output transistors (low or high) when P3 is set to output (an output port or a peripheral function output pin). The drive capacity of the corresponding output transistors is high when the DRR3_j bit (j = 3 to 5, or 7) in the DRR3 register is set to 1.

12.4.5 Open-Drain Control Register 3 (POD3)

Address 000C3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD3_7	—	POD3_5	POD3_4	POD3_3	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	POD3_3	Port P3_3 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b4	POD3_4	Port P3_4 open-drain control bit		R/W
b5	POD3_5	Port P3_5 open-drain control bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	POD3_7	Port P3_7 open-drain control bit	0: Not open-drain 1: Open-drain	R/W

The POD3 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD3_j bit (j = 3 to 5, or 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.4.6 Port 3 Function Mapping Register 0 (PML3)

Address 000CCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P33SEL1	P33SEL0	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	P33SEL0	Port P3_3 function select bits	b7 b6 0 0: I/O port or IVCMP3 input 0 1: $\overline{\text{TRCCLK}}$ 1 0: $\overline{\text{INT3}}$ 1 1: Do not set.	R/W
b7	P33SEL1			R/W

The PML3 register is used to select the P3_3 pin function.

12.4.7 Port 3 Function Mapping Register 1 (PMH3)

Address 000CDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P37SEL1	P37SEL0	—	—	P35SEL1	P35SEL0	P34SEL1	P34SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P34SEL0	Port P3_4 function select bits	b1 b0 0 0: I/O port or IVREF3 input 0 1: TRCIOC 1 0: INT2 1 1: Do not set.	R/W
b1	P34SEL1			R/W
b2	P35SEL0	Port P3_5 function select bits	b3 b2 0 0: I/O port 0 1: TRCIOD 1 0: KI2 1 1: VCOUT3	R/W
b3	P35SEL1			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	P37SEL0	Port P3_7 function select bits	b7 b6 0 0: I/O port 0 1: ADTRG 1 0: TRJO 1 1: TRCIOD	R/W
b7	P37SEL1			R/W

The PMH3 register is used to select the functions of pins P3_4, P3_5, and P3_7.

12.4.8 Pin Settings for Port 3

Tables 12.12 to 12.15 list the pin settings for port 3.

Table 12.12 Port P3_3/IVCMP3/TRCCLK/$\overline{\text{INT3}}$

Register	PD3	PMH3		Function
Bit	PD3_3	P33SEL		
		1	0	
Setting value	0	0	0	Input port/IVCMP3
	1	0	0	Output port
	X	0	1	TRCCLK input
	X	1	0	$\overline{\text{INT3}}$ input

X: 0 or 1

Table 12.13 Port P3_4/IVREF3/TRCIOC/$\overline{\text{INT2}}$

Register	PD3	PMH3		Timer RC Setting	Function
Bit	PD3_4	P34SEL			
		1	0		
Setting value	0	0	0	X	Input port/IVREF3
	1	0	0	X	Output port
	X	0	1	See **Table 12.23 TRCIOC Pin Settings**.	TRCIOC input
	X	0	1	See **Table 12.23 TRCIOC Pin Settings**.	TRCIOC output
	X	1	0	X	$\overline{\text{INT2}}$ input

X: 0 or 1

Table 12.14 Port P3_5/TRCIOD/$\overline{\text{KI2}}$/VCOUT3

Register	PD3	PMH3		Timer RC Setting	Function
Bit	PD3_5	P35SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.24 TRCIOD Pin Settings**.	TRCIOD input
	X	0	1	See **Table 12.24 TRCIOD Pin Settings**.	TRCIOD output
	X	1	0	X	$\overline{\text{KI2}}$ input
	X	1	1	X	VCOUT3 output

X: 0 or 1

Table 12.15 Port P3_7/$\overline{\text{ADTRG}}$/TRJO/TRCIOD

Register	PD3	PMH3		Timer RC Setting	Function
Bit	PD3_7	P37SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	X	$\overline{\text{ADTRG}}$ input
	X	1	0	X	TRJO output
	X	1	1	See **Table 12.24 TRCIOD Pin Settings**.	TRCIOD input
	X	1	1	See **Table 12.24 TRCIOD Pin Settings**.	TRCIOD output

X: 0 or 1

12.5 Port 4

Figure 12.3 shows the Port 4 Pin Configuration.

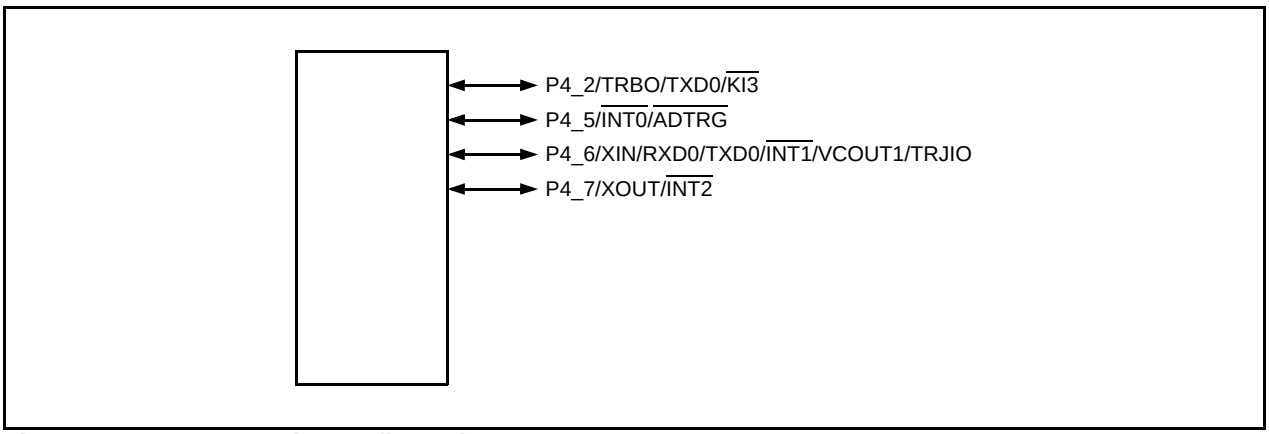


Figure 12.3 Port 4 Pin Configuration

12.5.1 Port P4 Direction Register (PD4)

Address 000ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD4_7	PD4_6	PD4_5	—	—	PD4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	PD4_2	Port P4_2 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	PD4_5	Port P4_5 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b6	PD4_6	Port P4_6 direction bit		R/W
b7	PD4_7	Port P4_7 direction bit		R/W

The PD4 register is used to select whether I/O ports are used as input or output.
Each bit in the PD4 register corresponds to individual ports.

12.5.2 Port P4 Register (P4)

Address 000B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P4_7	P4_6	P4_5	—	—	P4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	P4_2	Port P4_2 bit	0: Low level 1: High level	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	P4_5	Port P4_5 bit	0: Low level 1: High level	R/W
b6	P4_6	Port P4_6 bit		R/W
b7	P4_7	Port P4_7 bit		R/W

The P4 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P4 register. The P4 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pin. Each bit in the P4 register corresponds to individual ports.

12.5.3 Pull-Up Control Register 4 (PUR4)

Address 000B8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU4_7	PU4_6	PU4_5	—	—	PU4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	PU4_2	Port P4_2 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	PU4_5	Port P4_5 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b6	PU4_6	Port P4_6 pull-up control bit		R/W
b7	PU4_7	Port P4_7 pull-up control bit		R/W

The PUR4 register is used to control the port P4 pull-up resistors. I/O ports are pulled up when the corresponding PD4_j bit (j = 2, or 5 to 7) in the PD4 register is set to 0 (input mode (functions as I/O port)) and the PU4_j bit (j = 2, or 5 to 7) in the PUR4 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD4_j bit is set to 0 and the PU4_j bit is set to 1.
Do not set the corresponding PU4_j bit to 1 for the output pins for peripheral functions.

12.5.4 Open-Drain Control Register 4 (POD4)

Address 000C4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD4_7	POD4_6	POD4_5	—	—	POD4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	POD4_2	Port P4_2 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	POD4_5	Port P4_5 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b6	POD4_6	Port P4_6 open-drain control bit		R/W
b7	POD4_7	Port P4_7 open-drain control bit		R/W

The POD4 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD4_j bit (j = 2, or 5 to 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.5.5 Port 4 Function Mapping Register 0 (PML4)

Address 000CEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	P42SEL1	P42SEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	P42SEL0	Port P4_2 function select bits	b5 b4 0 0: I/O port 0 1: TRBO 1 0: $\overline{\text{TXD0}}$ 1 1: $\overline{\text{KI3}}$	R/W
b5	P42SEL1			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The PML4 register is used to select the P4_2 pin function.

12.5.6 Port 4 Function Mapping Register 1 (PMH4)

Address 000CFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P47SEL1	P47SEL0	P46SEL1	P46SEL0	P45SEL1	P45SEL0	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	P45SEL0	Port P4_5 function select bits	b3 b2 0 0: I/O port 0 1: $\overline{\text{INT0}}$ 1 0: $\overline{\text{ADTRG}}$ 1 1: Do not set.	R/W
b3	P45SEL1			R/W
b4	P46SEL0	Port P4_6 function select bits	bx b5 b4 0 0 0: I/O port or XIN input 0 0 1: RXD0 0 1 0: $\overline{\text{TXD0}}$ 0 1 1: $\overline{\text{INT1}}$ 1 0 0: VCOUT1 1 0 1: TRJIO Other than the above: Do not set. (bx: P46SEL2 bit in the PMH4E register)	R/W
b5	P46SEL1			R/W
b6	P47SEL0	Port P4_7 function select bits	b7 b6 0 0: I/O port or XOUT output 0 1: $\overline{\text{INT2}}$ Other than the above: Do not set.	R/W
b7	P47SEL1			R/W

The PMH4 register is used to select the functions of pins P4_5 to P4_7.

12.5.7 Port 4 Function Mapping Expansion Register (PMH4E)

Address 000D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	P46SEL2	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	P46SEL2	The P4_6 pin function is selected in conjunction with bits P46SEL0 to P46SEL1 in the PMH4 register. For details, see **12.5.6 Port 4 Function Mapping Register 1 (PMH4)**.		R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

The PMH4E register is used to select the port 4 function in conjunction with registers PML4 and PMH4.

12.5.8 Pin Settings for Port 4

Tables 12.16 to 12.19 list the pin settings for port 4.

Table 12.16 Port P4_2/TRBO/TXD0/$\overline{KI3}$

Register	PD4	PML4		Function
Bit	PD4_2	P42SEL		
		1	0	
Setting value	0	0	0	Input port
	1	0	0	Output port
	X	0	1	TRBO output
	X	1	0	TXD0 output
	X	1	1	$\overline{INT3}$ input

X: 0 or 1

Table 12.17 Port P4_5/$\overline{INT0}$/$\overline{ADTRG}$

Register	PD4	PMH4		Function
Bit	PD4_5	P45SEL		
		1	0	
Setting value	0	0	0	Input port
	1	0	0	Output port
	X	0	1	$\overline{INT0}$ input
	X	1	0	$\overline{ADTRG}$ input

X: 0 or 1

Table 12.18 Port P4_6/XIN/RXD0/TXD0/$\overline{INT1}$/VCOUT1/TRJIO

Register	PD4	PMH4E	PMH4		EXCKCR		TRJIOC	TRJMR			Function
Bit	PD4_6	P46SEL2	P46SEL		CKPT		TOPCR	TMOD			
			1	0	1	0		2	1	0	
Setting value	0	0	0	0	X	0	X	X	X	X	Input port
	1	0	0	0	X	0	X	X	X	X	Output port
	X	0	0	0	0	1	X	X	X	X	XIN clock input (external clock input)
	X	0	0	0	1	1	X	X	X	X	XIN oscillation
	X	0	0	1	X	X	X	X	X	X	RXD0 input
	X	0	1	0	X	X	X	X	X	X	TXD0 output
	X	0	1	1	X	X	X	X	X	X	$\overline{INT1}$ input
	X	1	0	0	X	X	X	X	X	X	VCOUT1 output
	X	1	0	1	X	X	0	Other than 000b, 001b			TRJIO input
	X	1	0	1	X	X	0	001b			TRJIO output

X: 0 or 1

Table 12.19 Port P4_7/XOUT/$\overline{INT2}$

Register	PD4	PMH4		EXCKCR		Function
Bit	PD4_7	P47SEL		CKPT		
		1	0	1	0	
Setting value	0	0	0	0	X	Input port
	1	0	0	0	X	Output port
	X	0	0	1	0	System clock (f) output
	X	0	0	1	1	XOUT output
	X	0	1	X	X	$\overline{INT2}$ input

X: 0 or 1

12.6 Port A

Figure 12.4 shows the Port A Pin Configuration.

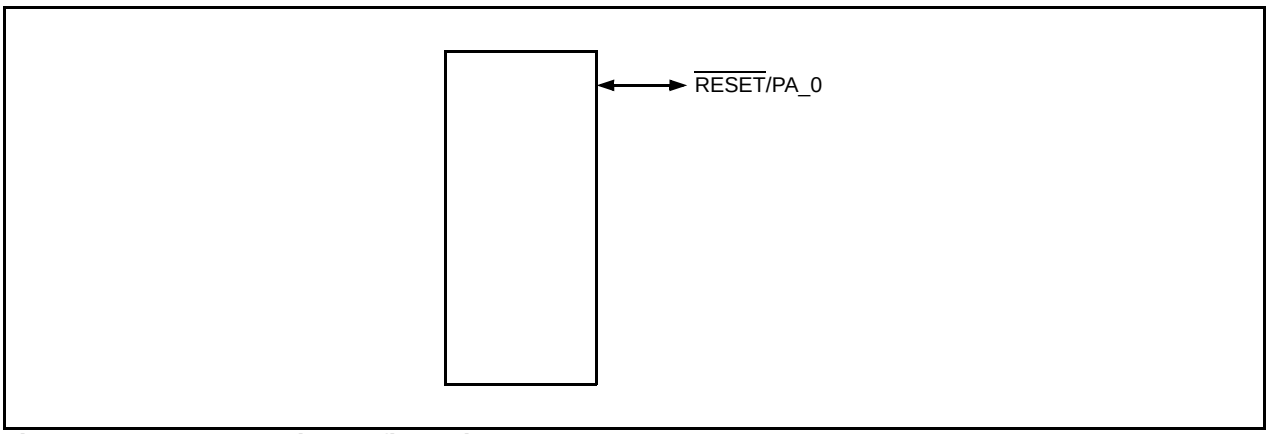


Figure 12.4 Port A Pin Configuration

12.6.1 Port PA Direction Register (PDA)

Address 000ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PDA_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDA_0	Port PA_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The PDA register is used to select whether PA_0 is used as input or output.

12.6.2 Port PA Register (PA)

Address 000B3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PA_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PA_0	Port PA_0 bit	0: Low level 1: High level	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The PA register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the PA register. The PA register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pin.

12.6.3 Port PA Mode Control Register (PAMCR)

Address 000C5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	HWRSTE	—	—	—	PODA_0
After Reset	0	0	0	1	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	PODA_0	Port PA_0 open-drain control bit (1)	0: Not open-drain 1: Open-drain	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	HWRSTE	Hardware reset enabled bit	0: Port PA_0 functions as an I/O port 1: Port PA_0 functions as a hardware reset ($\overline{\text{RESET}}$)	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

Note:
1. Setting this bit to 1 (open-drain) enables N-channel open-drain output and setting this bit to 0 (not open-drain) enables CMOS output.

The PAMCR register is used to control the port PA open-drain and the port A function. The open-drain is enabled when the peripheral function or output port function is selected.
Set the PAMCRE bit in the HRPR register to 1 (write enabled) before rewriting the PAMCR register.

12.6.4 Pin Setting for Port A

Table 12.20 lists the pin setting for port A.

Table 12.20 $\overline{\text{RESET}}$/Port PA_0

Register	PDA	PAMCR	Function
Bit	PDA_0	HWRSTE	
Setting value	X	1	$\overline{\text{RESET}}$
	0	0	Input port (1)
	1	0	Output port (2)

X: 0 or 1
Notes:
1. Connect a pull-up resistor. For details, see **12.11.1 Notes on PA_0 Pin**.
2. Setting the PODA_0 bit to 1 enables N-channel open-drain output.

12.7 Procedure for Setting Peripheral Functions Associated with Ports 1, 3, and 4

After a reset, use the following procedure to set the peripheral functions associated with ports 1, 3, and 4.
(1) Set the function mapping registers for ports 1, 3, and 4.
(2) Set the operating mode for the peripheral functions.
(3) Start operation of the peripheral functions.

12.8 Pin Settings for Peripheral Function I/O

Tables 12.21 to 12.24 list the pin settings for peripheral function I/O.

Table 12.21 TRCIOA Pin Settings

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting value	0	1	0	0	1	X	X	Timer mode waveform output (output compare function)
				1	X			
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1							
	1	0	X	X	X	0	1	PWM2 mode (TRCTRG input)
						1	X	

X: 0 or 1

Table 12.22 TRCIOB Pin Settings

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.23 TRCIOC Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.24 TRCIOD Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

12.9 Handling of Unused Pins

Table 12.25 lists the Handling of Unused Pins. Figure 12.5 shows the Handling of Unused Pins.

Table 12.25 Handling of Unused Pins

Pin Name	Connection
Ports P1, P3_3 to P3_5, P3_7, P4_2, P4_5 to 4_7	• Set each of these pins to input mode, and either connect the pin to VSS through a resistor (pull-down) or connect it to VCC through a resistor (pull-up). (2) • Set each of these pins to output mode and leave it open. (2, 3)
$\overline{\text{RESET}}$/PA_0 (1)	Connect to VCC through a pull-up resistor. (2)

Notes:
1. When the power-on reset is used.
2. Use lines that are as short as possible (2 cm or shorter) to handle unused pins in the vicinity of the MCU.
3. When these ports are set to output mode and left open, keep the following in mind. They remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be unstable and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. The program should periodically reconfigure the content for enhanced reliability.

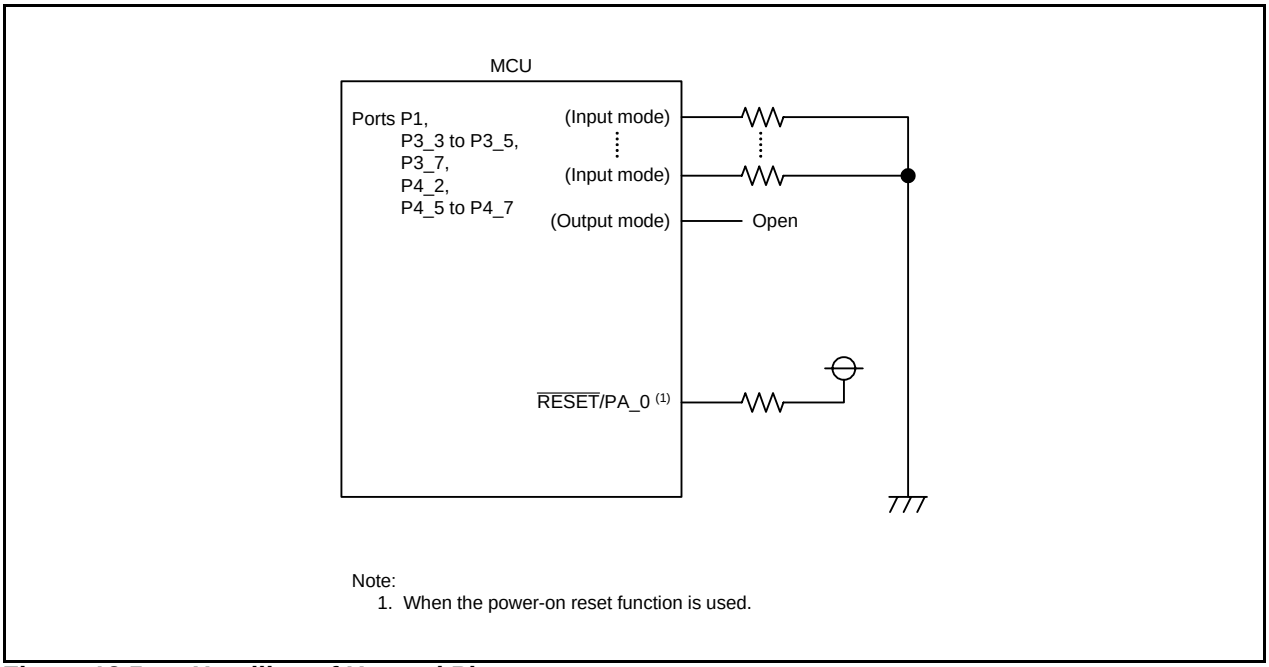


Figure 12.5 Handling of Unused Pins

12.10 I/O Port Configuration

Figures 12.6 to 12.18 show the I/O Port Configuration. Figure 12.19 shows the Pin Configuration.

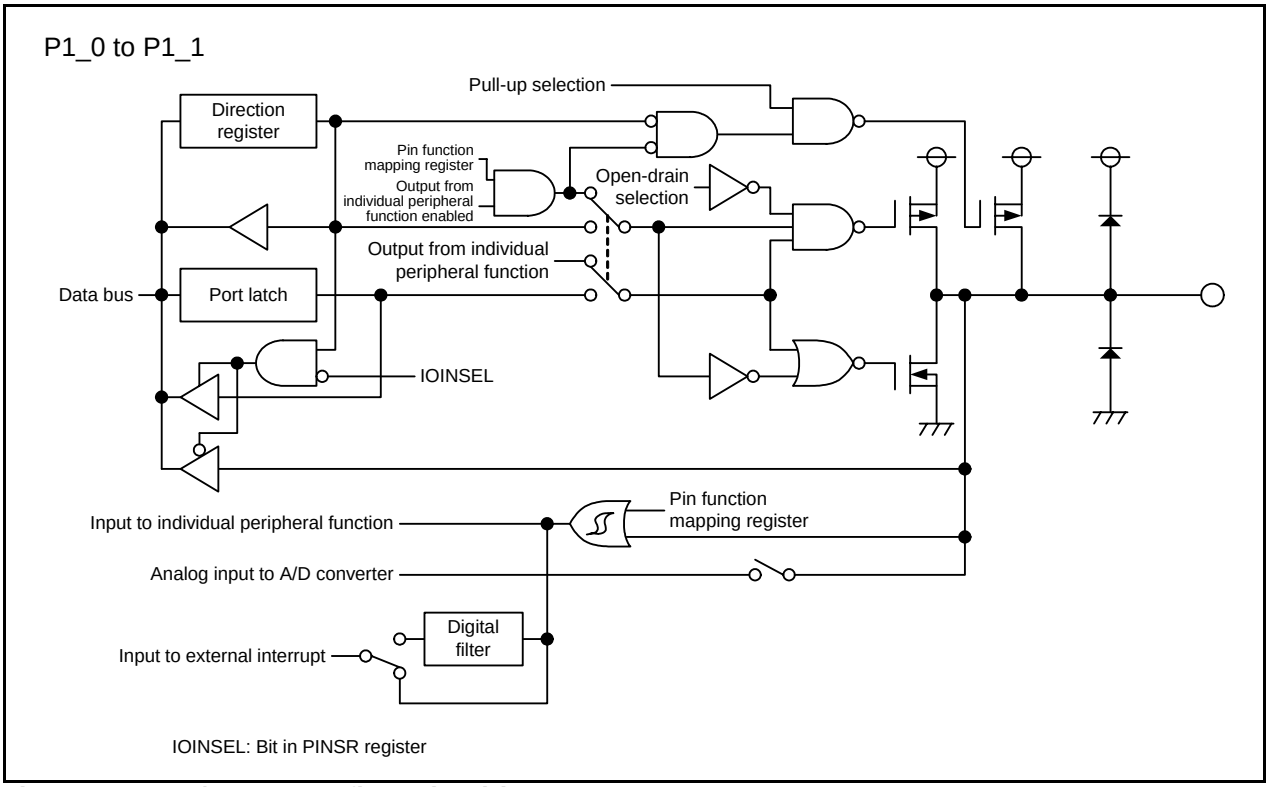


Figure 12.6 I/O Port Configuration (1)

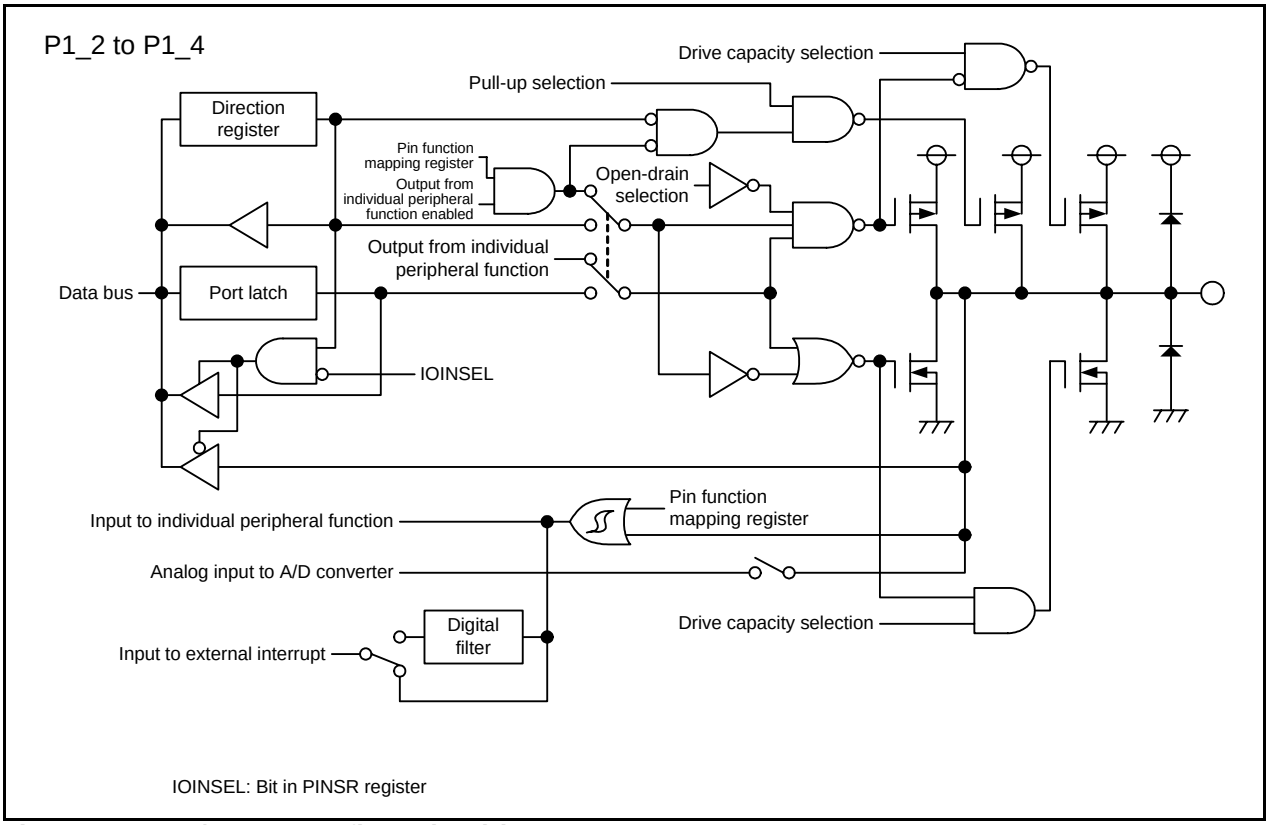


Figure 12.7 I/O Port Configuration (2)

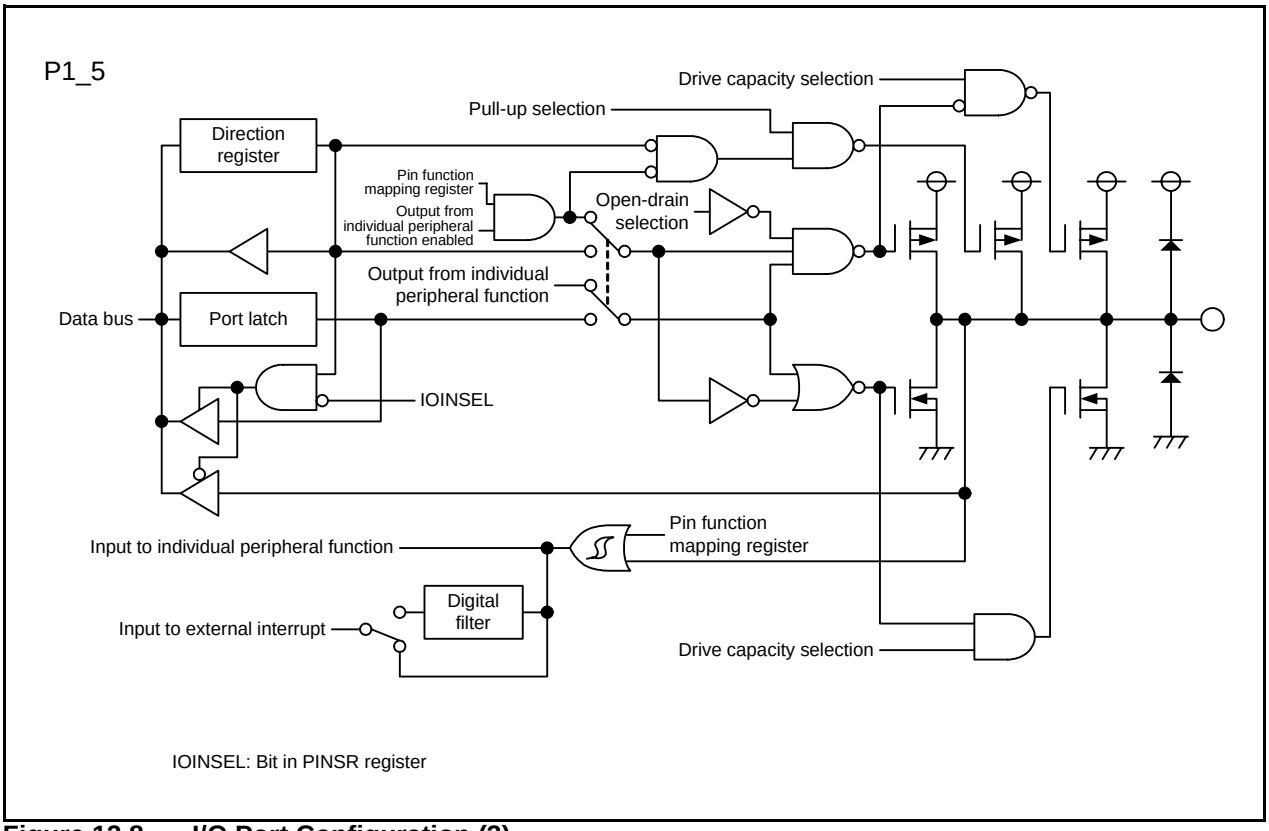


Figure 12.8 I/O Port Configuration (3)

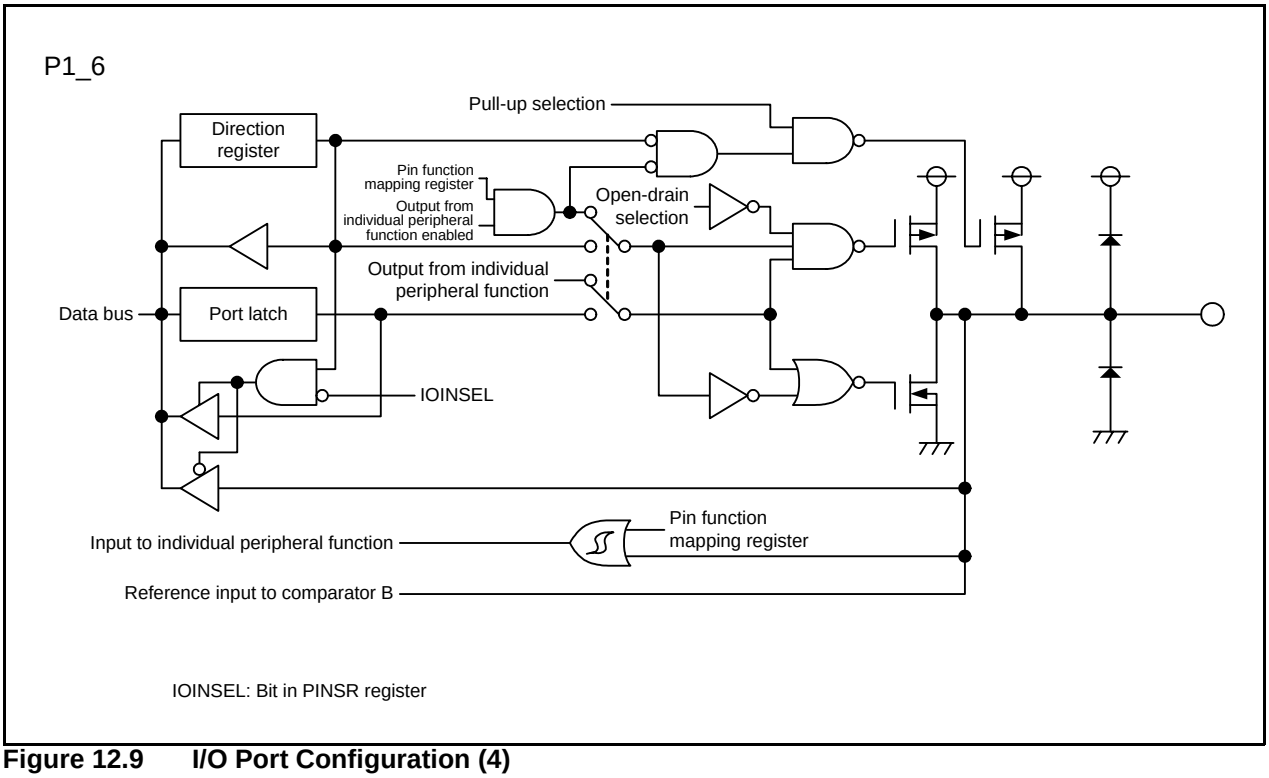


Figure 12.9 I/O Port Configuration (4)

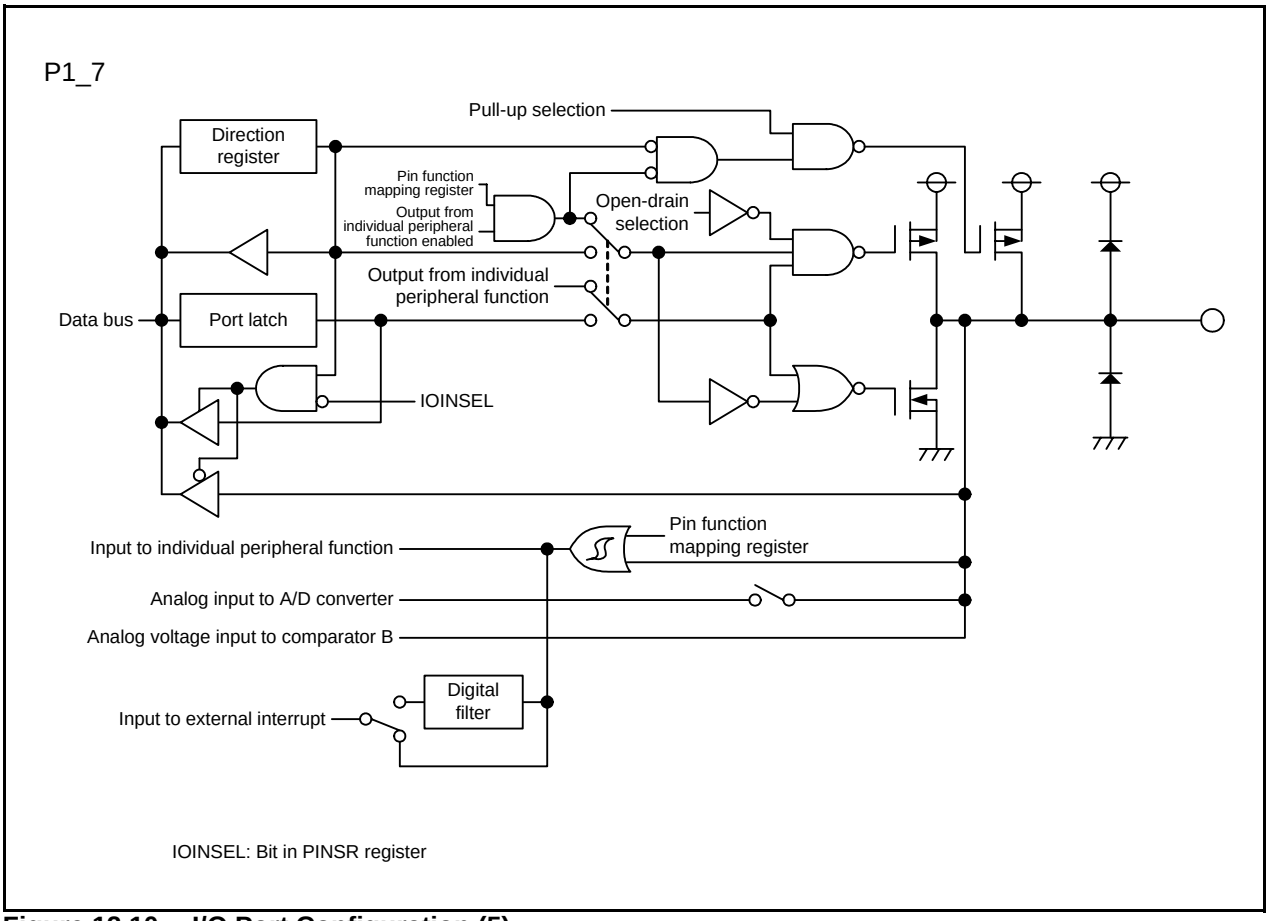


Figure 12.10 I/O Port Configuration (5)

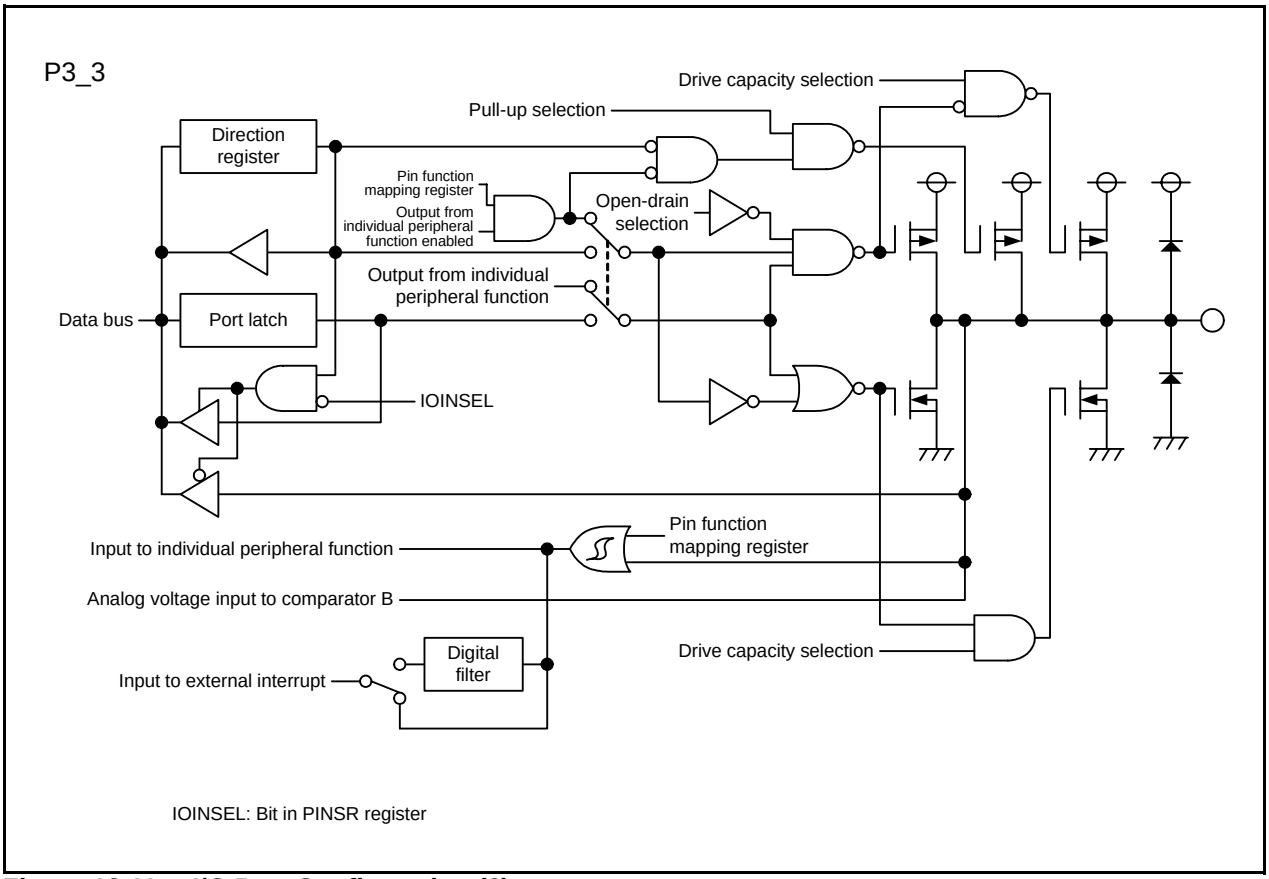


Figure 12.11 I/O Port Configuration (6)

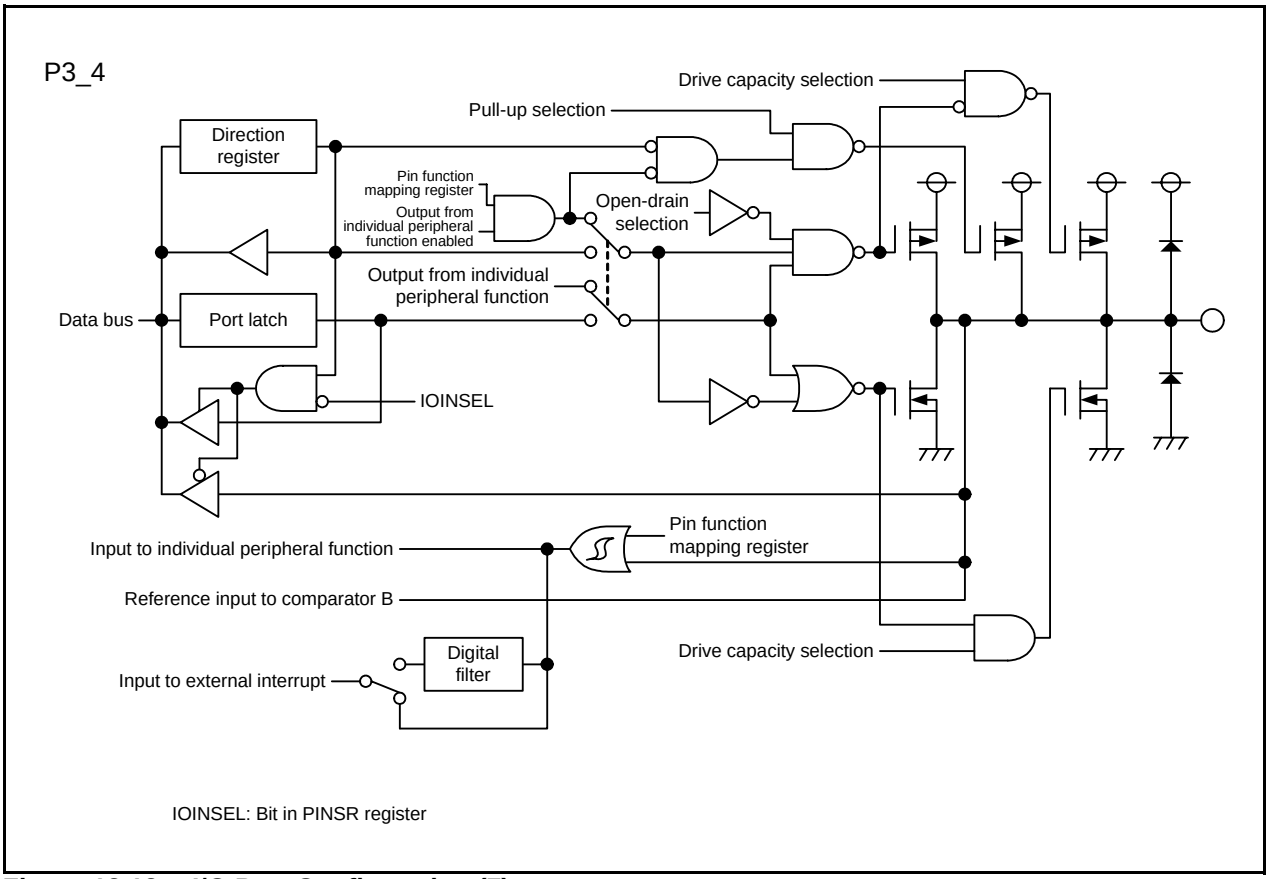


Figure 12.12 I/O Port Configuration (7)

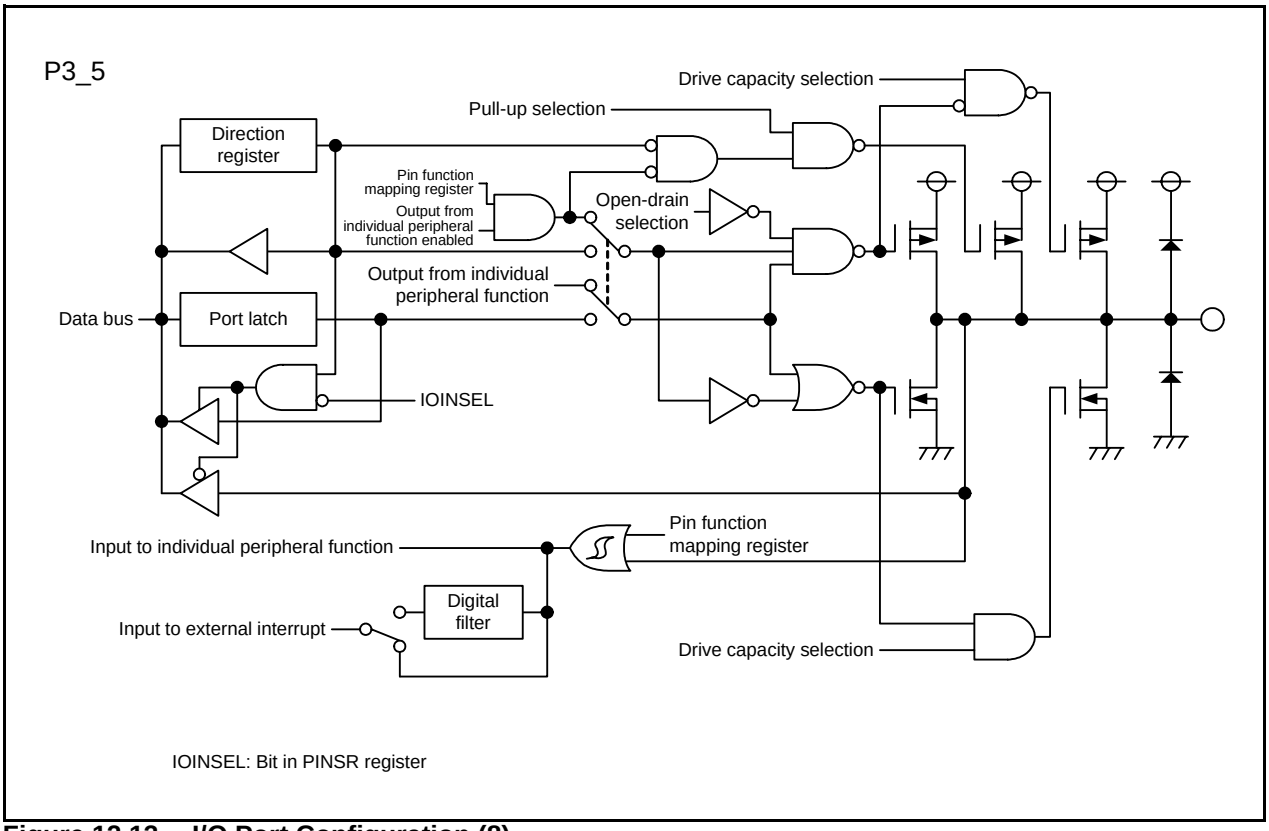


Figure 12.13 I/O Port Configuration (8)

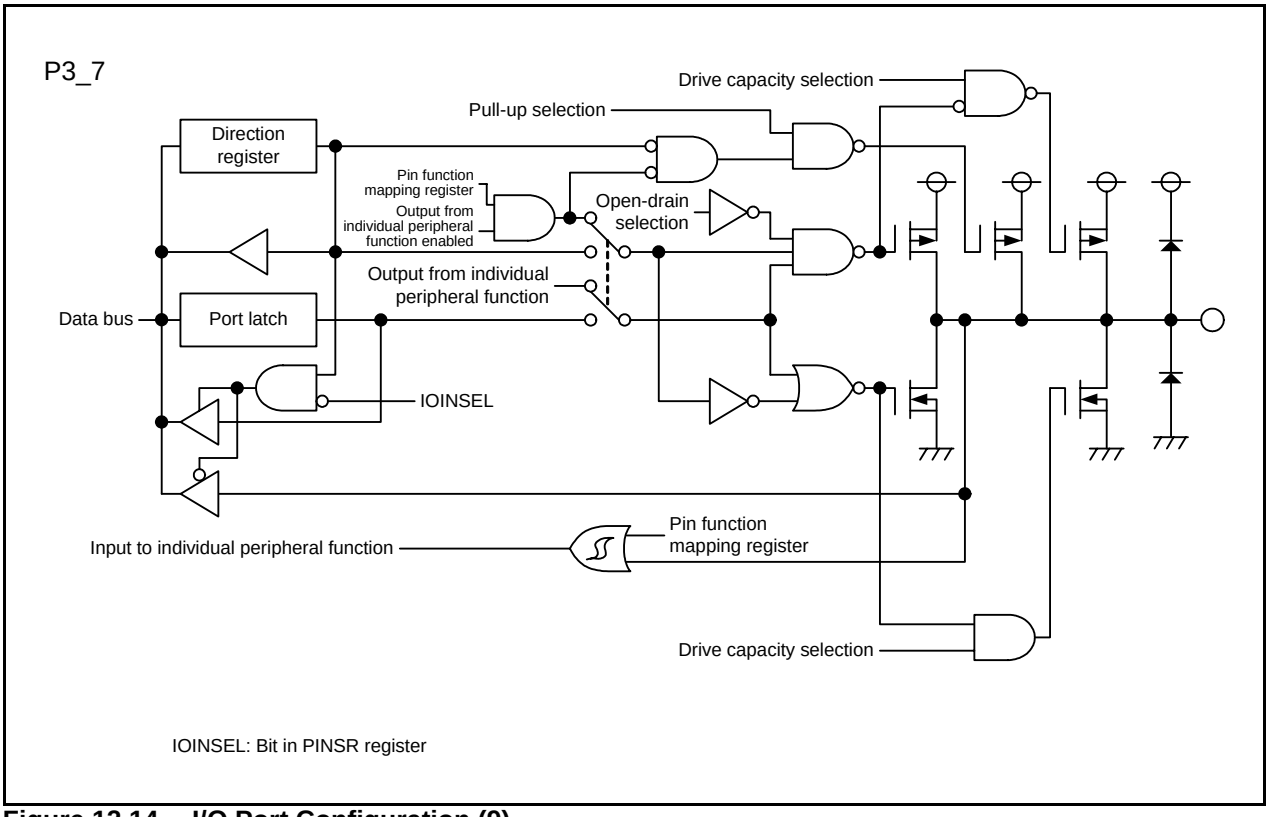


Figure 12.14 I/O Port Configuration (9)

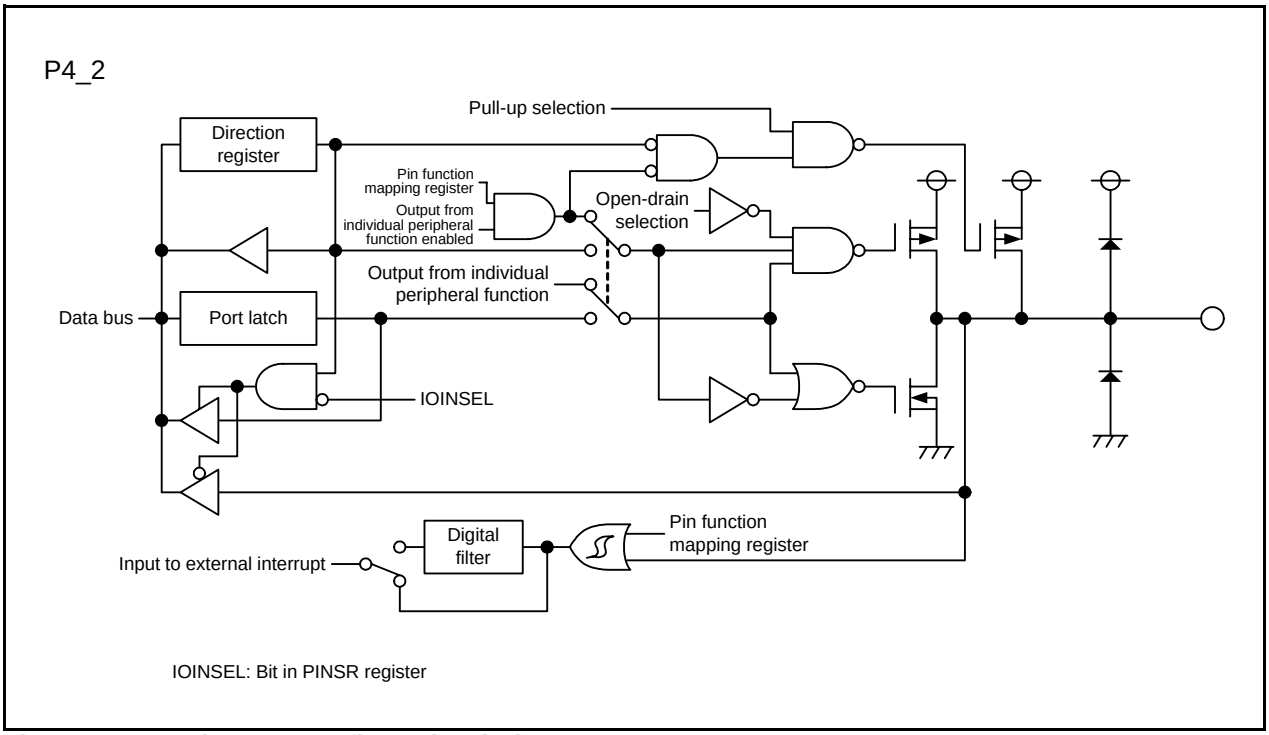


Figure 12.15 I/O Port Configuration (10)

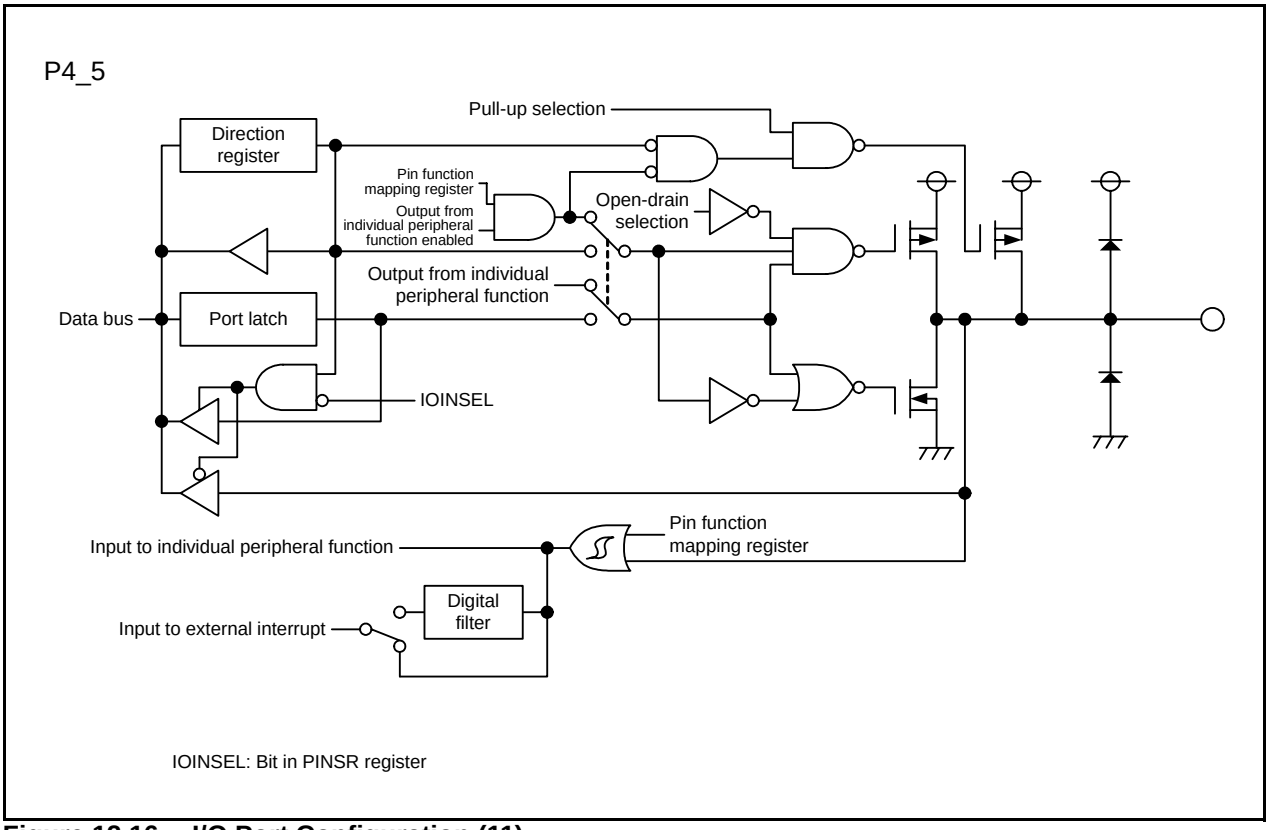


Figure 12.16 I/O Port Configuration (11)

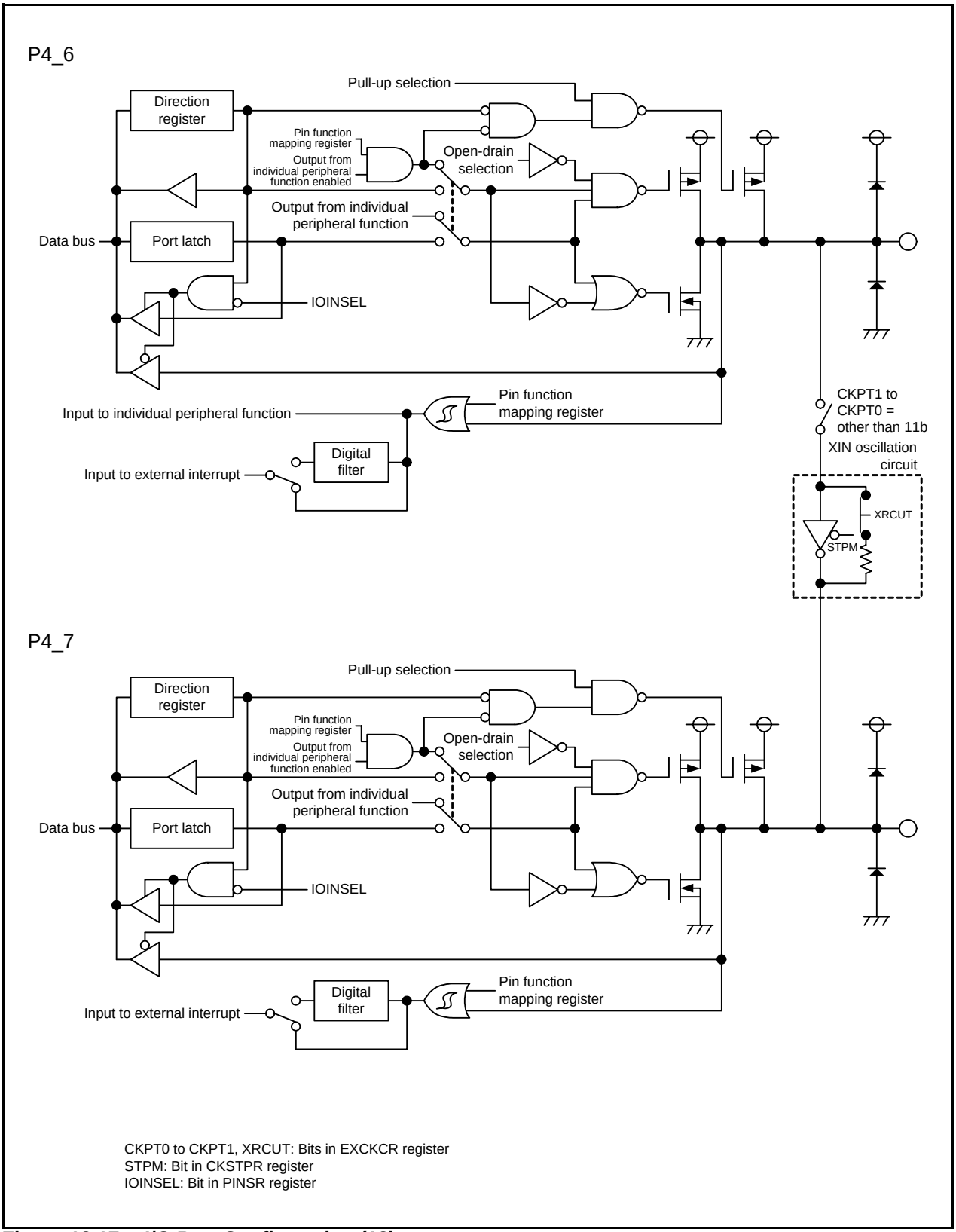


Figure 12.17 I/O Port Configuration (12)

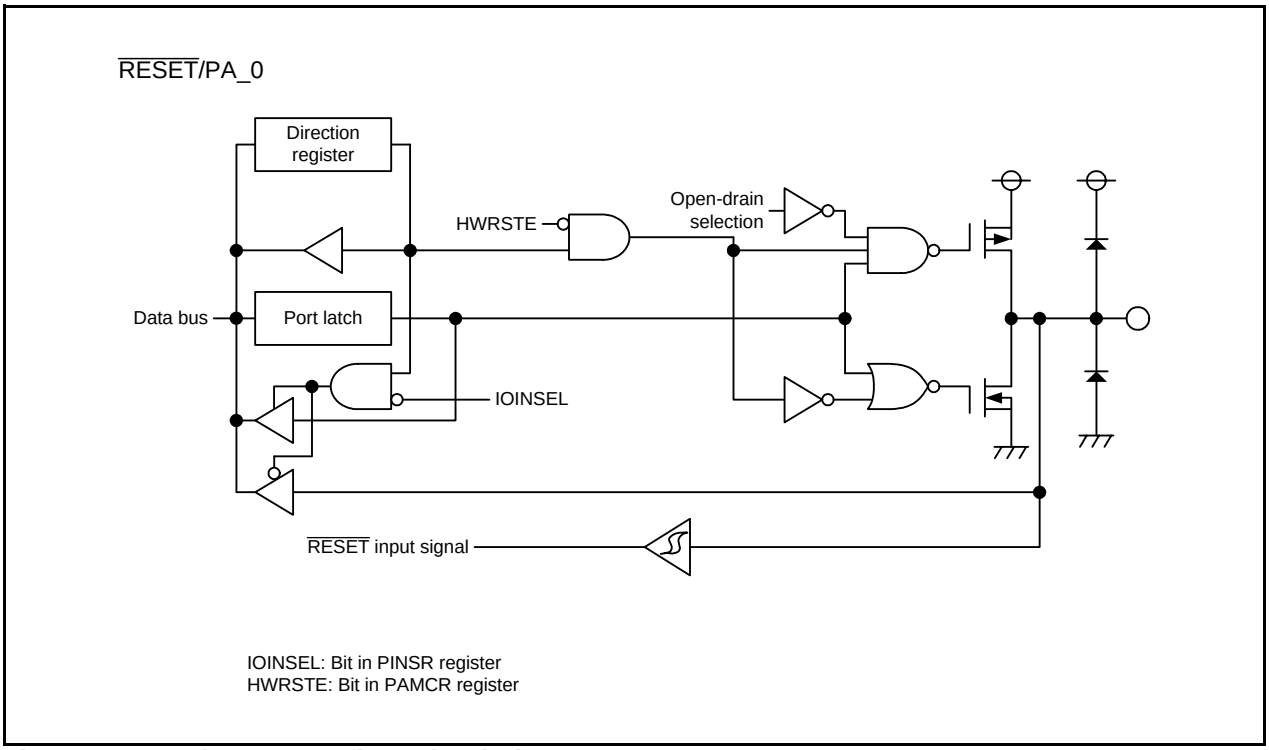


Figure 12.18 I/O Port Configuration (13)

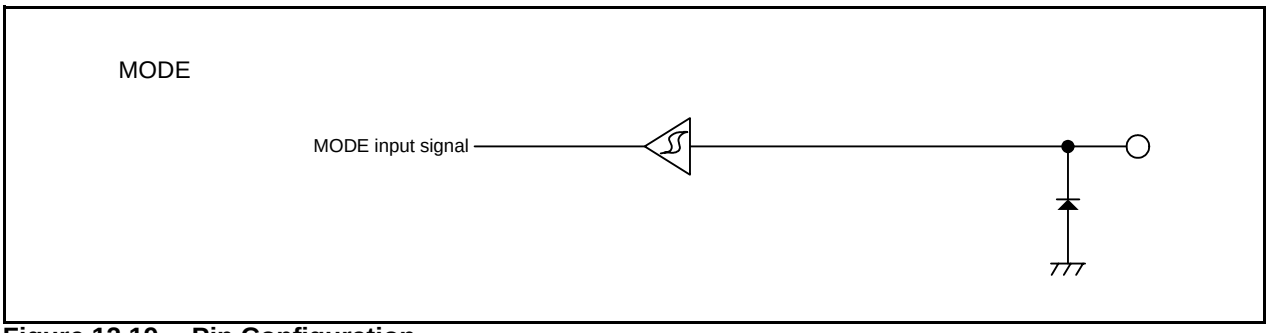


Figure 12.19 Pin Configuration

12.11 Notes on I/O Ports

12.11.1 Notes on PA_0 Pin

The PA_0 pin is multiplexed with the hardware reset function ($\overline{\text{RESET}}$). The PA_0 pin functions as the $\overline{\text{RESET}}$ function after any reset (hardware reset, power-on reset, voltage monitor 0 reset by voltage detection circuit, watchdog timer reset, and software reset) occurs. After the reset is cleared, the PA_0 pin can be set to the I/O port function or the hardware reset function by the HWRSTE bit in the PAMCR register. When a low level is input to the $\overline{\text{RESET}}$ pin before a reset is cleared, the level will be recognized by the MCU as hardware reset and the reset state will not be cleared until a high level is input to the $\overline{\text{RESET}}$ pin.
When the HWRSTE bit is set to 0, the $\overline{\text{RESET}}$/PA_0 pin becomes the PA_0 I/O port. When this pin is used as an input port, an external pull-up resistor must be connected. When used as an output port, the open-drain output function must be enabled to avoid conflicting with an external reset signal accidently. See the following assembly language.

• Program example to set PA_0 as an output port

```
MOV.B    #00000000b, HRPR
MOV.B    #00000001b, HRPR      ; PAMCRE = 1, un-protect PAMCR register
;
MOV.B    #00000001b, PAMCR     ; HWRSTE = 0, PODA_0 = 1
MOV.B    #00000001b, PDA       ; PDA_0 = 1, PA_0 output L
;
...
MOV.B    #00000001b, PA        ; PA_0 become hiz output (open drain)
```

12.11.2 I/O Pins for Peripheral Functions

In this MCU, the pin assignment of the peripheral functions can be changed using the port function mapping register. However, multiple pins must not be assigned to the same peripheral function input at the same time. Otherwise, no signal can be input correctly.

13. Timer RJ2

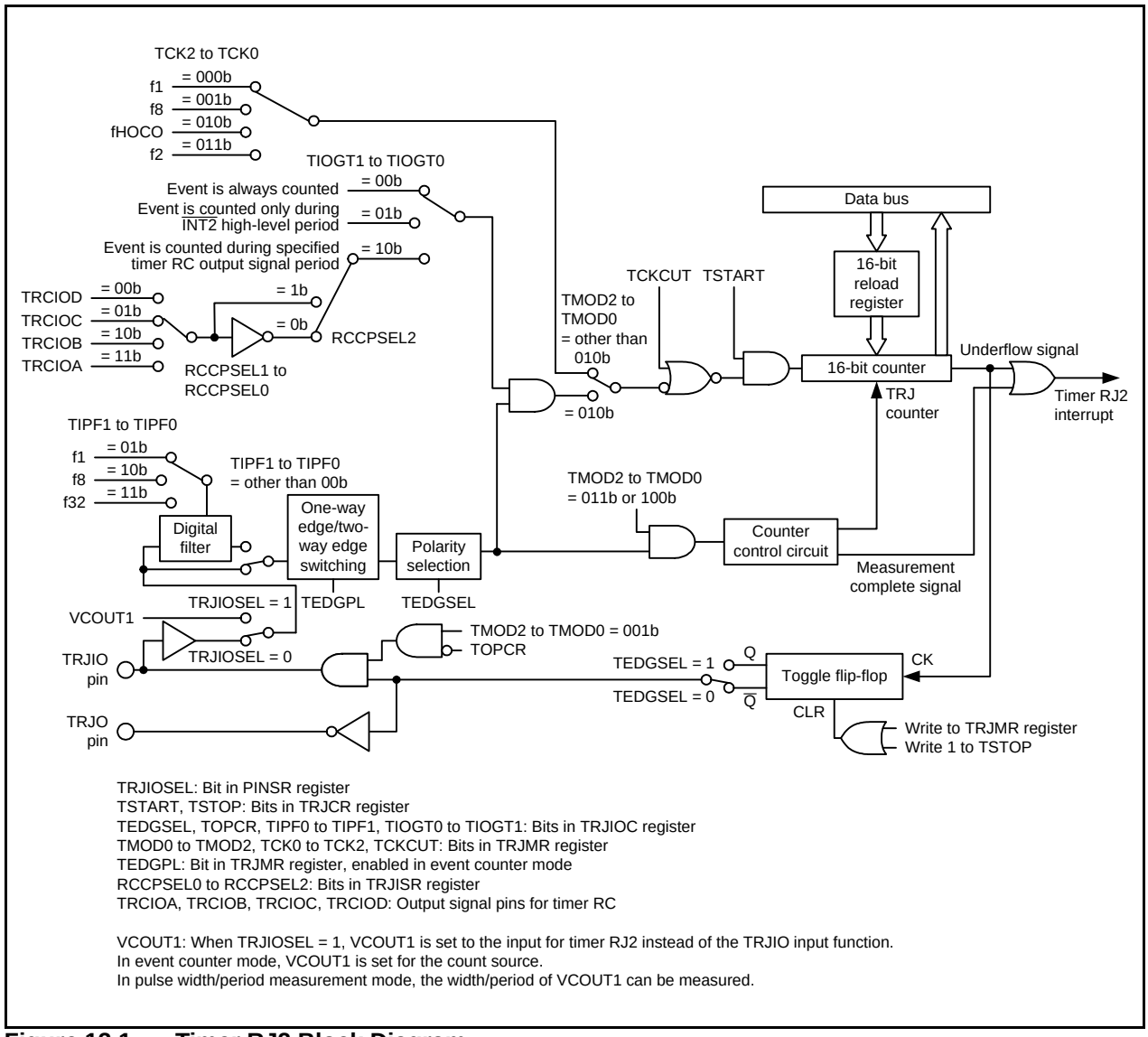
Timer RJ2 is a 16-bit timer that can be used for pulse output, external input pulse width or period measurement, and counting an internal source or external pulse. This timer consists of a reload register and down counter which are allocated to the same address.

13.1 Overview

Table 13.1 lists the Timer RJ2 Specifications. Figure 13.1 shows the Timer RJ2 Block Diagram.

Table 13.1 Timer RJ2 Specifications

Item		Description
Operating modes	Timer mode	The internal count source is counted.
	Pulse output mode	The internal count source is counted and the output is inverted at each underflow of the timer.
	Event counter mode	An external pulse is counted.
	Pulse width measurement mode	An external pulse width is measured.
	Pulse period measurement mode	An external pulse period is measured.
Count source		f1, f2, f8, fHOCO, or external pulse selectable
Interrupt		• When the counter underflows. • When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode. • When the set edge of the external input (TRJIO) is input in pulse period measurement mode.



TRJIOSEL: Bit in PINSR register
TSTART, TSTOP: Bits in TRJCR register
TEDGSEL, TOPCR, TIPF0 to TIPF1, TIOGT0 to TIOGT1: Bits in TRJIOC register
TMOD0 to TMOD2, TCK0 to TCK2, TCKCUT: Bits in TRJMR register
TEDGPL: Bit in TRJMR register, enabled in event counter mode
RCCPSEL0 to RCCPSEL2: Bits in TRJISR register
TRCIOA, TRCIOB, TRCIOC, TRCIOD: Output signal pins for timer RC

VCOUT1: When TRJIOSEL = 1, VCOUT1 is set to the input for timer RJ2 instead of the TRJIO input function.
In event counter mode, VCOUT1 is set for the count source.
In pulse width/period measurement mode, the width/period of VCOUT1 can be measured.

Figure 13.1 Timer RJ2 Block Diagram

13.2 I/O Pins

Table 13.2 lists the Timer RJ2 Pin Configuration.

Table 13.2 Timer RJ2 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT2}}$	P3_4, P4_7	I	Event counter mode count control
TRJIO (1)	P1_5, P1_7, P4_6	I/O	External pulse input and pulse output for timer RJ2
TRJO (1)	P1_6, P3_7	O	Pulse output for timer RJ2

Note:
1. When a pulse is output from TRJIO and TRJO simultaneously, TRJIO is set to the inverted output of TRJO.

13.3 Registers

Table 13.3 lists the Timer RJ2 Register Configuration.

Table 13.3 Timer RJ2 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RJ Counter Register	TRJ	FFh	000D8h	16
		FFh	000D9h	
Timer RJ Control Register	TRJCR	00h	000DAh	8
Timer RJ I/O Control Register	TRJIOC	00h	000DBh	8
Timer RJ Mode Register	TRJMR	00h	000DCh	8
Timer RJ Event Select Register	TRJISR	00h	000DDh	8
Timer RJ Interrupt Control Register	TRJIR	00h	000DEh	8

13.3.1 Timer RJ Counter Register (TRJ), Timer RJ Reload Register

Address 000D8h to 000D9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	Setting Range	R/W
b15 to b0	—	16-bit counter and reload register (1, 2, 3)	0001h to FFFFh	R/W

Notes:
1. When 1 is written to the TSTOP bit in the TRJCR register, the 16-bit counter is forcibly stopped and set to FFFFh.
2. The TRJ register must be accessed in 16-bit units. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units.
3. Do not set the TRJ register to 0000h in pulse width measurement mode and pulse period measurement mode.

TRJ is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.
The states of the reload register and the counter are changed depending on the TSTART bit in the TRJCR register. For details, see **13.4.1 Reload Register and Counter Rewrite Operation**.

13.3.2 Timer RJ Control Register (TRJCR)

Address 000DAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RJ count start bit (1)	0: Count is stopped 1: Count is started	R/W
b1	TCSTF	Timer RJ count status flag (1)	0: Count is stopped 1: Count is in progress	R
b2	TSTOP	Timer RJ count forced stop bit (2)	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	TEDGF	Active edge judgement flag	0: No active edge received 1: Active edge received	R/W
b5	TUNDF	Timer RJ underflow flag	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. For notes on using bits TSTART and TCSTF, see **13.5 Notes on Timer RJ2 (2)**.
2. When 1 (count is forcibly stopped) is written to the TSTOP bit, bits TSTART and TCSTF are initialized at the same time. The pulse output level is also initialized.

Use the MOV instruction to set the TRJCR register in pulse width measurement mode and pulse period measurement mode. To avoid changing TEDGF and TUNDF at this time, write 1 to these bits.

TSTART Bit (Timer RJ count start bit)

Count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count is started), the TCSTF bit is set to 1 (count is in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count is stopped) in synchronization with the count source. For details, see **13.5 Notes on Timer RJ2 (2)**.

TCSTF Bit (Timer RJ count status flag)

[Conditions for setting to 0]
- When 0 is written to the TSTART bit (the TCSTF bit is set to 0 in synchronization with the count source).
- When 1 is written to the TSTOP bit.

[Condition for setting to 1]
- When 1 is written to the TSTART bit (the TCSTF bit is set to 1 in synchronization with the count source).

TEDGF Bit (Active edge judgement flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Conditions for setting to 1]
- When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode.
- The set edge of the external input (TRJIO) is input in pulse period measurement mode.

TUNDF Bit (Timer RJ underflow flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Condition for setting to 1]
- When the counter underflows.

13.3.3 Timer RJ I/O Control Register (TRJIOC)

Address 000DBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	I/O polarity switch bit	Function varies depending on the operating mode.	R/W
b1	TOPCR	TRJIO output control bit	0: TRJIO output enabled (toggle output is started) 1: TRJIO output disabled (toggle output is stopped)	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	TIPF0	TRJIO input filter select bits	b5 b4 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJIO count control bits	b7 b6 0 0: Event is always counted 0 1: Event is counted only during $\overline{\text{INT2}}$ high-level period 1 0: Event is counted during timer RC output signal period specified by RCCPSEL bit in TRJISR register 1 1: Do not set.	R/W
b7	TIOGT1			R/W

TEDGSEL Bit (I/O polarity switch bit)

The TEDGSEL bit is used to switch the TRJO output polarity and the TRJIO I/O edge and polarity. In pulse output mode, only the inversion/non-inversion of toggle flip-flop is controlled. The toggle flip-flop is initialized when the TRJMR register is written or 1 is written to the TSTOP bit in the TRJCR register.

Table 13.4 TRJIO I/O Edge and Polarity Switching

Operating Mode	Function
Pulse output mode	0: Output is started at high 1: Output is started at low
Event counter mode	0: Count on rising edge 1: Count on falling edge
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge

Table 13.5 TRJO Output Polarity Switching

Operating Mode	Function
All modes	0: Output is started at low 1: Output is started at high

TOPCR Bit (TRJIO output control bit)

The TOPCR bit is enabled only in pulse output mode. When this bit is set to 0, a pulse can be output from the TRJIO pin. When it is set to 1, output is disabled and the port selected as the TRJIO function becomes high impedance.
In other operating modes, the functions listed in Table 13.6 are supported regardless of the setting of the TOPCR bit.

Table 13.6 TRJIO Pin Function

Operating Mode	Function
Timer mode	Not used
Event counter mode	Event input (count source input)
Pulse width measurement mode	Input for pulse width measurement
Pulse period measurement mode	Input for pulse period measurement

Bits TIPF0 to TIPF1 (TRJIO input filter select bits)

These bits are used to specify the sampling frequency of the filter for the TRJIO input. If the input to the TRJIO pin is sampled and the value matches three successive times, that value is taken as the input value.

Bits TIOGT0 to TIOGT1 (TRJIO count control bits)

These bits are enabled only in event counter mode.
They are used to select the period to count an event input from the TRJIO pin.
When bits TIOGT1 to TIOGT0 are set to 00b, an event is always counted.
When bits TIOGT1 to TIOGT0 are set to 01b, an event is counted while the $\overline{\text{INT2}}$ pin is held high.
When bits TIOGT1 to TIOGT0 are set to 10b, an event is counted for the period corresponding to the timer RC output set by the TRJISR register. Bits RCCPSEL0 to RCCPSEL1 in the TRJISR register are used to select the timer RC output signal and the RCCPSEL2 bit is used to select the level of the timer RC output signal.

13.3.4 Timer RJ Mode Register (TRJMR)

Address 000DCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RJ operating mode select bits	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Other than the above: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	TEDGPL	TRJIO edge polarity select bit	0: One-way edge 1: Two-way edge	R/W
b4	TCK0	Timer RJ count source select bits (1, 2)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fHOCO 0 1 1: f2 Other than the above: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RJ count source cutoff bit (2)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. When event counter mode is selected, the external input (TRJIO) is selected as the count source regardless of the setting of bits TCK0 to TCK2.
2. Do not switch or cut off the count source during count operation. When switching or cutting off the count source, set the TSTART bit in the TRJCR register to 0 (count is stopped) and the TCSTF bit to 0 (count is stopped) to stop the timer count.

Select the operating mode when the count is stopped (the TSTART bit is 0 and the TCSTF bit is 0).
When a value is written to the TRJMR register, the toggle flip-flop is initialized.

13.3.5 Timer RJ Event Select Register (TRJISR)

Address 000DDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	RCCPSEL2	RCCPSEL1	RCCPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCCPSEL0	Timer RC output signal select bits	b1 b0 0 0: TRCIOD 0 1: TRCIOC 1 0: TRCIOB 1 1: TRCIOA	R/W
b1	RCCPSEL1			R/W
b2	RCCPSEL2	Timer RC output signal inversion bit	0: Low-level period of timer RC output signal is counted 1: High-level period of timer RC output signal is counted	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

13.3.6 Timer RJ Interrupt Control Register (TRJIR)

Address 000DEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRJIE	TRJIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	TRJIF	Timer RJ interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b7	TRJIE	Timer RJ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

TRJIF Bit (Timer RJ interrupt request flag)

[Condition for setting to 0]
- When 0 is written to this bit after reading it as 1.

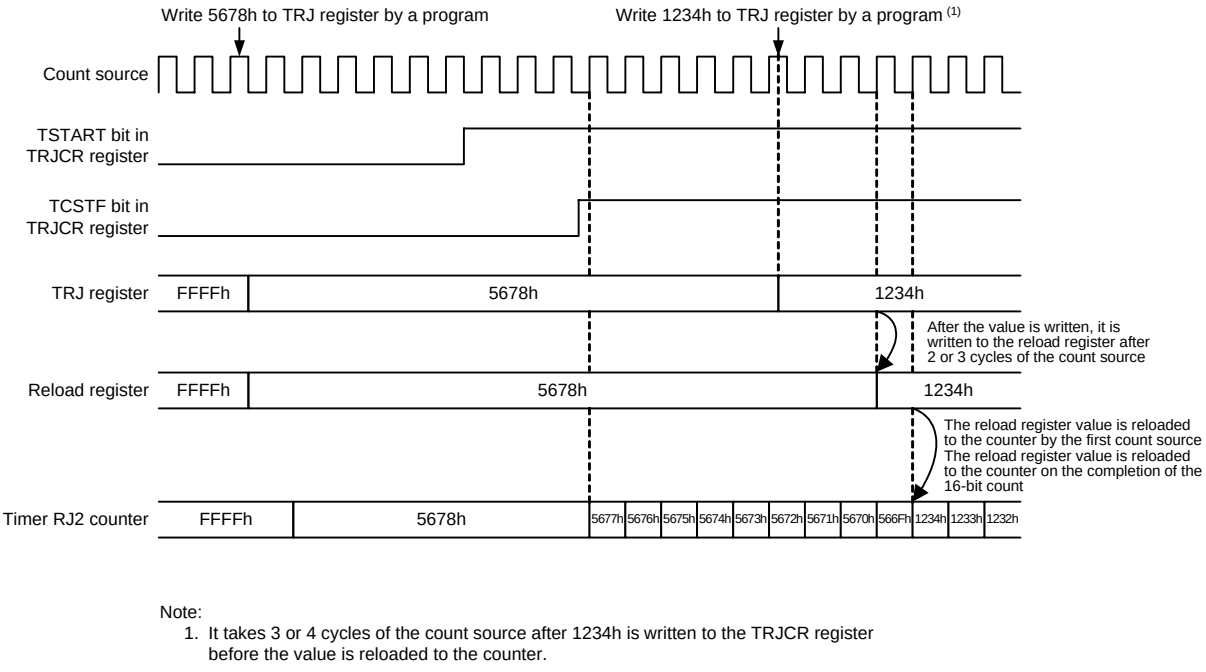
[Conditions for setting to 1]
- When timer RJ2 underflows.
- When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode.
- When the set edge of the external input (TRJIO) is input in pulse period measurement mode.

13.4 Operation

13.4.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value in the TSTART bit in the TRJCR register. When the TSTART bit is 0 (count is stopped), the count value is directly written to the reload register, and then to the counter in synchronization with the system clock (f). When the TSTART bit is 1 (count is started), the value is written to the reload register in synchronization with the count source after two or three cycles, and then to the counter in synchronization with the next count source.

Figure 13.2 shows the Timing of Rewrite Operation with TSTART Bit Value.



Note:
1. It takes 3 or 4 cycles of the count source after 1234h is written to the TRJCR register before the value is reloaded to the counter.

Figure 13.2 Timing of Rewrite Operation with TSTART Bit Value

13.4.2 Timer Mode

In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register.

The count value is decremented by 1 each time the count source is input, and an underflow occurs if the next count source is input after the count value reaches 0000h. The TRJIF bit in the TRJIR register is set to 1 (interrupt requested) at that time and the value set in the reload register is loaded simultaneously. When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.

Figure 13.3 shows an Operation Example in Timer Mode.

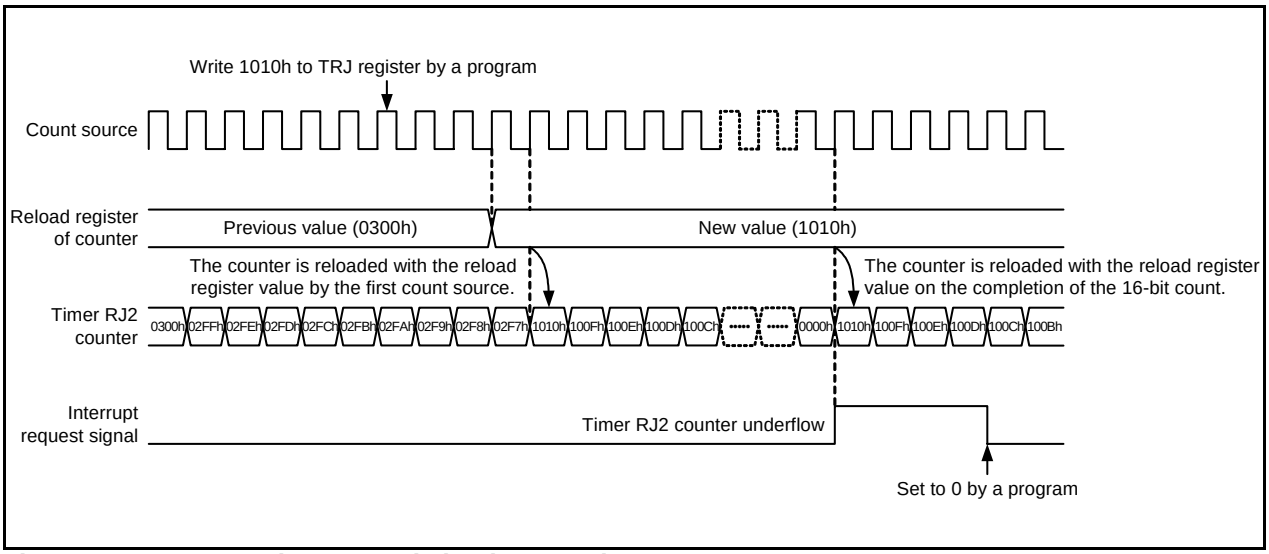
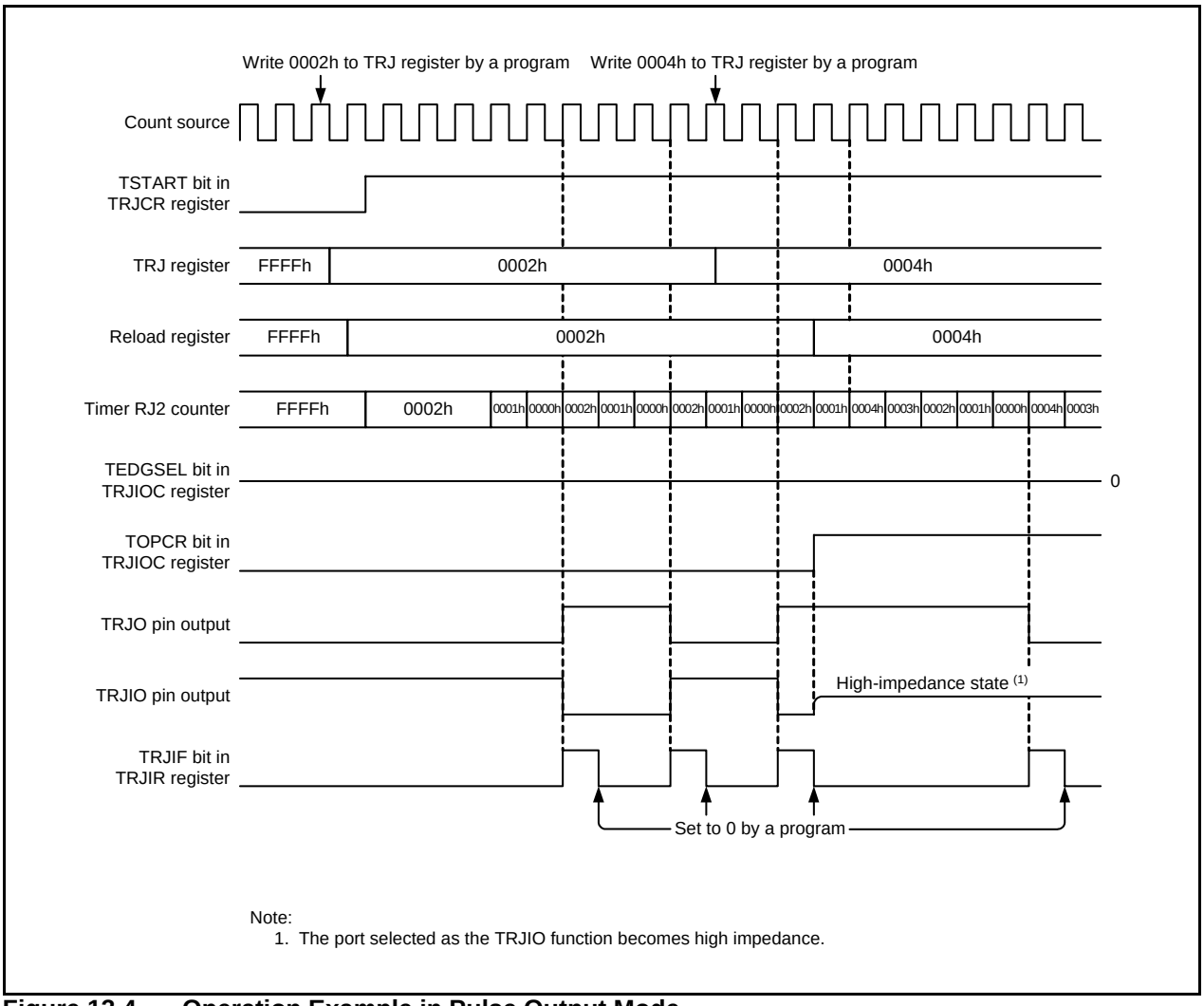


Figure 13.3 Operation Example in Timer Mode

13.4.3 Pulse Output Mode

In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register and a pulse is output from the TRJIO pin. The output level is inverted when an underflow occurs.
The count value is decremented by 1 each time the count source is input, and an underflow occurs if the next count source is input after the count value reaches 0000h. The TRJIF bit in the TRJIR register is set to 1 (interrupt requested) at that time and the value set in the reload register is loaded simultaneously. When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.
In addition, a pulse can be output from pins TRJIO and TRJO. The output level is inverted each time an underflow occurs. The pulse output from the TRJIO pin can be stopped by the TOPCR bit in the TRJIOC register.
Also, the output level can be selected by the TEDGSEL bit in the TRJIOC register.
Figure 13.4 shows an Operation Example in Pulse Output Mode.



Note:
1. The port selected as the TRJIO function becomes high impedance.

Figure 13.4 Operation Example in Pulse Output Mode

13.4.4 Event Counter Mode

In this mode, the counter is decremented by an external pulse signal input to the TRJIO pin.
Various periods for counting events can be set by bits TIOGT0 to TIOGT1 in the TRJIOC register and the TRJISR register. In addition, the filter function for the TRJIO input can be specified by bits TIPF0 to TIPF1 in the TRJIOC register.
Also, the output from the TRJO pin can be toggled even in event counter mode.
When event counter mode is used, see **13.5 Notes on Timer RJ2 (3) (8) (9)**.
Figure 13.5 shows an Operation Example in Event Counter Mode.

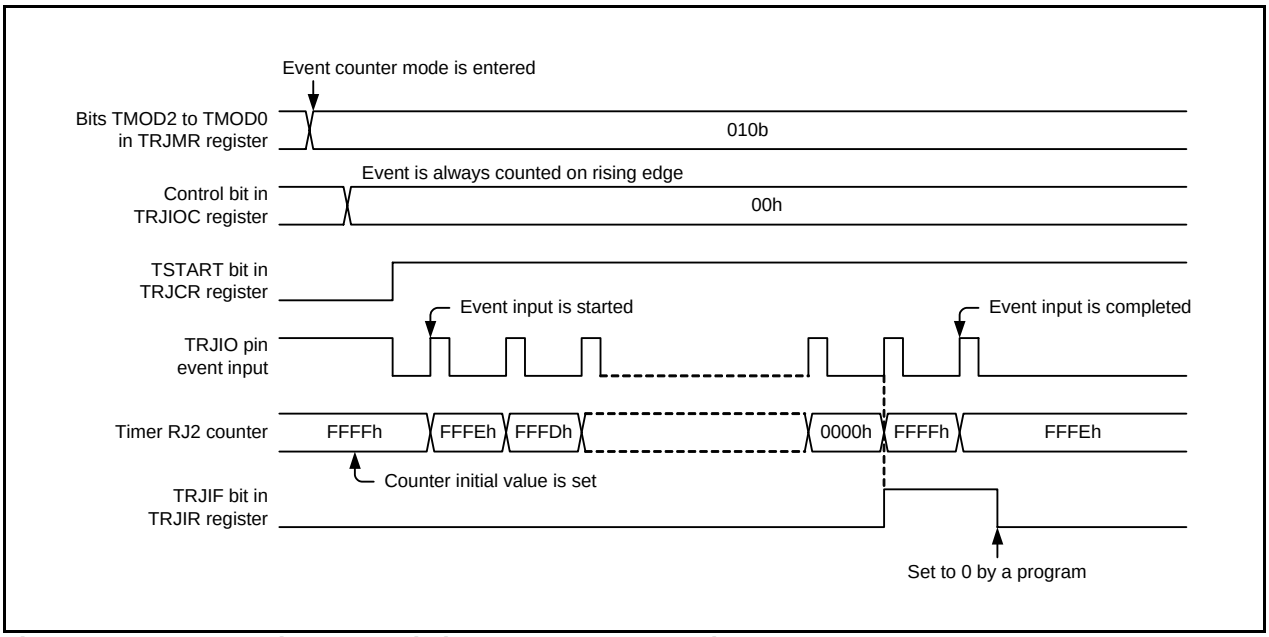


Figure 13.5 Operation Example in Event Counter Mode

13.4.5 Pulse Width Measurement Mode

In this mode, the pulse width of an external signal input to the TRJIO pin is measured.
When the level specified by the TEDGSEL bit in the TRJIOC register is input to the TRJIO pin, the decrement is started with the selected count source. When the specified level on the TRJIO pin ends, the counter is stopped, the TEDGF bit in the TRJCR register is set to 1 (active edge received), and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested). The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the TRJCR register is set to 1 (underflow) and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested). When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.
Figure 13.6 shows an Operation Example in Pulse Width Measurement Mode.
When accessing bits TEDGF and TUNDF in the TRJCR register, see **13.5 Notes on Timer RJ2 (4)**.

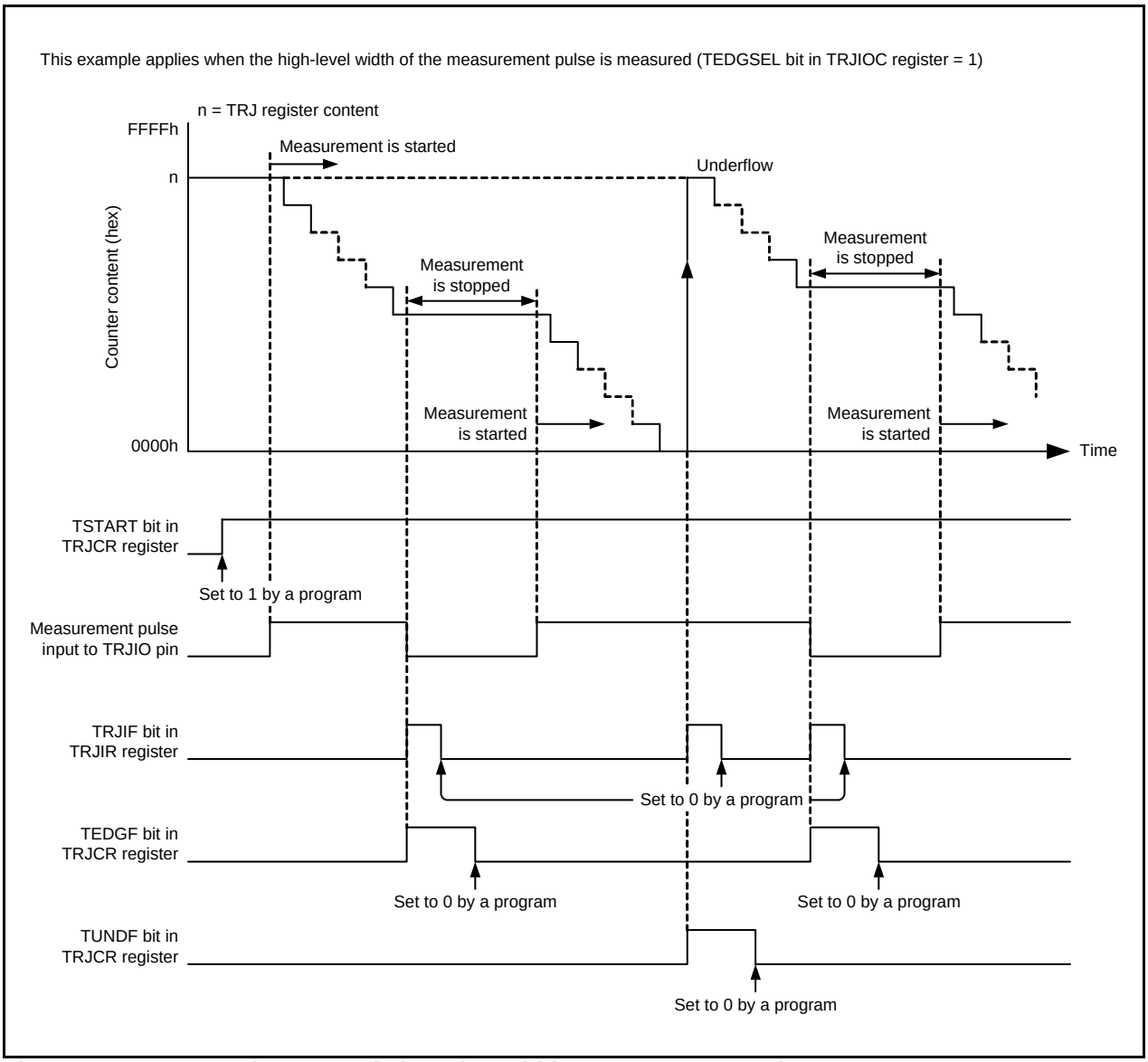


Figure 13.6 Operation Example in Pulse Width Measurement Mode

13.4.6 Pulse Period Measurement Mode

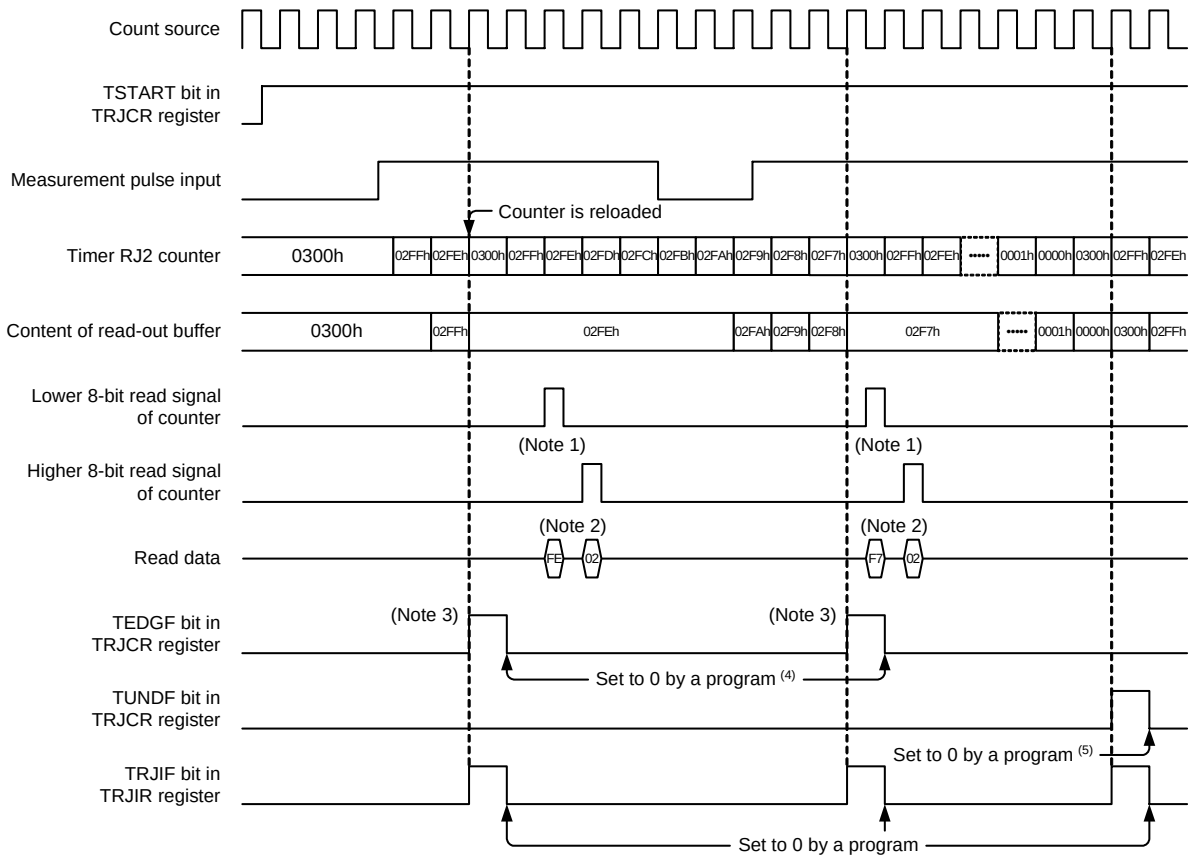
In this mode, the pulse period of an external signal input to the TRJIO pin is measured.

The counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register. When a pulse with the period specified by the TEDGSEL bit in the TRJIOC register is input to the TRJIO pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter on the next rising edge. The TEDGF bit in the TRJCR register is set to 1 (active edge received) and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested) at the same time. The read-out buffer (TRJ register) is read at this time and the difference from the reload value is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the TRJCR register is set to 1 (underflow) and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested). When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.

Figure 13.7 shows an Operation Example in Pulse Period Measurement Mode.

Only input pulses with a period longer than twice the period of the count source. Also, the low-level and high-level widths must be both longer than the period of the count source. If a pulse period shorter than these conditions is input, the input may be ignored.

This example applies when the initial value in the TRJ register is set to 0300h, the TEDGSEL bit in the TRJIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.



Notes:
1. Reading from the TRJ register must be performed during the period from when the TEDGF bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the TRJ register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
2. When the TRJ register is read in pulse period measurement mode, the content of the read-out buffer is be read.
3. After the active edge of the measurement pulse is input, the TRJ register is reloaded at the third rising edge of the count source. Then, the TEDGF bit in the TRJCR register is set to 1 (active edge received) at the fourth rising edge of the system clock (f).
4. To set to 0 by a program, use the MOV instruction to write 0 to the TEDGF bit in TRJCR register, and write 1 to the TUNDF bit at that time.
5. To set to 0 by a program, use the MOV instruction to write 0 to the TUNDF bit in TRJCR register, and write 1 to the TEDGF bit at that time.

Figure 13.7 Operation Example in Pulse Period Measurement Mode

13.4.7 Output Settings for Each Mode

Table 13.7 TRJIO Pin Setting

Operating Mode	TRJIOC Register		TRJIO Pin I/O
	TOPCR Bit	TEDGSEL Bit	
Timer mode	0 or 1	0 or 1	Input
Pulse output mode	1	0 or 1	Output disabled (1)
	0	1	Output is started at low
		0	Output is started at high
Event counter mode	0 or 1	0 or 1	Input
Pulse width measurement mode			
Pulse period measurement mode			

Note:
1. The port selected as the TRJIO function becomes high impedance.

Table 13.8 TRJO Pin Setting

Operating Mode	TRJIOC Register	TRJO Pin Output
	TEDGSEL Bit	
All modes	1	Output is started at high
	0	Output is started at low

13.5 Notes on Timer RJ2

(1) Timer RJ2 stops counting after a reset. Start the count only after setting the value in the timer.

(2) After 1 (count is started) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started from the first active edge of the count source after the TCSTF bit is set to 1.
After 0 (count is stopped) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 0.
Note:
1. Registers associated with timer RJ2: TRJ, TRJCR, TRJIOC, and TRJMR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count is started) and then input an external pulse.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program but remain unchanged even if 1 is written to these bits. If a read-modify-write instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In this case, write 1 using the MOV instruction to the TEDGF or TUNDF bit which is not supposed to be set to 0.

(5) Insert NOP instructions between writing to and reading from registers associated with the TRJ counter while the counter is stopped.

(6) When the TSTART bit in the TRJCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), allow at least three cycles of the count source clock for each write interval when writing to the TRJ register successively.

(7) Note the following when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.
Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.
When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.
Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.
After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.

(8) When the TEDGSEL bit in the TRJIOC register is set to 0 (count on rising edge) and the external signal (TRJIO) is counted in event counter mode, the signal may not be counted correctly depending on the state of the TSTART bit in the TRJCR register (see Figure 13.8).
If the TRJIO pin is set to low before the TSTART bit is set to 1 (count is started) and a valid event is input after the TSTART bit is set to 1, the signal is not counted on the first rising edge of the TRJIO input.
Thus, the number of counted events is obtained as follows:
Number of counted events = {(initial value in the counter – value in the counter on completion of the valid event + 1) + 1}
To avoid this, set the TRJIO pin to low after setting the TSTART bit to 1 (count is started) (see Figure 13.9).

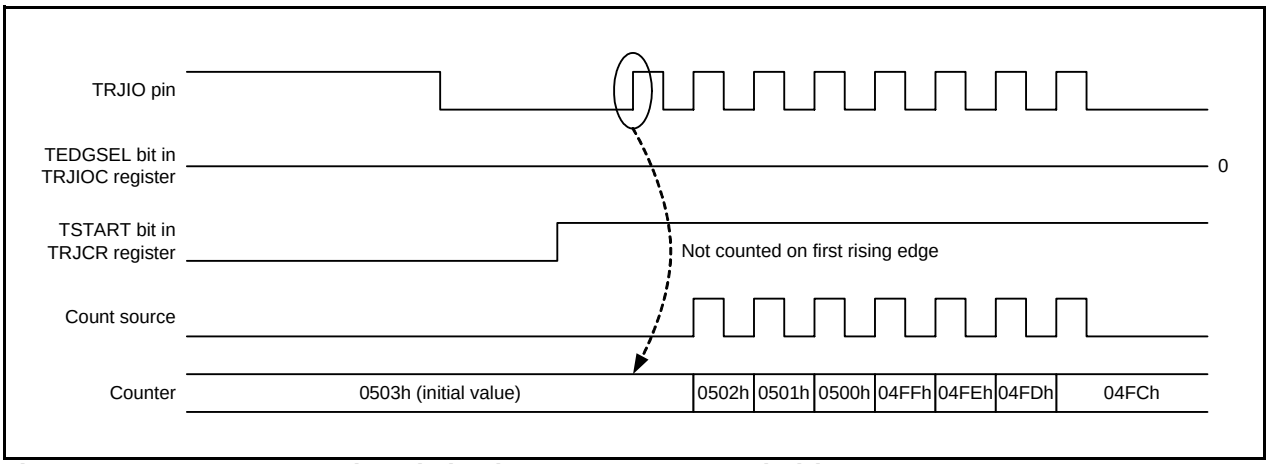


Figure 13.8 TSTART Setting Timing in Event Counter Mode (1)

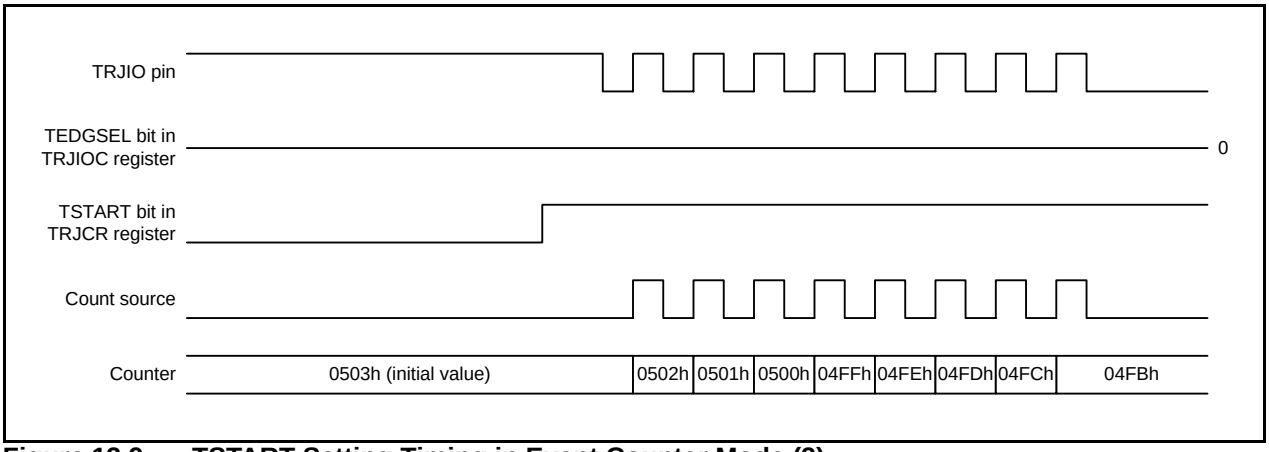


Figure 13.9 TSTART Setting Timing in Event Counter Mode (2)

(9) When the TEDGSEL bit in the TRJIOC register is set to 1 (count on falling edge) and the external signal (TRJIO) is counted in event counter mode, the signal may not be counted correctly depending on the state of the TSTART bit in the TRJCR register (see Figure 13.10).
Even if the TRJIO pin is set to low after the TSTART bit is set to 1 (count is started), the signal is not counted on the falling edge.
Thus, the number of counted events is obtained as follows:
Number of counted events = {(initial value in the counter – value in the counter on completion of the valid event + 1) + 1}
To avoid this, set the TSTART bit to 1 (count is started) and input a valid event after setting the TRJIO pin to low (see Figure 13.11).

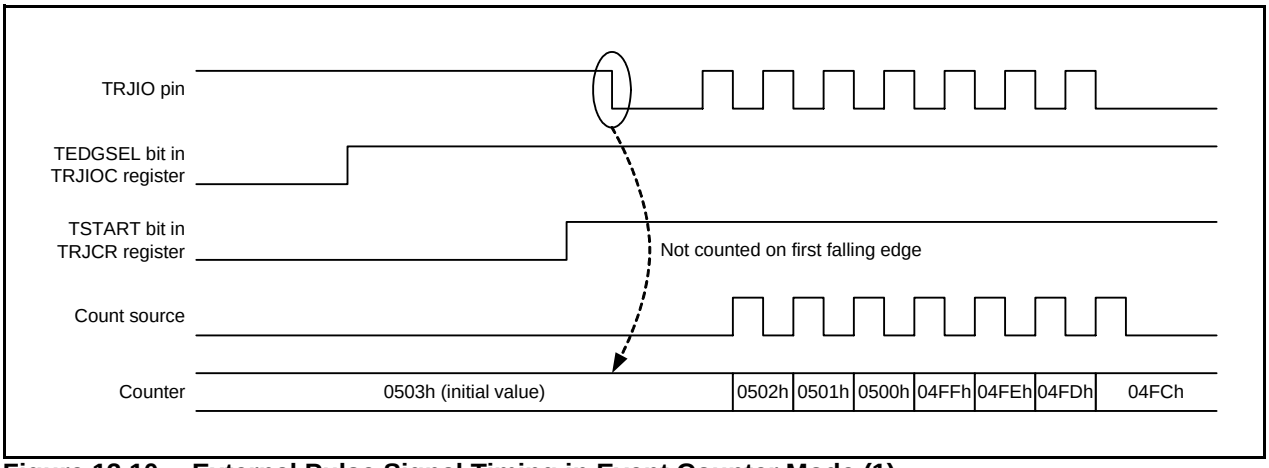


Figure 13.10 External Pulse Signal Timing in Event Counter Mode (1)

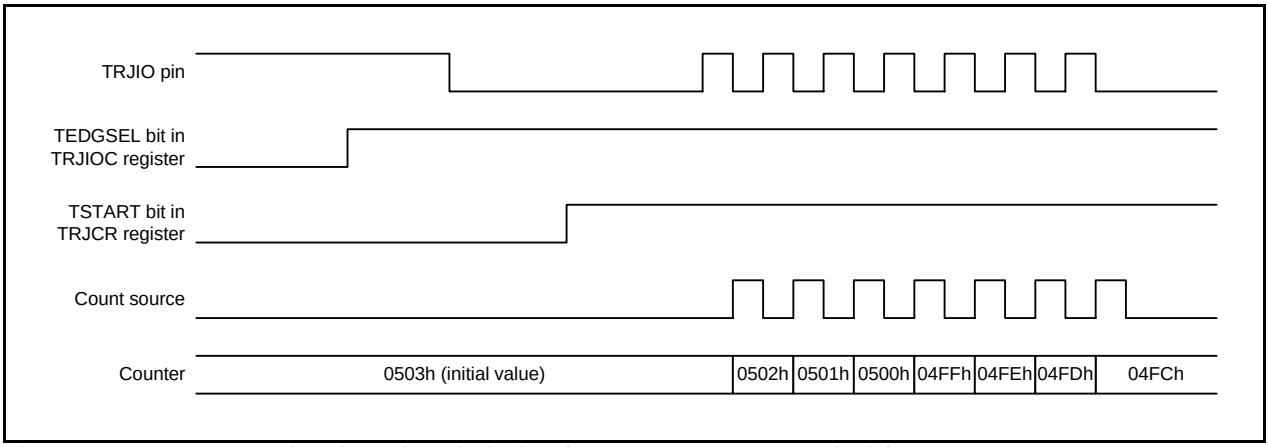


Figure 13.11 External Pulse Signal Timing in Event Counter Mode (2)

14. Timer RB2

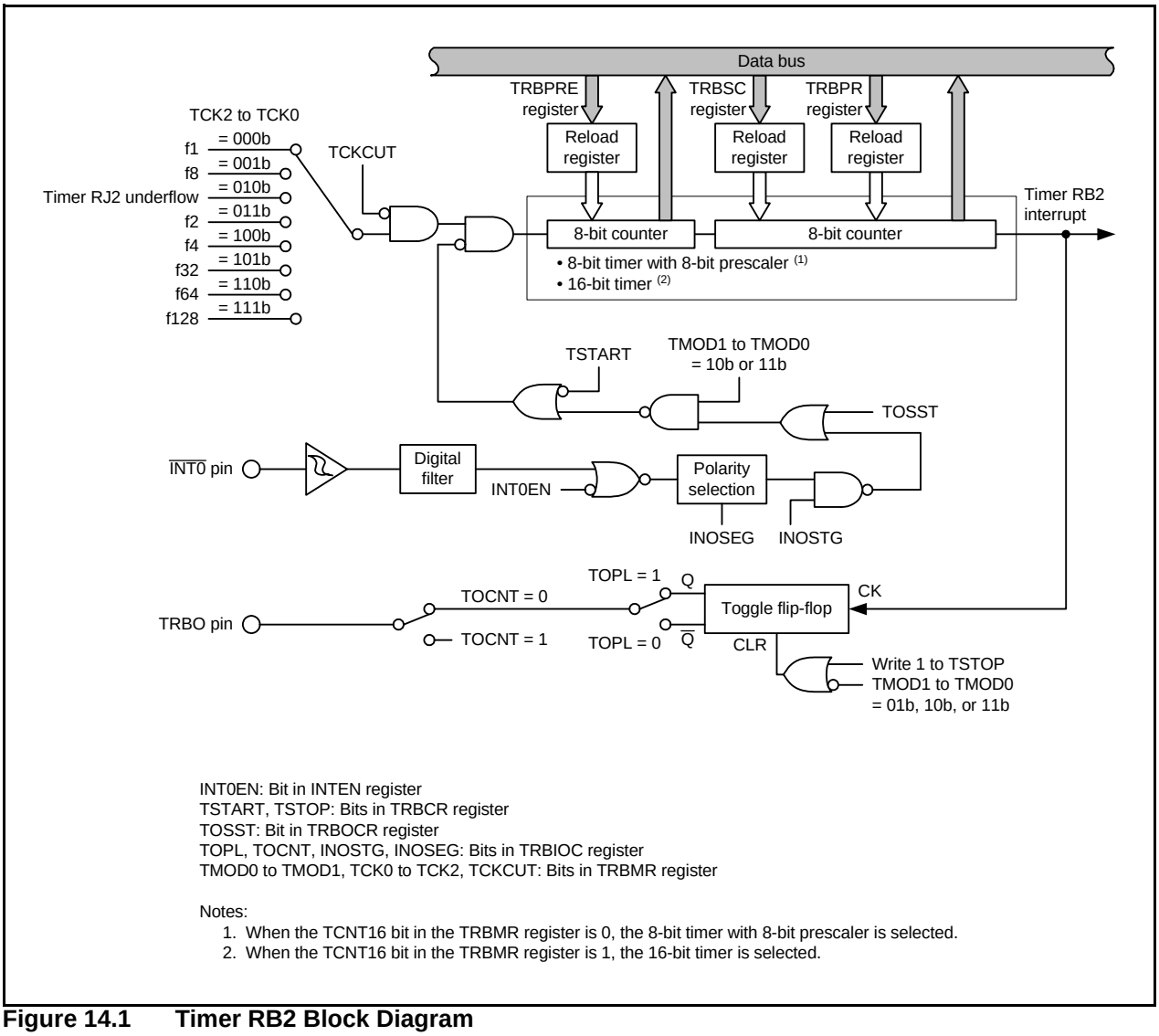
Timer RB2 can be used as an 8-bit timer with an 8-bit prescaler or as a 16-bit timer. The prescaler and timer each consist of a reload register and counter which are allocated to the same address. Timer RB2 has timer RB primary and timer RB secondary reload registers.

14.1 Overview

Table 14.1 lists the Timer RB2 Specifications. Figure 14.1 shows the Timer RB2 Block Diagram.

Table 14.1 Timer RB2 Specifications

Item		Description
Operating modes	Timer mode	An internal count source or timer RJ2 underflow is counted.
	Programmable waveform generation mode	An arbitrary pulse width is output successively.
	Programmable one-shot generation mode	A one-shot pulse is output.
	Programmable wait one-shot generation mode	A delayed one-shot pulse is output.
Count source		Selectable from f1, f2, f4, f8, f32, f64, f128, and timer RJ2 underflow.
Interrupt		Timer RB2 underflow



INT0EN: Bit in INTEN register
TSTART, TSTOP: Bits in TRBCR register
TOSST: Bit in TRBOCR register
TOPL, TOCNT, INOSTG, INOSEG: Bits in TRBIOC register
TMOD0 to TMOD1, TCK0 to TCK2, TCKCUT: Bits in TRBMR register

Notes:
1. When the TCNT16 bit in the TRBMR register is 0, the 8-bit timer with 8-bit prescaler is selected.
2. When the TCNT16 bit in the TRBMR register is 1, the 16-bit timer is selected.

Figure 14.1 Timer RB2 Block Diagram

14.2 I/O Pins

Table 14.2 lists the Timer RB2 Pin Configuration.

Table 14.2 Timer RB2 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P1_4, P4_5	I	External trigger
TRBO	P1_3, P4_2	O	Continuous pulse or one-shot pulse output

For details on $\overline{\text{INT0}}$, see **11. Interrupts**.

14.3 Registers

Table 14.3 lists the Timer RB2 Register Configuration.

Table 14.3 Timer RB2 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RB Control Register	TRBCR	00h	000E0h	8
Timer RB One-Shot Control Register	TRBOCR	00h	000E1h	8
Timer RB I/O Control Register	TRBIOC	00h	000E2h	8
Timer RB Mode Register	TRBMR	00h	000E3h	8
8-bit timer with 8-bit prescaler: Timer RB Prescaler Register 16-bit timer: Timer RB Primary/Secondary Register (Lower 8 Bits)	TRBPRE	FFh	000E4h	8
8-bit timer with 8-bit prescaler: Timer RB Primary Register 16-bit timer: Timer RB Primary Register (Higher 8 Bits)	TRBPR	FFh	000E5h	8
8-bit timer with 8-bit prescaler: Timer RB Secondary Register 16-bit timer: Timer RB Secondary Register (Higher 8 Bits)	TRBSC	FFh	000E6h	8
Timer RB Interrupt Control Register	TRBIR	00h	000E7h	8

14.3.1 Timer RB Control Register (TRBCR)

Address 000E0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit (1)	[When the TMOD1 bit in the TRBMR register is 0] 0: Count is stopped 1: Count is started [When the TMOD1 bit in the TRBMR register is 1] 0: Count is stopped 1: Count is enabled	R/W
b1	TCSTF	Timer RB count status flag (1)	[When the TMOD1 bit in the TRBMR register is 0] 0: Count is stopped 1: Count is in progress [When the TMOD1 bit in the TRBMR register is 1] 0: Count is stopped 1: Count is enabled	R
b2	TSTOP	Timer RB count forced stop bit (1, 2)	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. For notes on using bits TSTART, TCSTF, and TSTOP, see **14.8 Notes on Timer RB2**.
2. When 1 (count is forcibly stopped) is written to the TSTOP bit, the counter, registers TRBPRE, TRBPR, and TRBSC, bits TSTART and TCSTF, and bits TOSST, TOSSP, and TOSSTF in the TRBOCR register are initialized. The TRBO output is also initialized.

TSTART Bit (Timer RB count start bit)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When 1 is written to this bit.

TCSTF Bit (Timer RB count status flag)

[Conditions for setting to 0]
• When 0 is written to the TSTART bit.
• When 1 is written to the TSTOP bit.
[Condition for setting to 1]
• When 1 is written to the TSTART bit.

14.3.2 Timer RB One-Shot Control Register (TRBOCR)

Address 000E1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB one-shot start bit (1, 2)	When 1 is written to this bit, a one-shot trigger is generated. The read value is 0.	R/W
b1	TOSSP	Timer RB one-shot stop bit (2, 3)	When 1 is written to this bit, the one-shot pulse count (including wait time) is stopped. The read value is 0	R/W
b2	TOSSTF	Timer RB one-shot status flag	0: One-shot is stopped 1: One-shot is operating (including wait period)	R
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Make sure the TOSSTF bit is 0 (one-shot is stopped) before writing 1 (one-shot count is started) to the TOSST bit.
2. When 0 is written to this bit, the value is invalid.
3. Make sure the TOSSTF bit is 1 (one-shot is operating (including wait period)) before writing 1 (one-shot count is stopped) to the TOSSP bit.

TOSSTF Bit (Timer RB one-shot status flag)

[Conditions for setting to 0]
- When the TSTOP bit in the TRBCR register is set to 1 (count is forcibly stopped).
- When the count value reaches 00h and is reloaded in programmable one-shot generation mode.
- When the secondary count value reaches 00h and is reloaded in programmable wait one-shot generation mode.
- When the TOSSP bit is set to 1 (one-shot count is stopped).
- When the TSTART bit in the TRBCR register is set to 0 (count is stopped) and then 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register.

[Conditions for setting to 1]
- When the TOSST bit is set to 1 (one-shot count is started).
- When a trigger is input.

The TRBOCR register is enabled when bits TMOD1 to TMOD0 in the TRBMR register are 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

14.3.3 Timer RB I/O Control Register (TRBIOC)

Address 000E2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	See **Table 14.4 Functions of Timer RB Output Level Select Bit**.	R/W
b1	TOCNT	Timer RB output switch bit	0: Waveform output 1: Fixed-value output	R/W
b2	INOSTG	One-shot trigger control bit	0: One-shot trigger to $\overline{\text{INT0}}$ pin disabled 1: One-shot trigger to $\overline{\text{INT0}}$ pin enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

TOCNT Bit (Timer RB output switch bit)

The setting of the TOCNT bit is valid only in programmable waveform, programmable one-shot, and programmable wait one-shot generation modes.

For details on the change in the states of the TRBO output in each mode, see **14.5.3 TOCNT Bit Setting and Pin States**.

Table 14.4 Functions of Timer RB Output Level Select Bit

Operating Mode	Function	
Timer mode	Set to 0 in timer mode.	
Programmable waveform generation mode	0	High-level output during primary period Low-level output during secondary period Low-level output at timer stop
	1	Low-level output during primary period High-level output during secondary period High-level output at timer stop
Programmable one-shot generation mode	0	High-level one-shot pulse output Low-level output at timer stop
	1	Low-level one-shot pulse output High-level output at timer stop
Programmable wait one-shot generation mode	0	High-level one-shot pulse output Low-level output at timer stop and during wait period
	1	Low-level one-shot pulse output High-level output at timer stop and during wait period

14.3.4 Timer RB Mode Register (TRBMR)

Address 000E3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TWRC	TCNT16	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bits (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	TCNT16	Timer RB counter select bit (1)	0: 8-bit timer with 8-bit prescaler 1: 16-bit timer	R/W
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bits (1)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: Timer RJ2 underflow 0 1 1: f2 1 0 0: f4 1 0 1: f32 1 1 0: f64 1 1 1: f128	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. Only change these bits when bits TSTART and TCSTF in the TRBCR register are 0 (count is stopped).
2. For details on writing to the register and counter using the TWRC bit, see **14.5.2 Prescaler and Counter Using TWRC Bit**.

14.3.5 Timer RB Prescaler Register (TRBPRE)

Address 000E4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Initial Value	Setting Range	R/W
b7 to b0	Timer mode	An internal count source or the timer RJ2 underflow is counted.	FFh	00h to FFh	R/W
	Programmable waveform generation mode		FFh	00h to FFh	R/W
	Programmable one-shot generation mode		FFh	00h to FFh	R/W
	Programmable wait one-shot generation mode		FFh	00h to FFh	R/W

In the 8-bit timer with 8-bit prescaler, the TRBPRE register is used to set the period of the prescaler. Each time the prescaler decrements and underflows, the value in the TRBPRE register is reloaded. When read, the value is read from the prescaler.

In the 16-bit timer, the TRBPRE register is used as the lower 8-bit counter. Each time the counter decrements and underflows, the value in the TRBPRE register is reloaded. When read, the value is read from the lower 8 bits of the counter. Access the TRBPRE register first and then the TRBPR register.

The TRBPRE register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, see **Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**. The value is updated in synchronization with the count source.

14.3.6 Timer RB Primary Register (TRBPR)

Address 000E5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function		Initial Value	Setting Range	R/W
		8-Bit Timer with 8-Bit Prescaler	16-Bit Timer			
b7 to b0	Timer mode	Timer RB prescaler underflow is counted.	An internal count source or the timer RJ2 underflow is counted.	FFh	00h to FFh	R/W
	Programmable waveform generation mode	Timer RB prescaler underflow is counted. (1)		FFh	00h to FFh	R/W
	Programmable one-shot generation mode	Timer RB prescaler underflow is counted (the one-shot width is counted).		FFh	00h to FFh	R/W
	Programmable wait one-shot generation mode	Timer RB prescaler underflow is counted (the wait period is counted).		FFh	00h to FFh	R/W

Note:
1. The values in registers TRBPR and TRBSC are reloaded and counted alternately.

In the 8-bit timer with 8-bit prescaler, the TRBPR register is used to set the period of the counter and the primary period. When read, the value is from the 8-bit counter.
In the 16-bit timer, the TRBPR register is used to set the period of the higher 8-bit counter and the primary period. When read, the value is read from the higher 8 bits of the 16-bit timer. Access the TRBPRE register and then the TRBPR register.
The TRBPR register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, see **Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**.

14.3.7 Timer RB Secondary Register (TRBSC)

Address 000E6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function		Initial Value	Setting Range	R/W
		8-Bit Timer with 8-Bit Prescaler	16-Bit Timer			
b7 to b0	Timer mode	Disabled		FFh	Invalid	—
	Programmable waveform generation mode	Timer RB prescaler underflow	Internal count source or timer RJ2 underflow (1)	FFh	00h to FFh	R/W
	Programmable one-shot generation mode	Disabled		FFh	Invalid	—
	Programmable wait one-shot generation mode	Timer RB prescaler underflow	Internal count source or timer RJ2 underflow (1)	FFh	00h to FFh	R/W

Note:
1. The values in registers TRBPR and TRBSC are reloaded and counted alternately. The count value can be read from the TRBPR register while the secondary period is counted.

In the 8-bit timer with 8-bit prescaler, use the following procedure when writing to the TRBSC register.
(1) Write a value to the TRBSC register.
(2) Write a value to TRBPR register (write the same value as the previous one again even if the value is not changed).
In the 16-bit timer, use the following procedure when writing to the TRBSC register.
(1) Write values to registers TRBPRE and TRBSC.
(2) Write a value to TRBPR register (write the same value as the previous one again even if the value is not changed).

In the 8-bit timer with 8-bit prescaler, the TRBSC register is used to set the secondary period used in programmable waveform and programmable wait one-shot generation modes. When read, the value is read from the reload register.
In the 16-bit timer, the TRBSC register is used to set the higher 8-bit secondary period used in programmable waveform and programmable wait one-shot generation modes. This setting can be made in timer mode and programmable one-shot generation mode, but it is not used for counter operation. When read, the value is read from the reload register.
The TRBSC register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, see **Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**.

14.3.8 Timer RB Interrupt Control Register (TRBIR)

Address 000E7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRBIE	TRBIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	TRBIF	Timer RB interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b7	TRBIE	Timer RB interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

TRBIF Bit (Timer RB interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• See **Table 14.5 Conditions for Setting TRBIF Bit to 1**.

Table 14.5 Conditions for Setting TRBIF Bit to 1

Operating Mode	Condition
Timer mode	When timer RB2 underflows.
Programmable waveform generation mode	When timer RB2 underflows during the secondary period.
Programmable one-shot generation mode	When timer RB2 underflows.
Programmable wait one-shot generation mode	When timer RB2 underflows during the secondary period.

14.4 Operation

14.4.1 Timer Mode

In this mode, an internally generated count source or the timer RJ2 underflow is counted. Registers TRBOCR and TRBSC are not used.

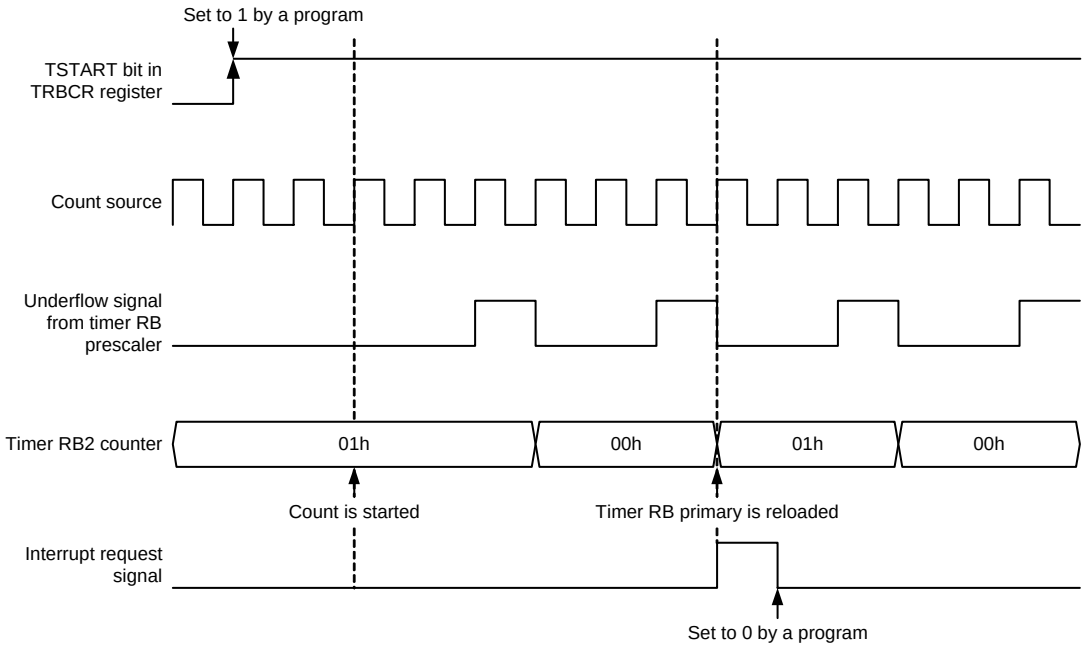
When 1 (count is started) is written to the TSTART bit in the TRBCR register, the count is started after the count source is sampled three times. When 0 (count is stopped) is written to the TSTART bit, the count is stopped after the count source is sampled three times. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped. The actual count state should be monitored with the TCSTF bit in the TRBCR register.

An interrupt request is generated when timer RB2 underflows.

When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written to while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to both the reload register and counter. When the TWRC bit is 1, values are written to the reload register only.

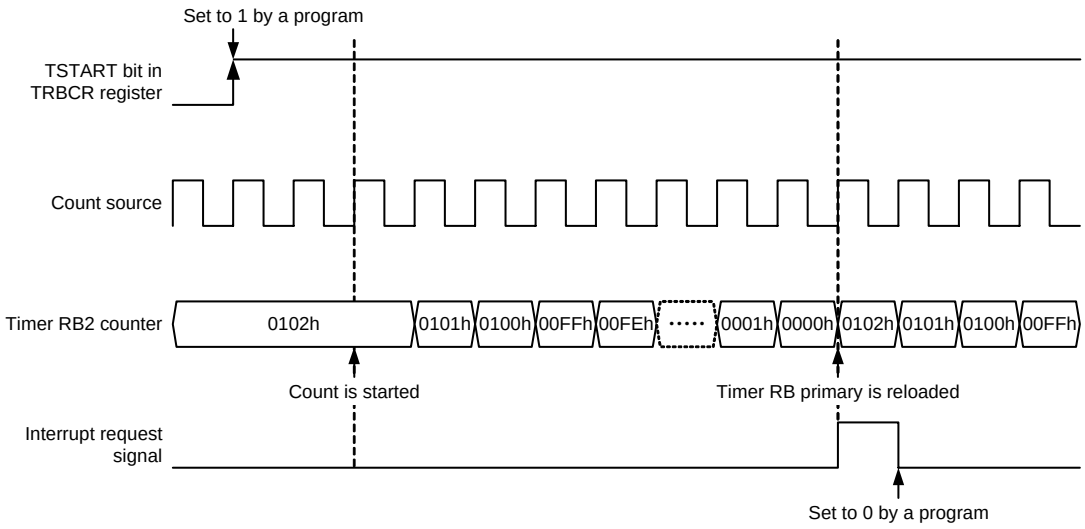
Figure 14.2 shows an Operation Example in Timer Mode.

• 8-bit timer with 8-bit prescaler in timer mode



The above diagram applies under the following conditions:
- TRBPRE register = 02h, TRBPR register = 01h
- TOCNT bit in TRBIOC register = 0 (waveform output)
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

• 16-bit timer in timer mode

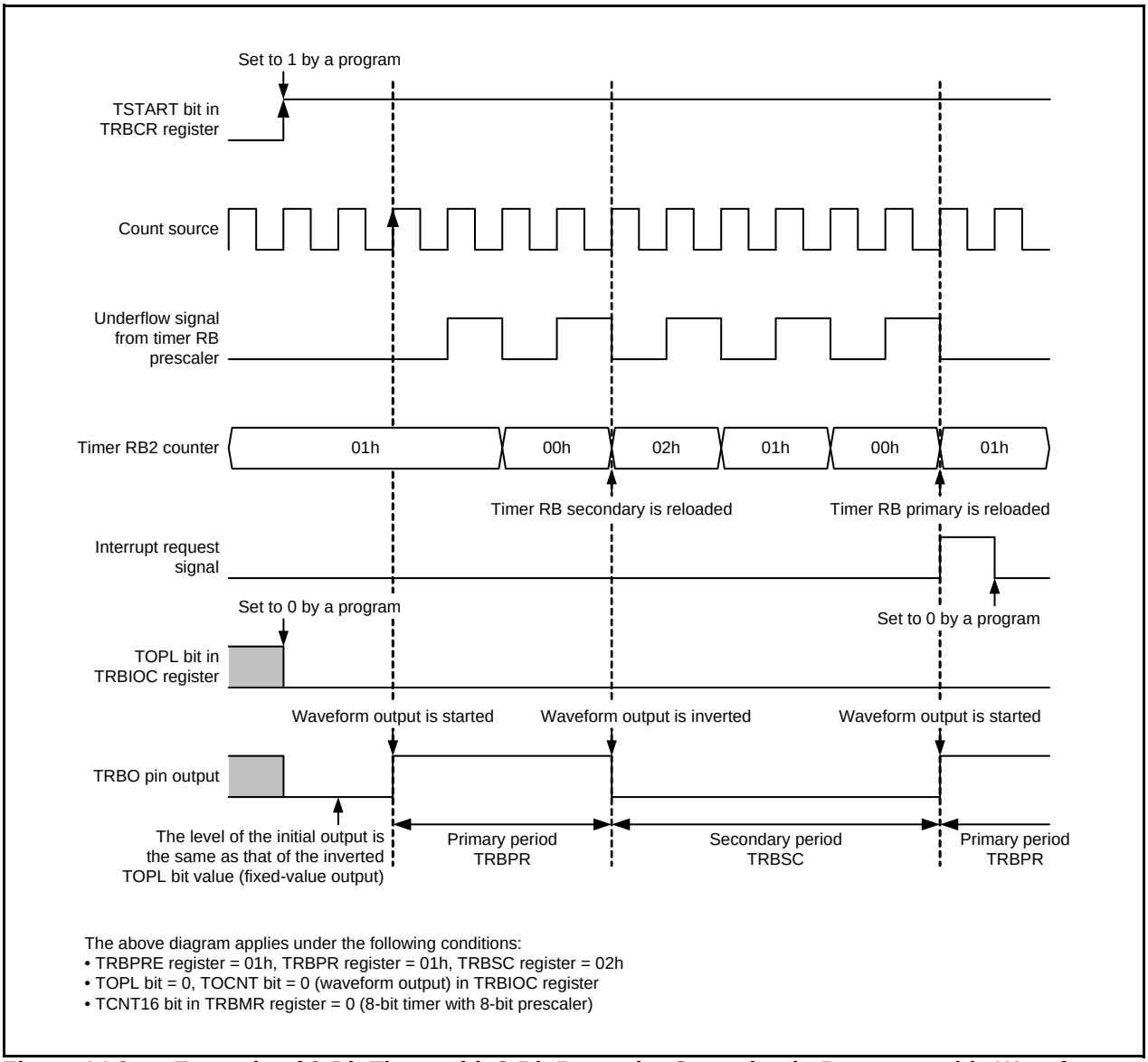


The above diagram applies under the following conditions:
- TRBPRE register = 02h, TRBPR register = 01h
- TOCNT bit in TRBIOC register = 0 (waveform output)
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.2 Operation Example in Timer Mode

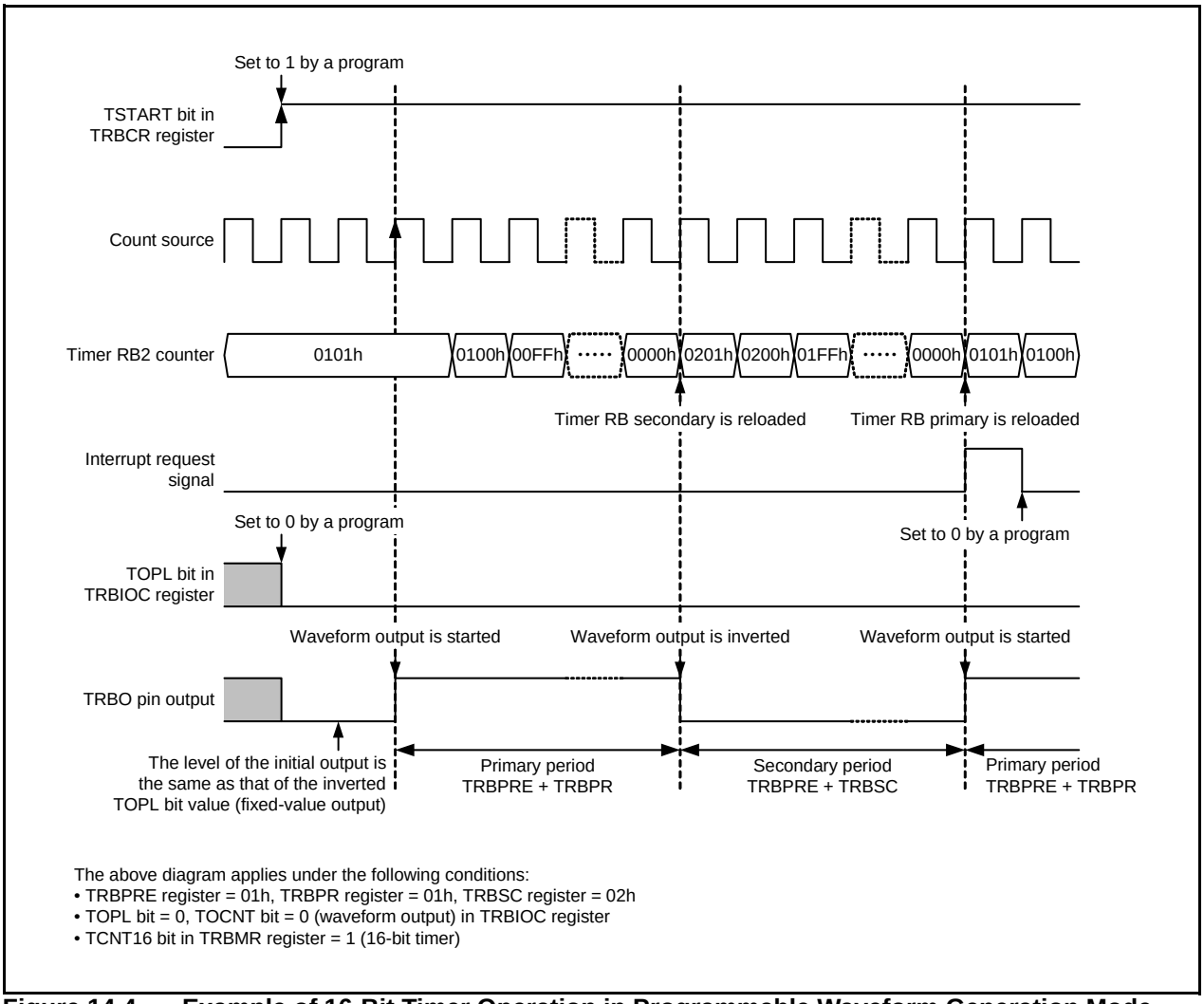
14.4.2 Programmable Waveform Generation Mode

In the 8-bit timer with 8-bit prescaler, the values in registers TRBPR and TRBSC are counted alternately.
In the 16-bit timer, the lower 8 bits are counted by the TRBPRE register and the higher 8 bits are counted by registers TRBPR and TRBSC alternately.
The TRBO pin outputs a signal which is inverted each time the counter underflows. The count is started from the value set in the TRBPR register. In programmable waveform generation mode, the TRBOCR register is not used.
When 1 (count is started) is written to the TSTART bit in the TRBCR register, the count is started after the count source is sampled three times. When 0 (count is stopped) is written to the TSTART bit, the count is stopped after the count source is sampled three times. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped. The actual count state should be monitored with the TCSTF bit in the TRBCR register.
An interrupt request is generated when timer RB2 underflows during the secondary period.
When registers TRBPRE and TRBPR are read, each count value can be read. Read the TRBPR register even while the secondary period is counted. When registers TRBPRE, TRBPR, and TRBSC are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
Figure 14.3 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Waveform Generation Mode. Figure 14.4 shows an Example of 16-Bit Timer Operation in Programmable Waveform Generation Mode.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 02h
- TOPL bit = 0, TOCNT bit = 0 (waveform output) in TRBIOC register
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

Figure 14.3 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Waveform Generation Mode



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 02h
- TOPL bit = 0, TOCNT bit = 0 (waveform output) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

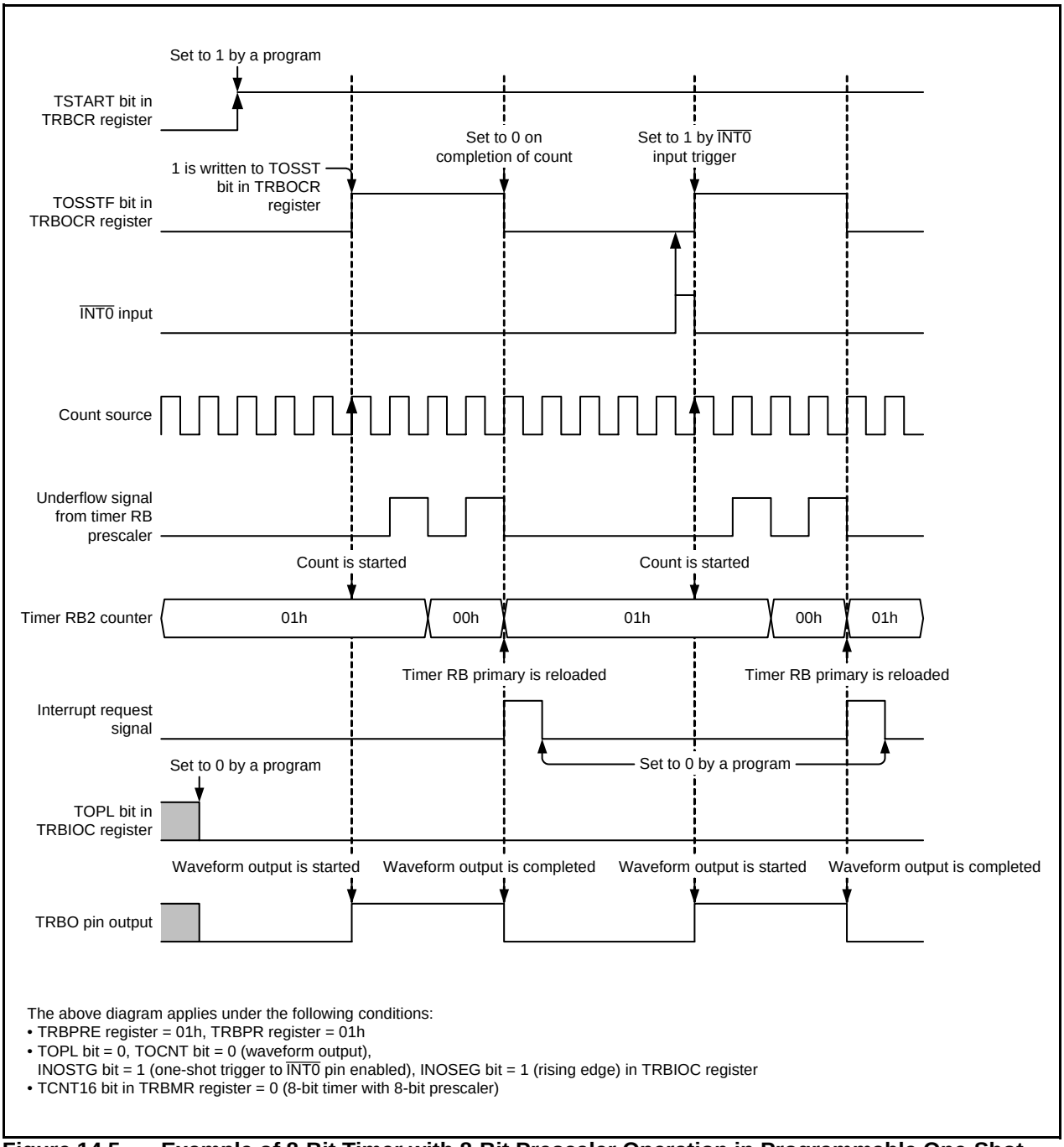
Figure 14.4 Example of 16-Bit Timer Operation in Programmable Waveform Generation Mode

14.4.3 Programmable One-Shot Generation Mode

In this mode, a one-shot pulse is output from the TRBO pin by a program or the $\overline{\text{INT0}}$ pin input. When a trigger is generated from that point, the timer operates only once to count a given length of the time equal to the setting value of the TRBPR register.
In the 8-bit timer with 8-bit prescaler, the count value is set in the TRBPR register.
In the 16-bit timer, the count value of the higher 8 bits is set in the TRBPR register and that of the lower 8 bits is set in the TRBPRE register.
In programmable one-shot generation mode, the TRBSC register is not used.
When 1 (one-shot count is started) is written to the TOSST bit in the TRBOCR register while the TCSTF bit in the TRBCR register is 1 (count is enabled), the count is started after the count source is sampled three times. If an enabled trigger is input to the $\overline{\text{INT0}}$ pin while the TCSTF bit is 1, the count is started after the count source is sampled three times. When the count value in the timer RB secondary overflows and then it is reloaded, the count is stopped. The count is also stopped with any of the following settings:

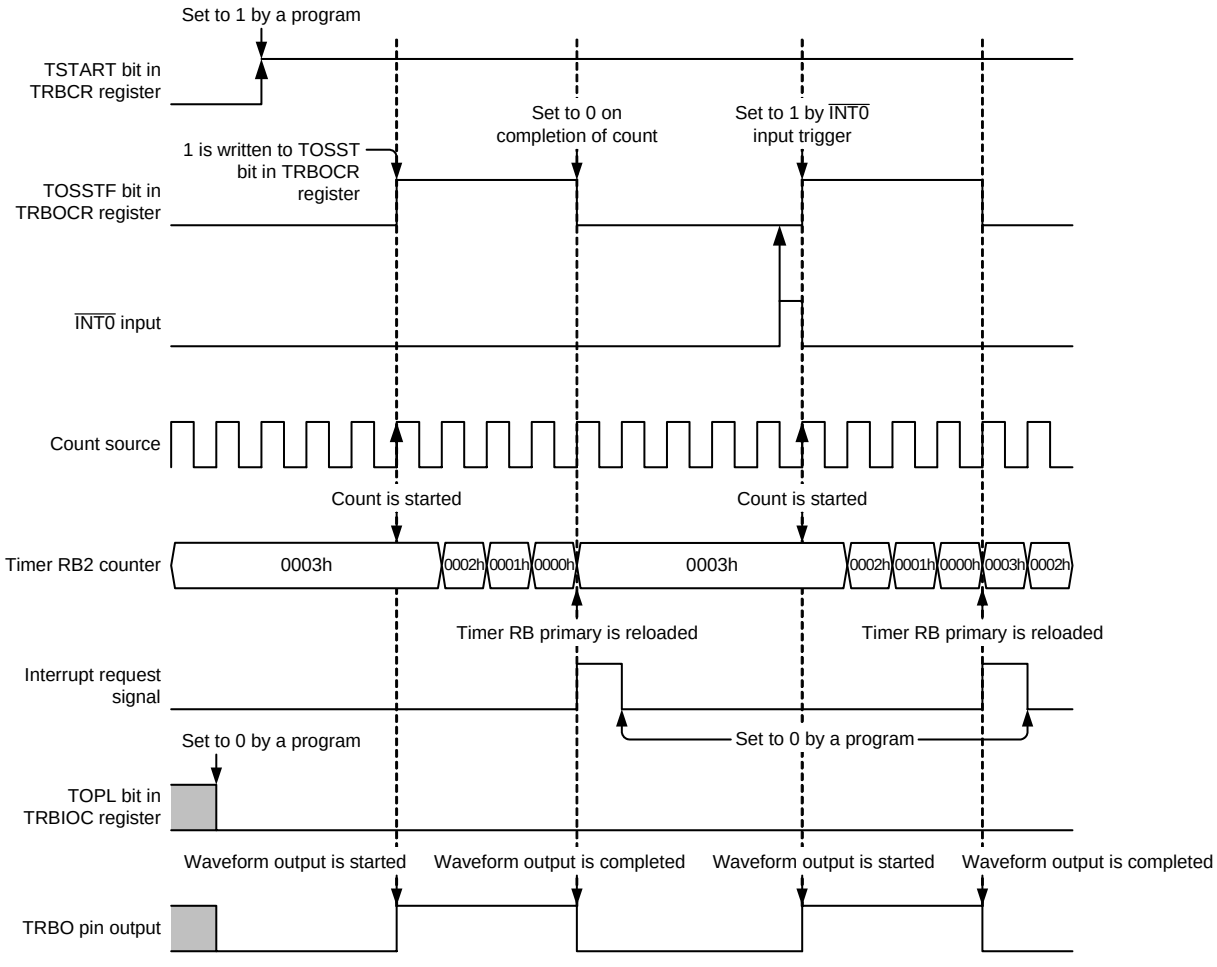
- When 1 (one-shot count is stopped) is written to the TOSSP bit in the TRBOCR register, the count is stopped after the count source is sampled three times.
- When 0 (count is stopped) is written to the TSTART bit in the TRBCR register, the count is stopped after the count source is sampled three times.
- When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.

The actual count state must be monitored with the TCSTF bit in the TRBCR register.
An interrupt request is generated when timer RB2 underflows.
When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
For the setting of trigger by the $\overline{\text{INT0}}$ input, see **14.7 INT0 Input Trigger Selection**.
Figure 14.5 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode. Figure 14.6 shows an Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

Figure 14.5 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode



The above diagram applies under the following conditions:
- TRBPRE register = 03h, TRBPR register = 00h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.6 Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode

14.4.4 Programmable Wait One-Shot Generation Mode

In this mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger ($\overline{\text{INT0}}$ pin input) after a specified period. When a trigger is generated from that point, the timer outputs a pulse only once for a given length of the time equal to the setting value of the TRBSC register after waiting for a given length of time equal to the setting value of the TRBPR register.

In the 8-bit timer with 8-bit prescaler, set the count value of the wait time in the TRBPR register and set the count value of the pulse width in the TRBSC register.

In the 16-bit timer, set the count value of the wait time of the higher 8 bits in the TRBPR register and that of the lower 8 bits in the TRBPRE register. Set the count value of the pulse width of the higher 8 bits in the TRBSC register and that of the lower 8 bits in the TRBPRE register.

When 1 (one-shot count is started) is written to the TOSST bit in the TRBOCR register while the TCSTF bit in the TRBCR register is 1 (count is enabled), the count is started after the count source is sampled three times. If an enabled trigger is input to the $\overline{\text{INT0}}$ pin while the TCSTF bit is 1, the count is started after the count source is sampled three times. When the count value in the timer RB secondary underflows and then it is reloaded, the count is stopped. The count is also stopped with any of the following settings:

- When 1 (one-shot count is stopped) is written to the TOSSP bit in the TRBOCR register, the count is stopped after the count source is sampled three times.
- When 0 (count is stopped) is written to the TSTART bit in the TRBCR register, the count is stopped after the count source is sampled three times.
- When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.

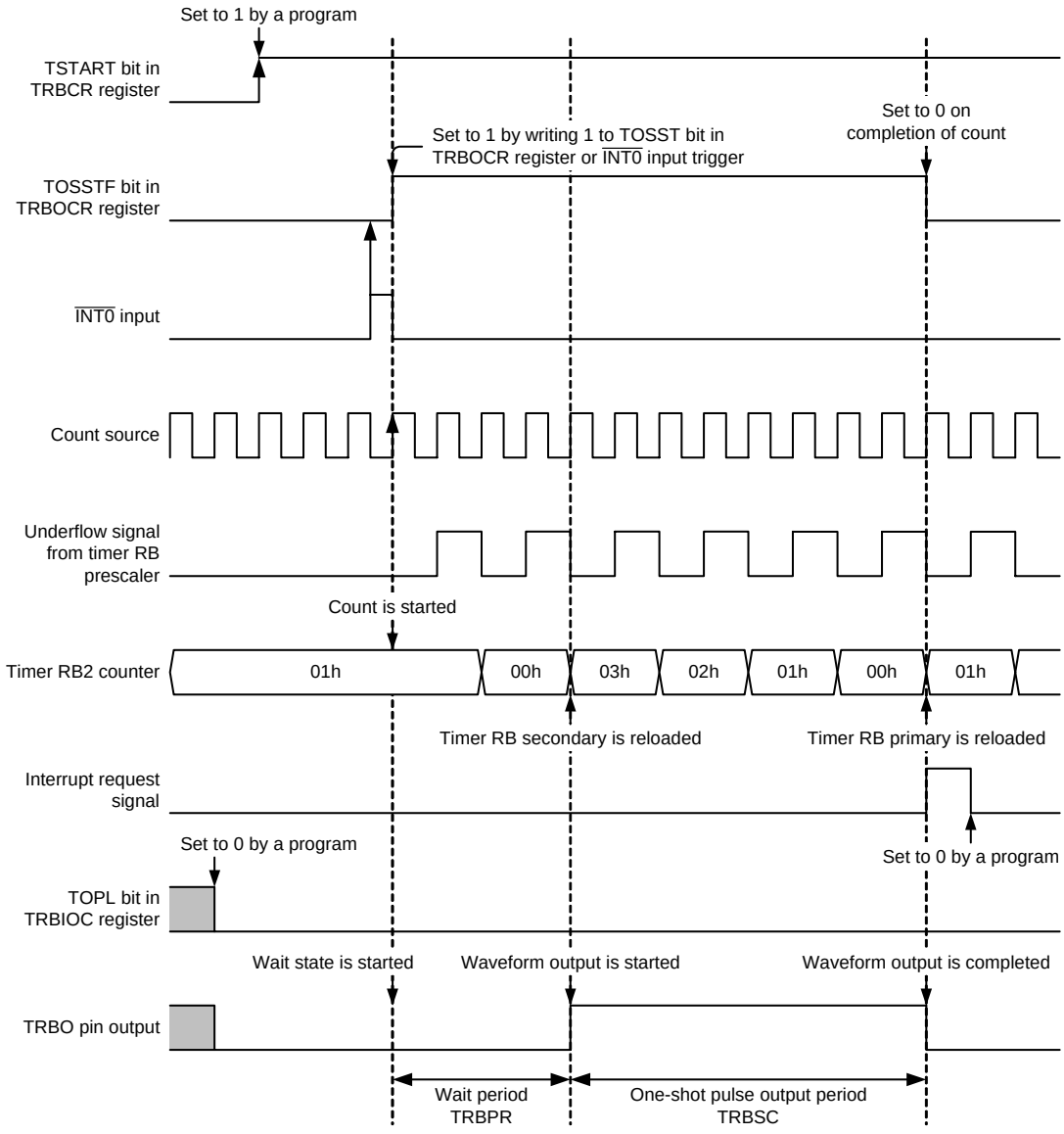
The actual count state must be monitored with the TCSTF bit in the TRBCR register.

An interrupt request is generated when timer RB2 underflows during the secondary period.

When registers TRBPRE and TRBPR are read, each count value is read. When registers TRBPRE, TRBPR, and TRBSC are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.

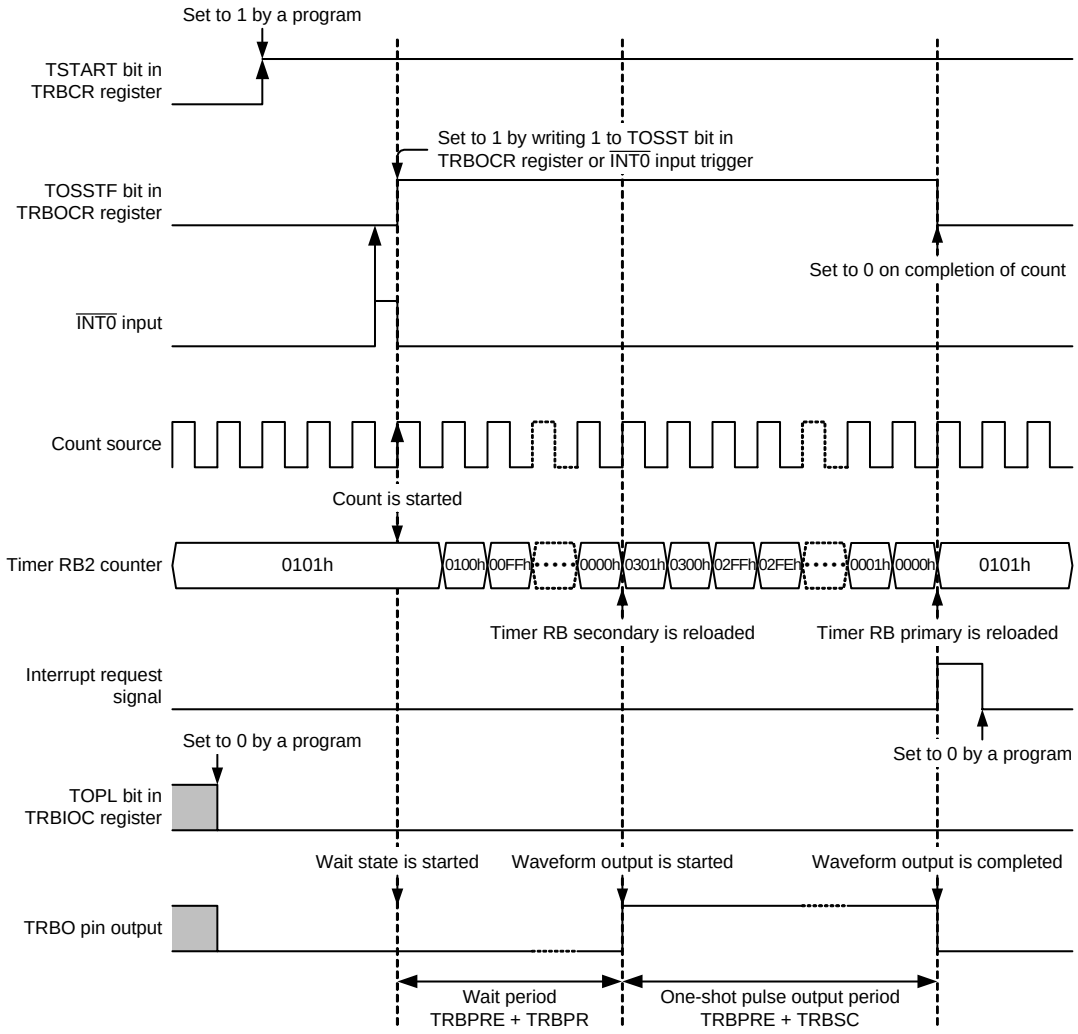
For the setting of trigger by the $\overline{\text{INT0}}$ input, see **14.7 $\overline{\text{INT0}}$ Input Trigger Selection**.

Figure 14.7 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Wait One-Shot Generation Mode. Figure 14.8 shows an Example of 16-Bit Timer Operation in Programmable Wait One-Shot Generation Mode.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 03h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

Figure 14.7 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Wait One-Shot Generation Mode



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 03h
- TOPL bit = 0, TOCNT bit = 0 (waveform output),
  INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.8 Example of 16-Bit Timer Operation in Programmable Wait One-Shot Generation Mode

14.5 Selectable Functions

14.5.1 Configuration and Update Timing for Registers TRBPRE, TRBPR, and TRBSC

Registers TRBPRE, TRBPR, and TRBSC are configured with a master – reload register structure. Figure 14.9 shows the Configuration of Registers TRBPRE, TRBPR, and TRBSC. When the TSTART bit in the TRBCR register is set to 0 (count is stopped), values are updated to the reload registers immediately after the registers are written. However, when the TSTART bit is 1 (count is started), the timing for updating the reload registers differs in each mode. In the 8-bit timer with 8-bit prescaler, after the TRBPRE register is written, the TRBPRE register reload register is updated in synchronization with the count source.
Table 14.6 lists the Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler. Table 14.7 lists the Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer.

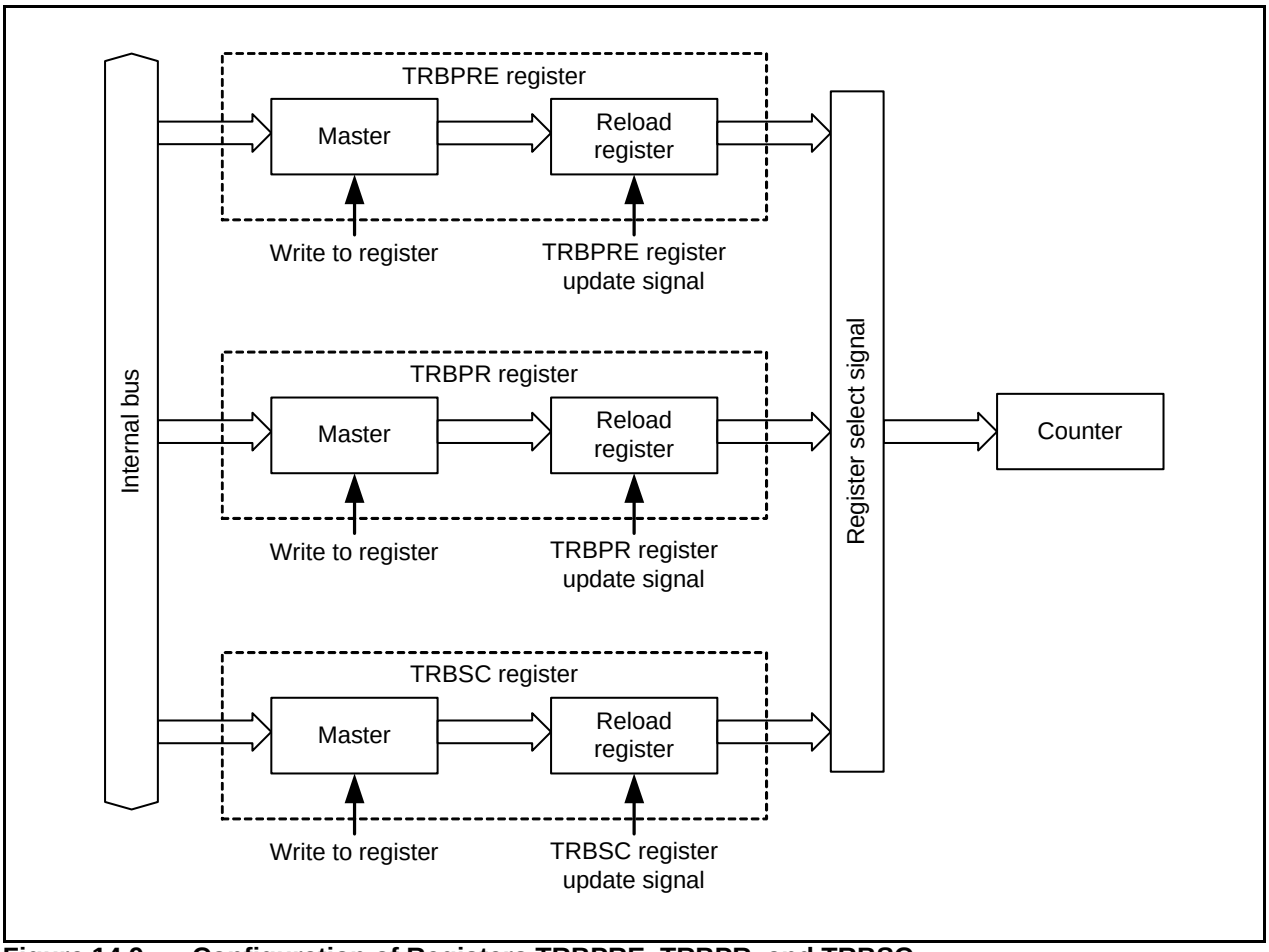


Figure 14.9 Configuration of Registers TRBPRE, TRBPR, and TRBSC

Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler

Operating Mode		Update Timing (1)	
		TRBPR Register	TRBSC Register
Timer mode		Updated in synchronization with the prescaler underflow.	
Programmable waveform generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the prescaler underflow after the TRBPR register is written. (2)	
Programmable one-shot generation mode		Updated in synchronization with the prescaler underflow. (3)	
Programmable wait one-shot generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the prescaler underflow after the TRBPR register is written. (2)	

TWRC: Bit in the TRBMR register

Notes:
1. For details, see **14.5.2 Prescaler and Counter Using TWRC Bit**.
2. When the TWRC bit is 0 (write to reload register and counter) in programmable waveform and programmable wait one-shot generation modes, if the data in registers TRBSC and TRBPR is updated during count operation, the waveform is output for the updated period from that time.
3. When the TWRC bit is 0 (write to reload register and counter) in programmable one-shot generation mode, if the data in the TRBPR register is updated during count operation, the waveform is output for the updated period from that time.

Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer

Operating Mode		Update Timing (1)	
		Registers TRBPRE and TRBPR	TRBSC Register
Timer mode		Updated in synchronization with the count source after the TRBPR register is written.	Updated in synchronization with the count source after the TRBSC register is written.
Programmable waveform generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the count source after the TRBPR register is written. (2)	
Programmable one-shot generation mode		Updated in synchronization with the count source after the TRBPR register is written.	Updated in synchronization with the count source after the TRBSC register is written. (3)
Programmable wait one-shot generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the count source after the TRBPR register is written. (2)	

TWRC: Bit in the TRBMR register

Notes:
1. For details, see **14.5.2 Prescaler and Counter Using TWRC Bit**.
2. When the TWRC bit is 0 (write to reload register and counter) in programmable waveform and programmable wait one-shot generation modes, if the data in registers TRBSC and TRBPR is updated during count operation, the waveform is output for the updated period from that time.
3. When the TWRC bit is 0 (write to reload register and counter) in programmable one-shot generation mode, if the data in the TRBPR register is updated during count operation, the waveform is output for the updated period from that time.

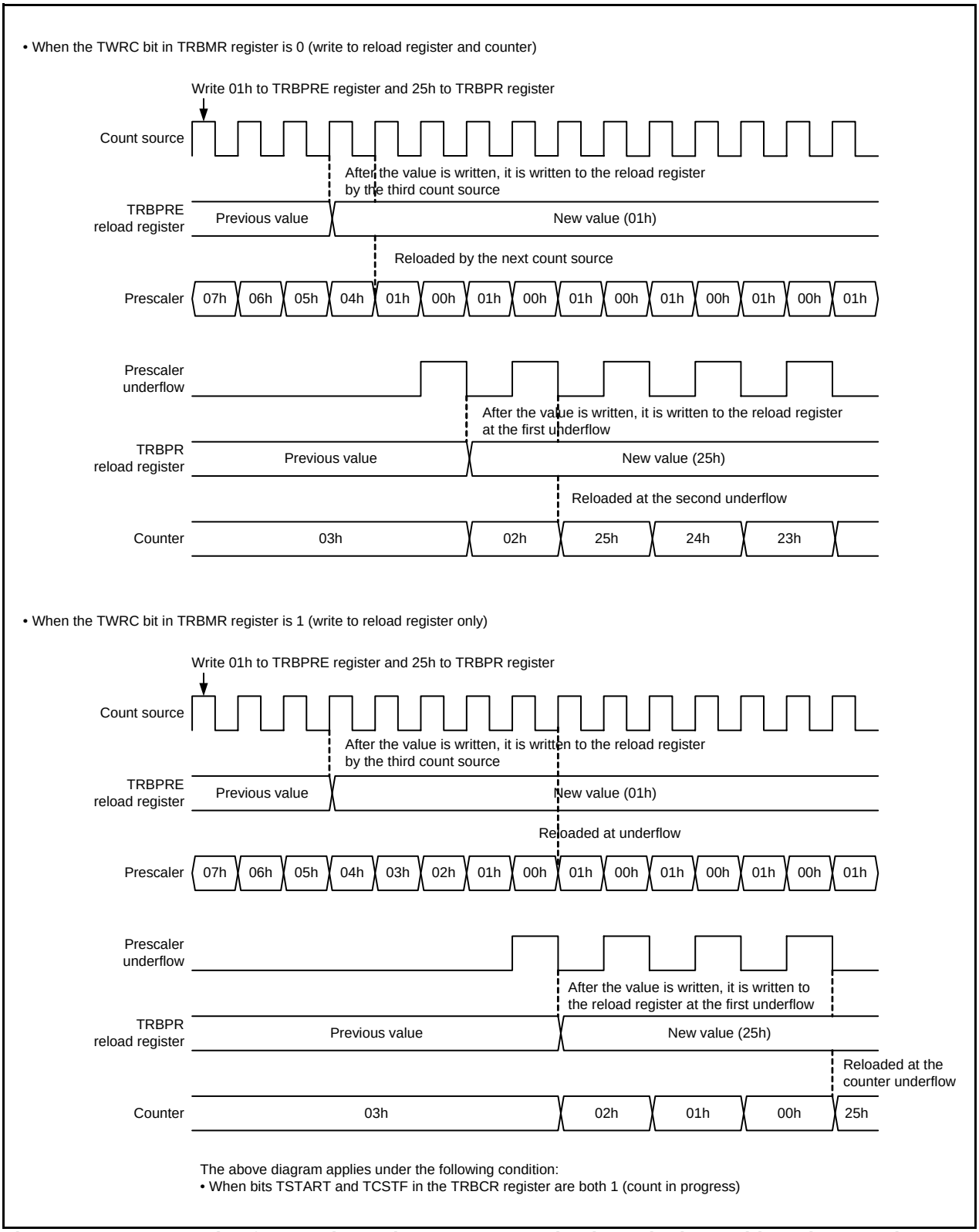
14.5.2 Prescaler and Counter Using TWRC Bit

In timer RB2, the TWRC bit in the TRBMR register can be used to select whether to write to the reload register only (TRBPR, TRBSC, TRBPRE) or both the reload register and counter. However, when the TCSTF bit in the TRBCR register is 0 (count is stopped), both the reload register and counter are written regardless of the setting of the TWRC bit.

In the 8-bit timer with 8-bit prescaler, when the TWRC bit is 0 (write to reload register and counter), transfer from the reload register to the prescaler is performed in synchronization with the count source, and transfer to the counter is performed in synchronization with prescaler underflows. Therefore, the count value is not updated immediately after the write instruction is executed. When the TWRC bit is 1 (write to reload register only), transfer from the reload register to the prescaler is performed in synchronization with prescaler underflows, and transfer to the counter is performed in synchronization with counter underflows. Only the value of the prescaler is updated before the counter underflows. Figures 14.10 and 14.11 show Examples of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler.

In the 16-bit timer, when the TWRC bit is 0 (write to reload register and counter), transfer to the 16-bit counter is performed in synchronization with the count source. When the TWRC bit is 1 (write to reload register only), transfer to the 16-bit counter is performed in synchronization with 16-bit counter underflows. Figures 14.12 and 14.13 show Examples of Counter Operation in 16-Bit Timer.

During programmable wait one-shot generation mode, when the TCSTF bit in the TRBCR register is 1 (count is in progress) and the TOSSTF bit in the TRBOCR register is 0 (one-shot is stopped), the reload register and counter can be written because the setting of the TWRC bit in the TRBMR register is invalid.



The above diagram applies under the following condition:
• When bits TSTART and TCSTF in the TRBCR register are both 1 (count in progress)

Figure 14.10 Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler (Timer Mode or Programmable One-Shot Generation Mode)

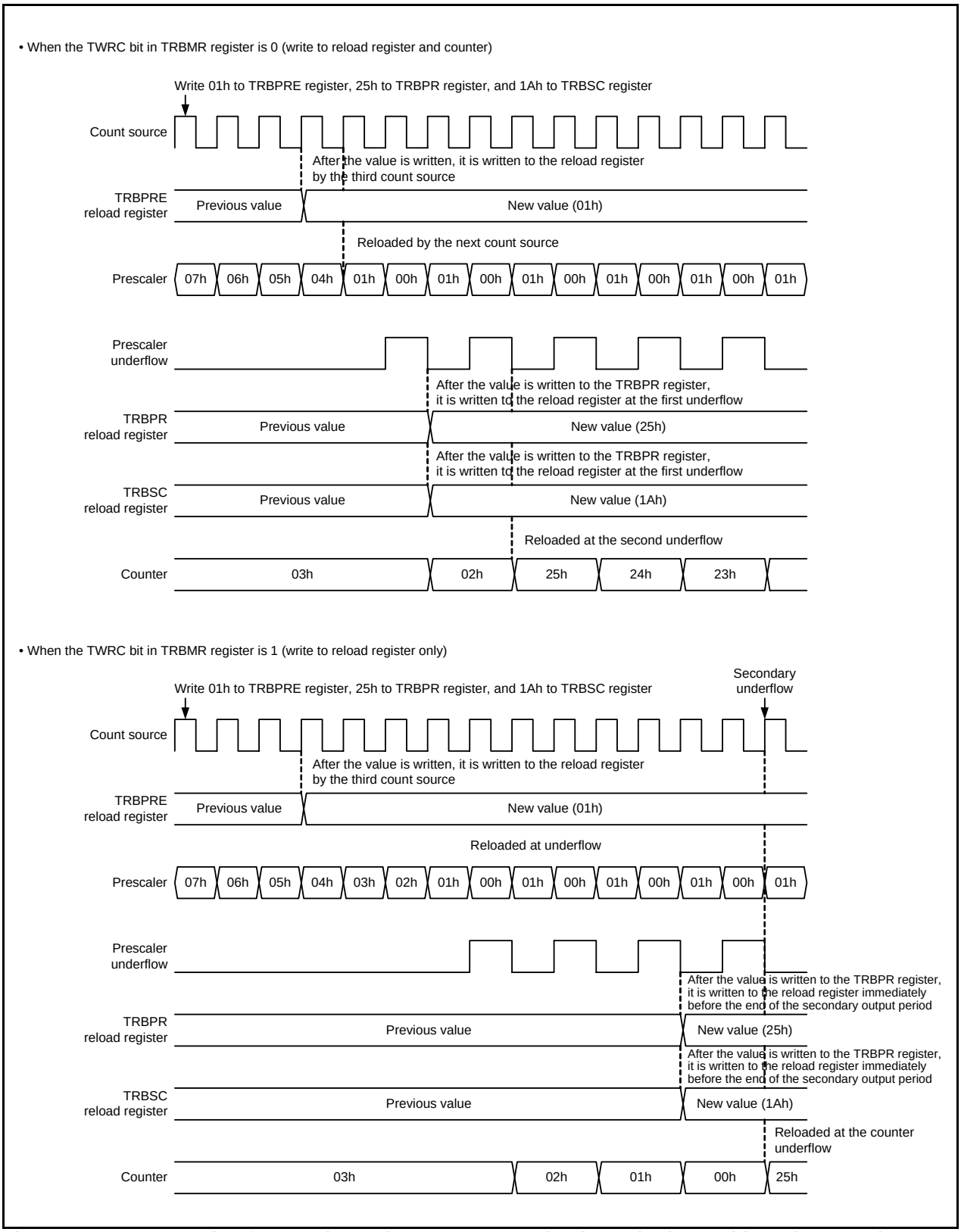


Figure 14.11 Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler (Programmable Waveform Generation Mode or Programmable Wait One-Shot Generation Mode)

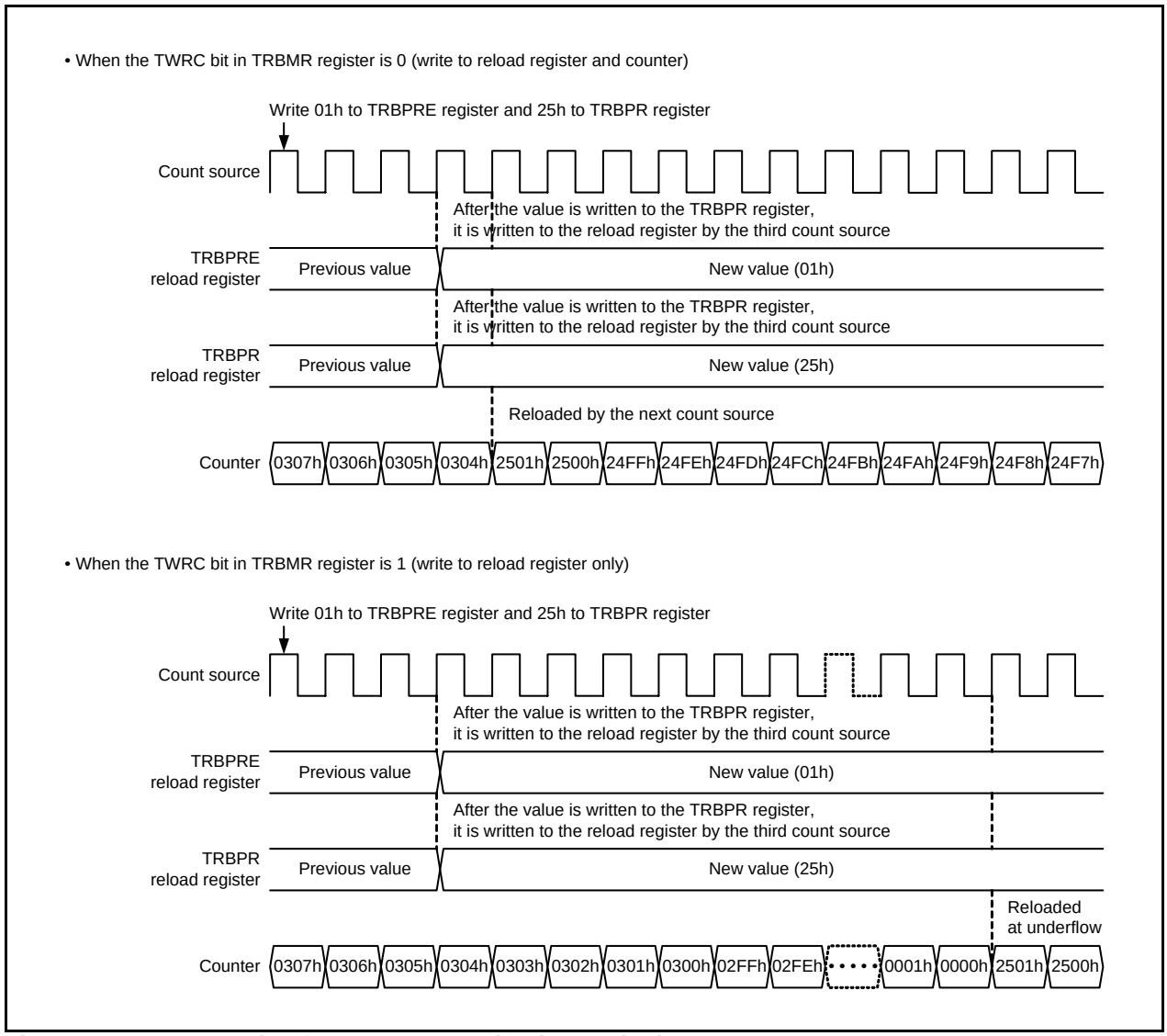


Figure 14.12 Example of Counter Operation in 16-Bit Timer (Timer Mode or Programmable One-Shot Generation Mode)

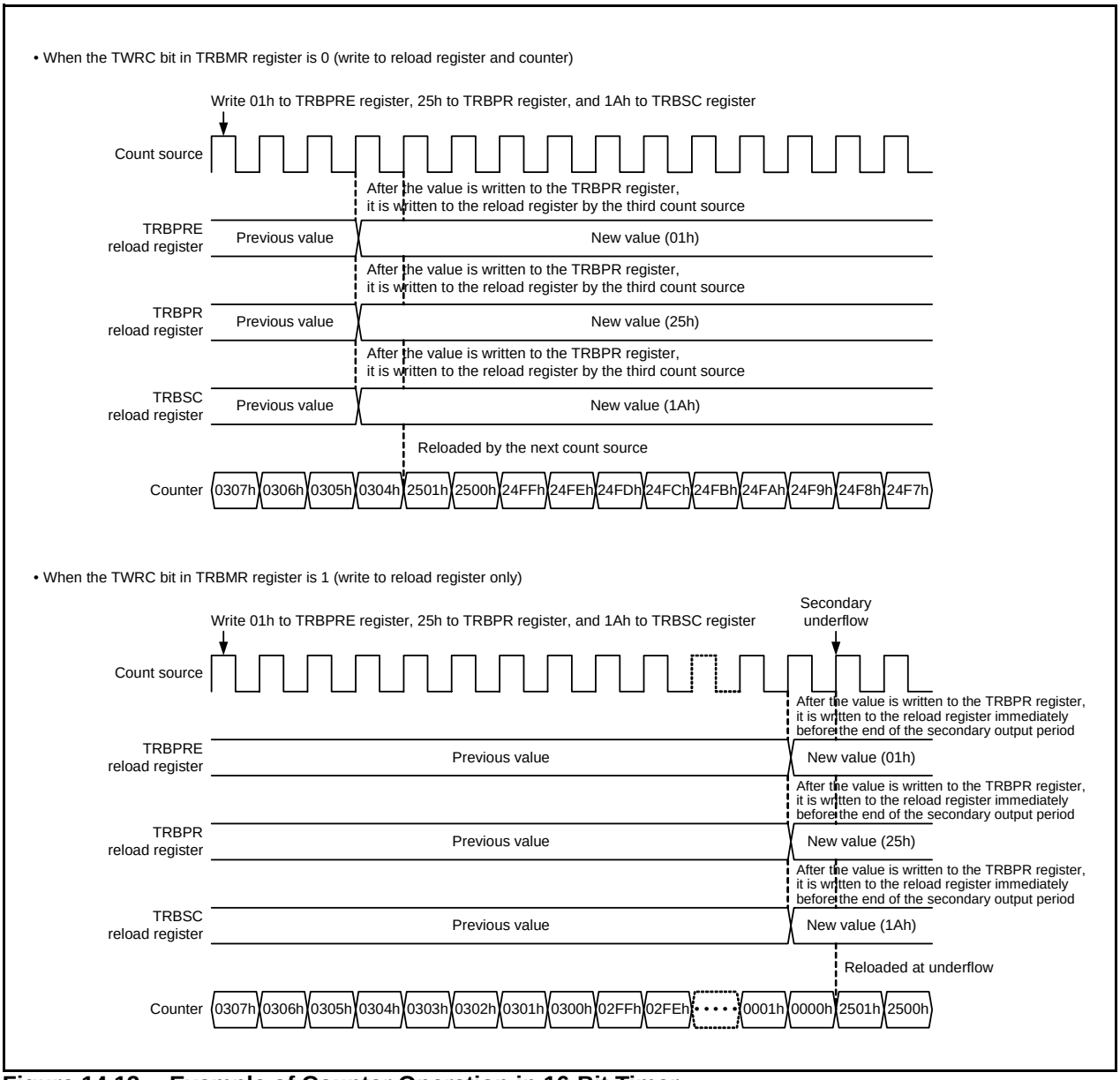


Figure 14.13 Example of Counter Operation in 16-Bit Timer (Programmable Waveform Generation Mode or Programmable Wait One-Shot Generation Mode)

14.5.3 TOCNT Bit Setting and Pin States

The TOCNT bit in the TRBIOC register can be used to select whether a timer waveform or fixed value is output. However, regardless of the setting of the TOCNT bit, an undefined value is output in timer mode and a waveform is output in programmable one-shot and programmable wait one-shot generation modes.
Table 14.8 lists the Output Data in Each Mode.

Table 14.8 Output Data in Each Mode

Operating Mode	Output Enabled/Disabled		Output Data
Timer mode	Output disabled		Undefined-value output
Programmable waveform generation mode	TCONT	0	Waveform output
		1	Fixed value (inverted value of TOPL)
Programmable one-shot generation mode	Output enabled		Waveform output
Programmable wait one-shot generation mode			

TOPL, TOCNT: Bits in TRBIOC register

If the TOCNT bit is rewritten in programmable waveform generation mode, the pin state is not changed immediately. The data is reflected in the pin state when one of the following conditions is met. Note that when the TOCNT bit is 1 (fixed-value output), the value, which is set for the primary period in the TOPL bit in the TRBIOC register, is output.

[Update conditions for pin states]
- When the TSTART bit in the TRBCR register is changed from 0 (count is stopped) to 1 (count is started).
- When the TRBPR register is reloaded to the counter.

14.6 Interrupt Request

When the TRBIF bit in the TRBIR register is 1 (interrupt requested) and the TRBIE bit is 1 (interrupt enabled), an interrupt request is generated to the CPU. The conditions for setting the TRBIF bit to 1 differ depending on the mode. See the descriptions of the TRBIF bit and individual modes.

14.7 $\overline{\text{INT0}}$ Input Trigger Selection

In programmable one-shot and programmable wait one-shot generation modes, when 1 (one-shot count is started) is written to the TOSST bit in the TRBCR register or a trigger is input to the $\overline{\text{INT0}}$ pin with the TCSTF bit in the TRBCR register set to 1 (count is in progress), one-shot operation is started.

When using the trigger input from the $\overline{\text{INT0}}$ pin, make the following settings beforehand.

(1) Set the port mapping register to set port P1_4 or P4_5 as the $\overline{\text{INT0}}$ pin.
(2) Set bits INT0F0 to INT0F1 in the INTF0 register to select the digital filter sampling clock for the $\overline{\text{INT0}}$ pin.
(3) Set the INT0EN bit in the INTEN register to 1 (enabled) to enable an interrupt.
(4) Set the INOSEG bit in the TRBIOC register to select the falling or rising edge.
(5) Set the INOSTG bit in the TRBIOC register to 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled).

When an interrupt request is generated by the trigger input from the $\overline{\text{INT0}}$ pin, note the following:

- Set bits INT0SA to INT0SB in the ISCR0 register to select the falling edge, rising edge, or two-way edge for the interrupt.

Even if a one-shot trigger is generated while the TOSSTF bit in the TRBOCR is 1 (one-shot is operating (including wait period)), timer RB2 operation is not influenced, but the IRI0 bit in the IRR3 register is changed.
For details on interrupts, see **11. Interrupts**.

14.8 Notes on Timer RB2

- Timer RB2 stops counting after a reset. Start the count after setting the value in the timer and prescaler.
- In the 8-bit timer with 8-bit prescaler, even if the prescaler and timer are read in 16-bit units, they are actually read sequentially byte by byte in the MCU. This may cause the value in the timer to be updated during reading of these two registers.
  In the 16-bit timer, access the TRBPRE register first and then the TRBPR register. Read the TRBPRE register first to read the count value in the lower byte. The count value in the higher byte will be retained. Next, read the TRBPR register to read the retained value in the higher byte. The timer value is not updated during reading of these two registers.
- In programmable one-shot and programmable wait one-shot generation modes, when the TOSSP bit in the TRBOCR register is set to 1 and the one-shot is stopped, the timer reloads the reload register value and is stopped. The timer count value must be read before the timer is stopped.
- After 1 (count is started) is written to the TSTART bit in the TRBCR register while the count is stopped, the TCSTF bit in the TRBCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started on the first active edge of the counter source after the TCSTF bit is set to 1.
  After 0 (count is stopped) is written to the TSTART bit during count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 0.
  Note:
  1. Registers associated with timer RB2:
     TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBPR, and TRBSC
- In timer mode, do not set both the TRBPRE and TRBPR registers to 00h at the same time.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), change the values of registers TRBPRE, TRBPR, and TRBSC, then wait for at least two cycles of the system clock (f) before setting the TSTART bit in the TRBCR register to 1 (count is started).
- When the TSTART bit in the TRBCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), do not change the values in registers TRBIOC and TRBMR, and the TRBIE bit in the TRBIR register.
- Make sure the TCSTF bit in the TRBCR register is 1 (count is in progress) before writing 1 (one-shot count is started) to the TOSST bit in the TRBOCR register. When the TCSTF bit is 0 (count is stopped), writing 1 (one-shot count is started) to the TOSST bit is invalid.
- When writing to registers TRBPRE, TRBPR, and TRBSC during count operation (the TSTART bit is 1 or the TCSTF bit is 1), note the following points:
  - When writing to the TRBPRE register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBPR register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBSC register successively, allow at least three cycles of the count source for each write interval.
- When the TRBPR register is rewritten in programmable waveform generation mode, do not write to the TRBPRE, TRBPR, or TRBSC register during the secondary output period as described below after rewriting.
  - 8-bit timer with 8-bit prescaler:
    Two cycles of the prescaler underflow before the secondary output period ends.
  - 16-bit timer:
    Two cycles of the count source clock before the secondary output period ends.
- When the underflow signal from timer RJ2 is used as the count source for timer RB2, set timer RJ2 to timer mode, pulse output mode, or event counter mode.

- When 1 is written to the TOSST bit or the TOSSP bit in the TRBOCR register, the TOSSTF bit is changed after two to three cycles of the count source. If 1 is written to the TOSSP bit from when 1 is written to the TOSST bit until the TOSSTF bit is set to 1, the TOSSTF bit may be set to 0 or 1 depending on the internal state. Likewise, if 1 is written to the TOSST bit from when 1 is written to the TOSSP bit until the TOSSTF bit is set to 0, the TOSSTF may be set to 0 or 1 depending on the internal state.
- In programmable waveform generation mode and programmable wait one-shot mode, write to the TRBSC register before writing to the TRBPR register. At the underflow during the secondary period after the TRBPR register is written, the value written to the TRBPR register is transferred to the counter. If registers TRBPR and TRBSC are written two or more times after the TRBPR register is written until the underflow during the secondary period, the last written value is transferred to the counter at the underflow.
- When 1 is written to the TSTOP bit in the TRBCR register during count operation, timer RB2 is immediately stopped.
- If the count is forcibly stopped by writing 1 to the TSTOP bit during count operation, the TRBIF bit in the TRBIR register may be set to 1 (interrupt requested). Set the TRBIF bit to 0 (no interrupt requested) before restarting the count.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), wait for at least two cycles of the system clock (f) after writing the values of registers TRBPRE and TRBPR before reading them.

15. Timer RC

Timer RC is a 16-bit timer that provides output compare and input capture functions and can count external events. It can be used as a multifunction timer with various applications such as generation of pulse output with an arbitrary duty cycle using the compare match between the timer RC counter and four general registers.

15.1 Overview

Table 15.1 lists the Timer RC Specifications. Table 15.2 lists the Timer RC Functions. Figure 15.1 shows the Timer RC Block Diagram. Table 15.3 lists Timer RC Pin Configuration.

Table 15.1 Timer RC Specifications

Item			Description
Count sources (counter input clocks)	Operating clock	Internal clock	• f1, f2, f4, f8, or f32: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 000b to 100b. • fHOCO: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 110b.
		External clock (external event count)	TRCCLK input: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 101b.
Pulse I/O pins			4
General registers			4 • Can be set as output compare or input capture registers individually. • Can be used as buffer registers for output compare or input capture.
Operating modes	Timer mode		• Output compare function: Low-level, high-level, or toggle output can be performed. • Input capture function: A rising edge, falling edge, or two-way edge can be detected. • Counter clear function: A count period can be set.
	PWM mode		PWM output with up to three phases.
	PWM2 mode		Pulse output with an arbitrary period and duty.
Interrupt sources			• Compare match/input capture multiplexed interrupt × 4 sources • Overflow interrupt
Others			• The initial value of the timer RC output can be set arbitrarily. • A/D conversions triggered by compare matches in registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD can be set.

Table 15.2 Timer RC Functions

Item		Counter	I/O Pin			
			TRCIOA	TRCIOB	TRCIOC	TRCIOD
General registers (output compare/input capture multiplexed registers)		Period setting with the TRCGRA register	TRCGRA register	TRCGRB register	TRCGRC register In buffer operation Buffer register for the TRCGRA register	TRCGRD register In buffer operation Buffer register for the TRCGRB register
Counter clear function		Input capture/ compare match for the TRCGRA register	Input capture/ compare match for the TRCGRA register	—	—	—
		TRCTRG input	—	—	—	—
Setting function for initial output level		—	Available	Available	Available	Available
Buffer operation		—	Available	Available	—	—
Compare match	Low-level output	—	Available	Available	Available	Available
	High-level output	—	Available	Available	Available	Available
	Toggle output	—	Available	Available	Available	Available
Input capture function		—	Available	Available	Available	Available
PWM mode		—	—	Available	Available	Available
PWM2 mode		—	—	Available	—	—
Interrupt sources		Overflow	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture

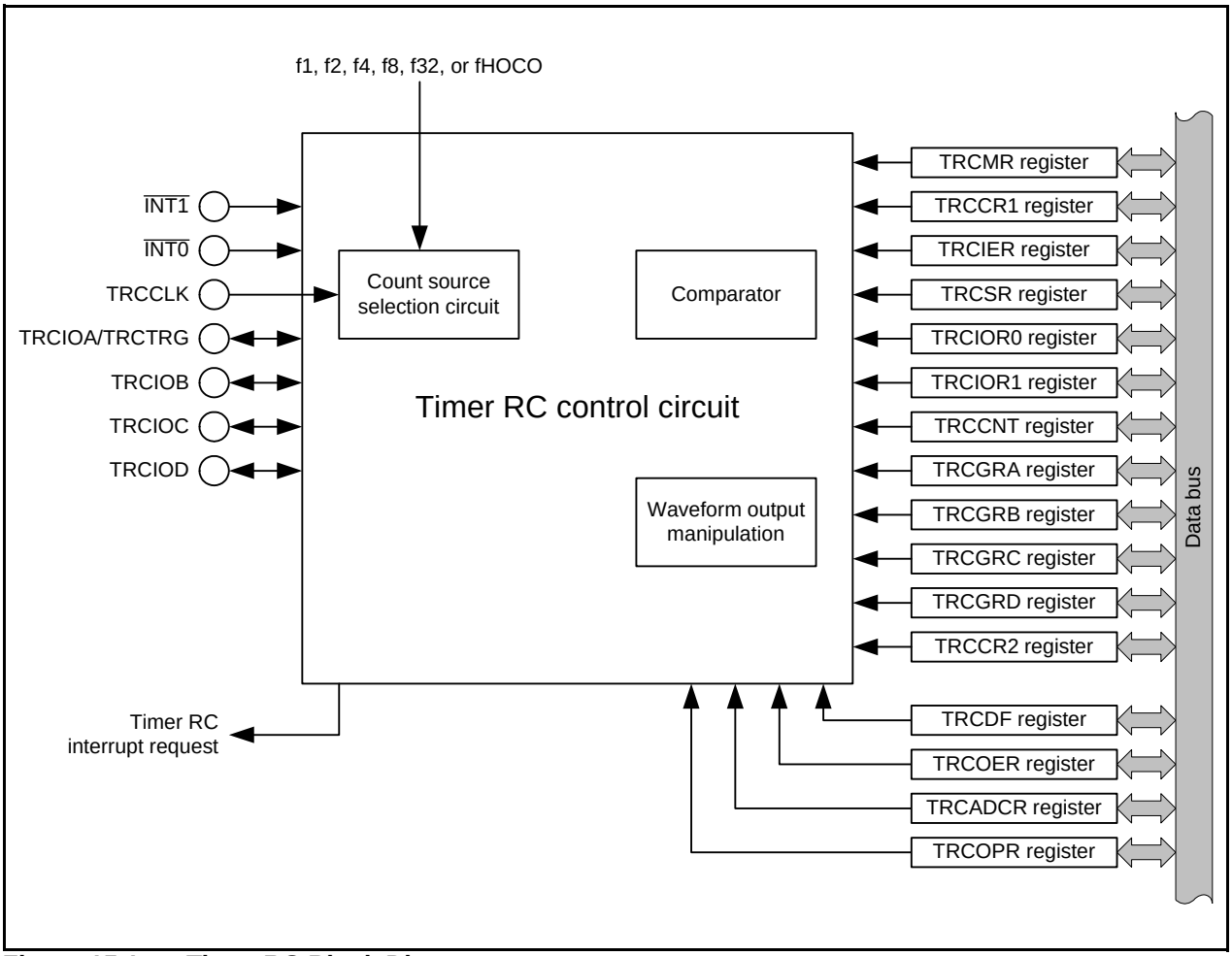


Figure 15.1 Timer RC Block Diagram

Table 15.3 Timer RC Pin Configuration

Pin Name	I/O	Function
TRCCLK	I	External clock input
TRCIOA/TRCTRG	I/O	TRCGRA output compare output/TRCGRA input capture input/external trigger input (TRCTRG)
TRCIOB	I/O	TRCGRB output compare output/TRCGRB input capture input/PWM output (in PWM mode)
TRCIOC	I/O	TRCGRC output compare output/TRCGRC input capture input/PWM output (in PWM mode)
TRCIOD	I/O	TRCGRD output compare output/TRCGRD input capture input/PWM output (in PWM mode)
$\overline{\text{INT0}}$	I	Timer output disabling control input
$\overline{\text{INT1}}$	I	Waveform output manipulation event input

15.2 Registers

Table 15.4 lists the Timer RC Register Configuration.

Table 15.4 Timer RC Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RC Counter	TRCCNT	00h	000E8h	16
		00h	000E9h	
Timer RC General Register A	TRCGRA	FFh	000EAh	16
		FFh	000EBh	
Timer RC General Register B	TRCGRB	FFh	000ECh	16
		FFh	000EDh	
Timer RC General Register C	TRCGRC	FFh	000EEh	16
		FFh	000EFh	
Timer RC General Register D	TRCGRD	FFh	000F0h	16
		FFh	000F1h	
Timer RC Mode Register	TRCMR	01001000b	000F2h	8
Timer RC Control Register 1	TRCCR1	00h	000F3h	8
Timer RC Interrupt Enable Register	TRCIER	01110000b	000F4h	8
Timer RC Status Register	TRCSR	01110000b	000F5h	8
Timer RC I/O Control Register 0	TRCIOR0	10001000b	000F6h	8
Timer RC I/O Control Register 1	TRCIOR1	10001000b	000F7h	8
Timer RC Control Register 2	TRCCR2	00011000b	000F8h	8
Timer RC Digital Filter Function Select Register	TRCDF	00h	000F9h	8
Timer RC Output Enable Register	TRCOER	01111111b	000FAh	8
Timer RC A/D Conversion Trigger Control Register	TRCADCR	11110000b	000FBh	8
Timer RC Waveform Output Manipulation Register	TRCOPR	00h	000FCh	8

15.2.1 Timer RC Counter (TRCCNT)

Address 000E8h to 000E9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	16-bit readable/writable up counter. When this counter overflows, the OVF bit in the TRCSR register is set to 1. If the OVIE bit in the TRCIER register is set to 1 (interrupt request (FOVI) by OVF bit is enabled) at this time, an interrupt request is generated.	0000h to FFFFh	R/W

The count source for the TRCCNT register is selected by bits CKS0 to CKS2 in the TRCCR1 register. When the CCLR bit in the TRCCR1 register is 1, the TRCCNT register is cleared to 0000h when a compare match with the TRCGRA register occurs.

TRCCNT register must be accessed in 16-bit units. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units.

15.2.2 Timer RC General Register A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, and TRCGRD)

Address 000EAh to 000EBh (TRCGRA), 000ECh to 000EDh (TRCGRB), 000EEh to 000EFh (TRCGRC), 000F0h to 000F1h (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Table 15.5 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	—	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BUFEA = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer registers. Can be used to hold transferred value from the general register. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOA
TRCGRD	BUFEB = 1		TRCIOB

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register

Table 15.6 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	—	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BUFEA = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOA
TRCGRD	BUFEB = 1		TRCIOB

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register

Table 15.7 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	—	General register. Set the PWM period.	—
TRCGRB	—	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BUFEA = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer register. Set the next PWM period. (Refer to **15.5.5 Buffer Operation Timing**.)	—
TRCGRD	BUFEB = 1	Buffer register. Set the next PWM output change point. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOB

h = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register
Note:
1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

Table 15.8 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	—	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	—	General register. Set the PWM output change point.	
TRCGRC (1)	BUFEA = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BUFEB = 0	(Not used in PWM2 mode)	—
TRCGRD	BUFEB = 1	Buffer register. Set the next PWM output change point. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOB pin

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register
Note:
1. Do not set the TRCGRB and TRCGRC registers to the same value.

15.2.3 Timer RC Mode Register (TRCMR)

Address 000F2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CTS	—	BUFEB	BUFEA	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	TRCIOB PWM mode select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	TRCIOC PWM mode select bit (1)		R/W
b2	PWMD	TRCIOD PWM mode select bit (1)		R/W
b3	PWM2	PWM2 mode select bit	0: PWM2 mode 1: Timer mode or PWM mode	R/W
b4	BUFEA	TRCGRC register function select bit (2)	0: Output compare or input capture register 1: TRCGRC register is used as a buffer register for TRCGRA register	R/W
b5	BUFEB	TRCGRD register function select bit	0: Output compare or input capture register 1: TRCGRD register is used as a buffer register for TRCGRB register	R/W
b6	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b7	CTS	TRCCNT count start bit	0: Count is stopped 1: Count is started	R/W

Notes:
1. These bits are enabled when the PWM2 bit is 1 (timer mode or PWM mode).
2. Set the BUFEA bit to 0 (general register) in PWM2 mode.

CTS Bit (TRCCNT count start bit)

[Conditions for setting to 0]
- When 0 is written to this bit.
- When a compare match occurs while the CSTP bit in the TRCCR2 register is 1 (increment is stopped) in PWM2 mode.

[Condition for setting to 1]
- When 1 is written to this bit.

15.2.4 Timer RC Control Register 1 (TRCCR1)

Address 000F3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	CKS2	CKS1	CKS0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	Timer output level select A bit	0: Output value 0 (1) 1: Output value 1 (1)	R/W
b1	TOB	Timer output level select B bit		R/W
b2	TOC	Timer output level select C bit		R/W
b3	TOD	Timer output level select D bit		R/W
b4	CKS0	Count source select bits	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: Falling edge of TRCCLK input (3) 1 1 0: fHOCO (2) 1 1 1: Do not set.	R/W
b5	CKS1			R/W
b6	CKS2			R/W
b7	CCLR	TRCCNT counter clear select bit	0: Clear disabled (free-running operation) 1: TRCCNT counter is cleared by input capture/compare match A	R/W

Notes:
1. The values set by bits TOA to TOD are reflected immediately after they are changed. Set the value when the CTS bit in the TRCMR register is 0 (count is stopped).
2. When selecting fHOCO, set these bits with the on-chip oscillator operating. When switching the count sources, set these bits with the counter stopped.
3. The pulse width of an external clock input to TRCCLK must be three or more cycles of the operating clock.

TOA Bit (Timer output level select A bit)

This bit is used to set the output value from the TRCIOA pin until the first compare match A occurs. In PWM mode, this bit is used to control the output level of the TRCIOA pin.

TOB Bit (Timer output level select B bit)

This bit is used to set the output value from the TRCIOB pin until the first compare match B occurs. In PWM mode, this bit is used to control the output level of the TRCIOB pin.

TOC Bit (Timer output level select C bit)

This bit is used to set the output value from the TRCIOC pin until the first compare match C occurs. In PWM mode, this bit is used to control the output level of the TRCIOC pin.

TOD Bit (Timer output level select D bit)

This bit is used to set the output value from the TRCIOD pin until the first compare match D occurs. In PWM mode, this bit is used to control the output level of the TRCIOD pin.

15.2.5 Timer RC Interrupt Enable Register (TRCIER)

Address 000F4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match A interrupt enable bit	0: Interrupt request (IMIA) by IMFA bit in TRCSR register is disabled 1: Interrupt request (IMIA) by IMFA bit in TRCSR register is enabled	R/W
b1	IMIEB	Input capture/compare match B interrupt enable bit	0: Interrupt request (IMIB) by IMFB bit in TRCSR register is disabled 1: Interrupt request (IMIB) by IMFB bit in TRCSR register is enabled	R/W
b2	IMIEC	Input capture/compare match C interrupt enable bit	0: Interrupt request (IMIC) by IMFC bit in TRCSR register is disabled 1: Interrupt request (IMIC) by IMFC bit in TRCSR register is enabled	R/W
b3	IMIED	Input capture/compare match D interrupt enable bit	0: Interrupt request (IMID) by IMFD bit in TRCSR register is disabled 1: Interrupt request (IMID) by IMFD bit in TRCSR register is enabled	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	OVIE	Timer overflow interrupt enable bit	0: Interrupt request (FOVI) by OVF bit in TRCSR register is disabled 1: Interrupt request (FOVI) by OVF bit in TRCSR register is enabled	R/W

15.2.6 Timer RC Status Register (TRCSR)

Address 000F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match A flag	[Condition for setting to 0] • When 0 is written to this bit after reading it as 1. (1) [Condition for setting to 1] • See **Table 15.9 Conditions for Setting Each Flag to 1**.	R/W
b1	IMFB	Input capture/compare match B flag		R/W
b2	IMFC	Input capture/compare match C flag		R/W
b3	IMFD	Input capture/compare match D flag		R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	OVF	Timer overflow flag	[Condition for setting to 0] • When 0 is written to this bit after reading it as 1. [Condition for setting to 1] • See **Table 15.9 Conditions for Setting Each Flag to 1**.	R/W

Note:
1. The results of writing this bit are as follows.
   • If the result of reading this bit is 1, writing 0 to this bit will set it to 0.
   • If the result of reading this bit is 0, writing 0 to this bit will not change its value. (If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written.)
   • Writing 1 has no effect.

Table 15.9 Conditions for Setting Each Flag to 1

Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input Capture Function	Output Compare Function		
IMFA	When the value in the TRCCNT register is transferred to the TRCGRA register on the input edge (1) of the TRCIOA pin.	When the values in registers TRCCNT and TRCGRA match.		
IMFB	When the value in the TRCCNT register is transferred to the TRCGRB register on the input edge (1) of the TRCIOB pin.	When the values in registers TRCCNT and TRCGRB match.		
IMFC	When the value in the TRCCNT register is transferred to the TRCGRC register on the input edge (1) of the TRCIOC pin.	When the values in registers TRCCNT and TRCGRC match. (2)		
IMFD	When the value in the TRCCNT register is transferred to the TRCGRD register on the input edge (1) of the TRCIOD pin.	When the values in registers TRCCNT and TRCGRD match. (2)		
OVF	When the TRCCNT register overflows from FFFFh to 0000h.			

Notes:
1. The edge is selected by bits IOj0 to IOj1 (j = A, B, C, or D) in registers TRCIO0 and TRCIOR1. However, all of bits IOA2 and IOB2 in the TRCIOR0 register and bits IOC2 and IOD2 in the TRCIOR1 register must be set to 1 (input capture function).
2. Includes when bits BUFEA and BUFEB in the TRCMR register are 1 (buffer registers for TRCGRA and TRCGRB).

15.2.7 Timer RC I/O Control Register 0 (TRCIOR0)

Address 000F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control A0 bit	[IOA2 = 0 (output compare function)]	R/W
b1	IOA1	TRCGRA control A1 bit	b1 b0 0 0: Pin output by compare match A is disabled 0 1: Low-level output from TRCIOA pin at compare match A 1 0: High-level output from TRCIOA pin at compare match A 1 1: Toggle output from TRCIOA pin at compare match A [IOA2 = 1 (input capture function)] b1 b0 0 0: Rising edge on TRCIOA pin 0 1: Falling edge on TRCIOA pin 1 0: Two-way edge on TRCIOA pin 1 1: Do not set.	R/W
b2	IOA2	TRCGRA control A2 bit (1)	0: Output compare function 1: Input capture function	R/W
b3	—	Reserved	Set to 1.	R/W
b4	IOB0	TRCGRB control B0 bit	[IOB2 = 0 (output compare function)]	R/W
b5	IOB1	TRCGRB control B1 bit	b5 b4 0 0: Pin output by compare match B is disabled 0 1: Low-level output from TRCIOB pin at compare match B 1 0: High-level output from TRCIOB pin at compare match B 1 1: Toggle output from TRCIOB pin at compare match B [IOB2 = 1 (input capture function)] b5 b4 0 0: Rising edge on TRCIOB pin 0 1: Falling edge on TRCIOB pin 1 0: Two-way edge on TRCIOA pin 1 1: Do not set.	R/W
b6	IOB2	TRCGRB control B2 bit (1)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. The write value must be 1. The read value is 1.		—

Note:
1. When bits BUFEA and BUFEB in the TRCMR register are set to 1, registers TRCGRA and TRCGRC, and registers TRCGRB and TRCGRD are paired. The same values must be set in the IOA2 bit and the IOC2 bit in the TRCIOR1 register, and in the IOB2 bit and the IOD2 bit in the TRCIOR1 register, respectively.

The setting of the TRCIOR0 register is invalid in PWM and PWM2 modes.

15.2.8 Timer RC I/O Control Register 1 (TRCIOR1)

Address 000F7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control C0 bit	[IOC2 = 0, IOC3 = 0 (output from TRCIOA pin at compare match C)] (1, 2) b1 b0 0 0: Pin output by compare match C is disabled 0 1: Low-level output from TRCIOA pin at compare match C 1 0: High-level output from TRCIOA pin at compare match C 1 1: Toggle output from TRCIOA pin at compare match C [IOC2 = 0, IOC3 = 1 (output from TRCIOC pin at compare match C)] (1) b1 b0 0 0: Pin output by compare match C is disabled 0 1: Low-level output from TRCIOC pin at compare match C 1 0: High-level output from TRCIOC pin at compare match C 1 1: Toggle output from TRCIOC pin at compare match C [IOC2 = 1, IOC3 = 1 (TRCIOC input edge selected at input capture C)] (3) b1 b0 0 0: Input capture C occurs on the rising edge of TRCIOC input 0 1: Input capture C occurs on the falling edge of TRCIOC input 1 0: Input capture C occurs on the two-way edge of TRCIOC input 1 1: Do not set.	R/W
b1	IOC1	TRCGRC control C1 bit		R/W
b2	IOC2	TRCGRC control C2 bit (4)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC control C3 bit	0: Output from TRCIOA pin at compare match C (8) 1: Output from TRCIOC pin at compare match C	R/W
b4	IOD0	TRCGRD control D0 bit	[IOD2 = 0, IOD3 = 0 (output from TRCIOB pin at compare match D)] (5, 6) b5 b4 0 0: Pin output by compare match D is disabled 0 1: Low-level output from TRCIOB pin at compare match D 1 0: High-level output from TRCIOB pin at compare match D 1 1: Toggle output from TRCIOB pin at compare match D [IOD2 = 0, IOD3 = 1 (output from TRCIOD pin at compare match D)] (5) b5 b4 0 0: Pin output by compare match D is disabled 0 1: Low-level output from TRCIOD pin at compare match D 1 0: High-level output from TRCIOD pin at compare match D 1 1: Toggle output from TRCIOD pin at compare match D [IOD2 = 1, IOD3 = 1 (TRCIOD input edge selected at input capture D)] (7) b5 b4 0 0: Input capture D occurs on the rising edge of TRCIOD input 0 1: Input capture D occurs on the falling edge of TRCIOD input 1 0: Input capture D occurs on the two-way edge of TRCIOD input 1 1: Do not set.	R/W
b5	IOD1	TRCGRD control D1 bit		R/W
b6	IOD2	TRCGRD control D2 bit (4)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD control D3 bit	0: Output from TRCIOB pin at compare match D (8) 1: Output from TRCIOD pin at compare match D	R/W

Notes:
1. When the BUFEA bit in the TRCMR register is 1 (TRCGRC register is used as a buffer register for TRCGRA register), the value of the TRCGRC register is transferred to the TRCGRA register at compare match A.
2. When the IOA2 bit in the TRCIOR0 register is 0 (output compare function), if compare matches A and C occur simultaneously, the output from the TRCIOA pin at compare match C takes precedence.
3. When the BUFEA bit is 1 (TRCGRC register is used as a buffer register for TRCGRA register), the value of the TRCGRA register is transferred to the TRCGRC register at input capture A. When the input capture edge of the TRCIOC pin selected by bits IOC0 to IOC1 is input, the IMFC bit in the TRCSR register is set to 1. However, the count value is not transferred to the TRCGRC register.

4. In buffer operation, registers TRCGRA and TRCGRC, and registers TRCGRB and TRCGRD are paired. The same values must be set in the IOC2 bit and the IOA2 bit in the TRCIOR0 register, and in the IOD2 bit and the IOB2 bit in the TRCIOR0 register, respectively.
5. When the BUFEB bit in the TRCMR register is 1 (TRCGRD register is used as a buffer register for TRCGRB register), the value of the TRCGRD register is transferred to the TRCGRB register at compare match B.
6. When the IOB2 bit in the TRCIOR0 register is 0 (output compare function), if compare matches B and D occur simultaneously, the output from the TRCIOB pin at compare match D takes precedence.
7. When the BUFEB bit is 1 (TRCGRD register is used as a buffer register for TRCGRB register), the value of the TRCGRB register is transferred to the TRCGRD register at input capture B. When the input capture edge of the TRCIOD pin selected by bits IOD0 to IOD1 is input, the IMFD bit in the TRCSR register is set to 1. However, the count value is not transferred to the TRCGRD register.
8. When IOC2 = 1, do not set the IOC3 bit to 0.
   When IOD2 = 1, do not set the IOD3 bit to 0.

The setting of the TRCIOR1 register is invalid in PWM and PWM2 modes.

15.2.9 Timer RC Control Register 2 (TRCCR2)

Address 000F8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSTP	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	TRCIOB PWM mode output level control bit (1)	0: Output level is active low 1: Output level is active high	R/W
b1	POLC	TRCIOC PWM mode output level control bit (1)		R/W
b2	POLD	TRCIOD PWM mode output level control bit (1)		R/W
b3	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b4	—			
b5	CSTP	Count stop bit (2)	0: Count is continued even after compare match with TRCGRA register 1: Count is stopped at compare match with TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bits (3)	b7 b6 0 0: TRCTRG input disabled 0 1: Rising edge 1 0: Falling edge 1 1: Both rising and falling edges	R/W
b7	TCEG1			R/W

Notes:
1. Enabled in PWM mode.
2. Enabled in the output compare function, PWM mode, and PWM2 mode. For notes on PWM2 mode, see **15.7.6 TRCMR Register in PWM2 Mode**.
3. Enabled in PWM2 mode.

15.2.10 Timer RC Digital Filter Function Select Register (TRCDF)

Address 000F9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA digital filter function bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB digital filter function bit (1)		R/W
b2	DFC	TRCIOC digital filter function bit (1)		R/W
b3	DFD	TRCIOD digital filter function bit (1)		R/W
b4	DFTRG	TRCTRG digital filter function bit (2)		R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	DFCK0	Digital filter clock select bits (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits CKS2 to CKS0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. Enabled in the input capture function.
2. Enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

15.2.11 Timer RC Output Enable Register (TRCOER)

Address 000FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (3)	[When the OPE bit in the TRCOPR register is 0 (waveform output manipulation disabled)] (1) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR0) 1: Output disabled (independent of settings of registers TRCMR and TRCIOR0) [When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled)] (2) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR0) 1: Output level is fixed or high impedance depending on TRCOPR register setting	R/W
b1	EB	TRCIOB output disable bit (3)		R/W
b2	EC	TRCIOC output disable bit (3)	[When the OPE bit in the TRCOPR register is 0 (waveform output manipulation disabled)] (1) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR1) 1: Output disabled (independent of settings of registers TRCMR and TRCIOR1) [When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled)] (2) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR1) 1: Output level is fixed or high impedance depending on TRCOPR register setting	R/W
b3	ED	TRCIOD output disable bit (3)		R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	PTO	Timer output disable bit	[When the OPE bit in the TRCOPR register is 0 (waveform output manipulation disabled)] 0: Bits EA to ED do not change even if a low level is input to the $\overline{\text{INT0}}$ pin 1: When a low level is input to the $\overline{\text{INT0}}$ pin, bits EA to ED are set to 1 (output disabled) (For $\overline{\text{INT0}}$, see **11. Interrupts**.) [When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled)] The function of the PTO bit is disabled (bits EA to ED do not change even if a low level is input to the $\overline{\text{INT0}}$ pin). This bit can be read or written.	R/W

Notes:
1. Bits EA to ED can be set by software. When the PTO bit is 1 and a low level is input to the $\overline{\text{INT0}}$ pin, bits EA to ED are set to 1 (output disabled)).
2. Regardless of the set value of the PTO bit, bits EA to ED do not change even if a low level is input to the $\overline{\text{INT0}}$ pin.
   When the RESTATS bit in the TRCOPR register is 1, bits EA to ED cannot be set by software. When the waveform output manipulation event selected by bits OPSEL0 to OPSEL1 in the TRCOPR register is input, bits EA to ED are set to 1. If the waveform output manipulation event is cancelled, bits EA to ED are set to 0.
   When the RESTATS bit is 0, bits EA to ED can be set by software. When the waveform output manipulation event selected by bits OPSEL0 to OPSEL1 is input, bits EA to ED are set to 1. However, bits EA to ED are not automatically set to 0 even if the waveform output manipulation event is cancelled. Set these bits to 0 by software.
3. Disabled when the corresponding pin is used as input capture input.

15.2.12 Timer RC A/D Conversion Trigger Control Register (TRCADCR)

Address 000FBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ADTRGDE	ADTRGCE	ADTRGBE	ADTRGAE
After Reset	1	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	TRCGRA A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match A 1: An A/D conversion start trigger occurs at compare match A	R/W
b1	ADTRGBE	TRCGRB A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match B 1: An A/D conversion start trigger occurs at compare match B	R/W
b2	ADTRGCE	TRCGRC A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match C 1: An A/D conversion start trigger occurs at compare match C	R/W
b3	ADTRGDE	TRCGRD A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match D 1: An A/D conversion start trigger occurs at compare match D	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	—			

15.2.13 Timer RC Waveform Output Manipulation Register (TRCOPR)

Address 000FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	OPE	RESTATS	OPOL1	OPOL0	OPSEL1	OPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OPSEL0	Waveform output manipulation event select bits (1)	b1 b0 0 0: Waveform output is manipulated during low-level period of comparator B1 (VCOUT1) output level 0 1: Waveform output is manipulated during low-level period of INT1 input level Other than the above: Waveform output is manipulated during low-level period of comparator B1 (VCOUT1) output level or INT1 input level	R/W
b1	OPSEL1			R/W
b2	OPOL0	Waveform output manipulation period output level select bits	b3 b2 0 0: When timer RC pin is pulled down, timer RC output level is fixed to high impedance during waveform output manipulation period 0 1: When timer RC pin is pulled up, timer RC output level is fixed to high impedance during waveform output manipulation period 1 0: Timer RC output level is fixed at low during waveform output manipulation period 1 1: Timer RC output level is fixed at high during waveform output manipulation period	R/W
b3	OPOL1			R/W
b4	RESTATS	Restart method select bit (2)	0: Output is restarted by software (3) 1: Output is automatically restarted (4)	R/W
b5	OPE	Waveform output manipulation enable bit (5)	0: Waveform output manipulation disabled 1: Waveform output manipulation enabled	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. When the OPE bit is 1 (waveform output manipulation enabled), bits EA to ED in the TRCOER register are set to 1 (output level is fixed or high impedance depending on TRCOPR register setting) if the waveform output manipulation event is input.
2. When the OPE bit is 0 (waveform output manipulation disabled), bits EA to ED in the TRCOER register are not affected by the setting of this bit.
3. When the OPE bit is 1 or the RESTATS bit is 0 (output is restarted by software), bits EA to ED in the TRCOER register are set to 0 by software. Bits EA to ED are not automatically set to 0 even if the waveform output manipulation event is cancelled.
4. When the OPE bit is 1 or the RESTATS bit is 1 (output is automatically restarted), bits EA to ED are automatically set to 0 if the waveform output manipulation event is cancelled.
5. When the OPE bit is 0, only the setting of the TRCOER register is used to manipulate the output for timer RC. When the OPE bit is 1, regardless of the setting of the PTO bit in the TRCOER register, the waveform output for timer RC is manipulated with the settings of the TRCOPR register. Bits EA to ED in the TRCOER register are used as the flags for manipulating the waveform output. When a waveform output manipulation event is input, bits EA to ED are set to 1.

15.3 Operation

Table 15.10 lists the Timer RC Operating Modes.

Table 15.10 Timer RC Operating Modes

Item	Description
Timer mode	Timer mode is used by setting the PWM2 bit to 0 and bits PWMB to PWMD to 0 in the TRCMR register. In this case, the output compare function or input capture function is used by setting bits IOA0 to IOA2 and IOB0 to IOB2 in the TRCIOR0 register and bits IOC0 to IOC2 and IOD0 to IOD2 in the TRCIOR1 register.
PWM mode	PWM mode is used by setting the PWM2 bit to 0 and bits PWMB to PWMD to 1 in the TRCMR register.
PWM2 mode	PWM2 mode is used by setting the PWM2 bit in the TRCMR register to 1.

Tables 15.11 to 15.14 list the settings of pins TRCIOA to TRCIOD. For the assignments of pins TRCIOA to TRCIOD, see **12. I/O Ports**.

Table 15.11 TRCIOA Pin Settings

Register	TRCOER	TRCMR	TRCIOR0			Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	
Setting value	0	1	0	0	1	Timer mode waveform output (output compare function)
				1	X	
	X	1	1	X	X	Timer mode (input capture function)
	Other than the above					I/O port

X: 0 or 1

Table 15.12 TRCIOB Pin Settings

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	Other than the above						I/O port

X: 0 or 1

Table 15.13 TRCIOC Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	PWM2 = 1 and other than the above						I/O port

X: 0 or 1

Table 15.14 TRCIOD Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	PWM2 = 1 and other than the above						I/O port

X: 0 or 1

15.3.1 Timer Mode

The TRCCNT register performs free-running or period count operations. Immediately after a reset, the TRCCNT register functions as a free-running counter. When the CTS bit in the TRCMR register to set to 1 (count is started), count operation is started. When the TRCCNT register overflows from FFFFh to 0000h, the OVF bit in the TRCSR register is set to 1, and an interrupt request is generated if the OVIE bit in the TRCIER register is 1 (interrupt request (FOVI) by OVF flag is enabled).
Figure 15.2 shows an Example of Free-Running Counter Operation.

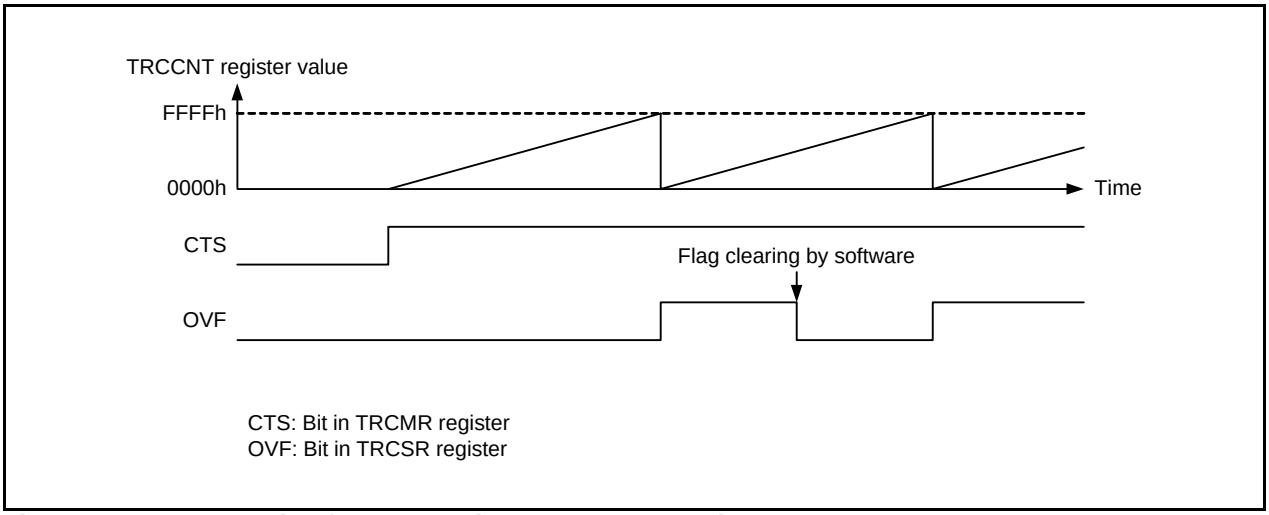


Figure 15.2 Example of Free-Running Counter Operation

When the TRCGRA register for period setting is set as an output compare register and the CCLR bit in the TRCCR1 register is set to 1, a period count operation is performed. When the count value matches the TRCGRA register, the TRCCNT register changes to 0000h and the IMFA bit in the TRCSR register is set to 1. If the corresponding IMIEA bit in the TRCIER register is 1 (interrupt request (IMIA) by IMFA bit in TRCSR register is enabled) at this time, an interrupt request is generated. The TRCCNT register continues increment operation from 0000h.
Figure 15.3 shows an Example of Period Counter Operation.

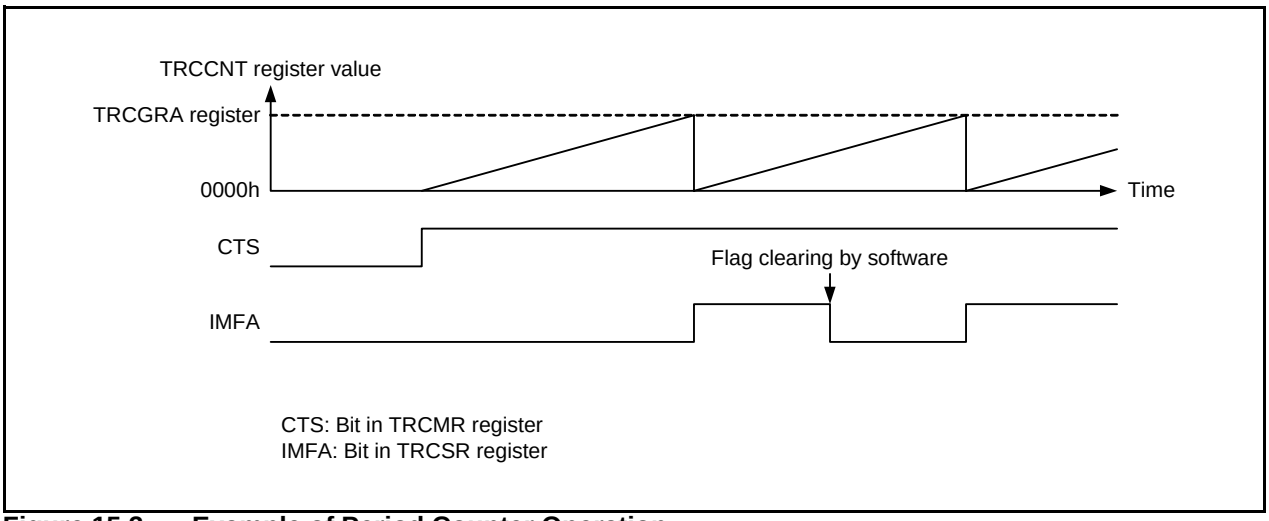


Figure 15.3 Example of Period Counter Operation

By setting the general register as an output compare register, low-level, high-level, or toggle output is performed by compare matches A to D from pins TRCIOA, TRCIOB, TRCIOC, TRCIOD.
Figure 15.4 shows an Example of Low-Level and High-Level Output Operation. The TRCCNT register is used for the free-running count operation, a low level is output at compare match B, and a high level is output at compare match A. When the set level and the pin level are the same, the pin level remains unchanged.

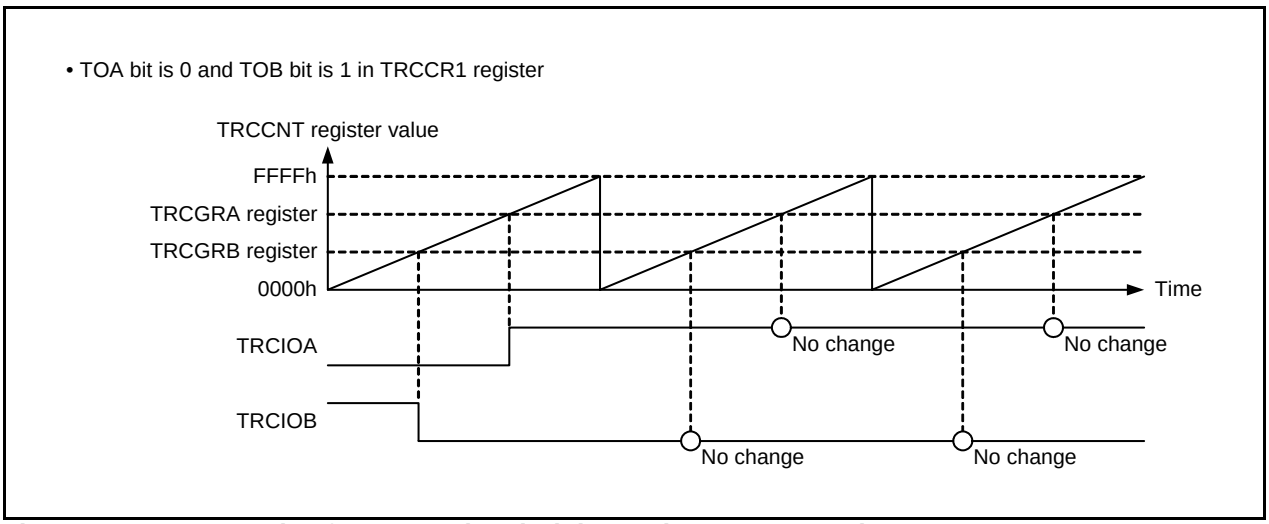


Figure 15.4 Example of Low-Level and High-Level Output Operation

Figure 15.5 shows an Example of Toggle Output Operation during Free-Running Count. The TRCCNT register is used for the free-running count operation, and toggle output is performed at compare matches A and B.

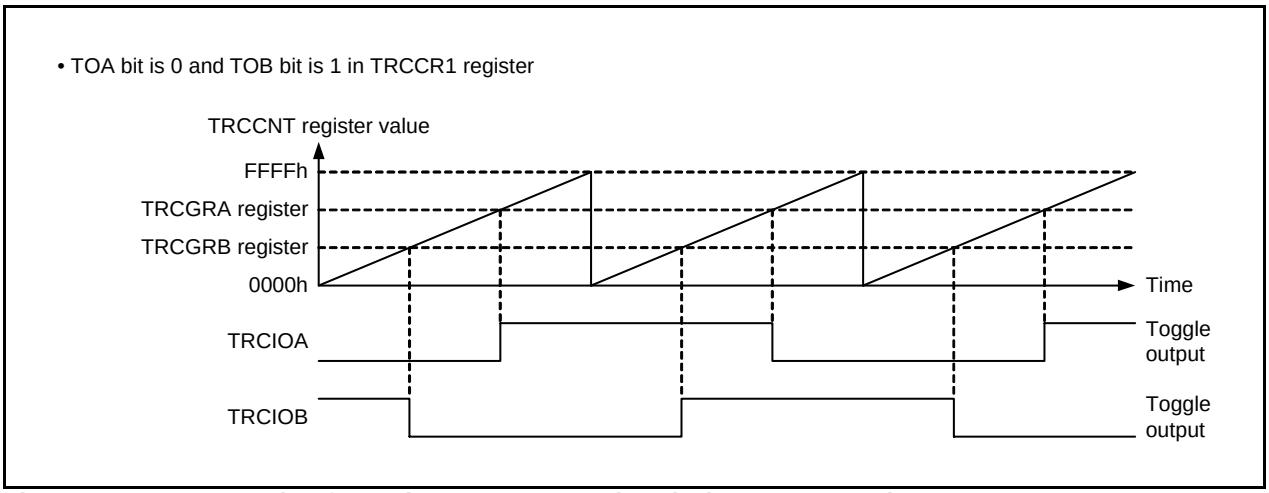


Figure 15.5 Example of Toggle Output Operation during Free-Running Count

Figure 15.6 shows an Example of Toggle Output Operation during Period Count. The TRCCNT register is used for the period count operation, and toggle output is performed at compare matches A and B.

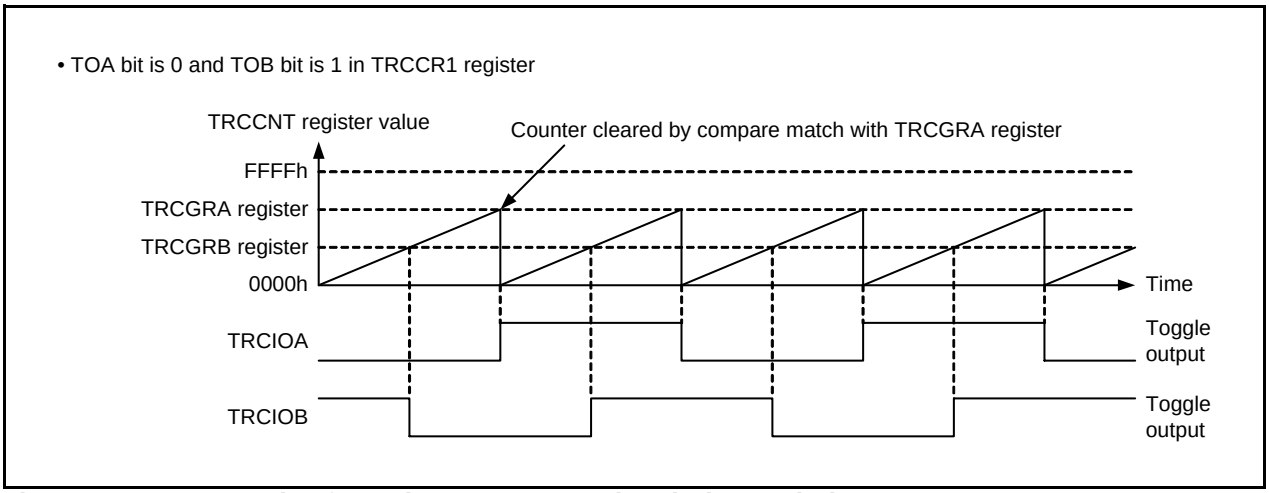


Figure 15.6 Example of Toggle Output Operation during Period Count

The input capture function can be used to measure the pulse width or period.
By setting the general register to be an input capture register, the value in the TRCCNT register on input edge detection of pins TRCIOA to TRCIOD is transferred to registers TRCGRA to TRCGRD. This value is used to measure the period. The detection edge can be selected to be a rising edge, falling edge, or two-way edge.
Figure 15.7 shows an Example of Input Capture Operation. The TRCCNT register is used for the free-running operation, and a two-way edge is selected for the input capture input to the TRCIOA pin and a falling edge is selected for the input capture input to the TRCIOB pin.

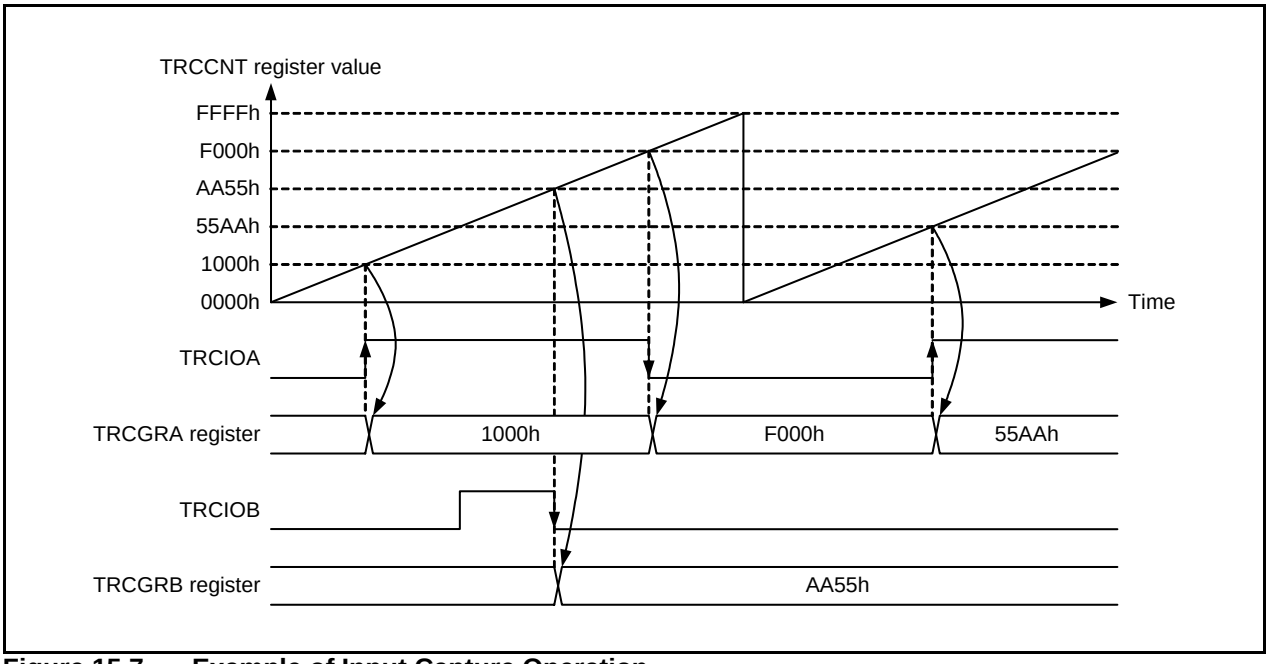


Figure 15.7 Example of Input Capture Operation

Figure 15.8 shows an Example of Buffer Operation during Input Capture. This example applies when the TRCGRA register is set as an input capture register and the TRCGRC register is set as a buffer register for the TRCGRA register. In this example, the TRCCNT register is used for the free-running count operation and both rising and falling edges are selected for the input capture input to the TRCIOA pin. Since buffer operation is set, the value in the TRCCNT register is stored in the TRCGRA register by input capture A and the value that has been stored in the TRCGRA register is transferred to the TRCGRC register at the same time.

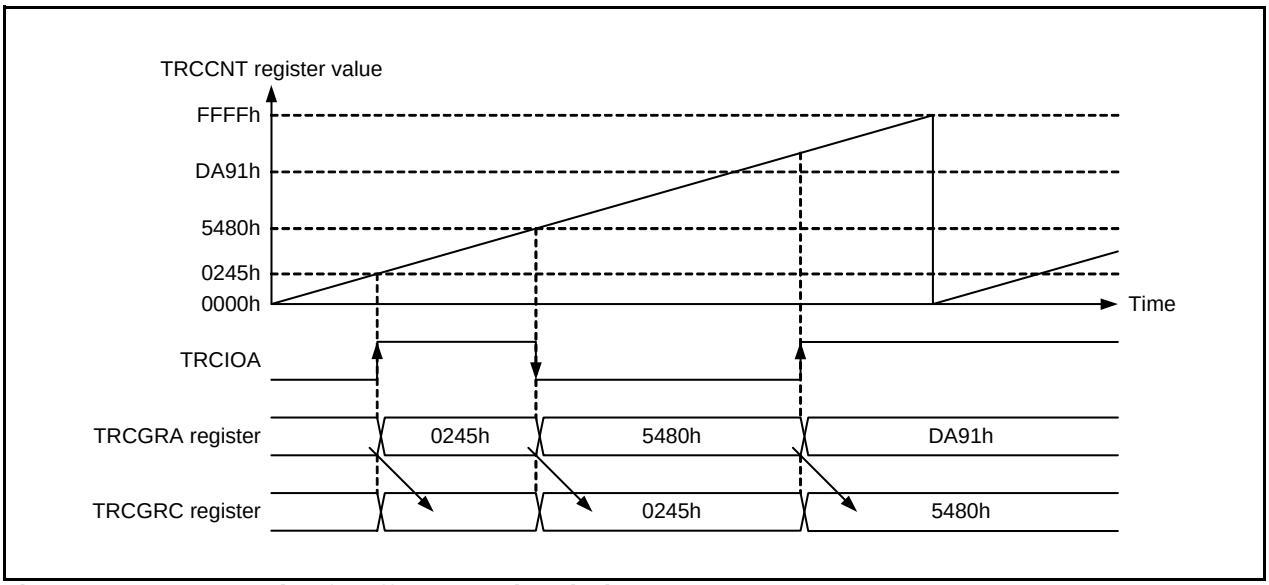


Figure 15.8 Example of Buffer Operation during Input Capture

15.3.2 PWM Mode

In PWM mode, when the TRCGRA register is set as the period register and registers TRCGRB, TRCGRC, and TRCGRD are set as duty registers, a PWM waveform is output from pins TRCIOB, TRCIOC, and TRCIOD individually. A PWM waveform with up to three phases can be output. In this mode, the general register automatically functions as an output compare register. The settings of bits IOB2, IOC2, and IOD2 are invalid. The initial output level of the corresponding pin is set according to the values in bits TOA to TOD in the TRCCR1 register and bits POLB to POLD in the TRCCR2 register.
Table 15.15 lists the Initial Output Levels of TRCIOB Pin.

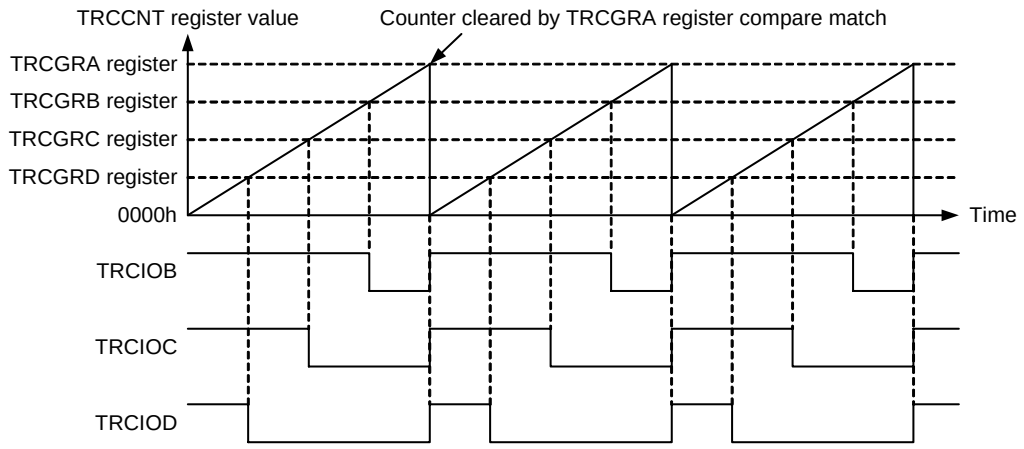
Table 15.15 Initial Output Levels of TRCIOB Pin

TOB Bit in TRCCR1 Register	POLB Bit in TRCCR2 Register	Initial Output Level
0	0	1
	1	0
1	0	0
	1	1

The output level is determined by bits POLB to POLD in the TRCCR2 register. When the POLB bit is 0 (output level is active low), the TRCIOB output pin is set to low at compare match B and high at compare match A. When the POLB bit is 1 (output level is active high), the TRCIOB output pin is set to high at compare match B and low at compare match A.
The setting values of bits PWMD to PWMB in TRCMR take precedence over those in registers TRCIOR0 and TRCIOR1. When the values set in the period and duty registers are the same, the output value remains unchanged even if a compare match occurs.

Figure 15.9 shows an Operation Example in PWM Mode.

• High-level output when TRCCNT register is cleared at compare match A. Low-level output at compare matches B, C, and D. (POLB bit = 0, POLC bit = 0, and POLD bit = 0 in TRCCR2 register)



• Low-level output when TRCCNT register is cleared at compare match A. High-level output at compare matches B, C, and D. (POLB bit = 1, POLC bit = 1, and POLD bit = 1 in TRCCR2 register)

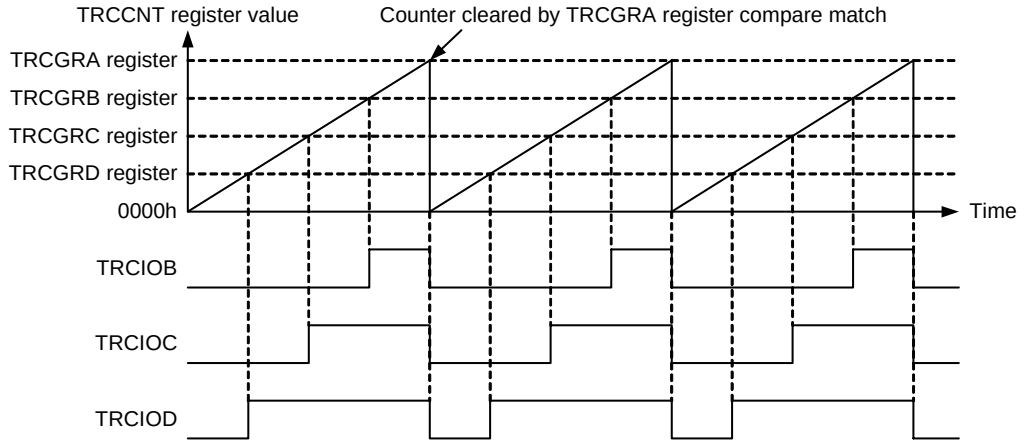


Figure 15.9 Operation Example in PWM Mode

Figure 15.10 shows an Example of Buffer Operation in PWM Mode. In this example, the TRCIOB pin is set to PWM mode and the TRCGRD register is set as the buffer register for the TRCGRB register. The TRCCNT register is cleared by compare match A, and output is set to low at compare match A and high at compare match B.
Since buffer operation is set, the output is changed when compare match B occurs, and the value in the buffer register TRCGRD is transferred to the TRCGRB register at the same time. This operation is repeated each time compare match B occurs.

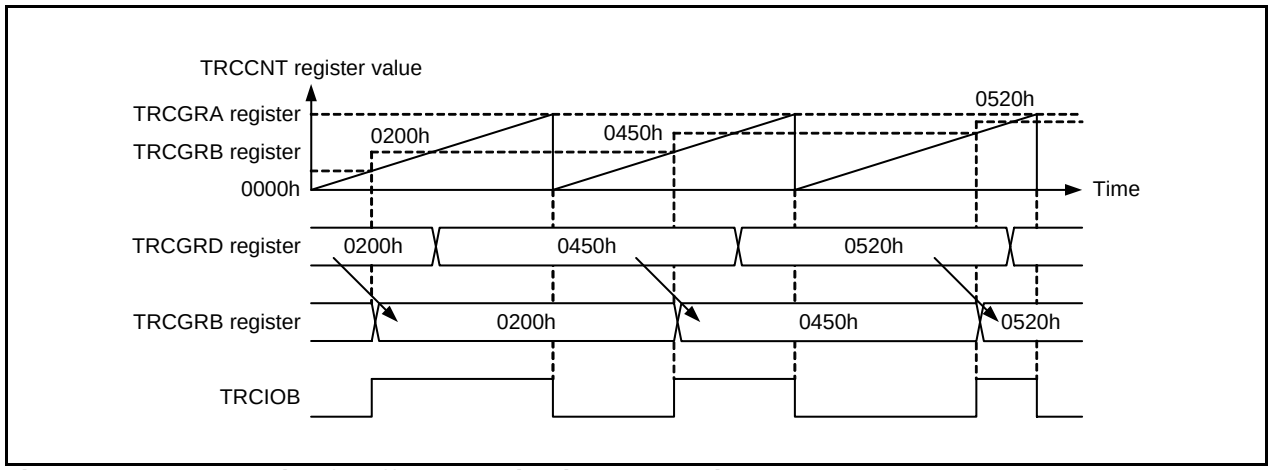
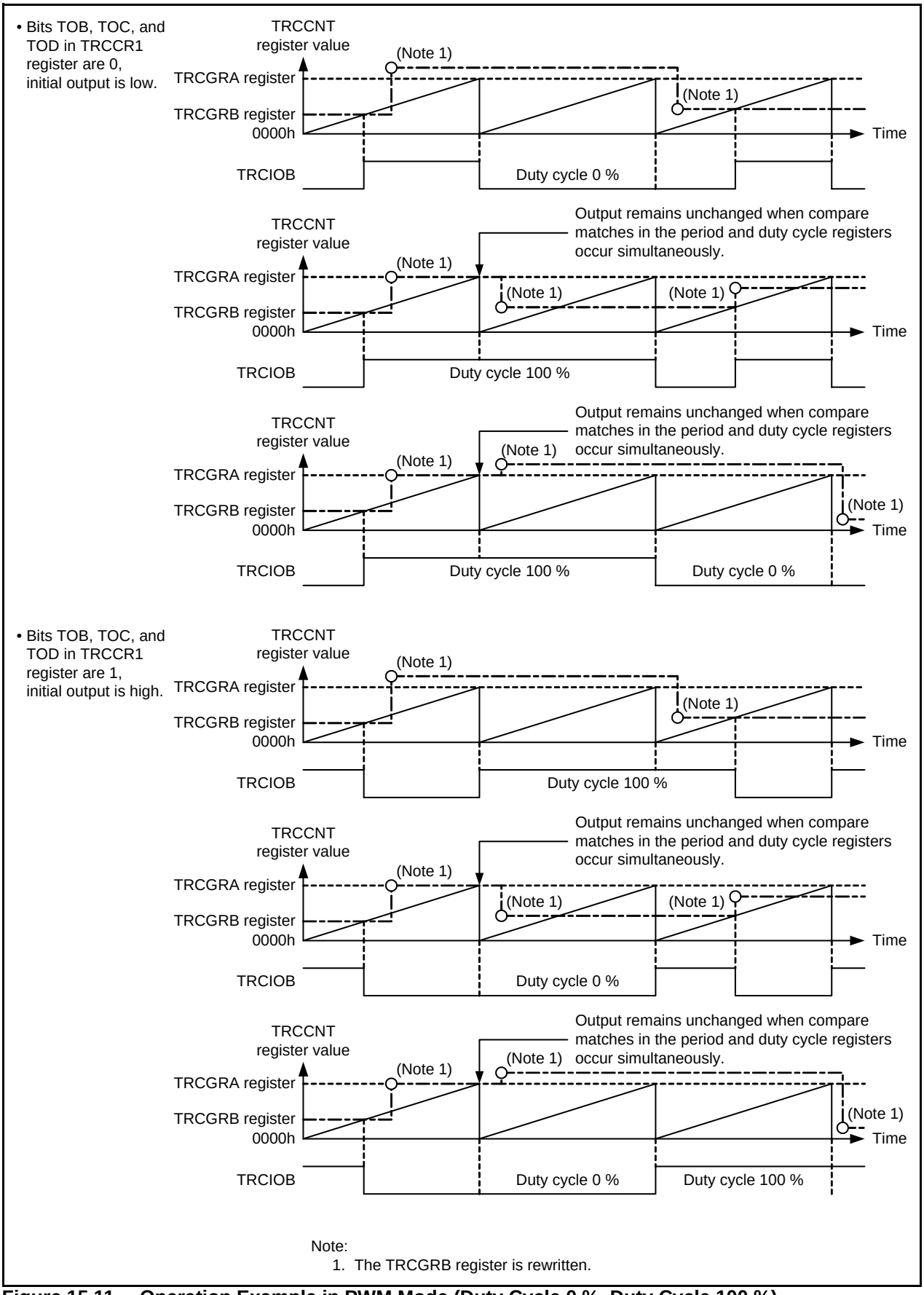


Figure 15.10 Example of Buffer Operation in PWM Mode

Figure 15.11 shows an Operation Example in PWM Mode (Duty Cycle 0 %, Duty Cycle 100 %).



Note:
1. The TRCGRB register is rewritten.

Figure 15.11 Operation Example in PWM Mode (Duty Cycle 0 %, Duty Cycle 100 %)

15.3.3 PWM2 Mode

Unlike PWM mode in PWM2 mode, a waveform is output from the TRCIOB pin at a compare match with registers TRCGRB and TRCGRC. When the BUFEB bit in the TRCMR register is set to 1 (TRCGRD register is used as a buffer register for TRCGRB register), the TRCGRD register functions as a buffer register for the TRCGRB register. The output level is determined by the TOB bit in the TRCCR1 register.

When the TOB bit is 0 (output value 0), a low level is output at a compare match with the TRCGRB register and a high level is output at a compare match with the TRCGRC register. When the TOB bit is 1 (output value 1), a high level is output at a compare match with the TRCGRB register and a low level is output at a compare match with the TRCGRC register.

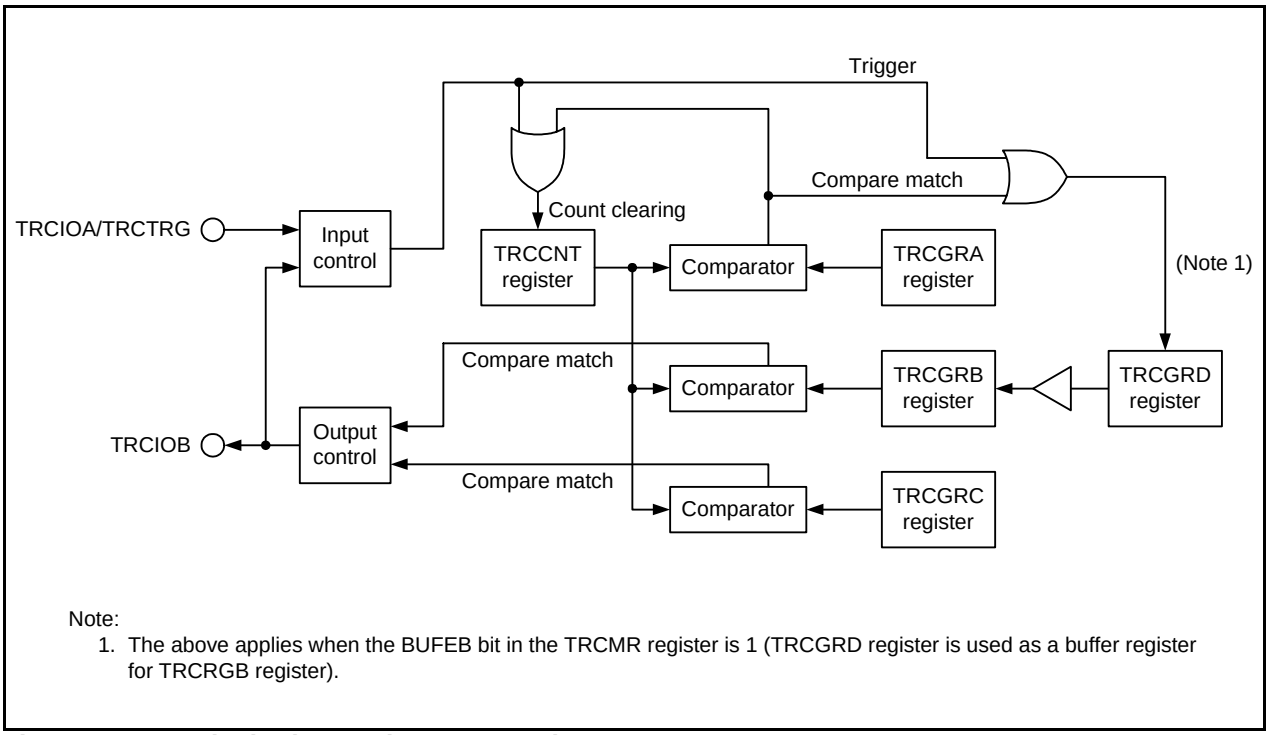
Table 15.16 lists the Combinations of Pin Functions and General Registers for PWM2 Mode and General Registers for PWM2 Mode. Figure 15.12 shows the Block Diagram in PWM2 Mode. Figure 15.13 shows the Timing of Buffer Operations for Registers TRCGRD and TRCGRB in PWM2 Mode.

The value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a compare match with the TRCGRA register. However, the counter is cleared only when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A). Also, when trigger input is enabled by bits TCEG0 to TCEG1 in the TRCCR2 register in PWM2 mode, the value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a trigger. The timer I/O pins that are not used in PWM2 mode can be used as I/O ports.

Table 15.16 Combinations of Pin Functions and General Registers for PWM2 Mode

Pin Name	I/O	Compare Match Register	Buffer Register
TRCIOA	I/O	Port function (1)/TRCTRG input	
TRCIOB	O	TRCGRB register	TRCGRD register
		TRCGRC register	—
TRCIOC	I/O	Port function (1)	
TRCIOD			

Note:
1. To use the port function, set the corresponding bit in registers PMLi and PMHi (i = 1, 3, or 4) to 0.



Note:
1. The above applies when the BUFEB bit in the TRCMR register is 1 (TRCGRD register is used as a buffer register for TRCRGB register).

Figure 15.12 Block Diagram in PWM2 Mode

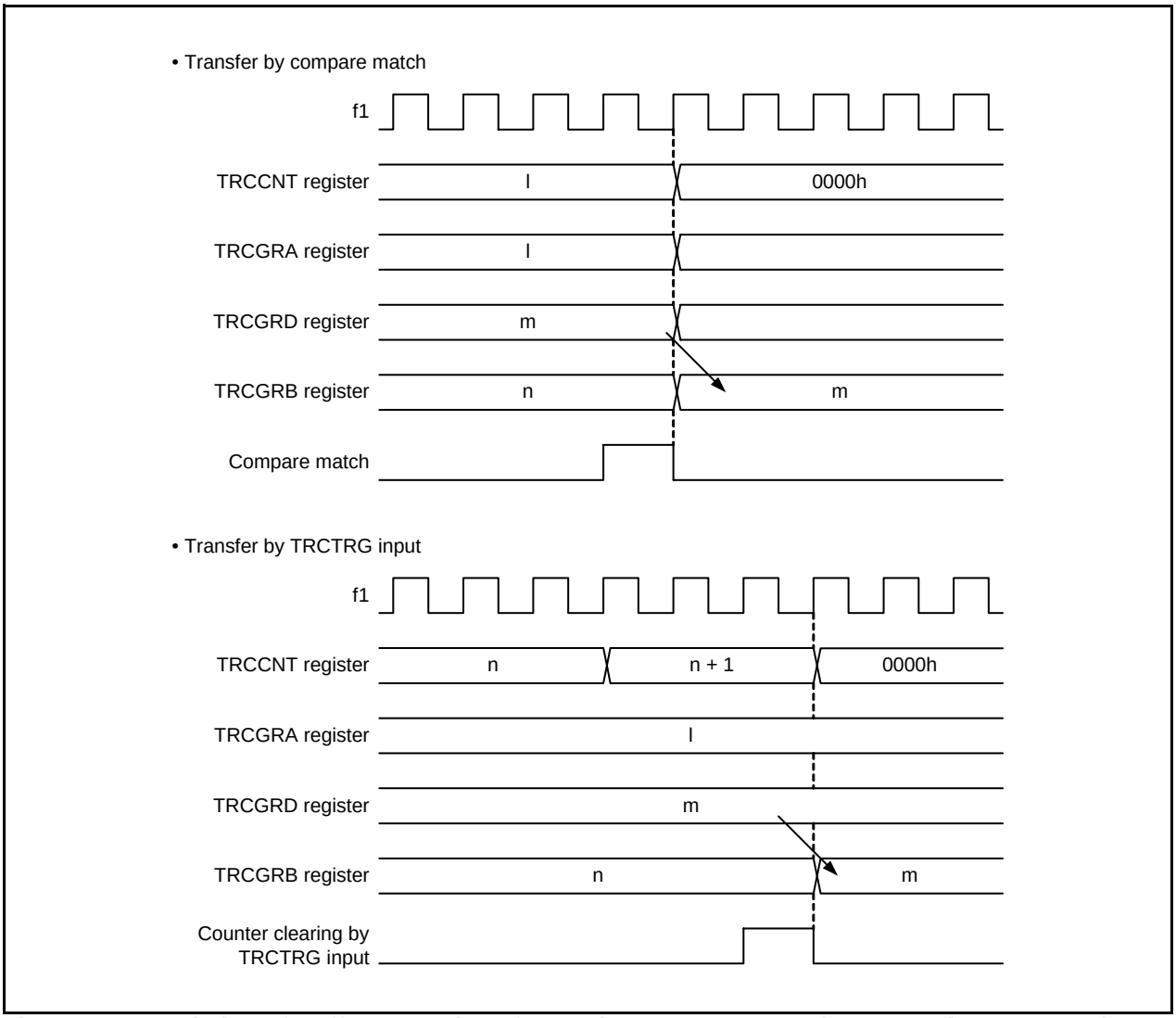


Figure 15.13 Timing of Buffer Operations for Registers TRCGRD and TRCGRB in PWM2 Mode

In PWM2 mode, the TRCTRG input is used to output a pulse with an arbitrary delay time and width from the TRCIOB pin.
Set bits TCEG1 to TCEG0 in the TRCCR2 register to 10b (falling edge) to set the falling edge for the TRCTRG input. Set the CSTP bit in the TRCCR2 register to 0 (increment is continued) to continue incrementing when compare match A with the TRCGRA register occurs. Set the BUFEB bit in the TRCMR register to 1 (TRCGRD register is used as a buffer register for TRCGRB register) to set the TRCGRD register as the buffer register. Set the TOB bit in the TRCCR1 register to 0 (output value 0) or 1 (output value 1) to set the initial level of the output level to 0 or 1. Next, set the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by compare match A.
Figure 15.14 shows an Operation Example in PWM2 Mode When TRCTRG Input is Enabled. Figure 15.15 shows an Operation Example in PWM2 Mode When TRCTRG Input is Disabled. These examples apply when the PWM2 bit in the TRCMR register is set to 0 (PWM2 mode) and a waveform is output from the TRCIOB pin.
In PWM2 mode, when the TOB bit in the TRCCR1 register is 0 (output value 0), the TRCTRG input edge is disabled while a high level is output from the TRCIOB pin. Likewise, when the TOB bit is 1 (output value 1), the TRCTRG input edge is disabled while a low level is output from the TRCIOB pin. In addition, transfer from registers TRCGRD to TRCGRB is performed when a compare match with the TRCGRA register or TRCTRG input occurs. However, if the TRCTRG input is disabled depending on the level of the TRCIOB pin, transfer from registers TRCGRD to TRCGRB is not performed.

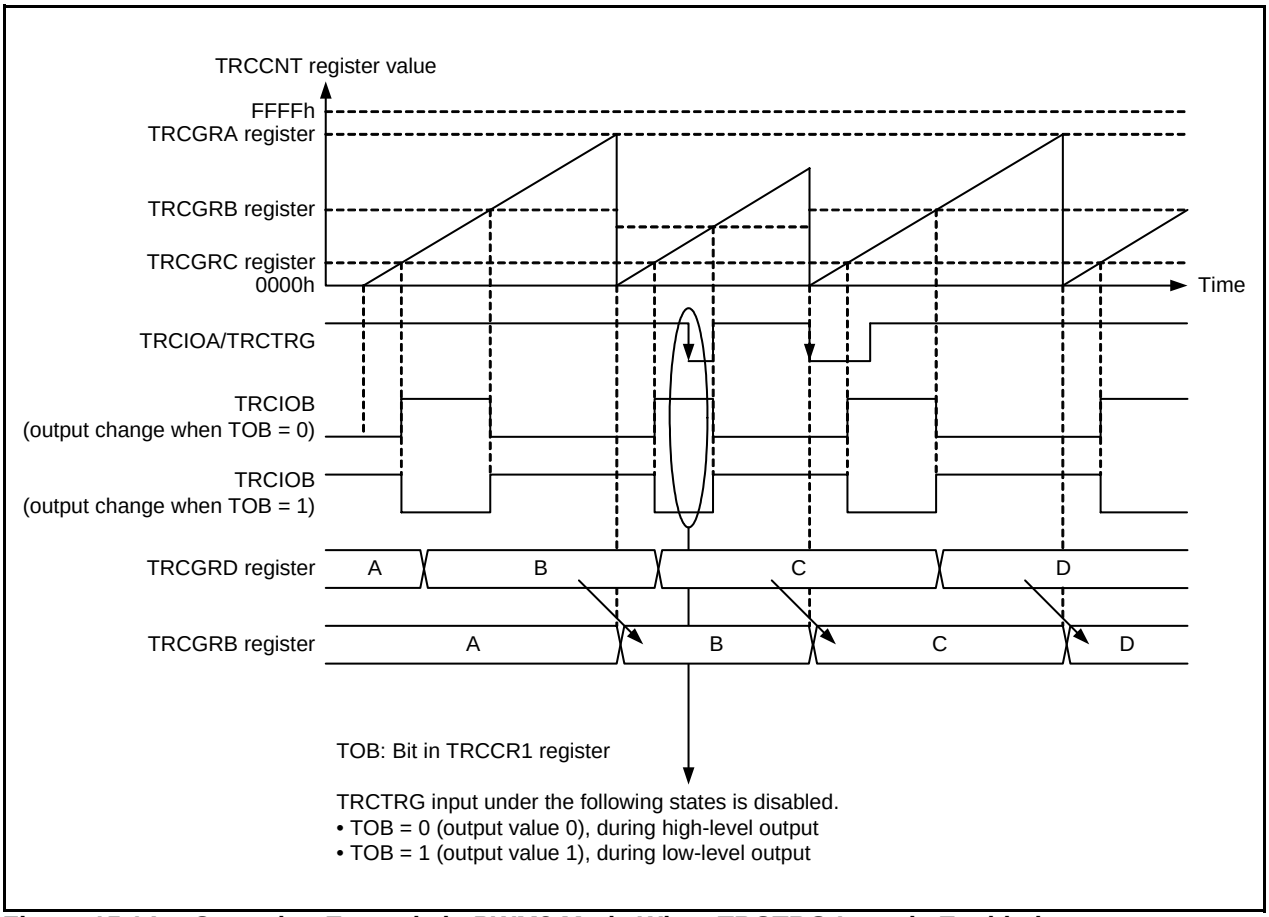


Figure 15.14 Operation Example in PWM2 Mode When TRCTRG Input is Enabled

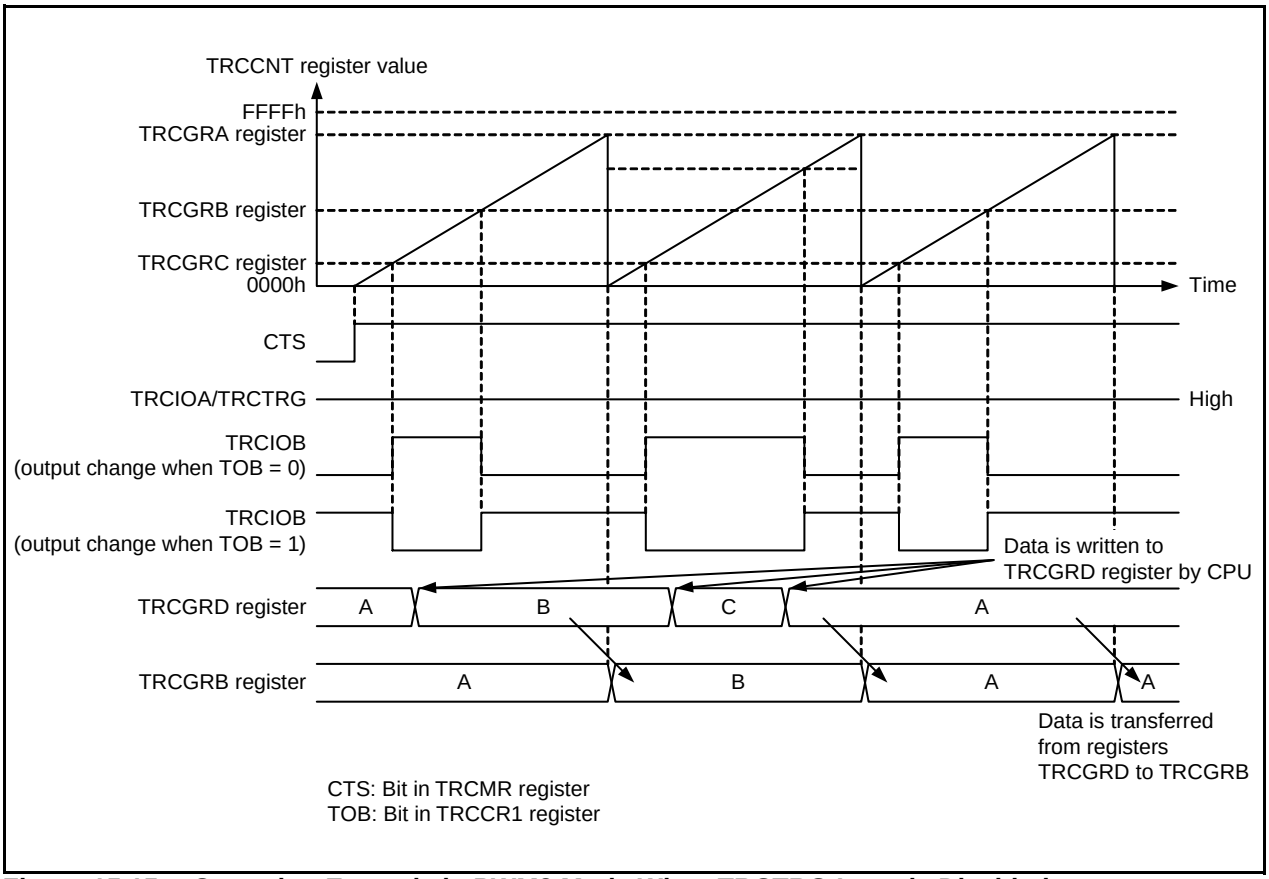


Figure 15.15 Operation Example in PWM2 Mode When TRCTRG Input is Disabled

Figure 15.16 shows an Example of Count Stop Operation in PWM2 Mode. In this example, the TOB bit in the TRCCR1 register is set to 0 (output value 0) and the TOB bit is set to 1 (output value 1).
By setting the CSTP bit in the TRCCR2 register to 1 (increment is stopped) and the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A), the counter is changed to 0000h and stopped by the compare match between registers TRCCNT and TRCGRA. By setting the CTS bit in the TRCMR register to 0 (count is stopped), the counter is forcibly stopped and the output is set to the initial level.

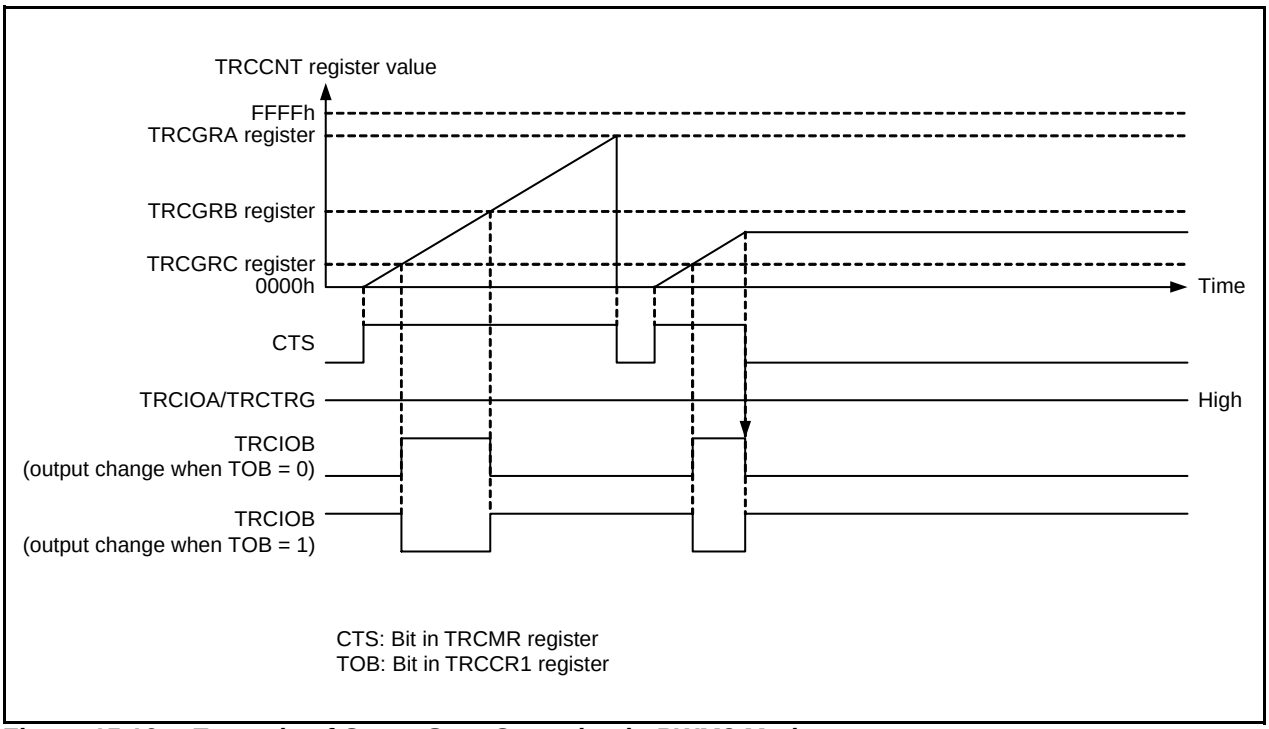


Figure 15.16 Example of Count Stop Operation in PWM2 Mode

Figure 15.17 shows an Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode.
The count is started when the CTS bit in the TRCMR register is set to 1 (count is started) under the following conditions. Then, the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output.

- Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG input disabled) to disable the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (increment is stopped) to stop the increment when compare match A with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by compare match A.
- The TOB bit in the TRCCR1 register is set to 0 (output value 0) to set the initial value of the output level to 0.

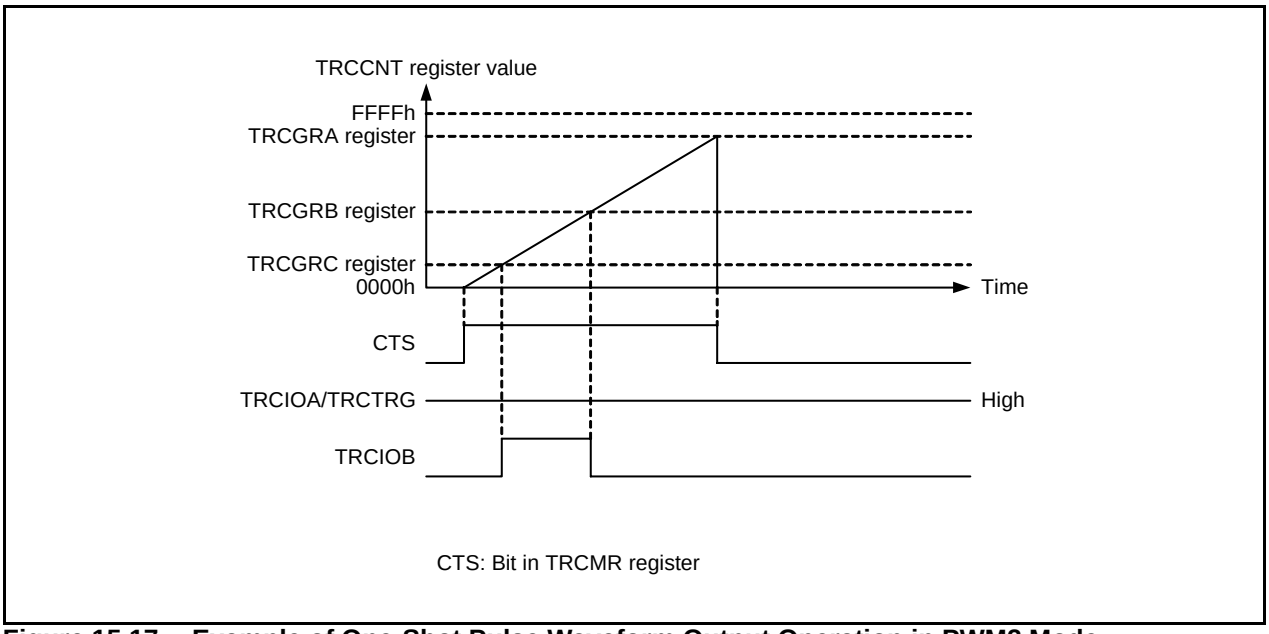


Figure 15.17 Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode

Figure 15.18 shows an Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input).
After the CTS bit in the TRCMR register is set to 1 (count is started), the increment is started on the rising edge of TRCIOA/TRCTRG, and the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output under the following conditions.

- Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 10b (falling edge) to set the falling edge of the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (increment is stopped) to stop the increment when a compare match with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by a compare match.
- The TOB bit in the TRCCR1 register is set to 0 (output value 0) to set the initial value of the output level to 0.

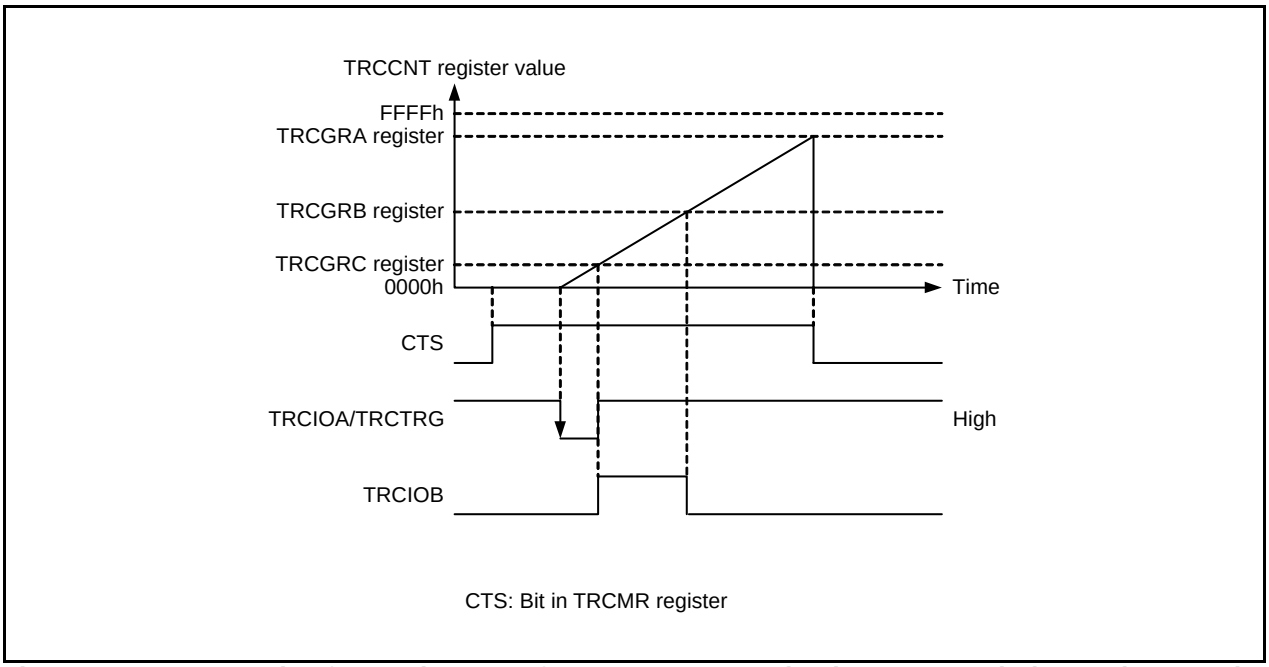


Figure 15.18 Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input)

15.4 Selectable Functions

15.4.1 Input Digital Filter for Input Capture

Figure 15.19 shows the Digital Filter Circuit Block Diagram. The TRCIOA to TRCIOD and TRCTRG input can be latched internally through the digital filter circuit. This circuit consists of three cascaded latch circuits and a match detection circuit. When the TRCIOA to TRCIOD and TRCTRG input are sampled on the clock selected by bits DFCK0 to DFCK1 in the TRCDF register and three outputs from the latch circuits match, the level is passed forward to the next circuit. If they do not match, the previous level is retained. That is, the pulse input with a width of three sampling clocks or more is recognized as a signal. If not, the change in the signal is recognized as noise and cancelled.

Do not use the digital filter immediately after a reset. Wait for four cycles of the sampling clock and make the setting for input capture before using the input capture function.

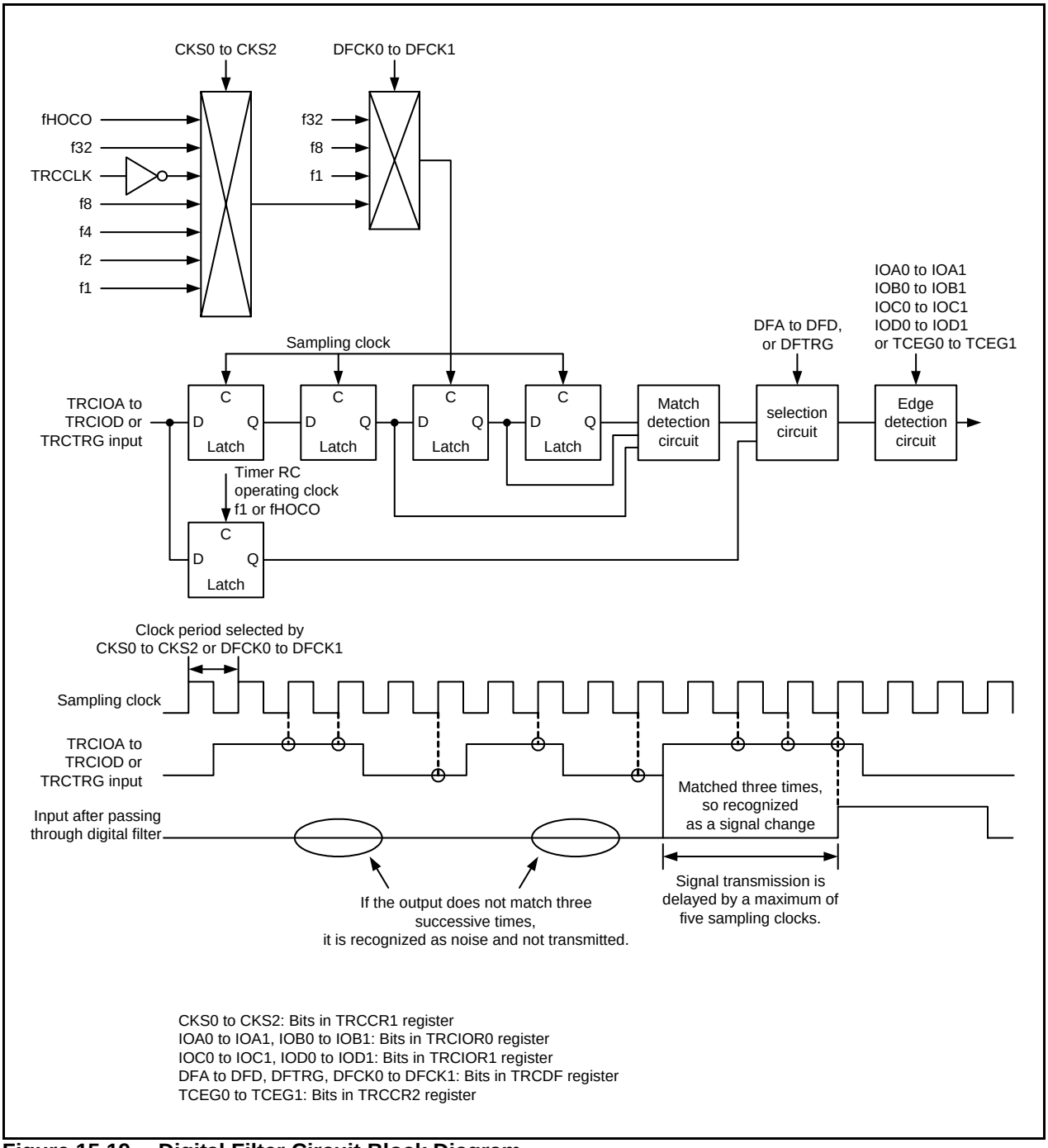


Figure 15.19 Digital Filter Circuit Block Diagram

15.4.2 A/D Conversion Start Trigger

By setting the TRCADCR register, an A/D conversion start trigger can be generated at compare matches A to D.
Figure 15.20 shows a Setting Example of A/D Conversion Start Trigger by Compare Matches B and C.

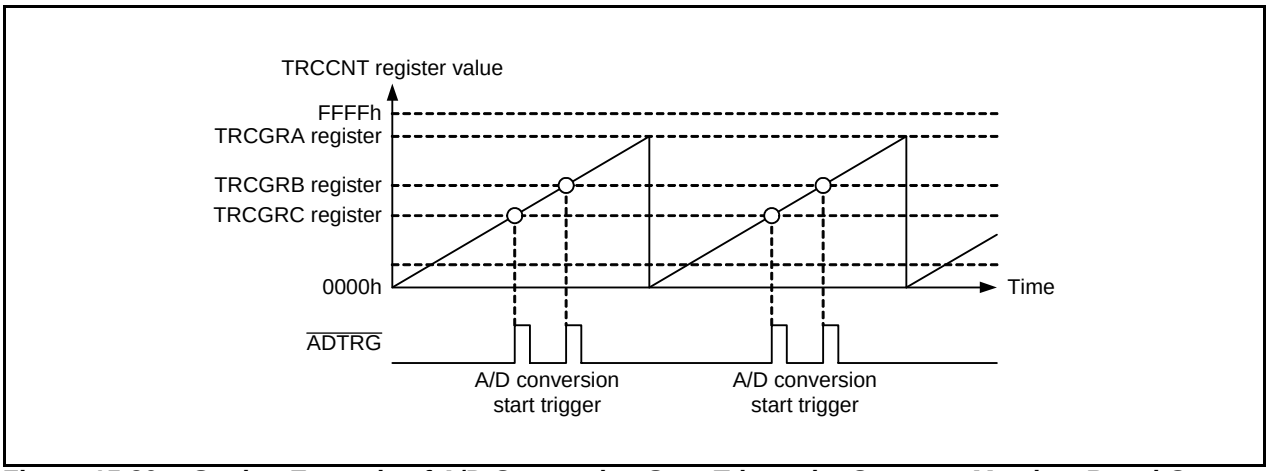


Figure 15.20 Setting Example of A/D Conversion Start Trigger by Compare Matches B and C

An A/D conversion start trigger is not generated from the buffer register during buffer operation. The TRCGRC register cannot operate as a buffer register for the TRCGRA register in PWM2 mode.
Table 15.17 lists the States Where A/D Conversion Start Trigger Sources are Generated.

Table 15.17 States Where A/D Conversion Start Trigger Sources are Generated

Operating Mode	Buffer Operation	A/D Conversion Start Trigger Source			
		TRCGRA	TRCGRB	TRCGRC	TRCGRD
Input capture	Used	No	No	No	No
	Not used	No	No	No	No
Compare match	Used	Yes	Yes	No	No
	Not used	Yes	Yes	Yes	Yes
PWM mode	Used	Yes	Yes	No	No
	Not used	Yes	Yes	Yes	Yes
PWM2 mode	Used	Yes	Yes	Yes	No
	Not used	Yes	Yes	Yes	Yes

Yes: An A/D conversion start trigger is generated.
No: No A/D conversion start trigger is generated.

15.4.3 Changing Output Pins and General Registers

The settings for bits IOC3 and IOD3 in the TRCIOR1 register can redirect the compare match output with registers TRCGRC and TRCGRD from pins TRCIOC and TRCIOD to pins TRCIOA and TRCIOB, respectively. The TRCIOA pin can output a combination of compare matches A and C and the TRCIOB pin can output a combination of compare matches B and D.
Figure 15.21 shows the Block Diagram for Changing Output Pins and General Registers.

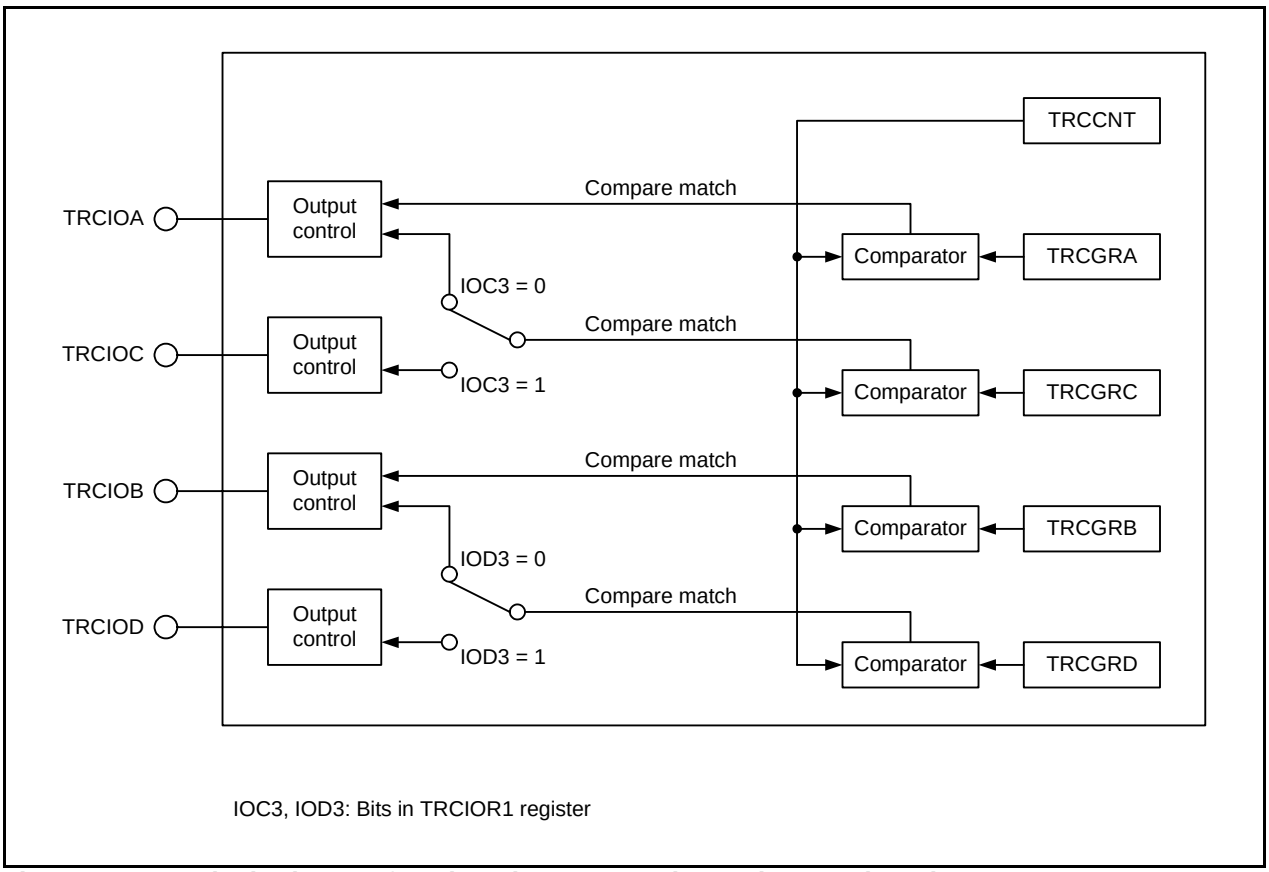


Figure 15.21 Block Diagram for Changing Output Pins and General Registers

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and the IOD3 bit to 0 (TRCIOB output register).
- Set bits BUFEA and BUFEB in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRA and TRCGRC. Also, set different values in registers TRCGRB and TRCGRD.

Figure 15.22 shows an Operation Example When TRCIOA and TRCIOB Output is not Overlapped. The following items must be set:

- Set the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the counter by a compare match and set the TRCCNT register for period count operation.
- Set bits IOA2 to IOA0 in the TRCIOR0 register to 011b (toggle output from TRCIOA pin at compare match A) for toggle output.
- Set bits IOB2 to IOB0 in the TRCIOR0 register to 011b (toggle output from TRCIOB pin at compare match B) for toggle output.
- Set bits IOC3 to IOC0 in the TRCIOR1 register to 0011b (toggle output from TRCIOA pin at compare match C) for toggle output.
- Set bits IOD3 to IOD0 in the TRCIOR1 register to 0011b (toggle output from TRCIOB pin at compare match D) for toggle output.

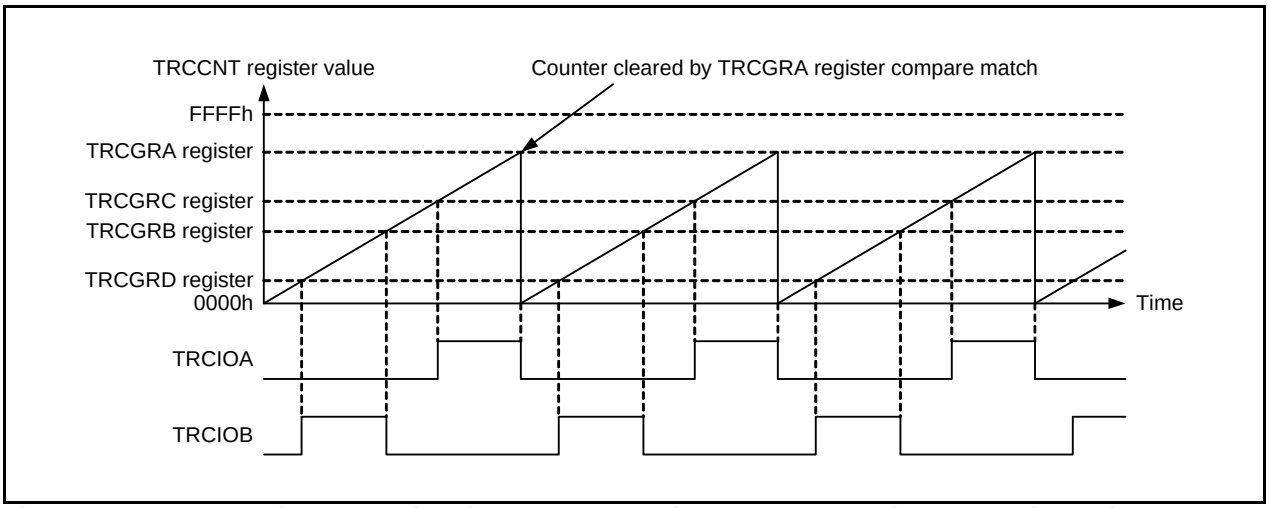


Figure 15.22 Operation Example When TRCIOA and TRCIOB Output is not Overlapped

15.4.4 Waveform Output Manipulation Function

By setting the TRCOPR register, the waveform output for timer RC can be controlled by the $\overline{INT1}$ pin input or comparator B1 output.

When the OPE bit in the TRCOPR register is 0, the waveform output manipulation function is disabled. The TRCIOA, TRCIOB, TRCIOC, and TRCIOD output from timer RC is output by setting registers TRCIOR0, TRCIOR1, and TRCOER. When the PTO bit in the TRCOER register is 1 (pulse output forced cutoff signal input $\overline{INT0}$ pin enabled), if a low level is input to the $\overline{INT0}$ pin, bits EA, EB, EC, and ED in the TRCOER register are set to all 1 (timer RC output disabled) and output pins TRCIOA to TRCIOD become high impedance.

When the OPE bit in the TRCOPR register is 1, the waveform output manipulation function is enabled. If a waveform output manipulation event is input, bits EA to ED in the TRCOER register are set to 1. Bits OPOL0 to OPOL1 in the TRCOPR register enable the output level of the timer RC pin to be fixed at low, high, or to high impedance during the waveform output manipulation period. After the waveform output manipulation event is cancelled, the waveform output manipulation for the timer RC pin is stopped and the output is restarted. The timing is automatically synchronized so that less than one cycle of waveform is not output after the output is restarted.

Figures 15.23 to 15.26 show Examples of Waveform Output Manipulation Operation.

- When the timer RC pin is pulled down, the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled), bits OPOL1 to OPOL0 are 00b (when timer RC pin is pulled down, timer RC output level is fixed to high impedance during waveform output manipulation period), and the RESTATS bit is 0 (output is restarted by software).

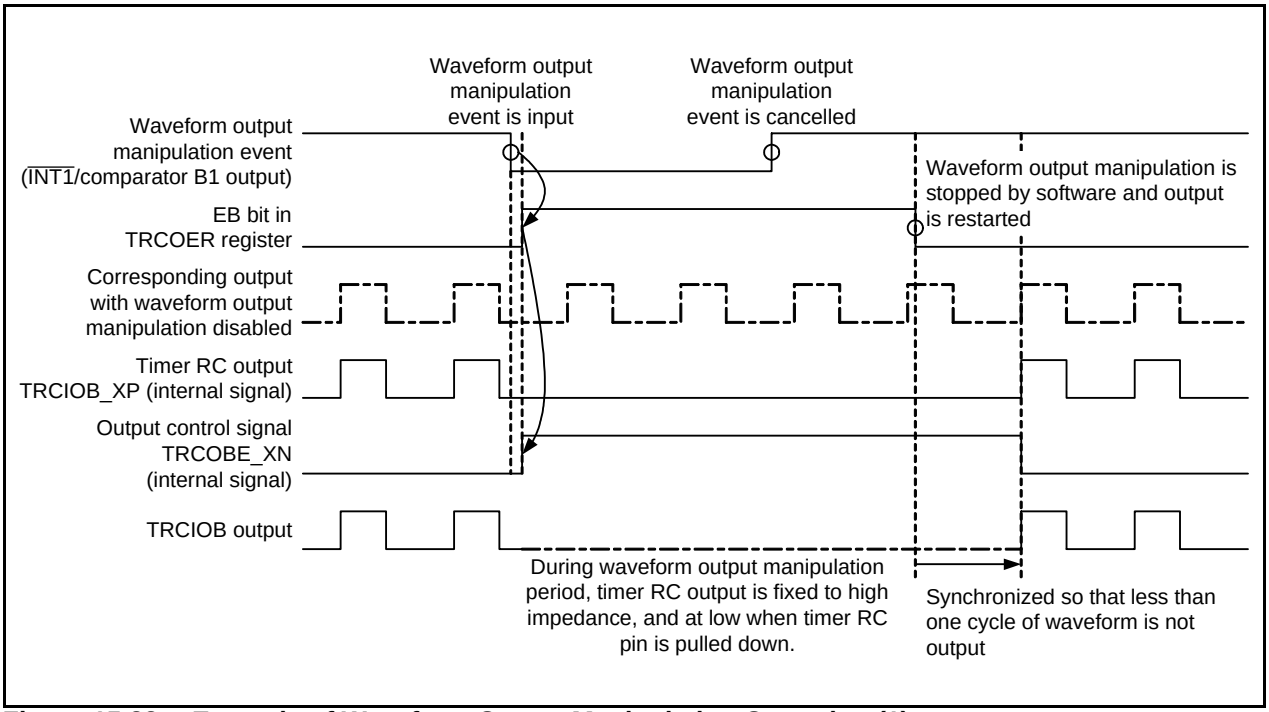


Figure 15.23 Example of Waveform Output Manipulation Operation (1)

• When the timer RC pin is pulled up, the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled), bits OPOL1 to OPOL0 are 01b (when timer RC pin is pulled up, timer RC output level is fixed to high impedance during waveform output manipulation period), and the RESTATS bit is 0 (output is restarted by software).

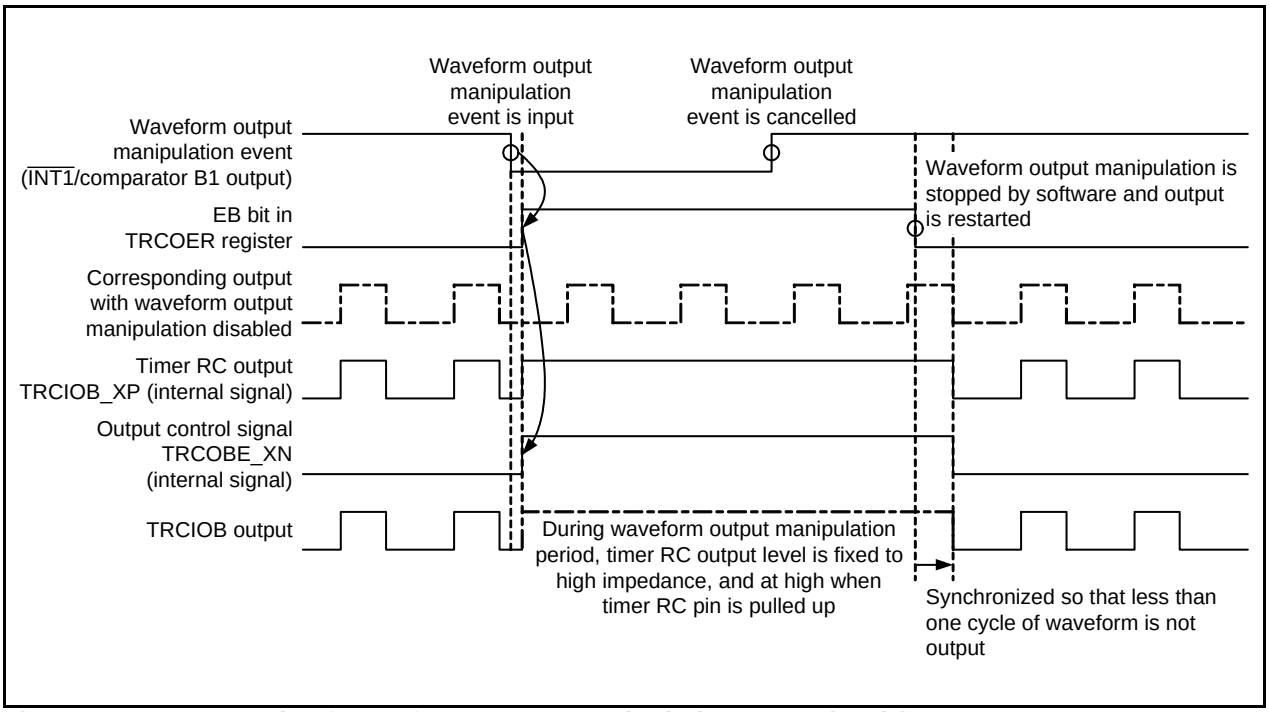


Figure 15.24 Example of Waveform Output Manipulation Operation (2)

• When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled), bits OPOL1 to OPOL0 are 10b (timer RC output level is fixed at low during waveform output manipulation period), and the RESTATS bit is 1 (output is automatically restarted).

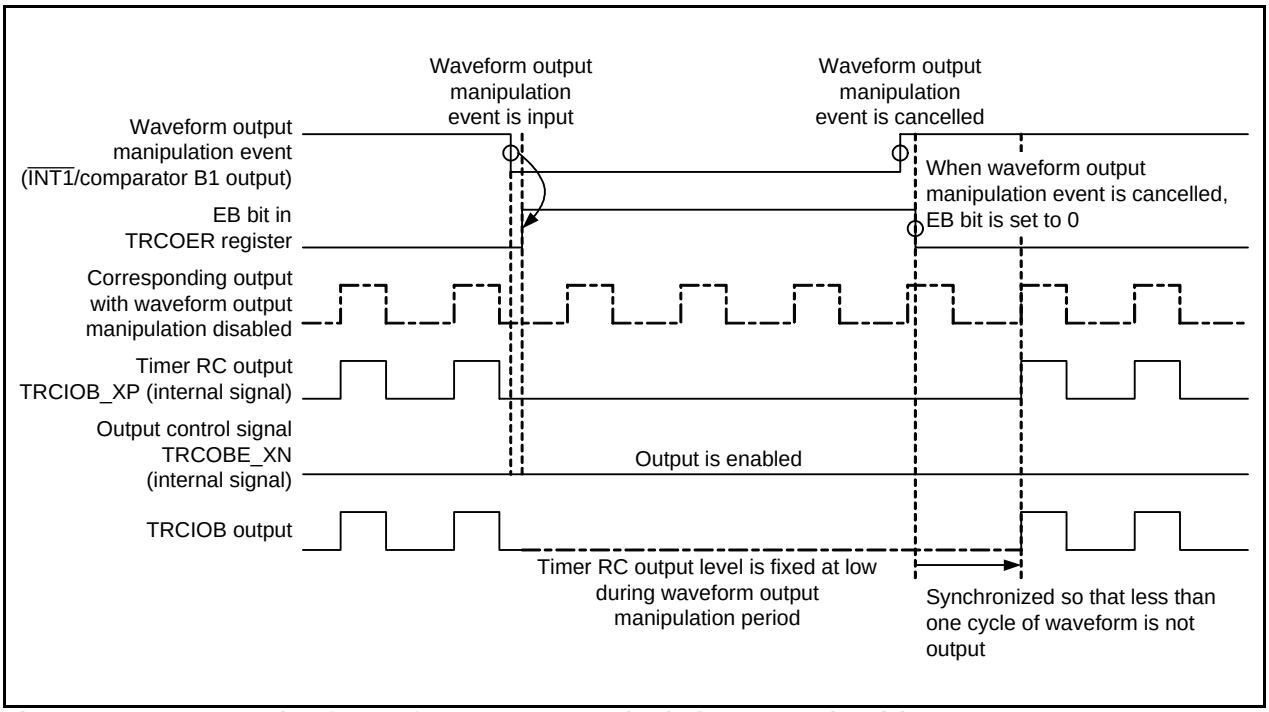


Figure 15.25 Example of Waveform Output Manipulation Operation (3)

• When the OPE bit in the TRCOPR register is 1 (waveform output manipulation control enabled), bits OPOL1 to OPOL0 are 11b (timer RC output level is fixed at high during waveform output manipulation period), and the RESTATS bit is 1 (output is automatically restarted).

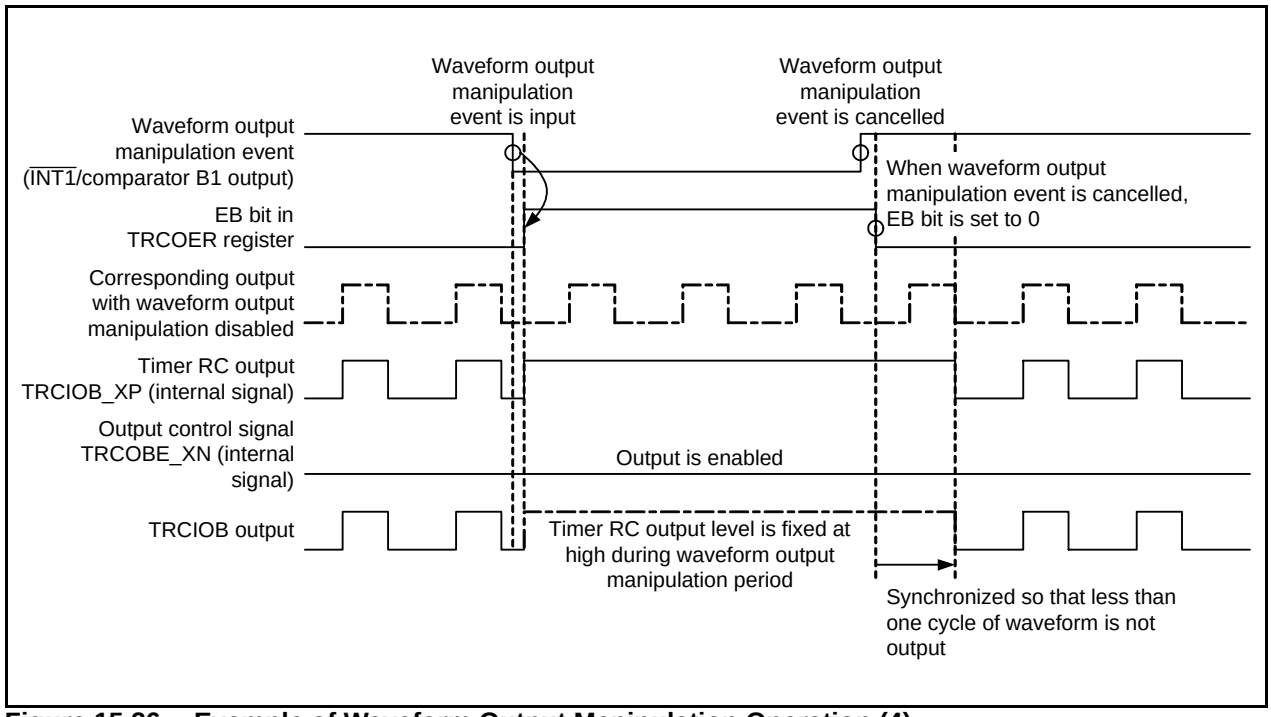


Figure 15.26 Example of Waveform Output Manipulation Operation (4)

15.5 Operation Timing

15.5.1 TRCCNT Register Count Timing

Figure 15.27 shows the Count Operation Timing.

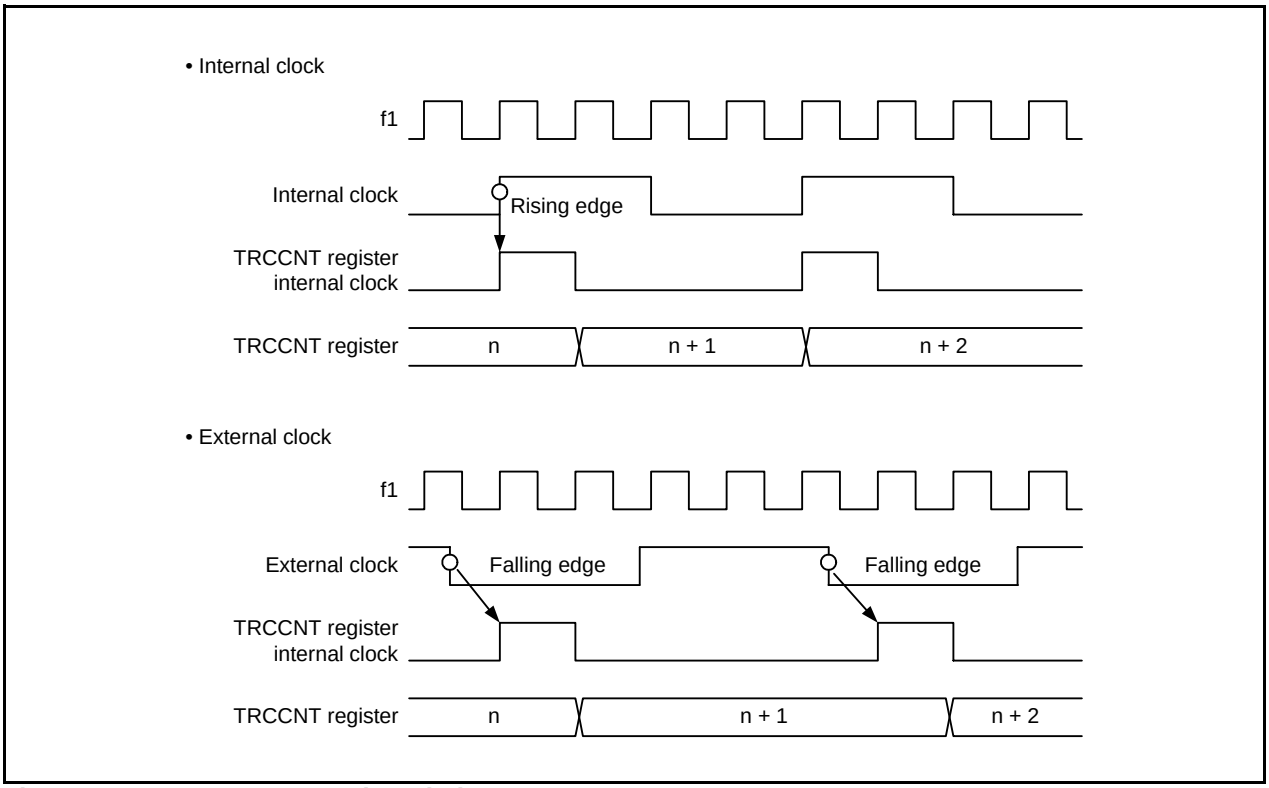


Figure 15.27 Count Operation Timing

15.5.2 Output Compare Output Timing

A compare match signal occurs at the last state (timing when the TRCCNT register updates a matched value) when the TRCCNT register and the general register match. When the compare match occurs, the output value set by the TRCIOR register is output to the output compare output pins (TRCIOA, TRCIOB, TRCIOC, and TRCIOD). After the TRCCNT register and the general register match, a compare match signal does not occur until an input clock to the TRCCNT register is generated.
Figure 15.28 shows the Output Compare Output Timing.

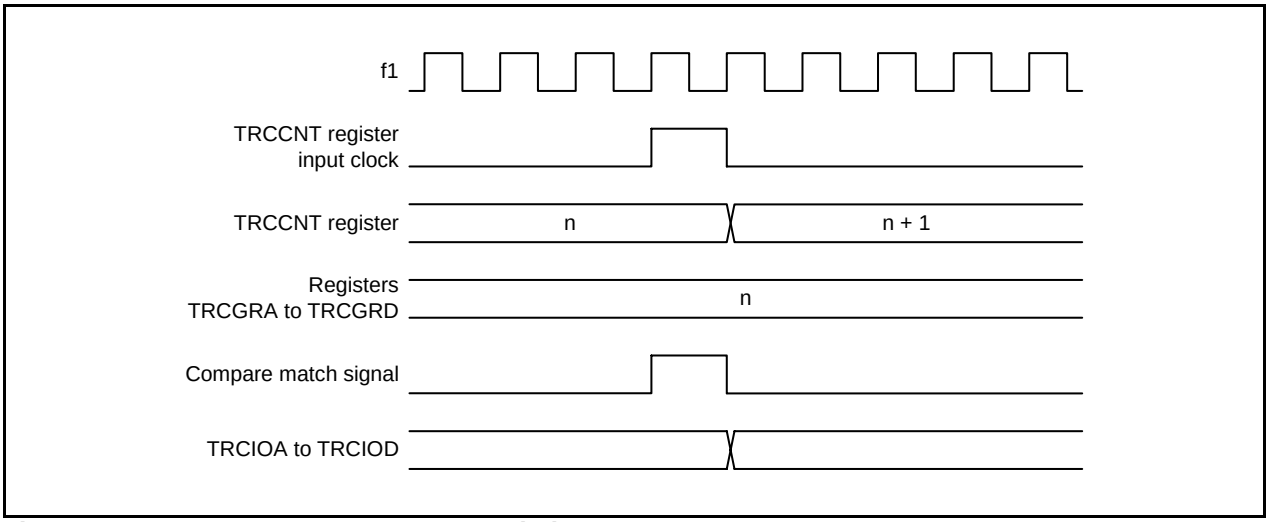


Figure 15.28 Output Compare Output Timing

15.5.3 Input Capture Input Timing

A falling edge, rising edge, or two-way edge can be selected for input capture input by setting registers TRCIOR0 and TRCIOR1.
Figure 15.29 shows the Input Capture Input Timing. This applies when a falling edge is selected.

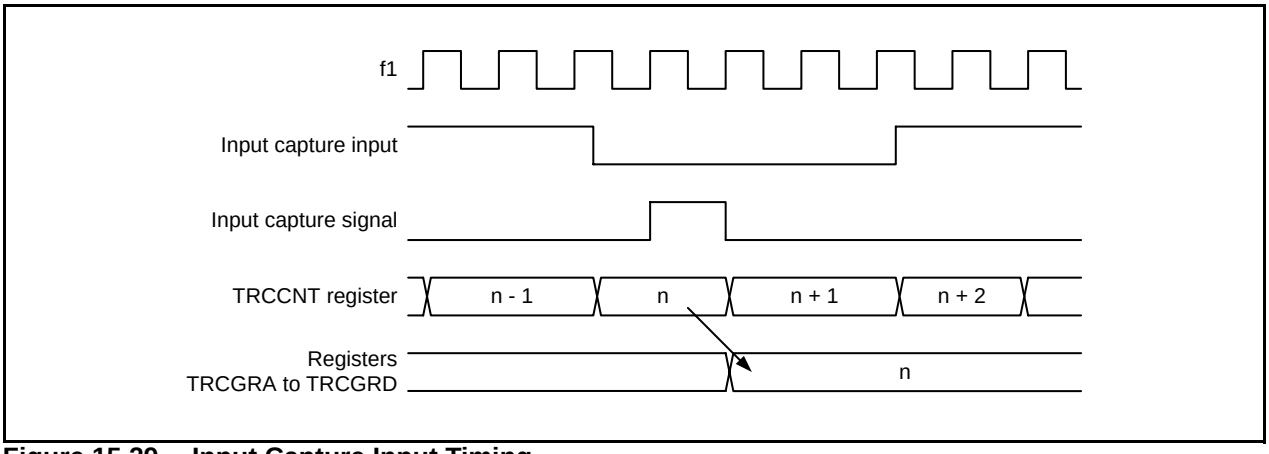


Figure 15.29 Input Capture Input Timing

15.5.4 Timing for Counter Clearing by Compare Match

Figure 15.30 shows the Timing for Counter Clearing by Compare Match. If the value in the TRCGRA register is n, the counter counts from 0 to n and the period is thus set to n + 1.

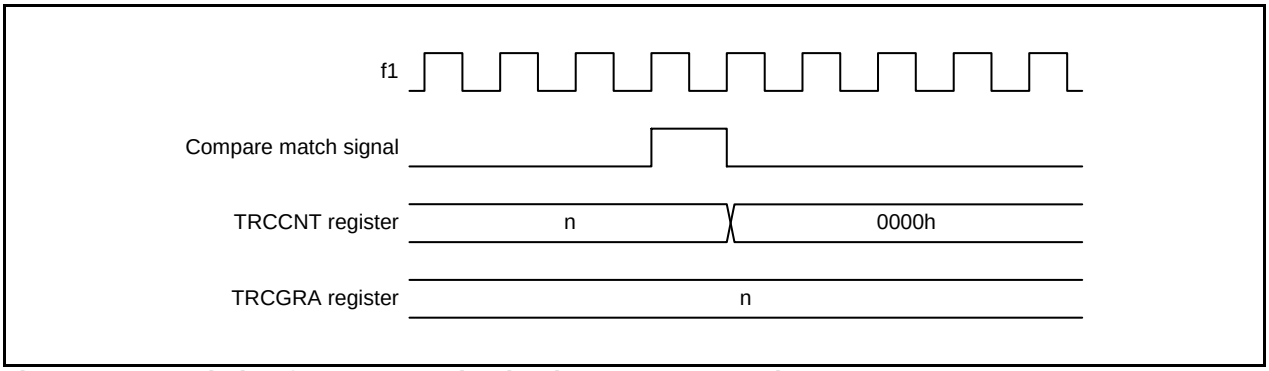


Figure 15.30 Timing for Counter Clearing by Compare Match

15.5.5 Buffer Operation Timing

Figure 15.31 shows the Buffer Operation Timing.

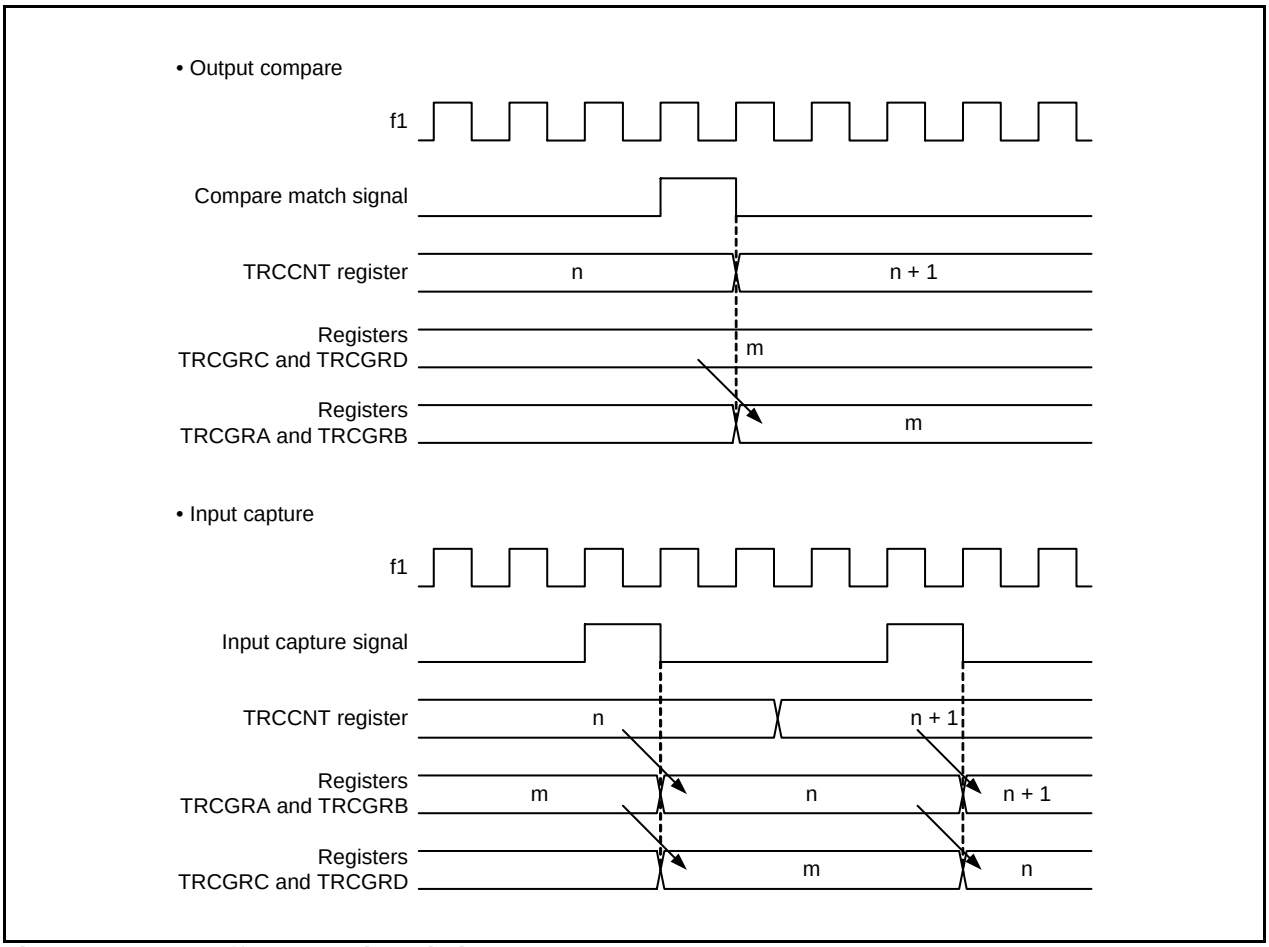


Figure 15.31 Buffer Operation Timing

15.5.6 Setting Timing at Compare Match

While the TRCSR register functions as an output compare register, bits IMFA to IMFD are set to 1 when TRCCNT register and the general registers (TRCGRA, TRCGRB, TRCGRC, TRCGRD) match.
A compare match signal occurs at the last state (timing when the TRCCNT register updates a matched value). Thus, after the TRCCNT register and the general register match, a compare match signal does not occur until an input clock to the TRCCNT register is generated.
Figure 15.32 shows the Timing at Compare Match.

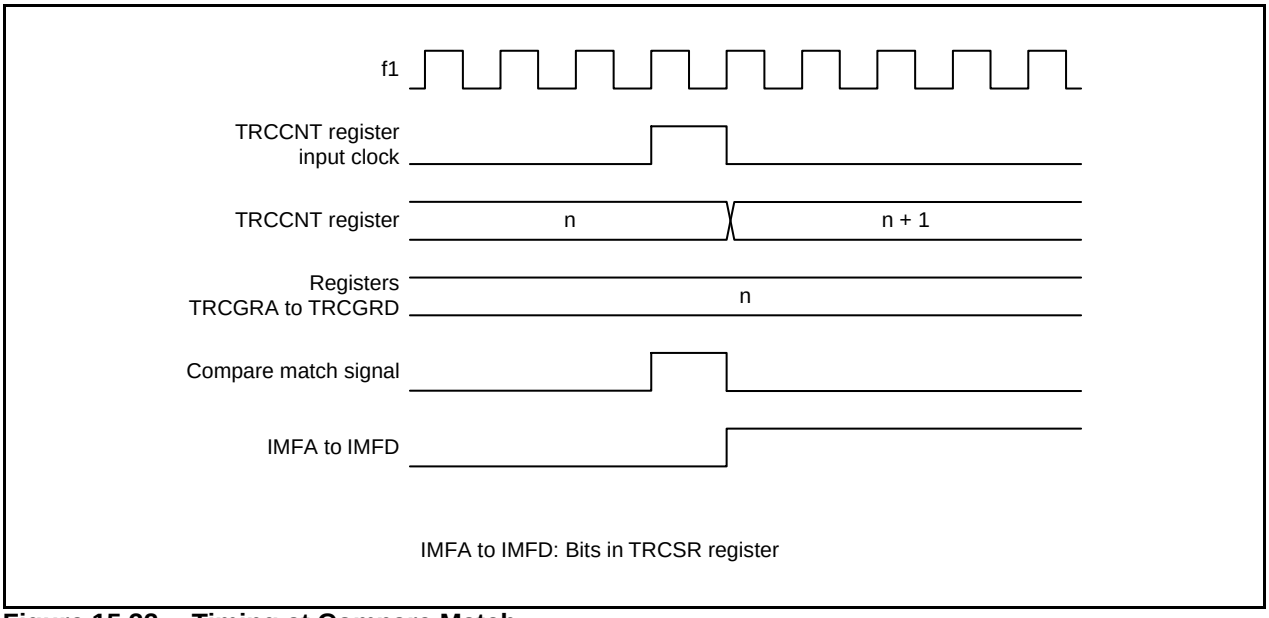


Figure 15.32 Timing at Compare Match

15.5.7 Setting Timing at Input Capture

While the TRCSR register functions as an input capture register, bits IMFA to IMFD are set to 1 when an input capture occurs.
Figure 15.33 shows the Timing at Input Capture.

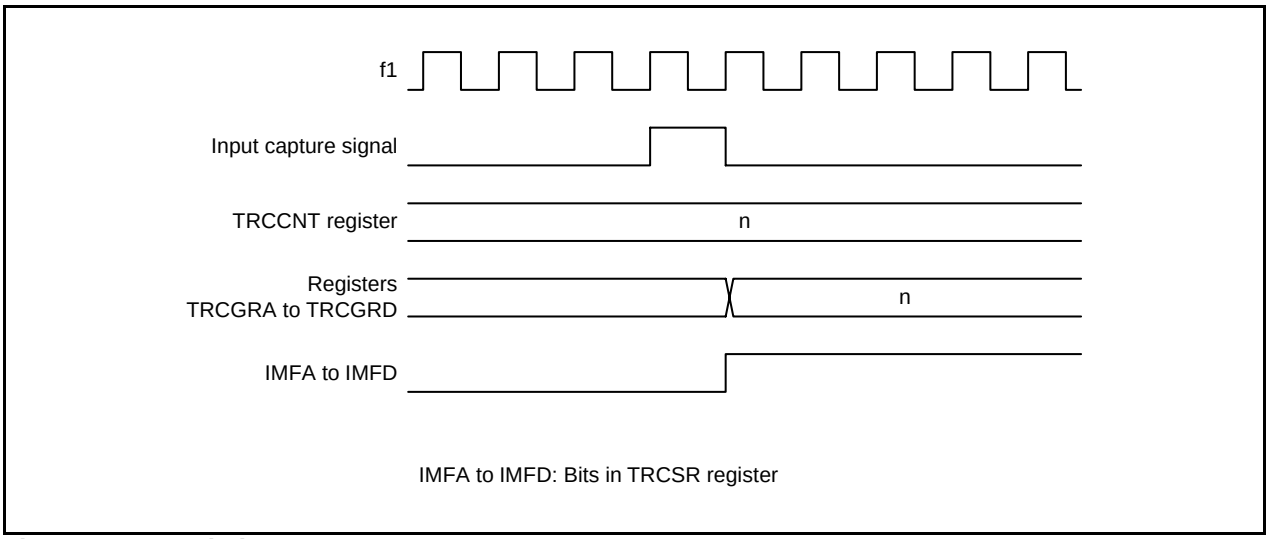


Figure 15.33 Timing at Input Capture

15.5.8 Timing for Setting Bits IMFA to IMFD and OVF to 0

Bits IMFA to IMFD and OVF are set to 0 when 0 is written after the CPU reads it as 1.
Figure 15.34 shows the Timing for Setting Bits IMFA to IMFD and OVF by CPU.

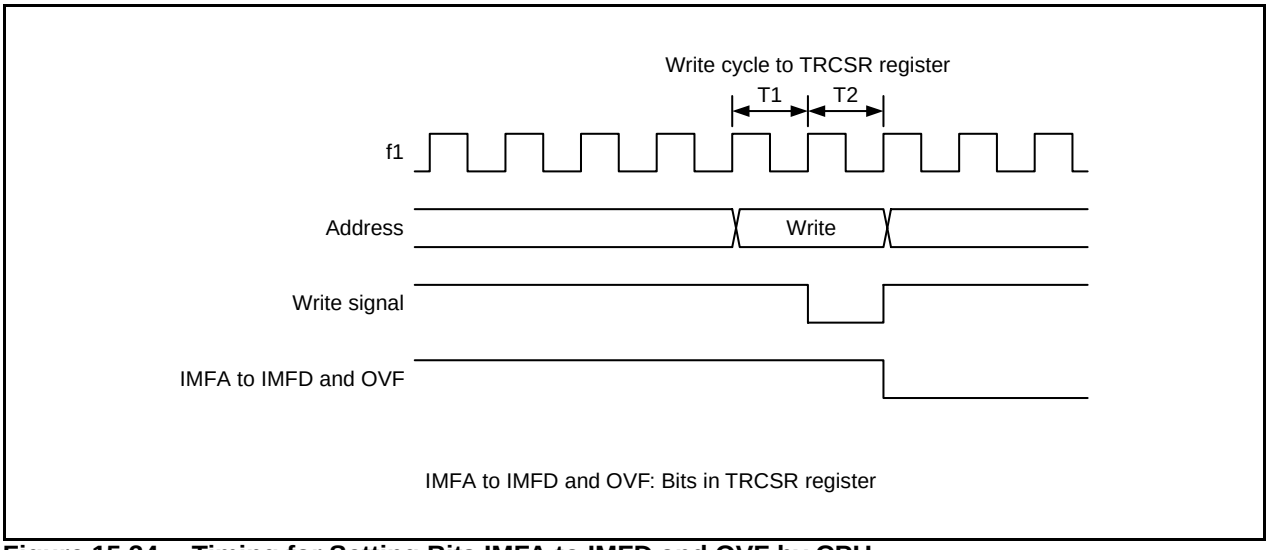


Figure 15.34 Timing for Setting Bits IMFA to IMFD and OVF by CPU

15.5.9 Timing of A/D Conversion Start Trigger due to Compare Match

Figure 15.35 shows the Timing of A/D Conversion Start Trigger due to Compare Match.

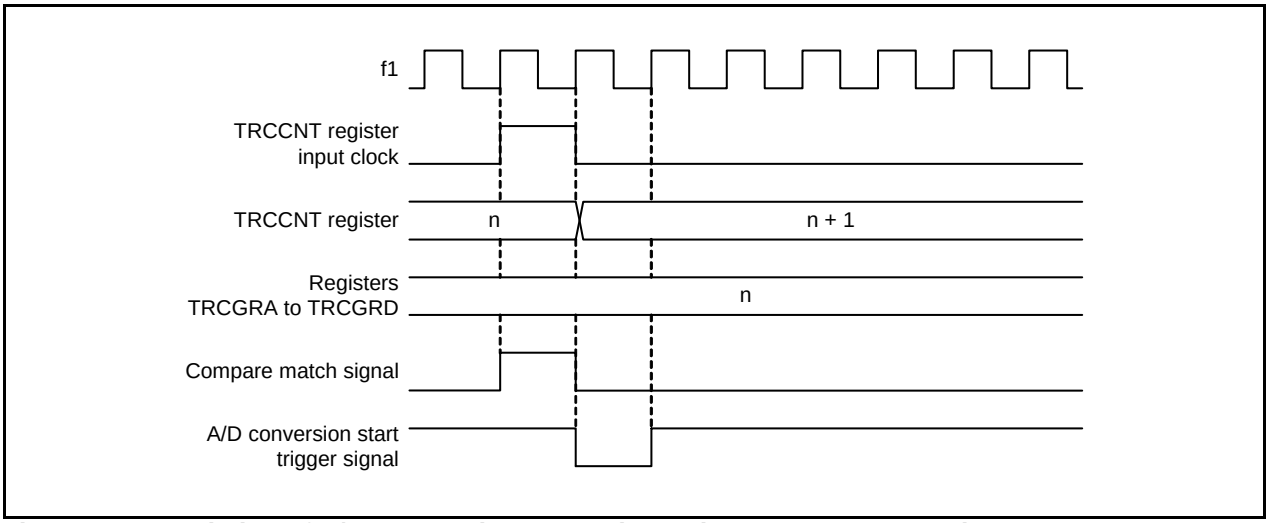


Figure 15.35 Timing of A/D Conversion Start Trigger due to Compare Match

15.6 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses bits ILVL35 and ILVL34 in the ILVL3 register, the IRTC bit in the IRR0 register, and a single vector.
Table 15.18 lists the Registers Associated with Timer RC Interrupt, and Figure 15.36 shows a Timer RC Interrupt Block Diagram.

Table 15.18 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register	Timer RC Interrupt Request Monitor Flag Register
TRCSR	TRCIER	ILVL3	IRR0

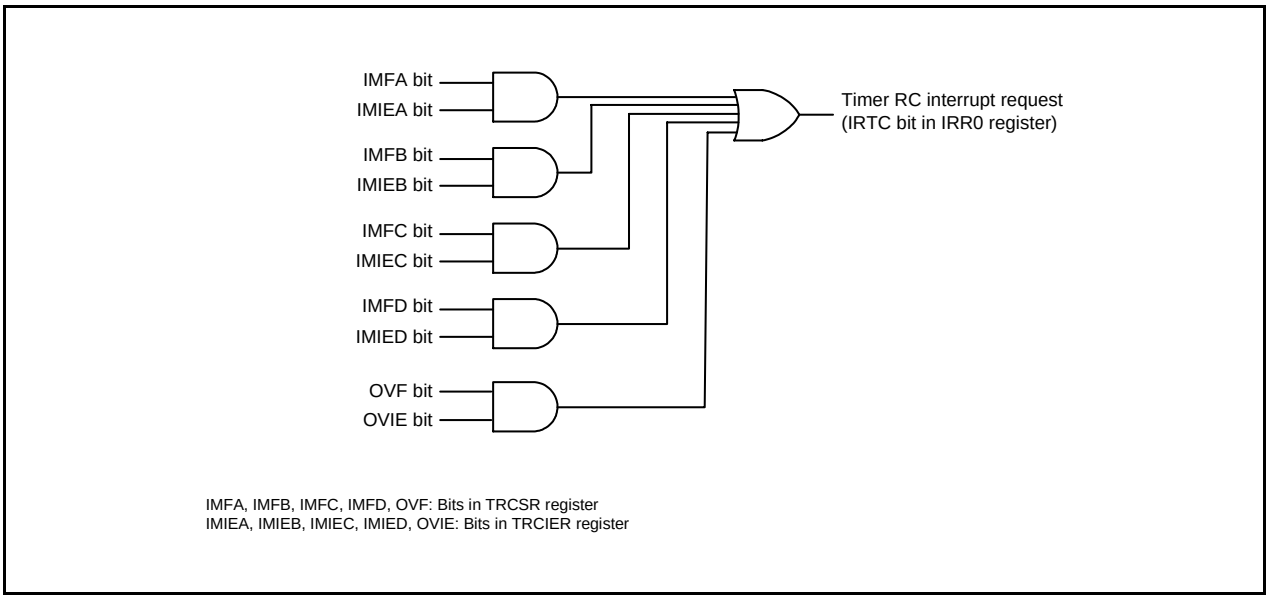


Figure 15.36 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IRTC bit, bits ILVL35 to ILVL34, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IRTC bit in the IRR0 register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IRTC bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IRTC bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IRTC bit is set to 1, the IRTC bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **15.2.6 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **15.2.5 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **11.4 Interrupt Control**, for details of the ILVL3 register and **11.3.2 Relocatable Vector Table**, for information on interrupt vectors.

15.7 Notes on Timer RC

15.7.1 TRCCNT Register

The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A).

- When writing a value to the TRCCNT register by a program while the CTS bit in the TRCMR register is set to 1 (count is started), ensure that the write timing does not coincide with when the TRCCNT register is set to 0000h.
- If the timing when the TRCCNT register is set to 0000h and is written coincide with each other, the value is not be written and the TRCCNT register is set to 0000h.

If the TRCCNT register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.W   #XXXXh, TRCCNT      ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.W   TRCCNT, DATA        ; Read
```

15.7.2 TRCCR1 Register

To set bits CKS2 to CKS0 in the TRCCR1 register to 110b (fHOCO), set fHOCO to the clock frequency higher than the system clock frequency.

15.7.3 TRCSR Register

If the TRCSR register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.B   #XXh, TRCSR         ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.B   TRCSR, DATA         ; Read
```

15.7.4 Count Source Switching

When switching the count sources, stop the count before switching. After switching the count sources, wait for at least two cycles of the system clock before writing to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Write to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

When changing the count source from fHOCO to another source and stopping fHOCO, wait for at least two cycles of the system clock after changing the clock setting before stopping fHOCO.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Set the HOCOE bit in the OCOCR register to 0 (high-speed on-chip oscillator off).

15.7.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 15.1 Timer RC Specifications**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 15.19 Digital Filter Circuit Block Diagram**)

- The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

15.7.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (increment is stopped), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

15.7.7 MSTCR Register

After stopping the timer RC count, set the MSTTRC bit in the MSTCR register to 1 (standby).

15.7.8 Mode Switching

- When switching the modes during operation, set the CTS bit in the TRCMR register to 0 (count is stopped) before switching.
- After switching the modes, set each flag in the TRCSR register to 0 before operation is started.

15.7.9 Procedure for Setting Registers Associated with Timer RC

Set the registers associated with timer RC following the procedure below:

(1) Set timer RC operating mode (bits PWMB, PWMC, PWMD, and PWM2 in the TRCMR register).
(2) Set the registers other than that set in (1).
(3) Set the port output to be enabled (bits EA to ED in the TRCOER register).

16. Serial Interface (UART0)

The serial interface consists of a single channel: UART0.

16.1 Overview

UART0 has a dedicated timer to generate the transfer clock. It supports two modes: Clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.
Table 16.1 lists the UART0 Specifications. Figure 16.1 shows the UART0 Block Diagram. Figure 16.2 shows the Transmit/Receive Unit Block Diagram. Table 16.2 lists the UART0 Pin Configuration. For details, see **Table 16.4 Clock Synchronous Serial I/O Mode Specifications** and **Table 16.6 Clock Asynchronous Serial I/O Mode Specifications**.

Table 16.1 UART0 Specifications

Item		Description
I/O pins		3 pins (CLK0, RXD0, and TXD0)
Clock synchronous serial I/O mode	Transfer data format	Transfer data length: 8 bits
	Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fi/2 (n + 1) fi = f1, f8, or f32 n: Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT (input from the CLK0 pin)
	Error detection	Overrun error
Clock asynchronous serial I/O mode	Transfer data format	• Character bits (transfer data): Selectable from 7, 8, or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bit: Selectable from 1 or 2 bits
	Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fj/16 (n + 1) fj = f1, f8, or f32 n: Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT/16 (n + 1) fEXT (input from the CLK0 pin) n: Value set in the U0BRG register (00h to FFh)
	Error detection	Overrun error, framing error, parity error, error sum flag
Interrupt sources		Transmit buffer empty or transmit complete interrupt (multiplexed), and receive complete interrupt

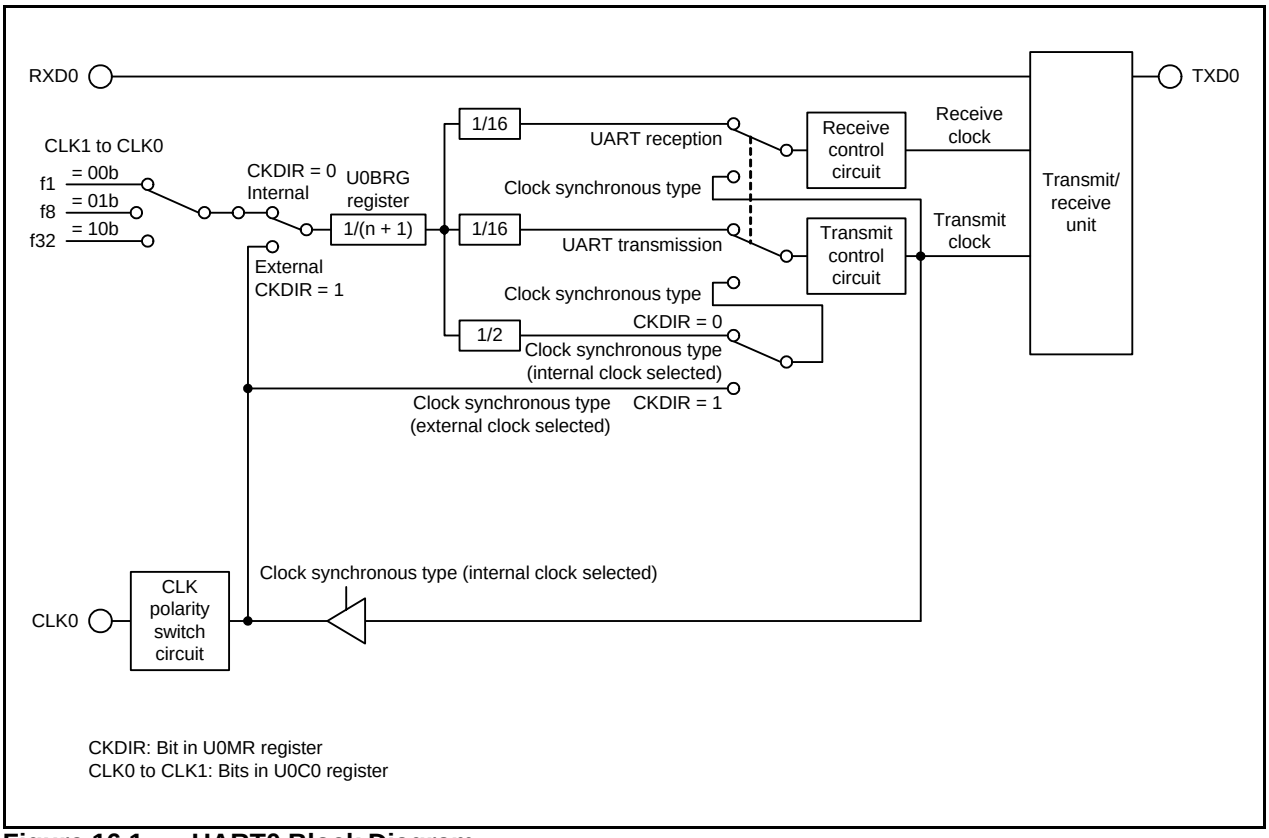
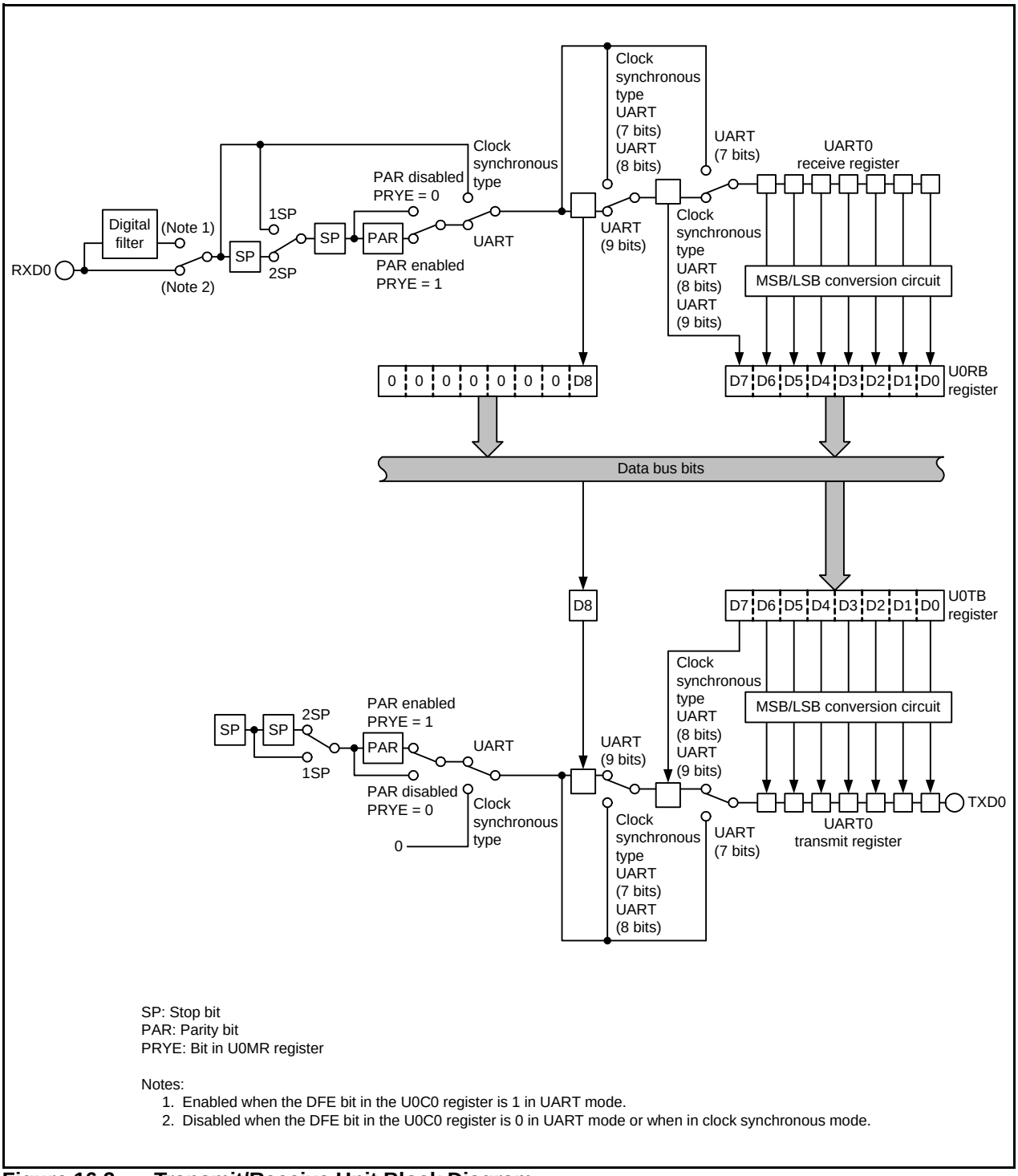


Figure 16.1 UART0 Block Diagram



SP: Stop bit
PAR: Parity bit
PRYE: Bit in U0MR register

Notes:
1. Enabled when the DFE bit in the U0C0 register is 1 in UART mode.
2. Disabled when the DFE bit in the U0C0 register is 0 in UART mode or when in clock synchronous mode.

Figure 16.2 Transmit/Receive Unit Block Diagram

Table 16.2 UART0 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
CLK0	P1_6	I/O	Transfer clock input and output
RXD0	P1_4, P1_5, P4_6	I	Serial data input
TXD0	P1_4, P4_2, P4_6	O	Serial data output

16.2 Registers

Table 16.3 lists the UART0 Register Configuration.

Table 16.3 UART0 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
UART0 Transmit/Receive Mode Register	U0MR	00h	00080h	8
UART0 Bit Rate Register	U0BRG	XXh	00081h	8
UART0 Transmit Buffer Register	U0TBL	XXh	00082h	8 (1)
	U0TBH	XXh	00083h	8 (1)
UART0 Transmit/Receive Control Register 0	U0C0	00001000b	00084h	8
UART0 Transmit/Receive Control Register 1	U0C1	00000010b	00085h	8
UART0 Receive Buffer Register	U0RBL	XXh	00086h	8 (1)
	U0RBH	XXh	00087h	8 (1)
UART0 Interrupt Flag and Enable Register	U0IR	00h	00088h	8

X: Undefined

Note:

1. For details on access, see the description of the individual registers.

16.2.1 UART0 Transmit/Receive Mode Register (U0MR)

Address 00080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bits (1, 2)	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than the above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit (3)	0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:

1. When setting bits SMD2 to SMD0 to 000b (serial interface disabled), set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. When bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode), the error flags (bits FER, PER, and SUM) in the U0RB register are disabled. When these bits are read, the values are undefined.
3. The PRY bit is enabled when the PRTYE bit is 1 (parity enabled).

16.2.2 UART0 Bit Rate Register (U0BRG)

Address 00081h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the set value is n, U0BRG divides the count source by n + 1.	00h to FFh	W

Write to the U0BRG register using the MOV instruction while transmission and reception are stopped.
Set bits CLK0 to CLK1 in the U0C0 register before writing to this register.

16.2.3 UART0 Transmit Buffer Register (U0TB)

Address 00082h (U0TBL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Address 00083h (U0TBH)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D8 to D0)	W
b1	—		W
b2	—		W
b3	—		W
b4	—		W
b5	—		W
b6	—		W
b7	—		W
b8	—		W
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

If the transfer data is 9 bits long, write to the U0TBH register first and then the U0TBL register in 8-bit units.
Write to the U0TB register using the MOV instruction. Word access is prohibited.

16.2.4 UART0 Transmit/Receive Control Register 0 (U0C0)

Address 00084h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	DFE	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	U0BRG count source select bits (1)	b1 b0 0 0: f1 0 1: f8 1 0: f32 1 1: Do not set.	R/W
b1	CLK1			R/W
b2	—	Reserved	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission is in progress) 1: The transmit register empty (transmission is completed)	R
b4	DFE	RXD0 digital filter enable bit (2)	0: Digital filter disabled 1: Digital filter enabled	R/W
b5	NCH	Data output select bit	0: TXD0 pin is set to CMOS output 1: TXD0 pin is set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit (3)	0: Transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock 1: Transmit data is output on the rising edge and receive data is input on the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Notes:
1. If the U0BRG count source is changed, set the U0BRG register again.
2. The DFE bit is enabled in clock asynchronous serial I/O mode. In clock synchronous serial I/O mode, set this bit to 0 (digital filter disabled).
3. The CKPOL bit is enabled in clock synchronous serial I/O mode.

16.2.5 UART0 Transmit/Receive Control Register 1 (U0C1)

Address 00085h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	U0RRM	U0IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the U0TB register 1: The U0TB register empty	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag (1)	0: The U0RB register empty 1: Data present in the U0RB register	R
b4	U0IRS	UART0 transmit interrupt source select bit	0: Transmit buffer is empty (TI = 1) 1: Transmission is completed (TXEPT = 1)	R/W
b5	U0RRM	UART0 continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Reserved	Set to 0.	R/W
b7	—			

Notes:
1. The RI bit is set to 0 when the U0RBH register is read.
2. In clock asynchronous I/O mode, set the U0RRM bit to 0 (continuous receive mode disabled).

16.2.6 UART0 Receive Buffer Register (U0RB)

Address 00086h (U0RBL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Address 00087h (U0RBH)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Receive data (D8 to D0)		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—			R
b7	—			R
b8	—			R
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error has occurred 1: An overrun error has occurred	R
b13	FER	Framing error flag (1, 2)	0: No framing error has occurred 1: A framing error has occurred	R
b14	PER	Parity error flag (1, 2)	0: No parity error has occurred 1: A parity error has occurred	R
b15	SUM	Error sum flag (1, 2)	0: No error has occurred 1: An error has occurred	R

Notes:

1. Bits OER, FER, PER, and SUM are set to 0 (no error has occurred) when bits SMD2 to SMD0 in the U0MR register are set to 000b (serial interface disabled) or the RE bit in the U0C1 register is set to 0 (reception disabled).
   The SUM bit is set to 0 (no error has occurred) when all of bits OER, FER, and PER are set to 0 (no error has occurred). In addition, bits FER and PER are set to 0 when the U0RBH register is read.
   When setting bits SMD2 to SMD0 in the U0MR register to 000b, set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the U0MR register are set to 001b (clock synchronous serial I/O mode). When these bits are read, the values are undefined.

The U0RB register must be read in 16-bit units. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units.

16.2.7 UART0 Interrupt Flag and Enable Register (U0IR)

Address 00088h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	U0TIF	U0RIF	—	—	U0TIE	U0RIE	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	U0RIE	UART0 receive interrupt enable bit	0: Receive interrupt disabled 1: Receive interrupt enabled	R/W
b3	U0TIE	UART0 transmit interrupt enable bit	0: Transmit interrupt disabled 1: Transmit interrupt enabled	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	U0RIF	UART0 receive interrupt flag	0: No receive interrupt requested 1: Receive interrupt requested	R/W
b7	U0TIF	UART0 transmit interrupt flag	0: No transmit interrupt requested 1: Transmit interrupt requested	R/W

U0RIF Bit (UART0 receive interrupt flag)

[Condition for setting to 0]
- When 0 is written to this bit after reading it as 1.

[Condition for setting to 1]
- When the RI bit in the U0C1 register is changed from 0 (the U0RB register empty) to 1 (data present in the U0RB register).

U0TIF Bit (UART0 transmit interrupt flag)

[Condition for setting to 0]
- When 0 is written to this bit after reading it as 1.

[Condition for setting to 1]
- When the transmit buffer becomes empty or transmission completes.

16.3 Operation

UART0 supports two modes: Clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.

16.3.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, transmission or reception is performed using a transfer clock.
Table 16.4 lists the Clock Synchronous Serial I/O Mode Specifications. Table 16.5 lists the Registers and Settings Used in Clock Synchronous Serial I/O Mode.

Table 16.4 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fi/(2 (n + 1)) fi = f1, f8, or f32 n = Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT (input from the CLK0 pin)
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U0C1 register must be 1 (reception enabled). • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Interrupt request generation timing	• For transmission: One of the following can be selected. - The U0IRS bit in the U0C1 register is 0 (transmit buffer is empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit in the U0C1 register is 1 (transmission is completed): When data transmission from the UART0 transmit register is completed. • For reception: When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (2) This error occurs if the next data reception is started and the 7th bit is received before the U0RB register is read.
Selectable functions	• CLK polarity selection The output and input timing of transfer data can be selected to be either the rising or the falling edge of the transfer clock. • LSB first or MSB first selection The start bit can be selected to be bit 0 or bit 7 when transmission and reception are started. • Continuous receive mode selection Reading the U0RB register enables reception at the same time.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   • The external clock is set to high when the CKPOL bit in the U0C0 register is 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock).
   • The external clock is set to low when the CKPOL bit is 1 (transmit data is output on the rising edge and receive data is input on the falling edge of the transfer clock).
2. If an overrun error occurs, the receive data (b0 to b7) in the U0RB register is undefined. The U0RIF bit in the U0IR register remains unchanged.

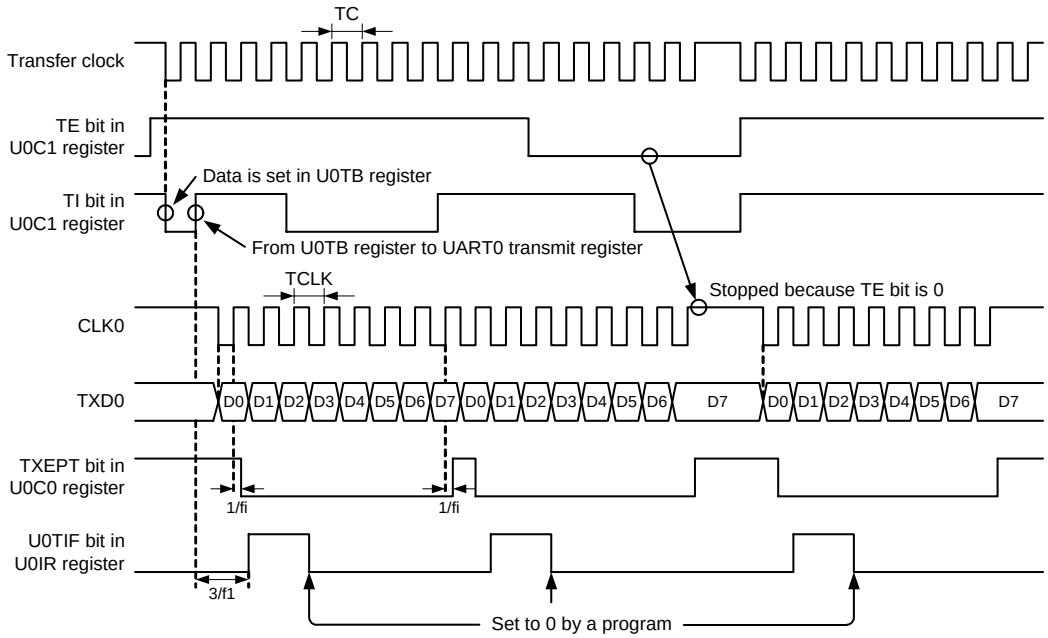
Table 16.5 Registers and Settings Used in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U0TB	b0 to b7	Set the transmit data.
U0RB	b0 to b7	The receive data can be read.
	OER	Overrun error flag
U0BRG	b0 to b7	Set the bit rate.
U0MR	SMD2 to SMD0	Set to 001b (clock synchronous serial I/O mode).
	CKDIR	Select an internal or external clock.
U0C0	CLK0 to CLK1	Select the U0BRG count source (f1, f8, or f32).
	TXEPT	Transmit register empty flag
	NCH	Select the output type (CMOS or N-channel open-drain output) of the TXD0 pin.
	CKPOL	Select the polarity of the transfer clock.
	UFORM	Select LSB first or MSB first.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U0IRS	Select the UART0 transmit interrupt source to be transmit buffer empty or transmit complete.
	U0RRM	Select continuous receive mode from disabled or enabled.

Note:
1. The write value must be 0 for all bits not listed in this table.

16.3.1.1 Operation Examples

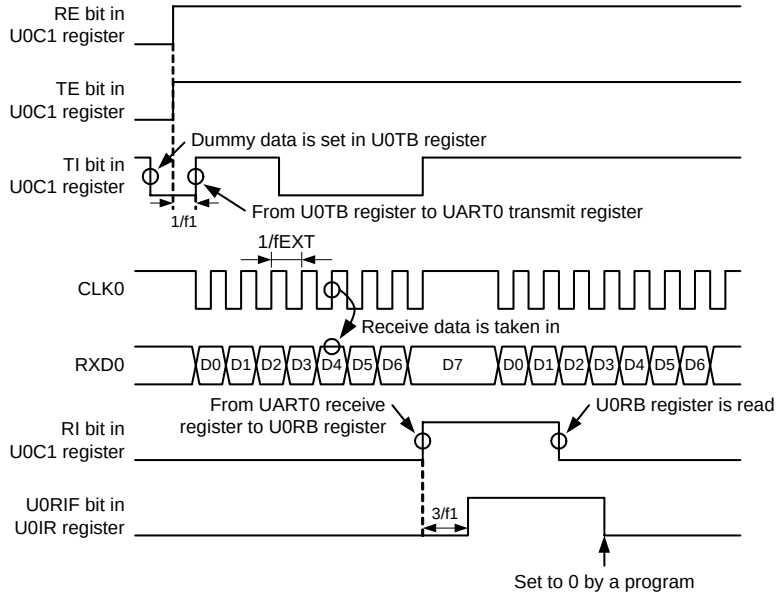
• Transmit timing example (internal clock selected)



The above diagram applies for the following settings:
- CKDIR bit in U0MR register = 0 (internal clock)
- CKPOL bit in U0C0 register = 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock)
- U0IRS bit in U0C1 register = 0 (transmit buffer is empty)

TC = TCLK = 2 (n + 1)/fi
fi: Frequency of U0BRG count source (f1, f8, or f32)
n: Value set in U0BRG register

• Receive timing example (external clock selected)



fEXT: Frequency of external clock

The above diagram applies for the following settings:
- CKDIR bit in U0MR register = 1 (external clock)
- CKPOL bit in U0C0 register = 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock)

The following requirements must be met when an input to the CLK0 pin is high before data reception:
- TE bit in U0C1 register → 1 (transmission enabled)
- RE bit in U0C1 register → 1 (reception enabled)
- Dummy data is written to U0TB register

Figure 16.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

16.3.1.2 Polarity Select Function

Figure 16.4 shows the Transfer Clock Polarity.
The CKPOL bit in the U0C0 register can be used to select the polarity of the transfer clock.

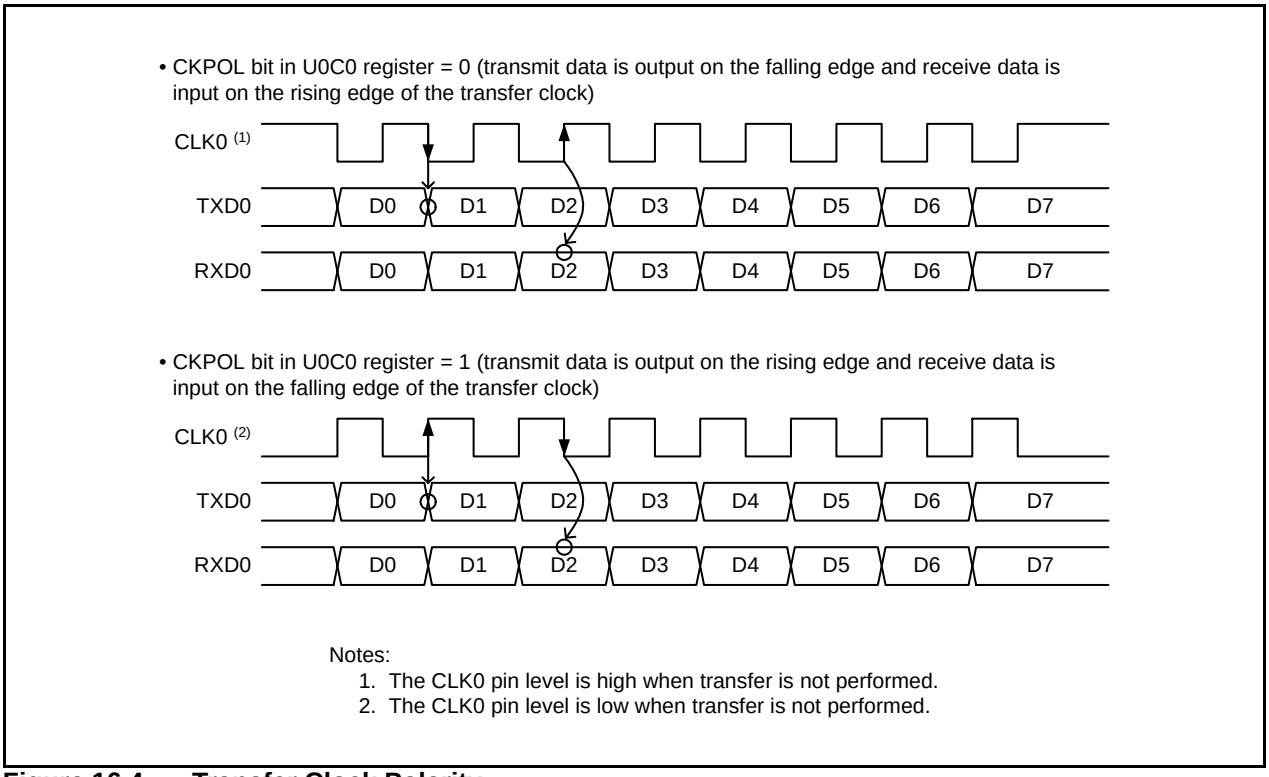


Figure 16.4 Transfer Clock Polarity

16.3.1.3 LSB First or MSB First Selection

Figure 16.5 shows the Transfer Format.
The UFORM bit in the U0C0 register can be used to select the transfer format.

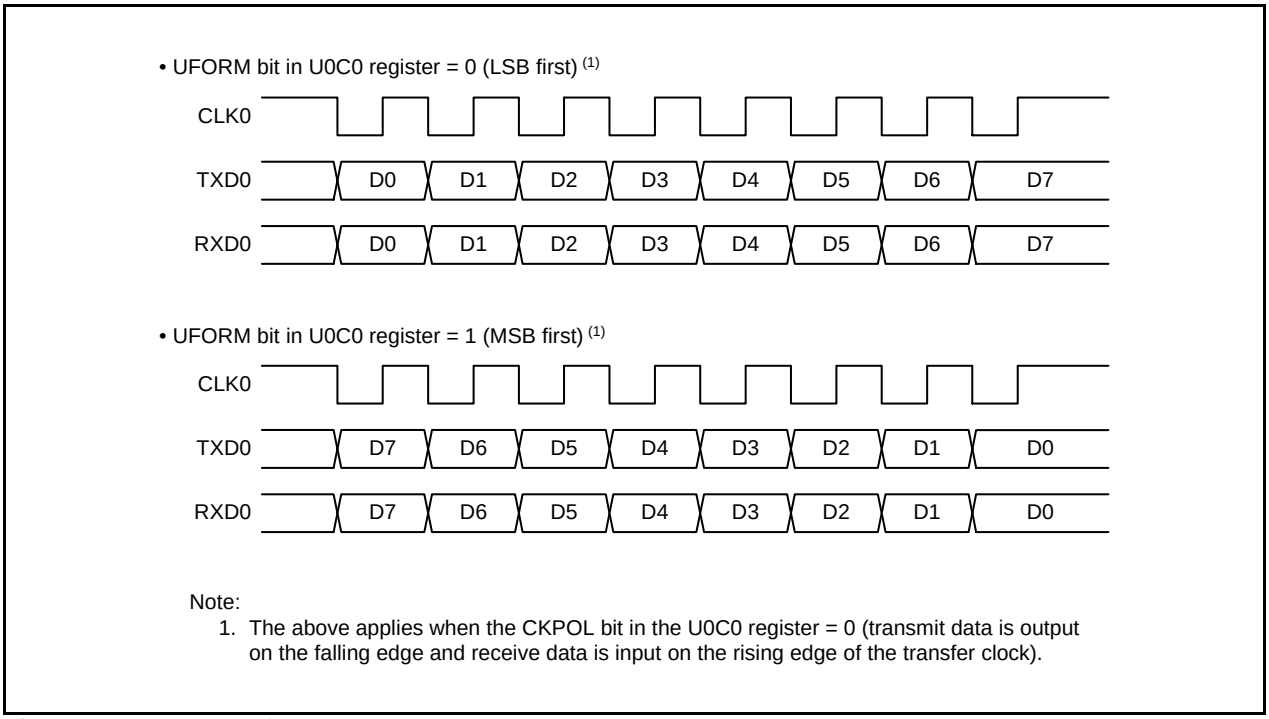


Figure 16.5 Transfer Format

16.3.1.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data present in the U0TB register). When the U0RRM bit is 1, do not write dummy data to the U0TB register by a program.

16.3.1.5 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedure below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

16.3.2 Clock Asynchronous Serial I/O (UART) Mode

In clock asynchronous serial I/O mode, transmission and reception are performed at an arbitrary bit rate and in an arbitrary format.
Table 16.6 lists the Clock Asynchronous Serial I/O Mode Specifications. Table 16.7 lists the Registers and Settings Used in Clock Asynchronous Serial I/O Mode.

Table 16.6 Clock Asynchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): Selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 or 2 bits
Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fj/16 (n + 1) fj = f1, f8, or f32 n = Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT/16 (n + 1) fEXT (input from the CLK0 pin) n = Value set in the U0BRG register (00h to FFh)
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the U0C1 register must be 1 (transmission enabled). • The TI bit in the U0C1 register must be 0 (data present in the U0TB register).
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the U0C1 register must be 1 (reception enabled). • Start bit detection
Interrupt request generation timing	• For transmission: One of the following can be selected. - The U0IRS bit in the U0C1 register is 0 (transmit buffer is empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit in the U0C1 register is 1 (transmission is completed): When data transmission from the UART0 transmit register is completed. • For reception: When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the next data reception is started and the next to last bit is received before the U0RB register is read. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register is undefined. The U0RIF bit in the U0IR register remains unchanged.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

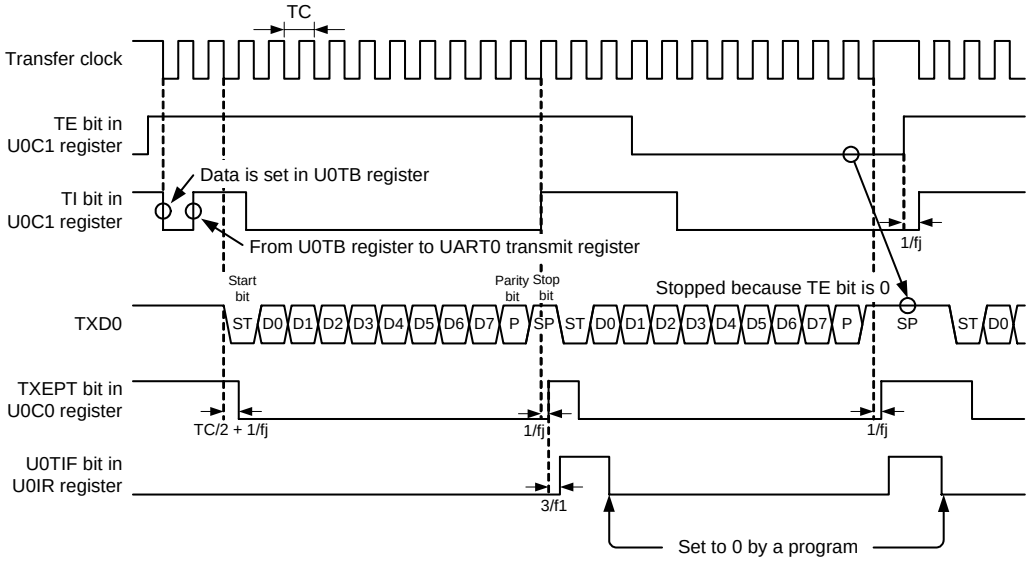
Table 16.7 Registers and Settings Used in Clock Asynchronous Serial I/O Mode

Register	Bit	Function
U0TB	b0 to b8	Set the transmit data. (1)
U0RB	b0 to b8	The receive data can be read. (2)
	OER	Overrun error flag
	FER	Framing error flag
	PER	Parity error flag
	SUM	Error sum flag
U0BRG	b0 to b7	Set the bit rate.
U0MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal or external clock.
	STPS	Select one or two stop bits.
	PRY, PRYE	Select whether parity is enabled and whether odd or even.
U0C0	CLK0 to CLK1	Select the U0BRG count source (f1, f8, or f32).
	TXEPT	Transmit register empty flag
	NCH	Select the output type (CMOS or N-channel open-drain output) of the TXD0 pin.
	CKPOL	Set to 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock).
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 (LSB first) when transfer data is 7 bits or 9 bits long.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U0IRS	Select the UART0 transmit interrupt source to be transmit buffer empty or transmit complete.
	U0RRM	Set to 0 (continuous receive mode disabled).

Notes:
1. The bits used are as follows:
   • Bits 0 to 6 when transfer data is 7 bits long
   • Bits 0 to 7 when transfer data is 8 bits long
   • Bits 0 to 8 when transfer data is 9 bits long
2. The contents of the following are undefined: Bits 7 and 8 when transfer data is 7 bits long, and bit 8 when transfer data is 8 bits long.

16.3.2.1 Operation Examples

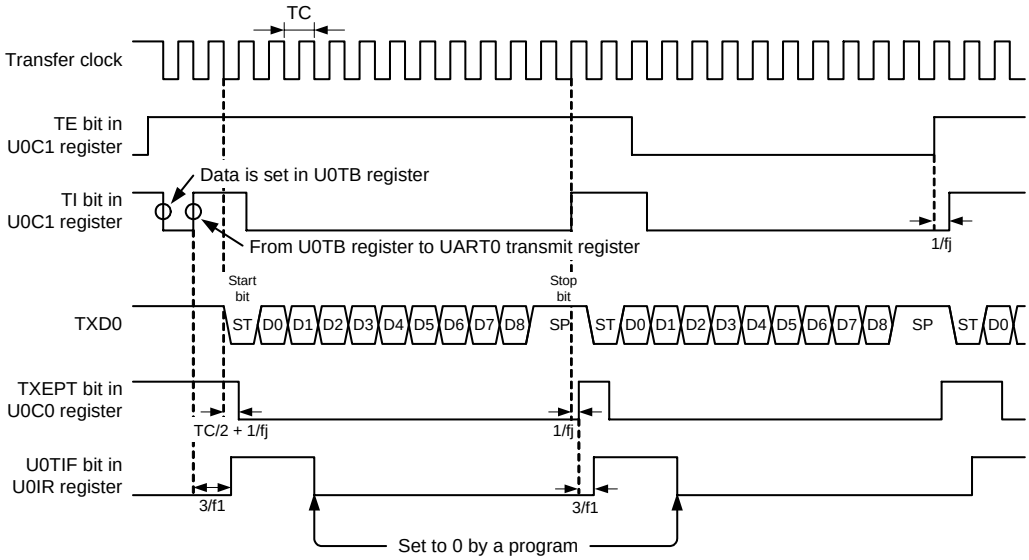
• When transfer data is 8 bits long (parity enabled, one stop bit)



The above diagram applies for the following settings:
- STPS bit in U0MR register = 0 (one stop bit)
- PRYE bit in U0MR register = 1 (parity enabled)
- U0IRS bit in U0C1 register = 1 (transmission is completed)

TC = 16 (n + 1)/fj or 16 (n + 1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, or f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

• When transfer data is 9 bits long (parity disabled, two stop bits)



The above diagram applies for the following settings:
- STPS bit in U0MR register = 1 (two stop bits)
- PRYE bit in U0MR register = 0 (parity disabled)
- U0IRS bit in U0C1 register = 0 (transmit buffer is empty)

TC = 16 (n + 1)/fj or 16 (n + 1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, or f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

Figure 16.6 Transmit Timing in Clock Asynchronous Serial I/O Mode

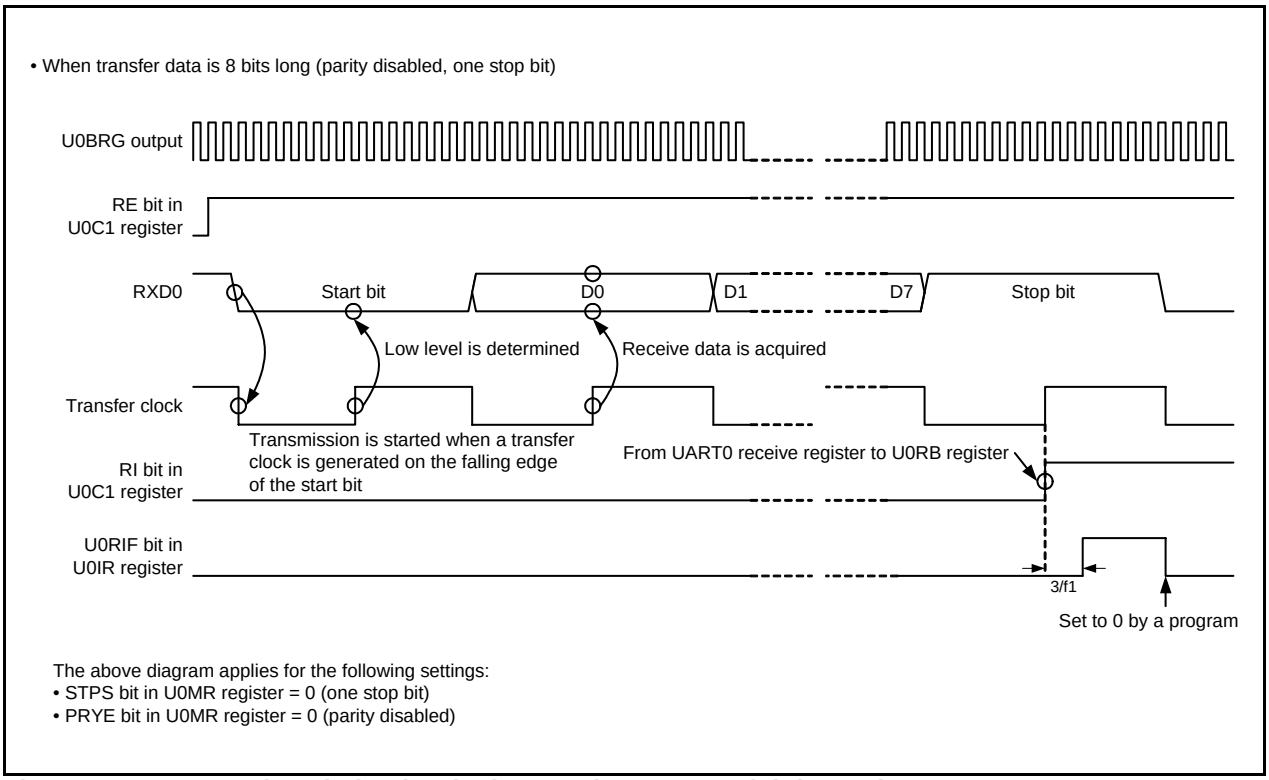


Figure 16.7 Receive Timing in Clock Asynchronous Serial I/O Mode

16.3.2.2 Bit Rate

In clock asynchronous serial I/O mode, the bit rate is obtained by dividing the frequency with the U0BRG register and further dividing it by 16.
The value to be set in the U0BRG register is calculated as follows:

• When an internal clock is selected

$$\text{Value set in U0BRG register} = \frac{\text{fj}}{\text{Bit rate} \times 16} - 1$$

fj: Frequency of U0BRG count source (f1, f8, or f32)

• When an external clock is selected

$$\text{Value set in U0BRG register} = \frac{\text{fEXT}}{\text{Bit rate} \times 16} - 1$$

fEXT: Frequency of U0BRG count source (external clock)

Table 16.8 Setting Example for Clock Asynchronous Serial I/O Mode (Internal Clock Selected)

Bit Rate (bps)	U0BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		Value Set in U0BRG Register	Actual Rate (bps)	Setting Error (%)	Value Set in U0BRG Register	Actual Rate (bps)	Setting Error (%)	Value Set in U0BRG Register	Actual Rate (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	—	—	—

Note:
1. For the high-speed on-chip oscillator, write the adjustment values in registers FR18S0 and FR18S1 to registers FRV1 and FRV2, respectively.
This applies when the high-speed on-chip oscillator is selected as the system clock and the PHISEL register is set to 00h (no division). For details on the accuracy of the high-speed on-chip oscillator, see **20. Electrical Characteristics**.

16.3.2.3 RXD0 Digital Filter

When the DFE bit in the U0C0 register is 1 (digital filter enabled), the RXD0 input is latched internally through the digital filter circuit for noise cancellation. The noise canceller consists of three cascaded latch circuits and a match detection circuit. When the RXD0 input is sampled on the base clock with frequency of 16 times the transfer rate and three latch outputs match, the level is passed forward to the next circuit. When they do not match, the previous level is retained.

That is, if the RXD0 input retains the same level for three clocks or more, it is recognized as a signal. If not, it is recognized as noise.

Figure 16.8 shows the RXD0 Digital Filter Block Diagram.

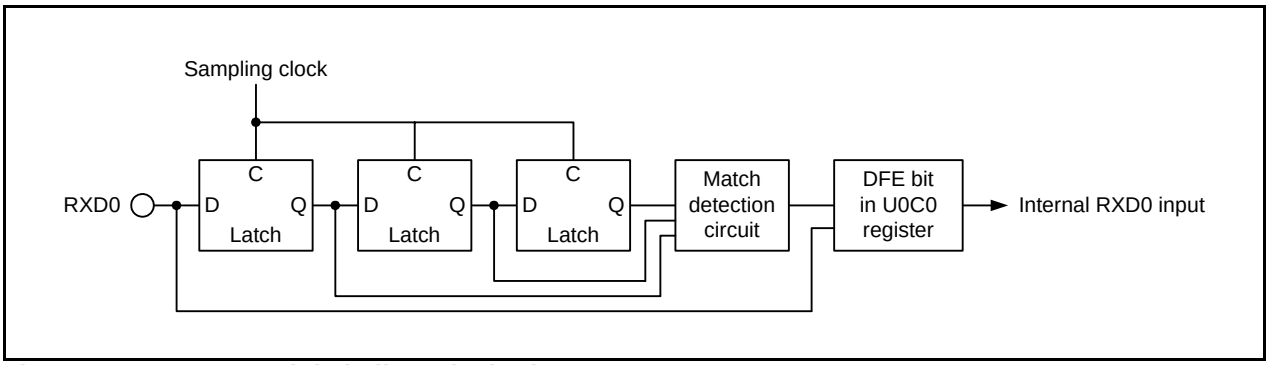


Figure 16.8 RXD0 Digital Filter Block Diagram

16.3.2.4 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedure below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

16.4 UART0 Interrupt

The UART0 interrupt requests are the transmit buffer empty or transmit complete interrupt, and the receive complete interrupt.
Table 16.9 lists the Interrupt Requests.

Table 16.9 Interrupt Requests

Interrupt Request	Interrupt Generation Condition
Transmit buffer empty	U0TIF = 1 (transmit interrupt requested) and U0TIE = 1 (transmit interrupt enabled)
Transmit complete	
Receive complete	U0RIF = 1 (receive interrupt requested) and U0RIE = 1 (receive interrupt enabled)

U0TIF, U0TIE, U0RIF, U0RIE: Bits in U0IR register
Note:
1. The CPU executes interrupt exception handling when the interrupt generation conditions are met and the I flag in the FLG register is 1.

16.5 Notes on Serial Interface (UART0)

Regardless of clock synchronous I/O mode or clock asynchronous I/O mode, read the U0RB register in 16-bit units.
When the U0RBH register is read, bits FER and PER in the U0RB register are set to 0 (no framing error, no parity error). Also, the RI bit in the U0C1 register is set to 0 (the U0RB register empty).
To check receive errors, use the data read from the U0RB register.

• Program example to read the receive buffer register

```
MOV.W    0086H, R0        ; Read the U0RB register
```

When the transfer data is 9 bits long in clock asynchronous I/O mode, write to the U0TB register in the order U0TBH first and then U0TBL in 8-bit units.

• Program example to write to the transmit buffer register

```
MOV.B    #XXH, 0083H      ; Write to the U0TBH register
MOV.B    #XXH, 0082H      ; Write to the U0TBL register
```

Do not set the MSTUART bit in the MSTCR register to 1 (standby) during communication. When setting the module to the standby state, confirm whether communication has completed. After communication has completed, set bits TE and RE in the U0C1 register to 0 (communication disabled) before setting the module to the standby state. After the module standby state is cleared, the initial settings for communication must be set again.

17. A/D Converter

This MCU features a 10-bit successive approximation A/D converter that can process analog inputs for up to six channels.

17.1 Overview

Table 17.1 lists the A/D Converter Specifications. Figure 17.1 shows the A/D Converter Block Diagram.

Table 17.1 A/D Converter Specifications

Item	Specification
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage	0 V to AVCC
Input channels	6 channels (AN0 to AN4, AN7)
Resolution	10 bits
A/D conversion clock	f1, f2, f4, f8, or fAD
Conversion time	2.2 μs (A/D conversion clock = 20 MHz)
A/D operating modes	• One-shot mode: A/D conversion is performed on the specified single channel for a single round. • Repeat mode: A/D conversion is performed on the specified single channel repeatedly. • Single sweep mode: A/D conversion is performed on the specified two channels for a single round. • Repeat sweep mode: A/D conversion is performed on the specified two channels repeatedly.
A/D conversion data register (× 2)	16-bit data register corresponding to each channel group where the A/D conversion result is stored (valid data length: 10 bits).
A/D conversion start conditions	• Software trigger • Conversion start trigger from timer RC • External trigger
Interrupt source	An A/D conversion interrupt is generated when A/D conversion completes.
Others	The A/D converter is set to standby by the MSTAD bit in the MSTCR register.

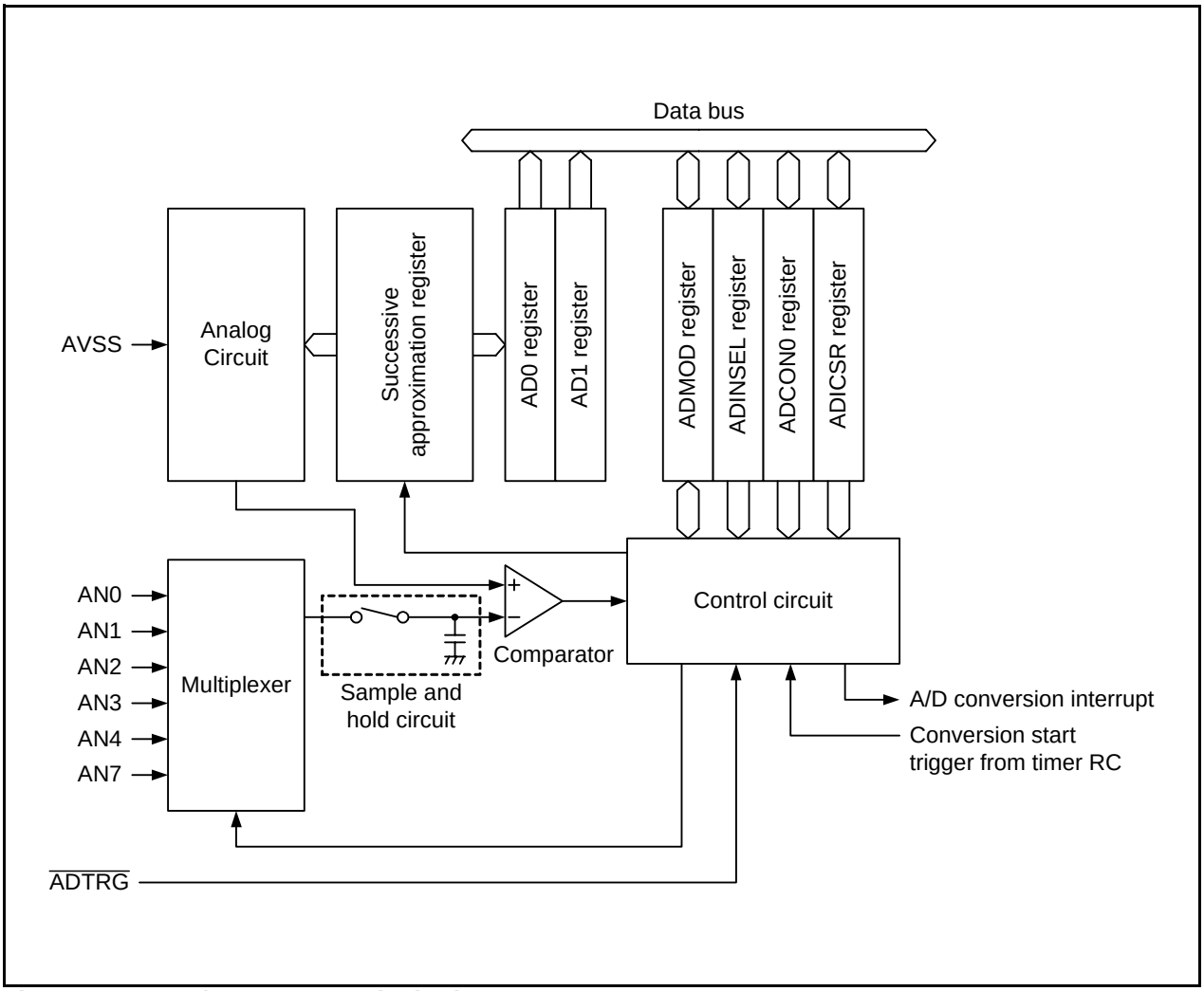


Figure 17.1 A/D Converter Block Diagram

Table 17.2 lists the A/D Converter Pin Configuration.
Pins AVCC and AVSS are used for the power supply to the analog block in the A/D converter.
The six analog input pins are divided into three channel groups.

Table 17.2 A/D Converter Pin Configuration

Pin Name	Assigned Pin	I/O	Function
AVCC	VCC	I	Power supply input for the A/D converter
AVSS	VSS	I	
AN0	P1_0	I	Analog input for channel group 0
AN1	P1_1	I	
AN2	P1_2	I	Analog input for channel group 1
AN3	P1_3	I	
AN4	P1_4	I	Analog input for channel group 2
AN7	P1_7	I	
$\overline{\text{ADTRG}}$	P3_7	I	External trigger input for starting A/D conversion

17.2 Registers

Table 17.3 lists the A/D Converter Register Configuration.

Table 17.3 A/D Converter Register Configuration

Register Name		Symbol	After Reset	Address	Access Size
A/D Register 0	Lower 8 bits	AD0L	XXh	00098h	8 or 16 (1)
	Higher 2 bits	AD0H	000000XXb	00099h	
A/D Register 1	Lower 8 bits	AD1L	XXh	0009Ah	8 or 16 (1)
	Higher 2 bits	AD1H	000000XXb	0009Bh	
A/D Mode Register		ADMOD	00h	0009Ch	8
A/D Input Select Register		ADINSEL	00h	0009Dh	8
A/D Control Register 0		ADCON0	00h	0009Eh	8
A/D Interrupt Control Status Register		ADICSR	00h	0009Fh	8

X: Undefined

Note:

1. For details on access, see the description of the individual registers.

17.2.1 A/D Register i (ADi) (i = 0 or 1)

Address 00098h (AD0L), 0009Ah (AD1L)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Address 00099h (AD0H), 0009Bh (AD1H)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	X	X

Bit	Symbol	Function	R/W
b7 to b0	—	Lower 8 bits in the A/D conversion result	R
b8	—	Higher 2 bits in the A/D conversion result	R
b9	—		
b10	—	Nothing is assigned. The write value must be 0. The read value is 0.	—
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

ADi (i = 0 or 1) is a 16-bit read-only register that stores the A/D conversion results. It is divided into ADiL (lower) and ADiH (higher). Table 17.4 lists the Correspondence between Analog Input Channels and ADi Register.

When the higher 6 bits in the ADiH register are read, the value is 0. Access can be made in 8-bit or 16-bit units. To read the ADi register as 8-bit units, read the ADiL register first and then ADiH register. When the ADi register is read as 16-bit units, it is read twice in 8-bit units.

Table 17.4 Correspondence between Analog Input Channels and ADi Register

Analog Input Channel			A/D Data Register that Stores Conversion Result
Channel Group 0 (ADGSEL1 to ADGSEL0 = 00b)	Channel Group 1 (ADGSEL1 to ADGSEL0 = 01b)	Channel Group 2 (ADGSEL1 to ADGSEL0 = 10b)	
AN0	AN2	AN4	AD0 register
AN1	AN3	AN7	AD1 register

ADGSEL0 to ADGSEL1: Bits in ADINSEL register

17.2.2 A/D Mode Register (ADMOD)

Address 0009Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	—	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	A/D conversion clock select bits	b2 b1 b0 0 0 0: f8 0 0 1: f4 0 1 0: f2 0 1 1: f1 1 0 0: fAD Other than the above: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	MD0	A/D operating mode select bits	b4 b3 0 0: One-shot mode 0 1: Repeat mode 1 0: Single sweep mode 1 1: Repeat sweep mode	R/W
b4	MD1			R/W
b5	—	Reserved	Set to 0.	R/W
b6	ADCAP0	A/D conversion trigger select bits	b7 b6 0 0: A/D conversion start by timer RC or external trigger is disabled 0 1: Do not set. 1 0: A/D conversion is started by conversion trigger from timer RC 1 1: A/D conversion is started by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

The ADMOD register must be written only when A/D conversion is stopped.

Bits CKS0 to CKS2 (A/D conversion clock select bits)

These bits are used to select the clock for A/D conversion.

Bits ADCAP0 to ADCAP1 (A/D conversion trigger select bits)

These bits are used to select or disable the trigger for starting A/D conversion.
When using a software trigger, set bits ADCAP1 to ADCAP0 to a value other than 01b.

17.2.3 A/D Input Select Register (ADINSEL)

Address 0009Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	—	—	—	—	—	CH0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Channel select bit	See **Table 17.5 Channel Groups and A/D Converter Input Channels**.	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	ADGSEL0	A/D input group select bits	b7 b6 0 0: Channel group 0 (AN0, AN1) 0 1: Channel group 1 (AN2, AN3) 1 0: Channel group 2 (AN4, AN7) 1 1: Do not set.	R/W
b7	ADGSEL1			R/W

The ADINSEL register must be written only when A/D conversion is stopped.

CH0 Bit (Channel select bit)

The input channel must be selected when the ADST bit in the ADCON0 register is 0 (A/D conversion stops).

Table 17.5 Channel Groups and A/D Converter Input Channels

	ADGSEL1 Bit	ADGSEL0 Bit	CH0 Bit	One-Shot Mode Repeat Mode	Single Sweep Mode Repeat Sweep Mode
Channel group 0	0	0	0	AN0	AN0, AN1
			1	AN1	
Channel group 1	0	1	0	AN2	AN2, AN3
			1	AN3	
Channel group 2	1	0	0	AN4	AN4, AN7
			1	AN7	

17.2.4 A/D Control Register 0 (ADCON0)

Address 0009Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start bit	0: A/D conversion stops 1: A/D conversion starts	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The ADCON0 register is used to control A/D conversion operation.

ADST Bit (A/D conversion start bit)

The ADST bit is used to start or stop A/D conversion.

[Conditions for setting to 0]
- When A/D conversion is completed in one-shot mode or single sweep mode.
- When 0 is written to this bit by software. (A/D conversion stops)

[Conditions for setting to 1]
- When 1 is written to this bit by software. (A/D conversion starts)
- When the A/D conversion start trigger enabled by the TRCADCR register is input.
- When an external trigger ($\overline{\text{ADTRG}}$) is input.

17.2.5 A/D Interrupt Control Status Register (ADICSR)

Address 0009Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADF	ADIE	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	ADIE	A/D conversion interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	ADF	A/D conversion interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)

Note:
1. Only 0 (no interrupt requested) can be written to the ADF bit.

ADF Bit (A/D conversion interrupt request bit)

This bit indicates whether an A/D conversion interrupt is requested. It also indicates whether A/D conversion has completed.

[Conditions for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Conditions for setting to 1]
• When A/D conversion is completed in one-shot mode or single sweep mode.
• When A/D conversion is completed on all the selected channels in repeat mode or repeat sweep mode.

17.3 Operation

This A/D converter provides operating four modes: One-shot, repeat, single sweep, and repeat sweep modes. This converter is a successive approximation type with 10-bit resolution.
The operating mode, analog input channel, and A/D conversion clock should be switched while the ADST bit in the ADCON0 register is 0 (A/D conversion stops).

17.3.1 Items Common to Multiple Modes

17.3.1.1 Input Sampling and A/D Conversion Time

The A/D converter includes a sample and hold circuit. When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts), the A/D converter samples the input and starts conversion after the A/D conversion start delay time (tD) has elapsed.
Figure 17.2 shows the A/D Conversion Timing. Table 17.6 lists the A/D Conversion Time.
As shown in Figure 17.2, the A/D conversion time (tCONV) includes tD and the input sampling time (tSPL). Here, tD is determined by the timing for writing to the ADCON0 register and is not a fixed value. The conversion time, therefore, varies within the range shown in Table 17.6.
In one-shot mode and single sweep mode, the ADF bit in the ADICSR register is set to 1 during end processing time, and the last A/D conversion result is stored in the ADi register.

- In one-shot mode
  A/D conversion time (tCONV) + end processing time (tEND)
- When two channels are selected in single sweep mode
  A/D conversion time (tCONV) + A/D conversion time (tCONV with no start delay time (tD) included) + end processing time (tEND)

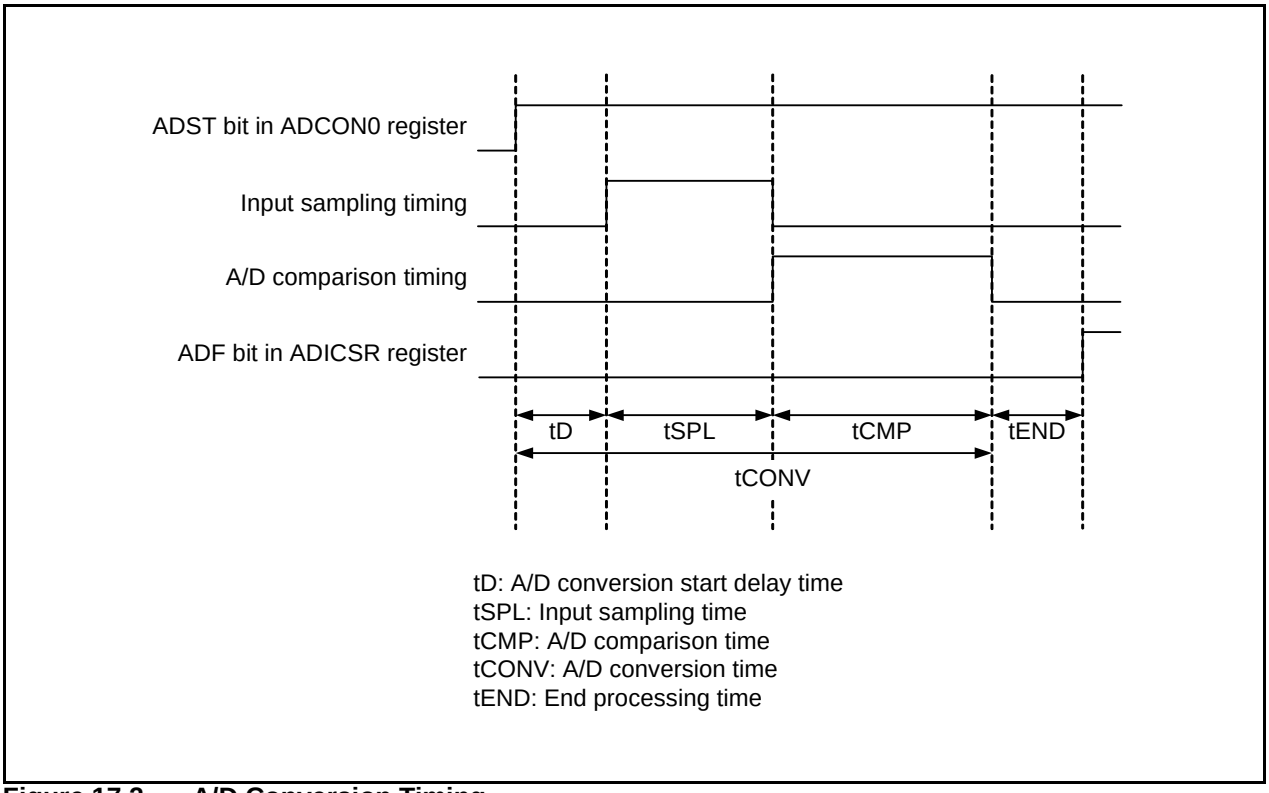


Figure 17.2 A/D Conversion Timing

Table 17.6 A/D Conversion Time

Item	Symbol	A/D Conversion Clock				
		f1	f2	f4	f8	fAD
		CKS0 = 1	CKS0 = 0	CKS0 = 1	CKS0 = 0	CKS0 = 0
		CKS1 = 1		CKS1 = 0		CKS1 = 0
		CKS2 = 0 (1)				CKS2 = 1 (2)
A/D conversion start delay time (3)	tD	3	3 to 4	3 to 6	3 to 10	3
Input sampling time	tSPL	16	31	61	121	16
A/D comparison time	tCMP	25	50	100	200	25
A/D conversion time	tCONV	44	84 to 85	164 to 167	324 to 331	44
End processing time	tEND	2 to 3 cycles of fAD				

CKS0, CKS1, CKS2: Bits in ADMOD register

Notes:
1. The numerical values in the table indicate the number of system clock (f) cycles.
2. The numerical values in the table indicate the number of fAD cycles.
3. In repeat mode, single sweep mode, and repeat sweep mode, there is no delay time during the A/D conversion time (tCONV) for the second and subsequent rounds.

17.3.1.2 External Trigger Input Timing

A/D conversion can also be started by an external trigger input. When bits ADCAP1 to ADCAP0 in the ADMOD register are 11b (A/D conversion is started by external trigger ($\overline{\text{ADTRG}}$)), an external trigger can be input to the $\overline{\text{ADTRG}}$ pin. The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) on the rising edge of the $\overline{\text{ADTRG}}$ input pin and A/D conversion is started. Other operations are the same as when the ADST bit in the ADCON0 register set to 1 by software.

Figure 17.3 shows the External Trigger Input Timing.

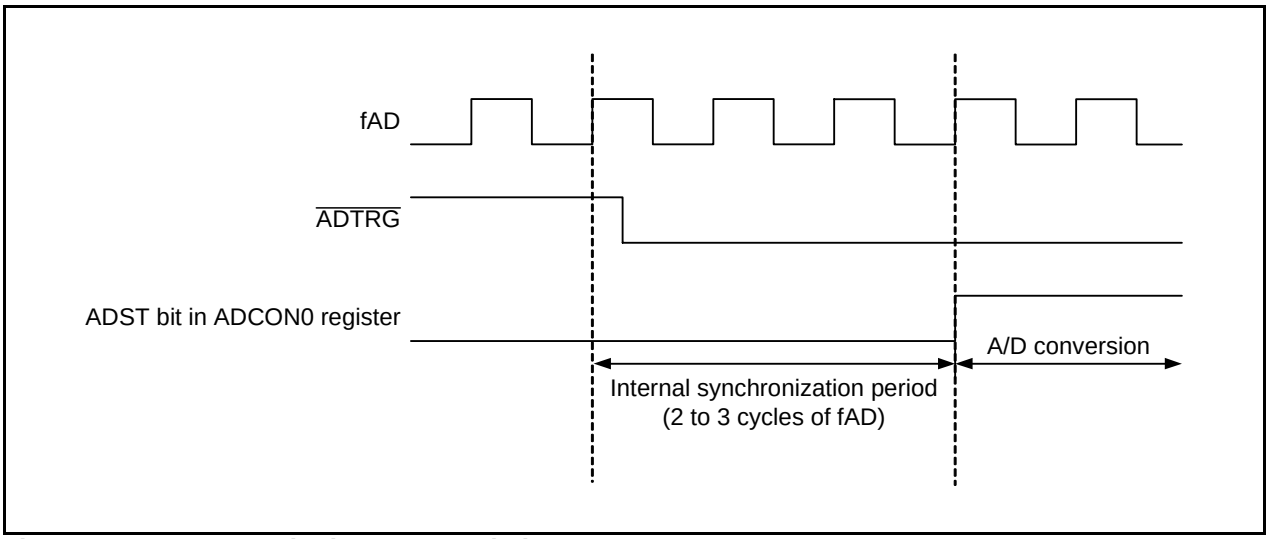


Figure 17.3 External Trigger Input Timing

17.3.2 One-Shot Mode

Figure 17.4 shows an Operation Example in One-Shot Mode When Channel 1 is Selected.
In one-shot mode, A/D conversion of an analog input is performed for the specified single channel a single time as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started on the selected channel.
(2) When A/D conversion completes, the result is transferred to the ADi register (i = 0 or 1) corresponding to the channel.
(3) When A/D conversion completes, the ADF bit in the ADICSR register is set to 1 (interrupt requested). Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).
(4) The ADST bit remains at 1 (A/D conversion starts) during A/D conversion. When conversion completes, the ADST bit is automatically set to 0 (A/D conversion stops) and the A/D converter enters the standby state. When the ADST bit is set to 0 during A/D conversion, A/D conversion is stopped and the A/D converter enters the standby state.

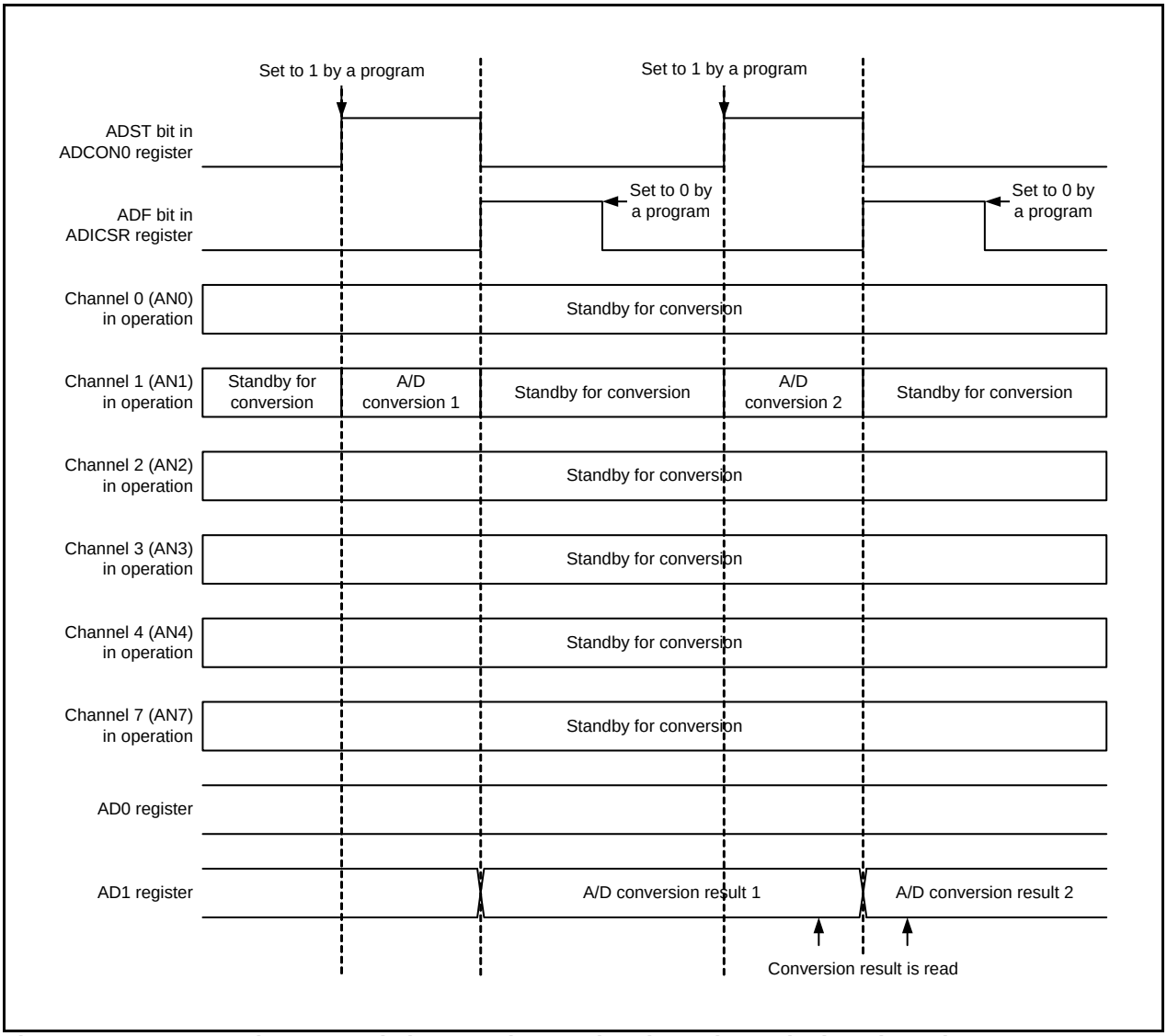
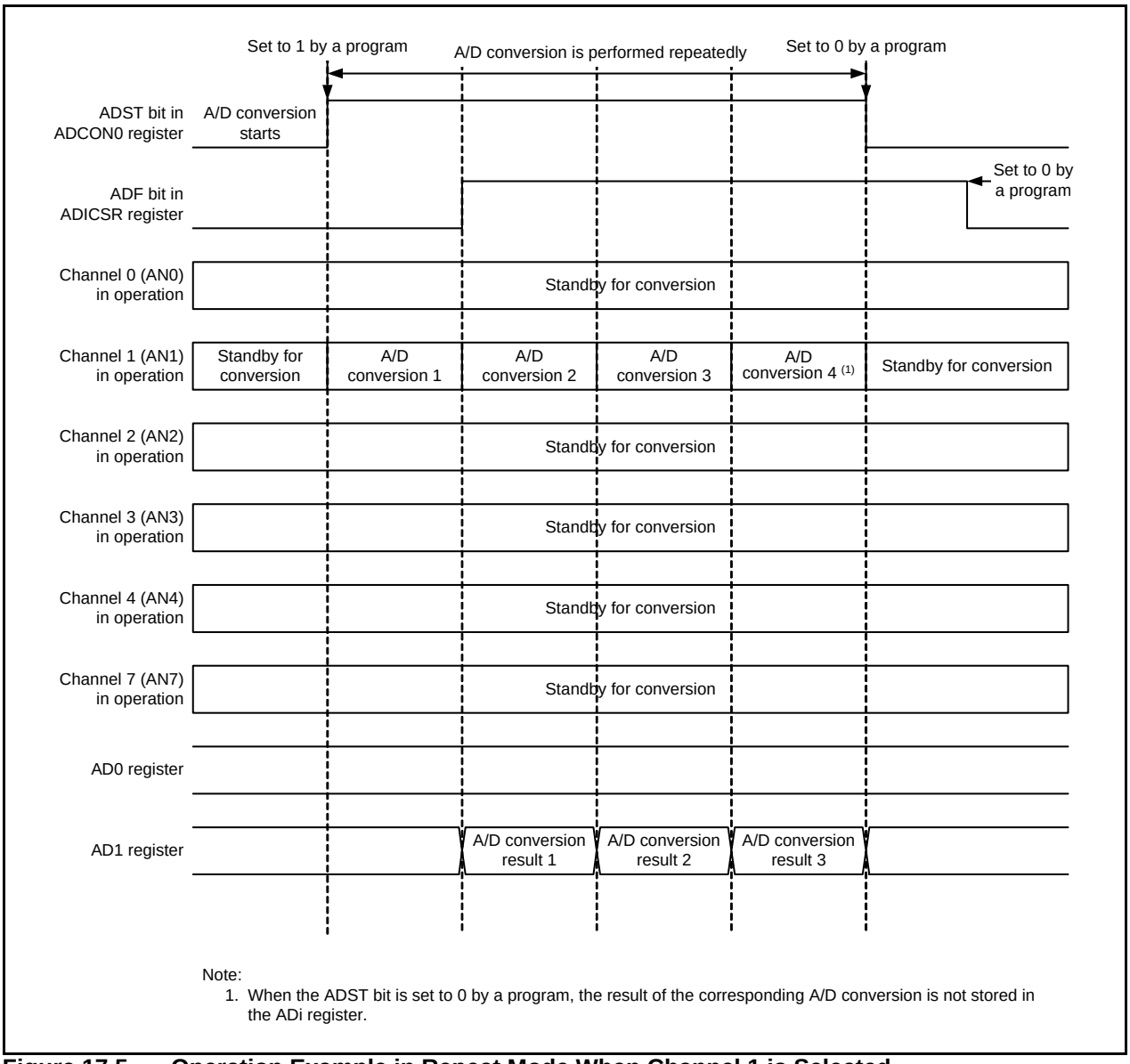


Figure 17.4 Operation Example in One-Shot Mode When Channel 1 is Selected

17.3.3 Repeat Mode

Figure 17.5 shows an Operation Example in Repeat Mode When Channel 1 is Selected.
In repeat mode, A/D conversions of an analog input are performed for the specified single channel repeatedly as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started on the selected channel.
(2) When A/D conversion completes, the result is transferred to the ADi register (i = 0 or 1) corresponding to the channel.
(3) When A/D conversion completes, the ADF bit in the ADICSR register is set to 1 (interrupt requested). Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).
(4) While the ADST bit is 1 (A/D conversion starts), steps between (2) and (3) are repeated. When the ADST bit is set to 0 (A/D conversion stops), A/D conversion is stopped and the A/D converter enters the standby state. Then, when the ADST bit is set to 1, A/D conversion is restarted on the selected channel.



Note:
1. When the ADST bit is set to 0 by a program, the result of the corresponding A/D conversion is not stored in the ADi register.

Figure 17.5 Operation Example in Repeat Mode When Channel 1 is Selected

17.3.4 Single Sweep Mode

Figure 17.6 shows an Operation Example in Single Sweep Mode When Channels 0 and 1 are Selected.
In single sweep mode, A/D conversions of the analog inputs are performed for the specified two channels a single time as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. When channel group 2 is selected, A/D conversion is started from AN4.

(2) When A/D conversion has completed on each channel, the result is transferred to the corresponding ADi register (i = 0 or 1).

(3) When A/D conversion has completed on all the selected channels, the ADF bit in the ADICSR register is set to 1 (interrupt requested).
Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).

(4) The ADST bit remains 1 (A/D conversion starts) during A/D conversion. When A/D conversion has completed on all the selected channels, the ADST bit is automatically set to 0 (A/D conversion stops) and the A/D converter enters the standby state. When the ADST bit is set to 0 during A/D conversion, A/D conversion is stopped and the A/D converter enters the standby state.

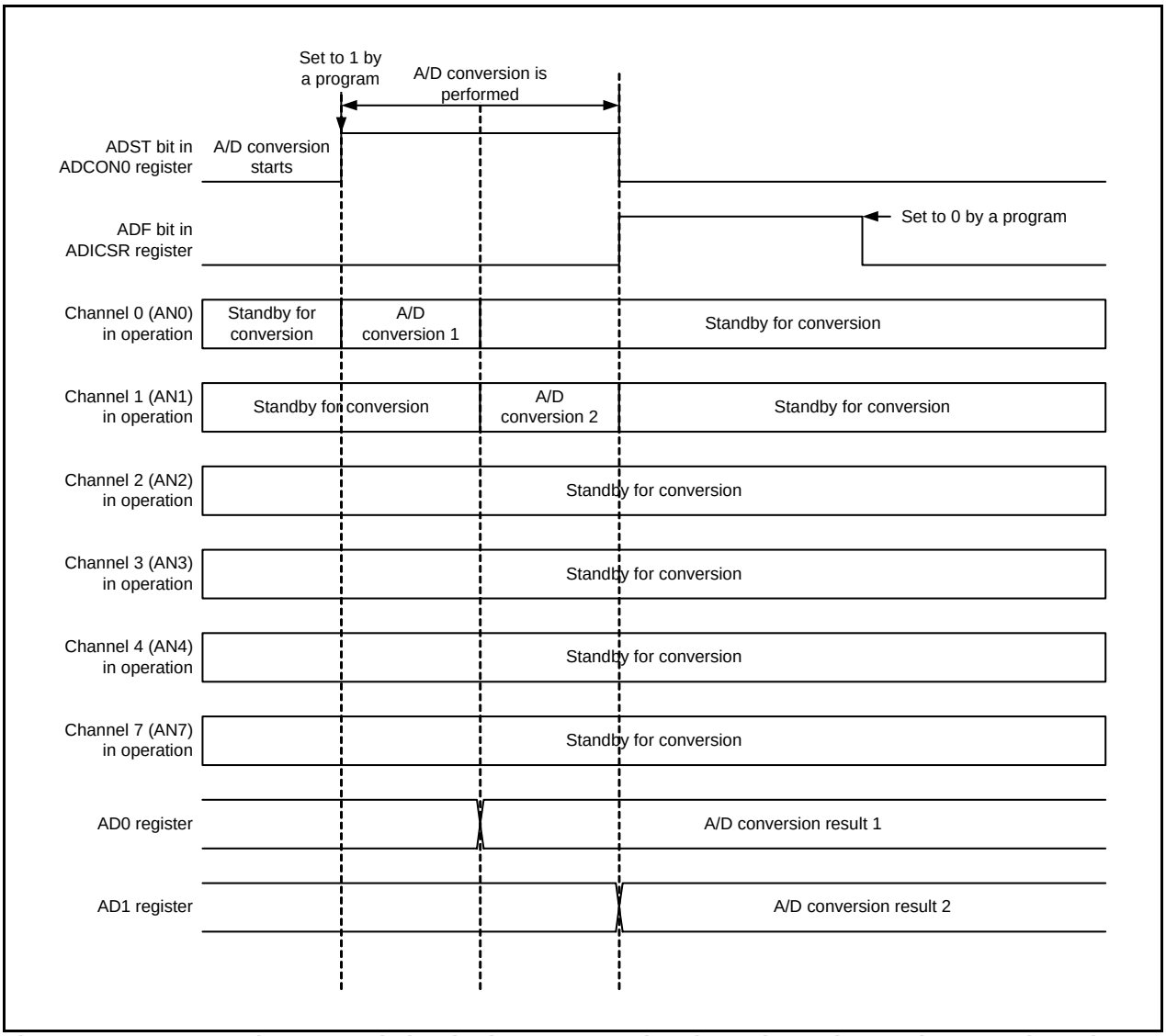


Figure 17.6 Operation Example in Single Sweep Mode When Channels 0 and 1 are Selected

17.3.5 Repeat Sweep Mode

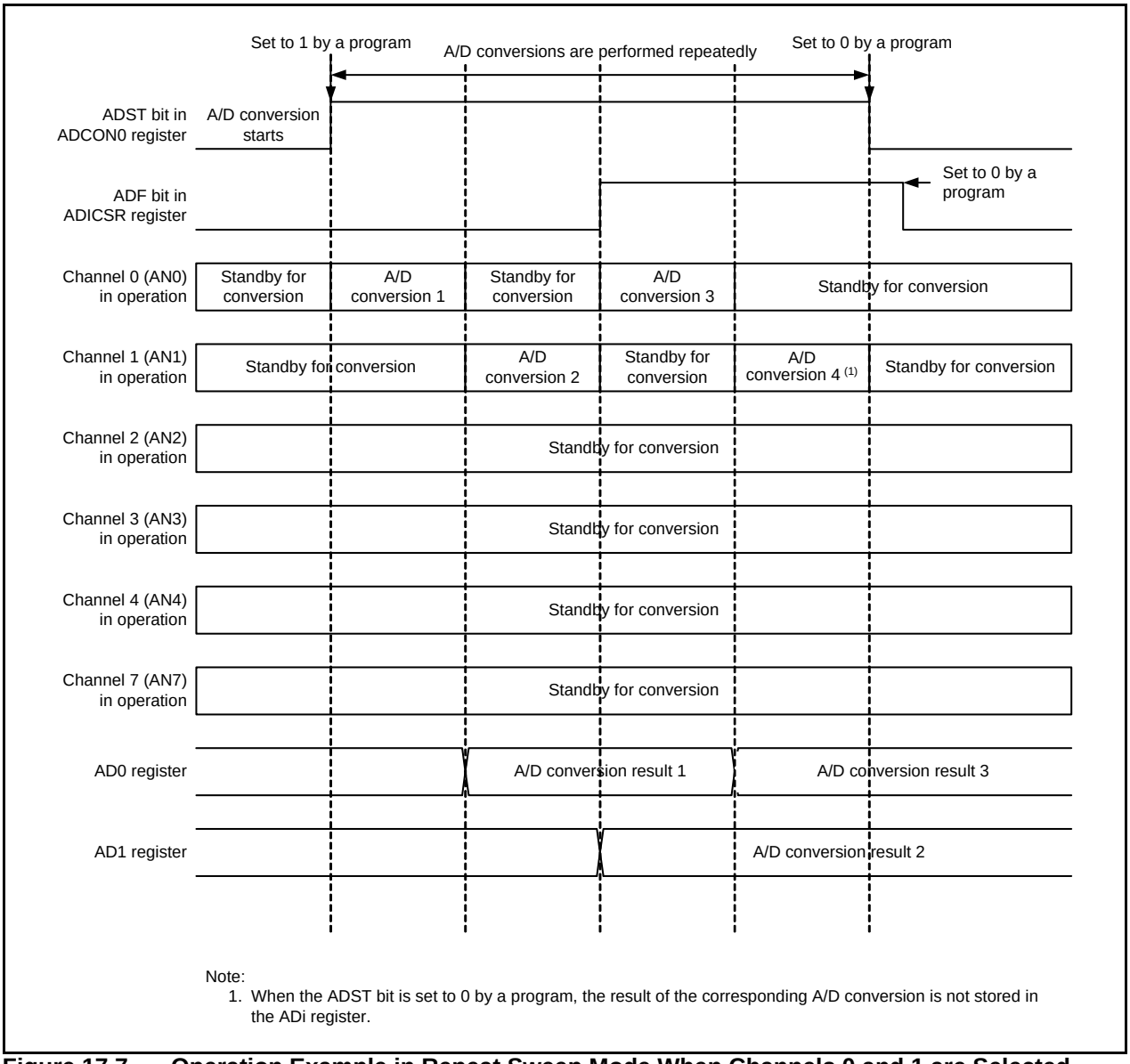
Figure 17.7 shows an Operation Example in Repeat Sweep Mode When Channels 0 and 1 are Selected.
In repeat sweep mode, A/D conversions of the analog inputs are performed for the specified two channels repeatedly as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. When channel group 2 is selected, A/D conversion is started from AN4.

(2) When A/D conversion has completed on each channel, the result is transferred to the corresponding ADi register (i = 0 or 1).

(3) When A/D conversion has completed on all the selected channels, the ADF bit in the ADICSR register is set to 1 (interrupt requested).
Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).

(4) While the ADST bit is 1 (A/D conversion starts), steps between (2) and (3) are repeated. When the ADST bit is set to 0 (A/D conversion stops), A/D conversion is stopped and the A/D converter enters the standby state. Then, when the ADST bit is set to 1, A/D conversion is restarted from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. When channel group 2 is selected, A/D conversion is started from AN4.



Note:
1. When the ADST bit is set to 0 by a program, the result of the corresponding A/D conversion is not stored in the ADi register.

Figure 17.7 Operation Example in Repeat Sweep Mode When Channels 0 and 1 are Selected

17.4 A/D Converter Interrupt

Table 17.7 lists the A/D Converter Interrupt.
When A/D conversion completes, the ADF bit in the ADICSR register is set to 1 (interrupt requested). If the ADIE bit is 1 (interrupt enabled), an A/D conversion interrupt is generated.

Table 17.7 A/D Converter Interrupt

Interrupt Source	Interrupt Name	Interrupt Flag
Completion of A/D conversion	A/D conversion interrupt	The ADF bit in the ADICSR register

17.5 Notes on A/D Converter

17.5.1 A/D Converter Standby Setting

The A/D converter can be set to standby or active using the MSTAD bit in the MSTCR register.
Stop A/D conversion before setting to module standby. Register access is enabled by clearing the A/D converter standby state. For details, see **5. System Control**.

17.5.2 Sensor Output Impedance during A/D Conversion

To perform A/D conversion accurately, charging of the internal capacitor C shown in Figure 17.8 must be completed within the period of time specified as T (sampling time). Let the output impedance of the sensor equivalent circuit be R0, the internal resistance of the microcomputer be R, the accuracy (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in 10-bit mode).

$$\text{VC is generally } VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$$

$$\text{And when } t = T,\ VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

$$\text{Hence, } R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$$

Figure 17.8 shows the Analog Input Pin and External Sensor Equivalent Circuit. The user can obtain an impedance R0 that makes the pin-to-pin voltage VC increase from 0 to VIN – (0.1/1024) VIN within time T when the difference between VIN and VC becomes 0.1 LSB. The value, (0.1/1024) indicates a precondition for the calculation of R0 when the degradation due to insufficient capacitor charge is suppressed to 0.1 LSB during A/D conversion in 10-bit mode. The actual error, however, is the absolute accuracy plus 0.1 LSB.
A/D conversion clock = 20 MHz, T = 0.8 μs. Output impedance R0 through which an capacitor C is fully charged within T is obtained as follows:

T = 0.8 μs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.8 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 4.4 \times 10^{3}$$

Thus the maximum output impedance of a sensor circuit for an accuracy (error) of 0.1 LSB or less is 4.4 kΩ maximum.

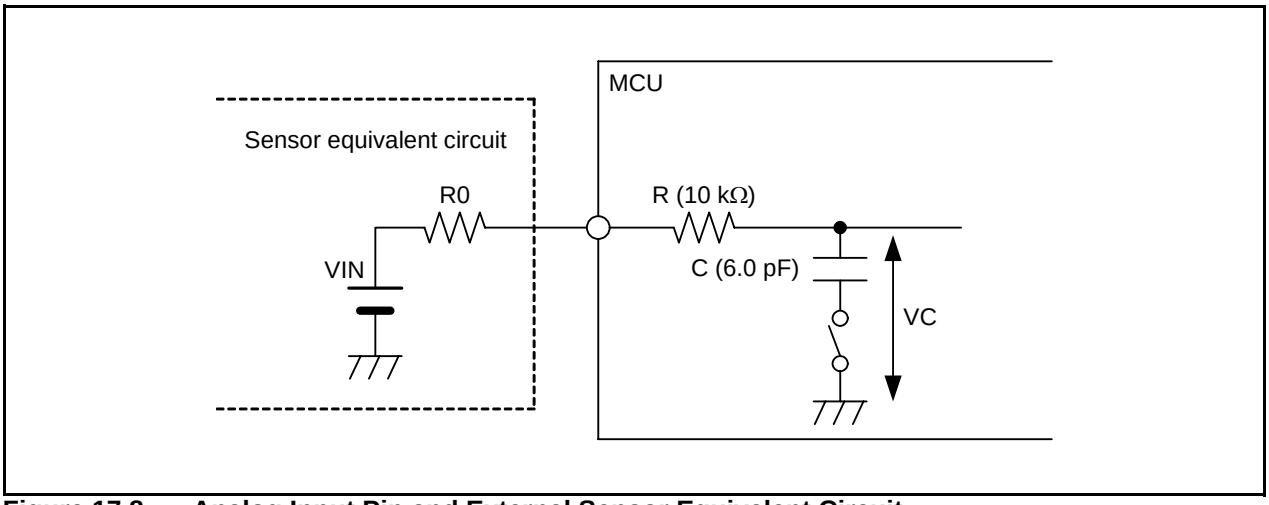


Figure 17.8 Analog Input Pin and External Sensor Equivalent Circuit

17.5.3 Register Setting

- Registers ADMOD and ADINSEL must be written only when A/D conversion is stopped.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion while the WCKSTP bit in the CKSTPR register is 1 (system clock is stopped in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) or the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) during A/D conversion.
- During A/D conversion, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate the conversion, the conversion result from the A/D converter will be undefined and no interrupt will be generated. The value of the ADi register (i = 0 or 1) which is not engaged in A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use any of the values of the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

18. Comparator B

Comparator B consists of two independent comparators, B1 and B3, which compare an analog input voltage with a reference input voltage.

18.1 Overview

The comparison result between the reference input voltage and the analog input voltage can be read by software. Table 18.1 lists the Comparator B Specifications. Figure 18.1 shows the Comparator B Block Diagram. Table 18.2 lists the Comparator B Pin Configuration.

Table 18.1 Comparator B Specifications

Item	Specification	
Input voltage	Reference input	Input from the reference pin (IVREFi)
	Analog input	Input voltage from the analog pin (IVCMPi)
Comparison result	The result can be read from the WCBiOUT bit in the WCMPR register or monitored with the VCOUTi pin.	
Interrupt request generation timing	When the comparison result changes.	
Digital filter function	• The digital filter can be enabled or disabled. • The sampling frequency can be selected (f1, f8, or f32).	

i = 1 or 3

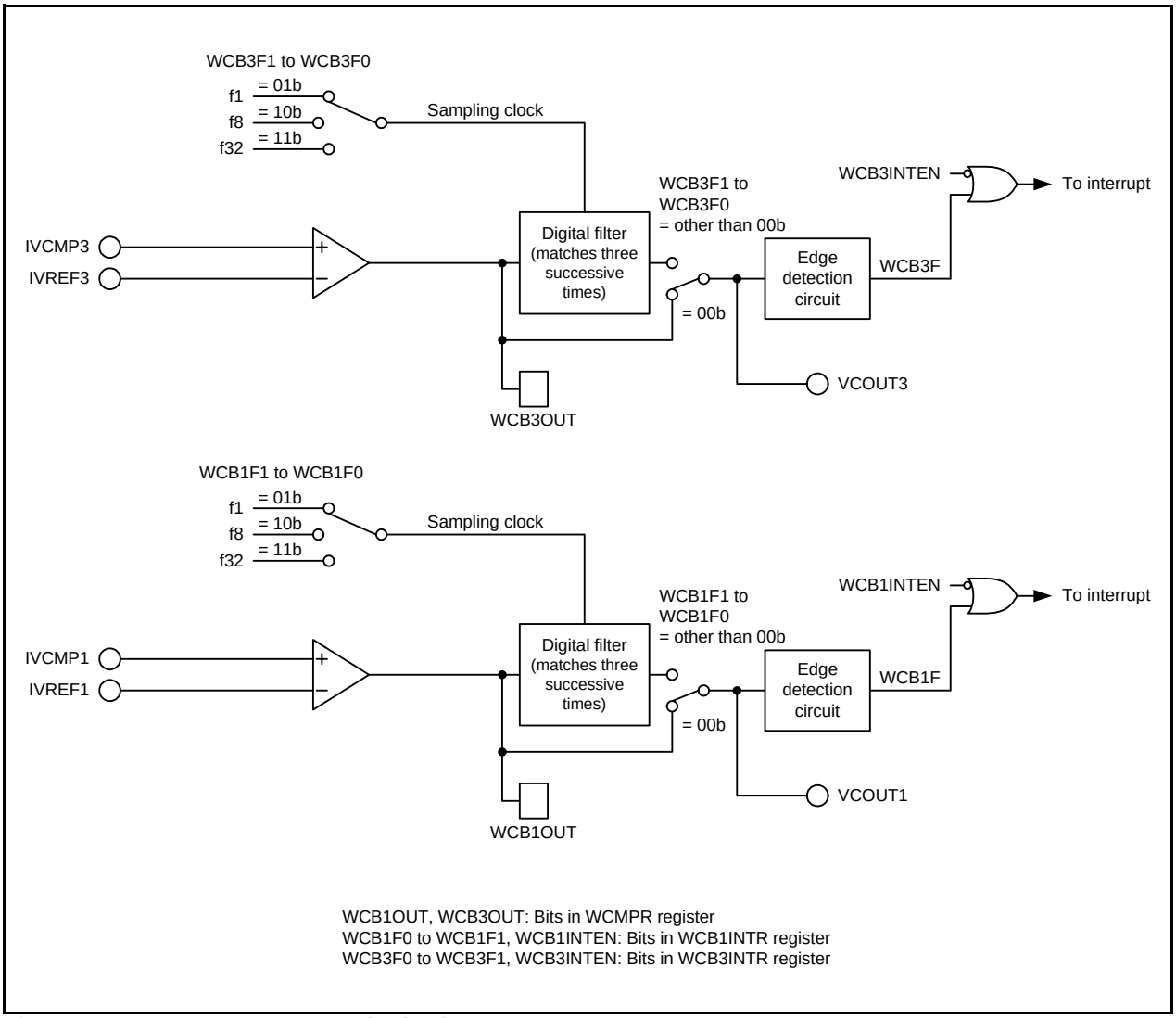


Figure 18.1 Comparator B Block Diagram

Table 18.2 Comparator B Pin Configuration

Pin Name	Assigned Pin	I/O	Function
IVCMP1	P1_7	I	Analog voltage input for comparator B1
IVREF1	P1_6	I	Reference voltage input for comparator B1
VCOUT1	P1_5 or P4_6	O	Comparison result output for comparator B1
IVCMP3	P3_3	I	Analog voltage input for comparator B3
IVREF3	P3_4	I	Reference voltage input for comparator B3
VCOUT3	P3_5	O	Comparison result output for comparator B3

Note:
1. When port P1_5 or port P4_6 is set as the VCOUT1 pin while operation of comparator B1 is disabled (WCB1M0 = 0), the initial level of the pin is set to low. When port P3_5 is set as the VCOUT3 pin while operation of comparator B3 is disabled (WCB3M0 = 0), the initial level of the pin is set to low.

18.2 Registers

Table 18.3 lists the Comparator B Register Configuration.

Table 18.3 Comparator B Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Comparator B Control Register	WCMPR	00h	00180h	8
Comparator B1 Interrupt Control Register	WCB1INTR	00h	00181h	8
Comparator B3 Interrupt Control Register	WCB3INTR	00h	00182h	8

18.2.1 Comparator B Control Register (WCMPR)

Address 00180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WCB3OUT	—	—	WCB3M0	WCB1OUT	—	—	WCB1M0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WCB1M0	Comparator B1 operation enable bit	0: Operation disabled 1: Operation enabled	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—			
b3	WCB1OUT	Comparator B1 monitor flag	0: IVCMP1 < IVREF1 or comparator B1 disabled 1: IVCMP1 > IVREF1	R
b4	WCB3M0	Comparator B3 operation enable bit	0: Operation disabled 1: Operation enabled	R/W
b5	—	Reserved	Set to 0.	R/W
b6	—			
b7	WCB3OUT	Comparator B3 monitor flag	0: IVCMP3 < IVREF3 or comparator B3 disabled 1: IVCMP3 > IVREF3	R

18.2.2 Comparator B1 Interrupt Control Register (WCB1INTR)

Address 00181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WCB1F	WCB1INTEN	WCB1S1	WCB1S0	—	—	WCB1F1	WCB1F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WCB1F0	Comparator B1 filter select bits	b1 b0 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b1	WCB1F1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	WCB1S0	Comparator B1 interrupt edge select bits	b5 b4 0 0: When the analog input voltage is lower than the reference input voltage 0 1: When the analog input voltage is higher than the reference input voltage 1 0: Do not set. 1 1: When the analog input voltage is lower or higher than the analog input voltage	R/W
b5	WCB1S1			R/W
b6	WCB1INTEN	Comparator B1 interrupt enable signal bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	WCB1F	Comparator B1 interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W

WCB1F Bit (Comparator B1 interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When an interrupt request is generated.

18.2.3 Comparator B3 Interrupt Control Register (WCB3INTR)

Address 00182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WCB3F	WCB3INTEN	WCB3S1	WCB3S0	—	—	WCB3F1	WCB3F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WCB3F0	Comparator B3 filter select bits	b1 b0 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b1	WCB3F1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	WCB3S0	Comparator B3 interrupt edge select bits	b5 b4 0 0: When the analog input voltage is lower than the reference input voltage 0 1: When the analog input voltage is higher than the reference input voltage 1 0: Do not set. 1 1: When the analog input voltage is lower or higher than the analog input voltage	R/W
b5	WCB3S1			R/W
b6	WCB3INTEN	Comparator B3 interrupt enable signal bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	WCB3F	Comparator B3 interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W

WCB3F Bit (Comparator B3 interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When an interrupt request is generated.

18.3 Operation

Comparator B1 and comparator B3 compare an input voltage from the reference voltage input pin (IVREFi) and an input voltage from the analog input voltage pin (IVCMPi) (i = 1 or 3).

18.3.1 Comparator Bi Digital Filter (i = 1 or 3)

In comparator Bi, the digital filter can be used. The sampling clock can be selected by bits WCBiF0 to WCBiF1 in the WCBiINTR register. The WCBiOUT signal output from comparator Bi is sampled on every sampling clock. When the level matches three successive times, the WCBiF bit in the WCBiINTR register is set to 1 (interrupt requested).
Figure 18.2 shows an Example of Comparator Bi Digital Filter Operation.

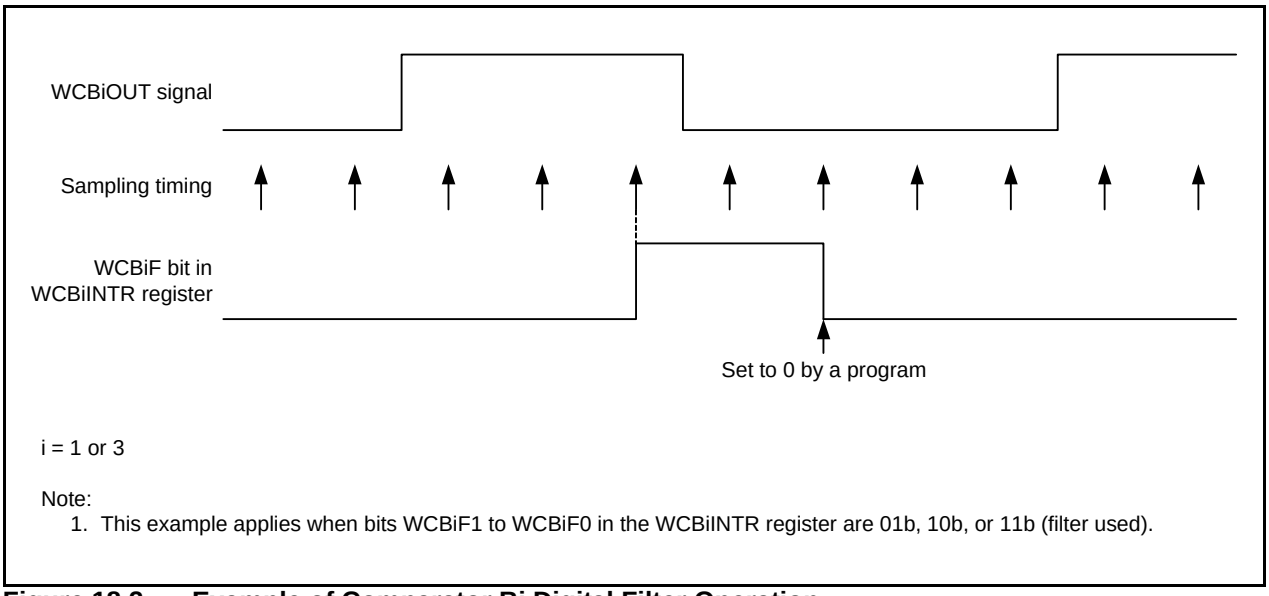


Figure 18.2 Example of Comparator Bi Digital Filter Operation

18.3.2 Comparator Bi (i = 1 or 3) Setting Procedure and Operation Example

Comparator B1 and comparator B3 operate independently of each other.
Table 18.4 lists the Procedure for Setting Registers Associated with Comparator B.

Table 18.4 Procedure for Setting Registers Associated with Comparator B

Step	Register	Bit	Setting Value
1	Select the functions of pins IVCMPi and IVREFi. For the settings, see **12. I/O Ports**.		
2	WCBiINTR	WCBiF1 to WCBiF0	• Enable or disable the digital filter. • Select the sampling frequency.
3	WCMPR	WCB1M0	1 (operation enabled)
		WCB3M0	
4	Wait for the comparator stabilization time (100 μs max.).		
5	ILVL2	ILVL21 to ILVL20	When an interrupt is used: Select the interrupt priority level for comparator B1.
		ILVL25 to ILVL24	When an interrupt is used: Select the interrupt priority level for comparator B3.
6	WCBiINTR	WCBiS1 to WCBiS0	When an interrupt is used: Select the input polarity.
7	WCBiINTR	WCBiF	0 (no interrupt requested)
8	WCBiINTR	WCBiINTEN	When an interrupt is used: 1 (interrupt enabled)

i = 1 or 3

Figure 18.3 shows an Example of Comparator Bi (i = 1 or 3) Operation.
When the analog input voltage is higher than the reference input voltage, the WCBiOUT bit in the WCMPR register is set to 1. When the analog input voltage is lower than the reference input voltage, the WCBiOUT bit is set to 0.
When a comparator Bi interrupt (i = 1 or 3) is used, set the WCBiINTEN bit in the WCBiINTR register to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bi interrupt request is generated. For details on interrupts, see **11. Interrupts**.

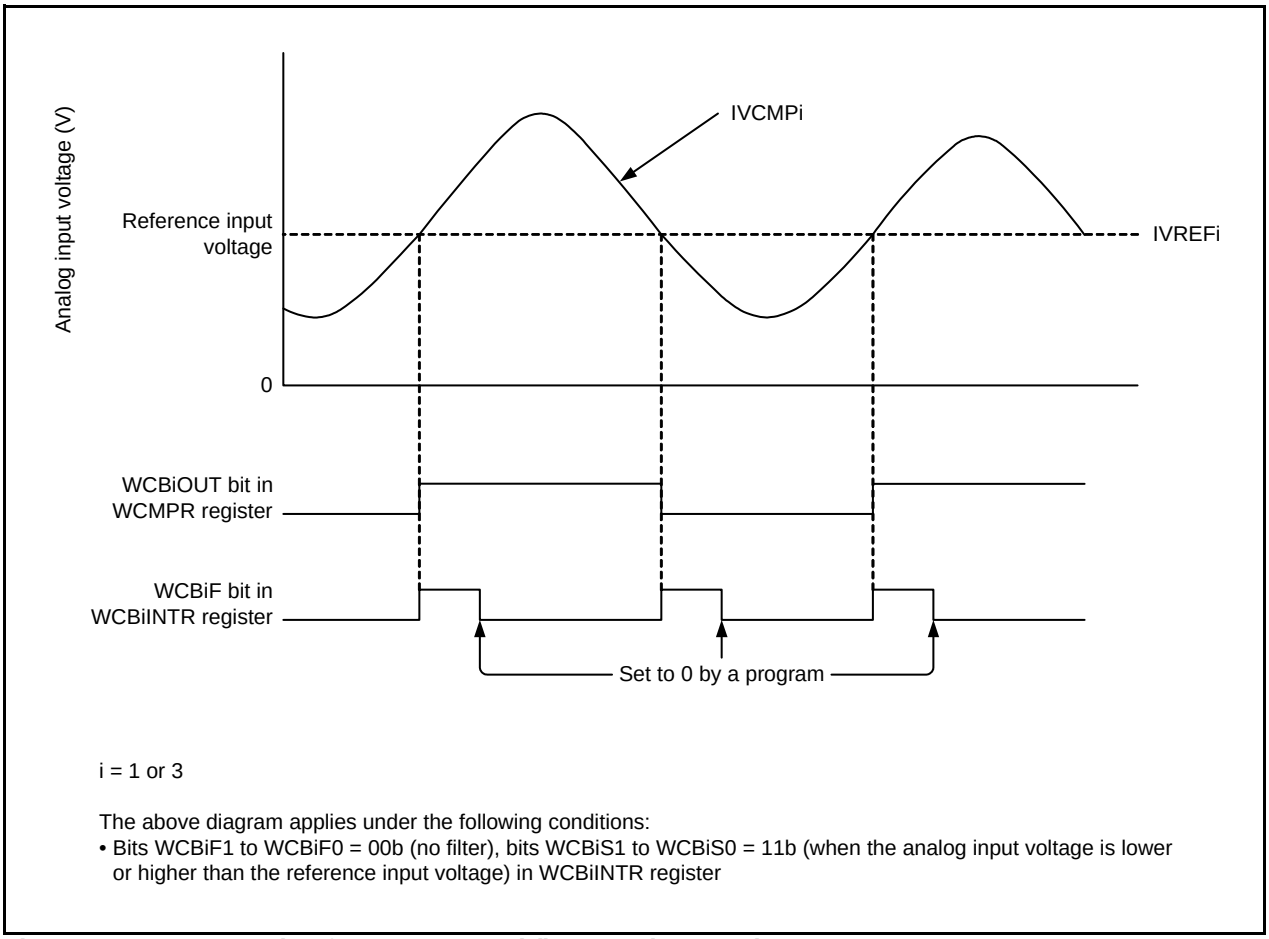


Figure 18.3 Example of Comparator Bi (i = 1 or 3) Operation

19. Flash Memory

The flash memory supports two rewrite modes: CPU rewrite mode and standard serial I/O mode.

19.1 Overview

Table 19.1 lists the Flash Memory Specifications (see **Tables 1.3** and **1.4 Specifications** for items not listed in Table 19.1). Table 19.2 outlines Flash Memory Rewrite Mode.

Table 19.1 Flash Memory Specifications

Item		Specification
Flash memory operating modes		2 modes (CPU rewrite and standard serial I/O modes)
Erase block division		See **Figure 19.1 Flash Memory Block Diagram**.
Programming method		Byte units
Erase method		Block erase
Program/erase control method (1)		Program/erase control by software commands
Rewrite control method	Blocks 1 and 2 (program ROM) (2)	Rewrite protect control in block units by lock bits
	Blocks A and B (data flash)	Individual rewrite control on blocks A and B by bits FMR16 to FMR17 in the FMR1 register
Number of commands		6 commands
Program/erase endurance (3)	Blocks 1 and 2 (program ROM) (2)	10,000 times
	Blocks A and B (data flash)	
ID code check function (4)		Standard serial I/O mode supported

Notes:
1. When programming/erasing the program ROM and the data flash, use a VCC supply voltage in the range of 1.8 V to 5.5 V.
2. The number of blocks and their division differ depending on products. For details, see **Figure 19.1 Flash Memory Block Diagram**.
3. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. When rewrites are performed 100 or more times, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used up before performing an erase operation. Avoid rewriting only particular blocks and average out the number of programming/erasure of the blocks. It is also advisable to retain data on the number of erasure of each block and limit the number to a certain extent.
4. For details on the ID code check function, see **19.3 ID Code Check Function**.

Table 19.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode
Function	The user ROM area is rewritten by executing software commands from the CPU.	The user ROM area is rewritten using a dedicated serial programmer.
Rewritable area	User ROM	User ROM
Rewrite programs	User program	Standard boot program

19.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved).
Figure 19.1 shows the Flash Memory Block Diagram.
The user ROM area contains program ROM and data flash.
• Program ROM: Flash memory mainly used for storing programs
• Data flash: Flash memory mainly used for storing data to be rewritten
The user ROM area is divided into several blocks.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area when the MCU is shipped. The boot ROM area is allocated separately from the user ROM area.

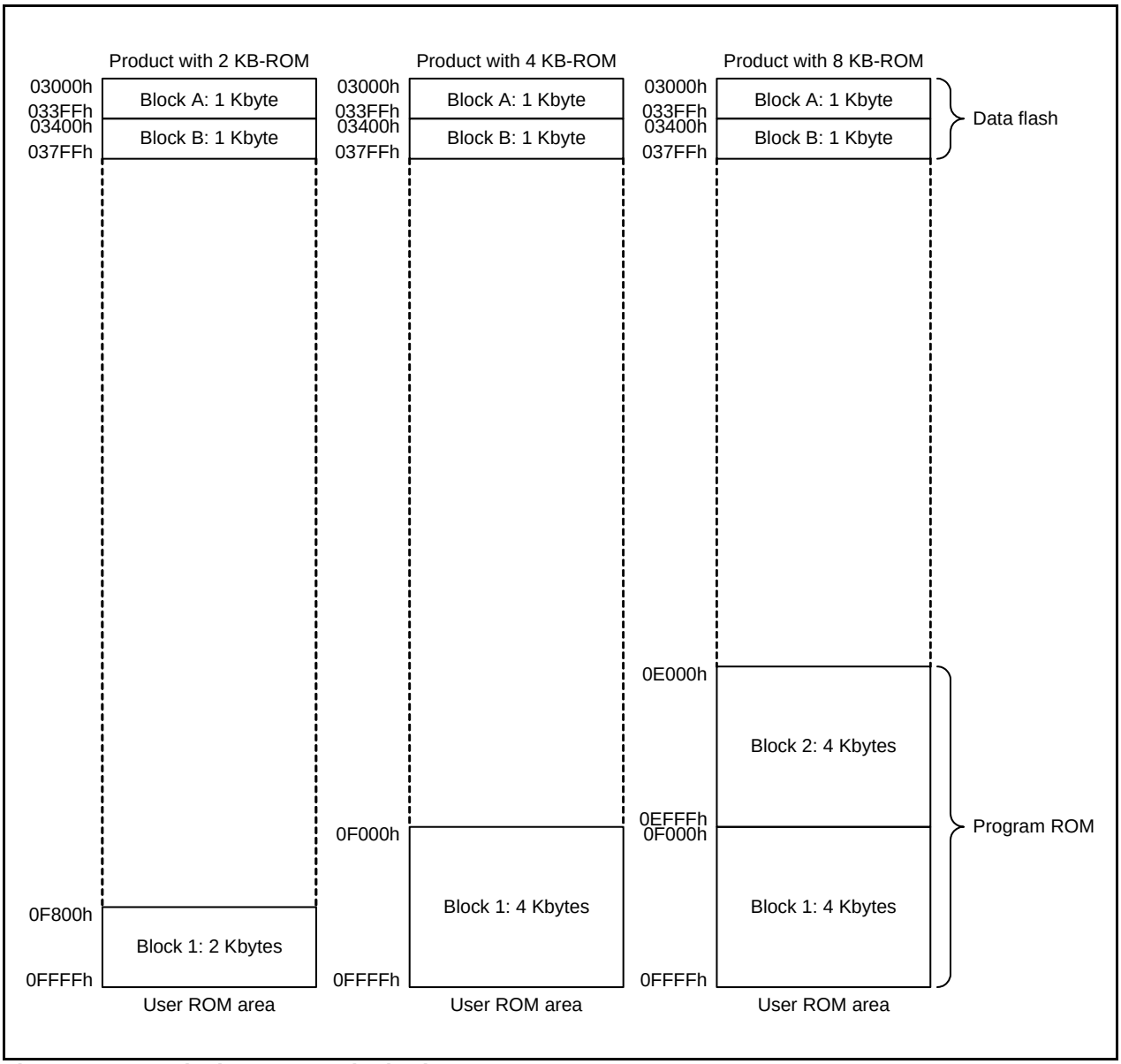


Figure 19.1 Flash Memory Block Diagram

19.3 ID Code Check Function

The ID code check function prevents the flash memory from being read, rewritten, or erased when standard serial I/O mode is used. This function is implemented by checking the ID codes written in the ID code area.
The ID code area is assigned to certain of the highest addresses for each vector in the fixed vector table, 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Figure 19.2 shows the ID Code Area.

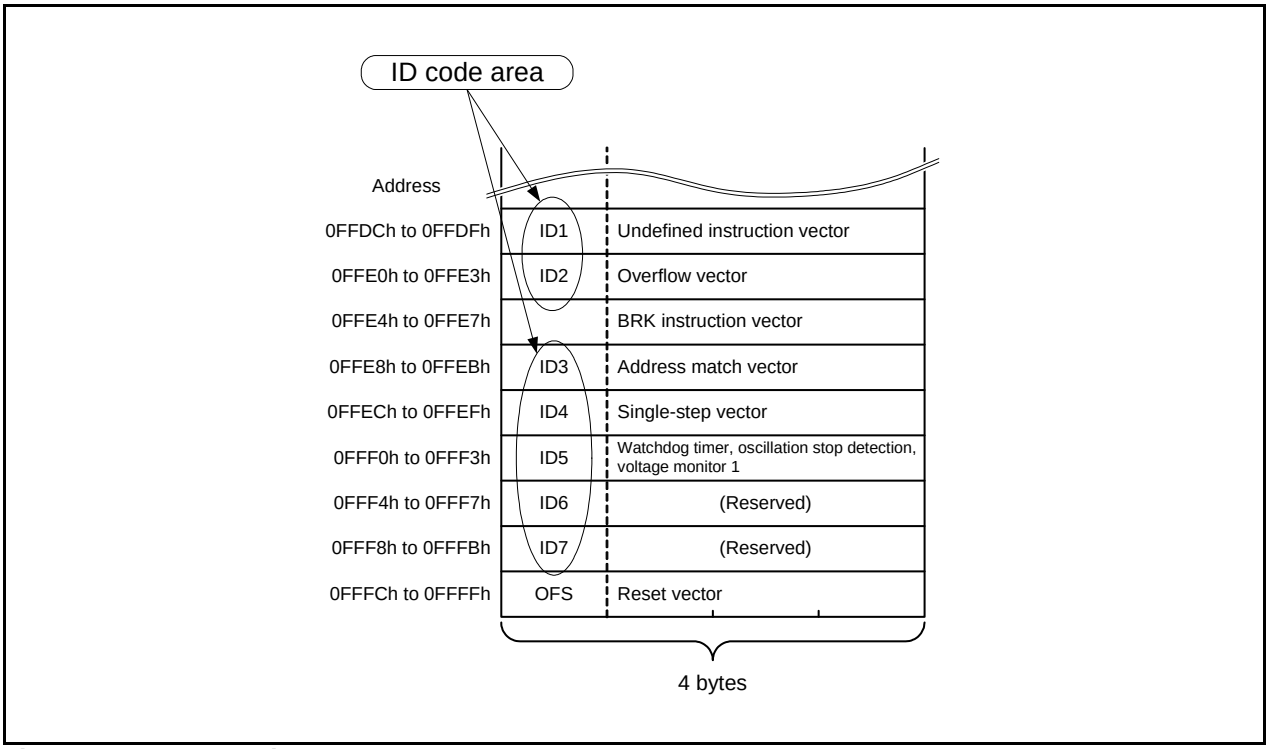


Figure 19.2 ID Code Area

19.3.1 Operation

The ID code check function is used in standard serial I/O mode. Its operation differs depending on whether the three bytes in the reset vector at addresses 0FFFCh to 0FFFEh are FFFFFFh or not.
If the value is FFFFFFh, the ID codes are not examined and all commands are accepted.
If the value is not FFFFFFh, the ID codes stored in the ID code area (stored ID code) and those sent from the serial programmer or the on-chip debugging emulator are examined to see whether they match. If they match, the commands are accepted. Otherwise, the commands are not accepted. To use the serial programmer or the on-chip debugging emulator, write predetermined ID codes, in advance, to the ID code area. In addition to the reserved word (see **19.3.2 Reserved Words**), any ID codes can be used.

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

19.3.2 Reserved Words

The ID code with the character combination “ALeRASE” in ASCII is the reserved word for the forced erase function. The ID code “Protect” is the reserved word for the standard serial I/O mode disabled function. Table 19.3 lists the ID Code Reserved Words. When the combination of ID codes and addresses match those listed in Table 19.3, respectively, the ID codes forms the reserved word. When the forced erase function or standard serial I/O mode disabled function is not used, use another combination of ID codes.

Table 19.3 ID Code Reserved Words

ID Code Storage Address		Reserved Word of ID Code (ASCII) (1)	
		ALeRASE (forced erase function)	Protect (standard serial I/O mode disabled function)
0FFDFh	ID1	41h: A (upper-case)	50h: P (upper-case)
0FFE3h	ID2	4Ch: L (upper-case)	72h: r (lower-case)
0FFEBh	ID3	65h: e (lower-case)	6Fh: o (lower-case)
0FFEFh	ID4	52h: R (upper-case)	74h: t (lower-case)
0FFF3h	ID5	41h: A (upper-case)	65h: e (lower-case)
0FFF7h	ID6	53h: S (upper-case)	63h: c (lower-case)
0FFFBh	ID7	45h: E (upper-case)	74h: t (lower-case)

Note:
1. When the combination of ID codes and addresses match those listed in Table 19.3 respectively, the set of characters forms the corresponding reserved word.

19.3.2.1 Forced Erase Function

This function is used in standard serial I/O mode. When the sent ID codes are “ALeRASE” in ASCII and the stored ID codes are the same, the entire data in the user ROM area will be erased (forced erase). Even if the stored ID codes are other than “ALeRASE” (see **Table 19.3 ID Code Reserved Words**), the entire data in the user ROM area will be erased if bits ROMCP1 to ROMCR in the OFS register are any value other than 01b (ROM code protect disabled). If the stored ID codes are any value other than “ALeRASE” (see **Table 19.3 ID Code Reserved Words**) and when bits ROMCP1 to ROMCR in the OFS register are 01b (ROM code protect enabled), a forced erase is not performed and the ID codes are examined with the ID code check function.
Table 19.4 lists the Conditions and Operations of Forced Erase Function.

Also, when the stored ID codes are set to “ALeRASE” in ASCII, if the sent ID codes are “ALeRASE”, the data in the user ROM area will be erased. If the sent ID codes are any value other than “ALeRASE”, the ID codes do not match and no command is accepted, thus the user ROM area remains protected.

Table 19.4 Conditions and Operations of Forced Erase Function

Condition			Operation
ID Code from Serial Programmer or On-Chip Debugging Emulator	ID Code in ID Code Storage Address	Bits ROMCP1 to ROMCR in OFS Register	
ALeRASE	ALeRASE	—	Erasure of the whole user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code examination (ID code check function)
Other than ALeRASE	ALeRASE	—	ID code examination (ID code check function. No ID code match.)
	Other than ALeRASE (1)	—	ID code examination (ID code check function)

Note:
1. See **19.3.2.2 Standard Serial I/O Mode Disabled Function** for the case where the ID codes are “Protect”.

19.3.2.2 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the stored ID codes are “Protect” in ASCII (see **Table 19.3 ID Code Reserved Words**), no communication with the serial programmer or the on-chip debugging emulator is performed. This prevents the flash memory from being read, written, or erased using the serial programmer or the on-chip debugging emulator.

If the stored ID codes are set to “Protect” in ASCII when bits ROMCP1 to ROMCR in the OFS register are 01b (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, written, or erased using the serial programmer or the on-chip debugging emulator.

19.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly with the MCU mounted on a board without using a ROM programmer. Software commands should be executed only for blocks in the user ROM area.
The MCU has a suspend function (program-suspend, erase-suspend) which halts erase or program operation temporarily in CPU rewrite mode. During suspend, the flash memory can be read and the read lock bit status command can be sent. For erase-suspend only, the flash memory can be programmed and the read lock bit status is enabled. For program-suspend only, the read lock bit status of the flash memory is enabled.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 19.5 lists the Differences between EW0 Mode and EW1 Mode.

Table 19.5 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	User mode	User mode
Area where rewrite control program can be allocated	User ROM	User ROM
Areas where rewrite control program can be executed	RAM (The rewrite control program must be transferred before being executed.)	User ROM or RAM
Rewritable area	User ROM	User ROM (Other than blocks which contain the rewrite control program.)
Software command restrictions	—	Program and block erase commands cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering suspend	Read array mode	Read array mode
CPU state during programming/block erase	The CPU operates.	The CPU is put in the hold state. (I/O ports retain the states before the command is executed.)
Flash memory status detection	Read bits FST2 to FST7 in the FST register by a program.	Read bits FST2 to FST7 in the FST register by a program.
Conditions for entering erase/program-suspend	• Set bits FMR20 to FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	Max. 20 MHz	Max. 20 MHz

19.5 Registers (CPU Rewrite Mode)

Table 19.6 lists the Flash Memory Register Configuration.

Table 19.6 Flash Memory Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Flash Memory Status Register	FST	10000000b	001A9h	8
Flash Memory Control Register 0	FMR0	00h	001AAh	8
Flash Memory Control Register 1	FMR1	00h	001ABh	8
Flash Memory Control Register 2	FMR2	00h	001ACh	8
Flash Memory Refresh Control Register	FREFR	00h	001ADh	8

19.5.1 Flash Memory Status Register (FST)

Address 001A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	FST3	FST2	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt requested 1: Flash ready status interrupt requested	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt requested 1: Flash access error interrupt requested	R/W
b2	FST2	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	FST3	Program-suspend status flag	0: Program not suspended 1: Program suspended	R
b4	FST4	Program error status flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error status flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Erase not suspended 1: Erase suspended	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt requested) by a program.
   Read this bit (dummy read) before writing 0 (no flash ready status interrupt requested) to the RDYSTI bit.
   To check this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt requested) by a program.
   Read this bit (dummy read) before writing 0 (no flash access error interrupt requested) to the BSYAEI bit.
   To check this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command sequence error occurs.
4. When this bit is 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash ready status interrupt request flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erase completes, or suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt requested).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt requested).

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• If the flash memory status transits from busy to ready when the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt request enabled).

The status changes from busy to ready in the following states:
• Completion of programming/erasing the flash memory
• Suspend acknowledgement
• Completion of forced termination
• Completion of the lock bit program
• Completion of the read lock bit status
• Completion of the block blank check
• When the flash memory can be read after it has been activated from disabling flash memory stop.

BSYAEI Bit (Flash access error interrupt request flag)

The BSYAEI bit is set to 1 (flash access error interrupt requested) if the user ROM area is read or written while the flash memory is busy when the BSYAEIE bit in the FMR0 register is 1 (flash access error interrupt enabled). The BSYAEI bit is also set to 1 if a block erase error, program error, block blank check error, command sequence error, or lock bit program error occurs when the CMDERIE bit in the FMR0 register is 1 (interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt requested).

[Conditions for setting to 0]
• When 0 is written to this bit after reading it as 1.
• When the clear status register command is executed.
[Conditions for setting to 1]
• If the user ROM area is read or written while the flash memory is busy when the BSYAEIE bit in the FMR0 register is 1 (flash access error interrupt enabled).
(Note that the read value is undefined. Writing has no effect.)
• If a block erase error, program error, block blank check error, command sequence error, or lock bit program error occurs when the CMDERIE bit in the FMR0 register is 1 (interrupt enabled).

FST2 Bit (LBDATA monitor flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and then read the FST2 bit after the FST7 bit is set to 1 (ready).
This bit is updated when the program, erase, and read lock bit status commands are generated. When the read lock bit status command is input, the FST7 bit is set to 0 (busy). When the FST7 bit is set to 1 (ready), the lock bit status is stored in the FST2 bit. The data in the FST2 bit is retained until the next command is input.

FST3 Bit (Program-suspend status flag)

This is a read-only bit indicating the suspend status. This bit is set to 1 when a program-suspend request is acknowledged and a program-suspend status is entered; otherwise it is set to 0.

FST4 Bit (Program error status flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise it is set to 0. For details, see the description in **19.6.7 Full Status Check**.

FST5 Bit (Erase error/blank check error status flag)

This is a read-only bit indicating the status of auto-erase or block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise it is set to 0. For details, see the description in **19.6.7 Full Status Check**.

FST6 Bit (Erase-suspend status flag)

This is a read-only bit indicating the suspend status. This bit is set to 1 when an erase-suspend request is acknowledged and an erase-suspend status is entered; otherwise it is set to 0.

FST7 Bit (Ready/busy status flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:
• During programming
• During erasure
• During the lock bit program
• During the read lock bit status
• During the block blank check
• During forced stop operation
• The flash memory is being stopped
• The flash memory is being activated
Otherwise, the FST7 bit is set to 1 (ready).

19.5.2 Flash Memory Control Register 0 (FMR0)

Address 001AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1, 5)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory is stopped	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	0: No erase/write sequence reset 1: Erase/write sequence reset	R/W
b5	CMDERIE	Erase/write error, blank check error, command sequence error interrupt enable bit	Erase/write error, blank check error, command sequence error 0: Interrupt disabled 1: Interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit (5)	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit (5)	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. Only write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is 1 (CPU rewrite mode enabled). Set the FMSTP bit to 1 (flash memory is stopped) when the FST7 bit in the FST register is 1 (ready).
3. The CMDRST bit can be set when the FMR01 bit is 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is 0 (busy).
4. Set the FMR01 bit to 0 (CPU rewrite mode disabled) only when the RDYSTI bit in the FST register is 0 (no flash ready status interrupt requested) and the BSYAEI bit is 0 (no flash access error interrupt requested).
5. This bit is set to 0 when the FMR01 bit is 0 (CPU rewrite mode disabled).

FMR01 Bit (CPU rewrite mode select bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 mode select bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash memory stop bit)

This bit is used to initialize the control circuits and to reduce the amount of current consumed in the flash memory. When the FMSTP bit is set to 1 (flash memory is stopped), the flash memory cannot be accessed. Therefore, only write to the FMSTP bit by a program transferred to the RAM.

To reduce the power consumption further in high-speed on-chip oscillator mode and low-speed on-chip oscillator mode (XIN clock is stopped), set the FMSTP bit to 1 (flash memory is stopped). Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) during A/D conversion.

Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory is stopped).

For details on the setting of this bit, see **10.5.10 Stopping Flash Memory**.

CMDRST Bit (Erase/write sequence reset bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or block erase command.
If the program or block erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erase command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly terminated and reading from the flash memory is enabled.

CMDERIE Bit (Erase/write error, blank check error, command sequence error interrupt enable bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:
• Program error
• Block erase error
• Command sequence error
• Block blank check error
• Lock bit program error
When the CMDERIE bit is set to 1 (interrupt enabled), an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.
To change the CMDERIE bit from 0 (interrupt disabled) to 1 (interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash access error interrupt enable bit)

This bit enables flash access error interrupt generation if the flash memory being rewritten is accessed.
To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), follow the steps below:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt requested) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash ready status interrupt enable bit)

This bit enables flash ready status interrupt generation when the status of the flash memory sequence changes from busy to ready.
To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), follow the steps below:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt requested) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

19.5.3 Flash Memory Control Register 1 (FMR1)

Address 001ABh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR17	FMR16	—	—	FMR13	WTFMSTP	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	WTFMSTP	Flash memory stop bit in wait mode	0: Flash memory operates in wait mode 1: Flash memory is stopped in wait mode	R/W
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	FMR16	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software commands acceptable) 1: Rewrite disabled (software commands not acceptable, no error occurred)	R/W
b7	FMR17	Data flash block B rewrite disable bit (2, 3)		R/W

Notes:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. To set this bit to 0, first write 1 and then write 0 immediately. Interrupts must be disabled between writing 1 and then writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

WTFMSTP Bit (Flash memory stop bit in wait mode)

When the WTFMSTP bit is 1 (flash memory is stopped in wait mode), the flash memory is stopped when wait mode is entered. To perform A/D conversion in wait mode, set the WTFMSTP bit to 0 (flash memory operates in wait mode).

FMR13 Bit (Lock bit disable select bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. For details on the lock bit, see **19.6.5 Data Protect Function**.
The FMR13 bit is used to enable the lock bit function only and the lock bit data remains unchanged. However, when a block erase command is executed while the FMR13 bit is 1 (lock bit disabled), the lock bit data set to 0 (lock bit enabled) is changed to 1 (lock bit disabled) after erase completes.

[Conditions for setting to 0]
- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and the program/erase command completes.
- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and program-suspend/erase-suspend is entered.
- When a command sequence error occurs.
- When the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- When the FMSTP bit in the FMR0 register is set to 1 (flash memory is stopped).
- When the CMDRST bit in the FMR0 register is set to 1 (erase/write sequence reset).

[Condition for setting to 1]
- When 1 is written to this bit by a program.

FMR16 Bit (Data flash block A rewrite disable bit)

When the FMR16 bit is set to 0, data flash block A accepts program and block erase commands.

FMR17 Bit (Data flash block B rewrite disable bit)

When the FMR17 bit is set to 0, data flash block B accepts program and block erase commands.

19.5.4 Flash Memory Control Register 2 (FMR2)

Address 001ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Suspend enable bit (1)	0: Suspend disabled 1: Suspend enabled	R/W
b1	FMR21	Suspend request bit (2)	0: Restart 1: Suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Suspend request disabled by interrupt request 1: Suspend request enabled by interrupt request	R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	FMR27	Low-current-consumption read mode enable bit (1, 3)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. The FMR21 bit can be set when the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMR20 bit is 1 (suspend enabled).
3. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU write mode disabled). Set this bit to 0 to perform A/D conversion.

FMR20 Bit (Suspend enable bit)

When the FMR20 bit is set to 1 (enabled), the suspend function is enabled.

FMR21 Bit (Suspend request bit)

When the FMR21 bit is set to 1 (suspend request), program/erase-suspend mode is entered. When the FMR22 bit is 1 (suspend request enabled by interrupt request), if an interrupt request for the enabled interrupt is generated, the FMR21 bit is automatically set to 1 (suspend request) and suspend mode is entered. To restart auto-erase or auto-programming, set the FMR21 bit to 0 (restart).

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Conditions for setting to 1]
- When the FMR22 bit is 1 (suspend request enabled by interrupt request) at the time an interrupt request is generated.
- When 1 is written to this bit by a program while the flash memory is busy.

FMR22 Bit (Interrupt request suspend request enable bit)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) at the time an interrupt request is generated during auto-erase or auto-programming. Set the FMR22 bit to 1 when erase-suspend is used while the user ROM area is rewritten in EW1 mode.

FMR27 Bit (Low-current-consumption read mode enable bit)

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **10.5.11 Low-Current-Consumption Read Mode** for details.

When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-current-consumption read mode.

After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

19.5.5 Flash Memory Refresh Control Register (FREFR)

Address 001ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	REF5	REF4	REF3	REF2	REF1	REF0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	REF0	Periodic refresh interval control bits	Value in the FREFR register = fs/10^3 (the result value is expressed as an integer) If the clock source for the CPU clock (fs) is the low-speed on-chip oscillator, it is taken to be the minimum fLOCO value (60 kHz). Ex: Value set in the FREFR register when the CPU clock (fs) is set to 12.5 kHz: (12.5 × 10^3/10^3) = 12 = 001100b	R/W
b1	REF1			R/W
b2	REF2			R/W
b3	REF3			R/W
b4	REF4			R/W
b5	REF5			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The FREFR register is used to control the interval between refresh operations when the FMR27 bit in the FMR2 register is 1 (low-current-consumption read mode enabled). First set the FMR27 bit in the FMR2 register to 0 (low-current-consumption read mode disabled) to set the value in the register. After that, set the FMR27 bit to 1 (low-current-consumption read mode enabled).

19.6 CPU Rewrite Mode

Each mode is described as below.

19.6.1 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), CPU rewrite mode is entered and software commands are accepted. Since the FMR02 bit in the FMR0 register is 0 at this time, EW0 mode is selected.

Software commands are used to control programming/erase. The FST register can be used to confirm the status when programming/erase is completed.

To enter suspend during auto-erase or auto-programming, set the FMR20 bit to 1 (suspend enabled) and the FMR21 bit to 1 (suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST3 bit is set to 1 (during program-suspend) or the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST3 bit is set to 0, programming completes. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (restart), auto-erase or auto-programming is restarted. To confirm whether auto-programming or auto-erase has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST3 bit is set to 0 (other than program-suspend) or the FST6 bit is set to 0 (other than erase-suspend).

19.6.2 EW1 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled) and then the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected. The FST register can be used to confirm the status when programming/erase is completed.

To enable the suspend function during auto-erase or auto-programming, set the FMR20 bit in the FMR2 register to 1 (suspend enabled) and the FMR22 bit to 1 (suspend request enabled by interrupt request) and then execute the block program/erase command. The interrupt to enter suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (suspend request) and auto-erase or auto-programming is suspended after td(SR-SUS). Set the FMR21 bit to 0 (restart) to restart auto-erase or auto-programming after interrupt handling is completed.

19.6.3 Suspend Operation

The erase-suspend function temporarily halts the auto-erase during the operation.
The program suspend function temporarily halts the auto-programming during the operation.
When auto-erase or auto-programming is suspended, the following operation can be executed (see **Table 19.7 Executable Operation during Suspend**).

- When auto-erase of any block in the user ROM is suspended, auto-programming and reading of another block in the user ROM can be executed.
- When auto-programming of any block in the user ROM is suspended, reading of another block in the user ROM can be executed.

Table 19.7 Executable Operation during Suspend

		Operation during Suspend							
		Block where erase or program operation is executed before entering suspend				Block where erase or program operation is not yet executed before entering suspend			
		Erase	Program	Read lock bit status	Read	Erase	Program	Read lock bit status	Read
Command in execution	Erase	No	No	No	No	No	Yes	Yes	Yes
	Program	No	No	No	No	No	No	Yes	Yes

Notes:
1. “Yes” indicates operation is possible by using the suspend function and “No” indicates operation is disabled.
2. The block erase command can be executed for erasure. The program and lock bit program commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The block blank check operation is disabled during suspend.
3. The MCU enters read array mode immediately after entering suspend.

Figure 19.3 shows the Timing for Erase-Suspend Operation. Figure 19.4 shows the Timing for Program-Suspend Operation.

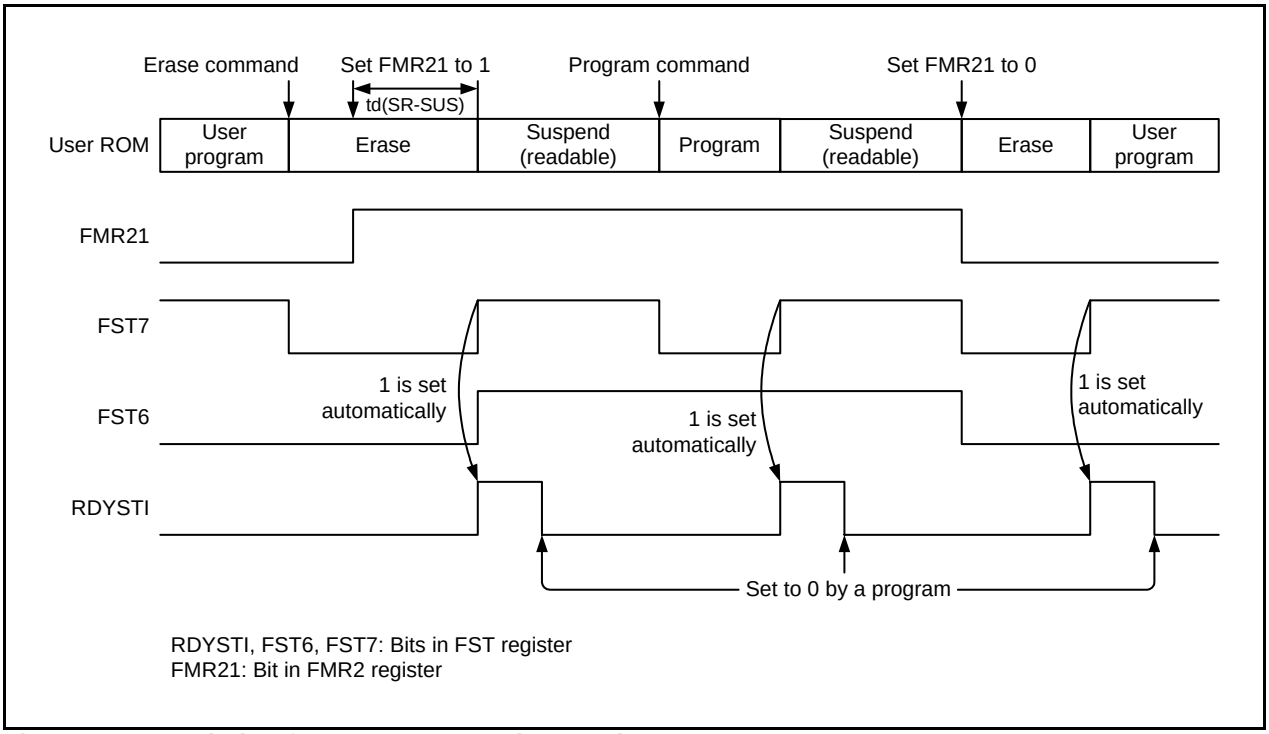


Figure 19.3 Timing for Erase-Suspend Operation

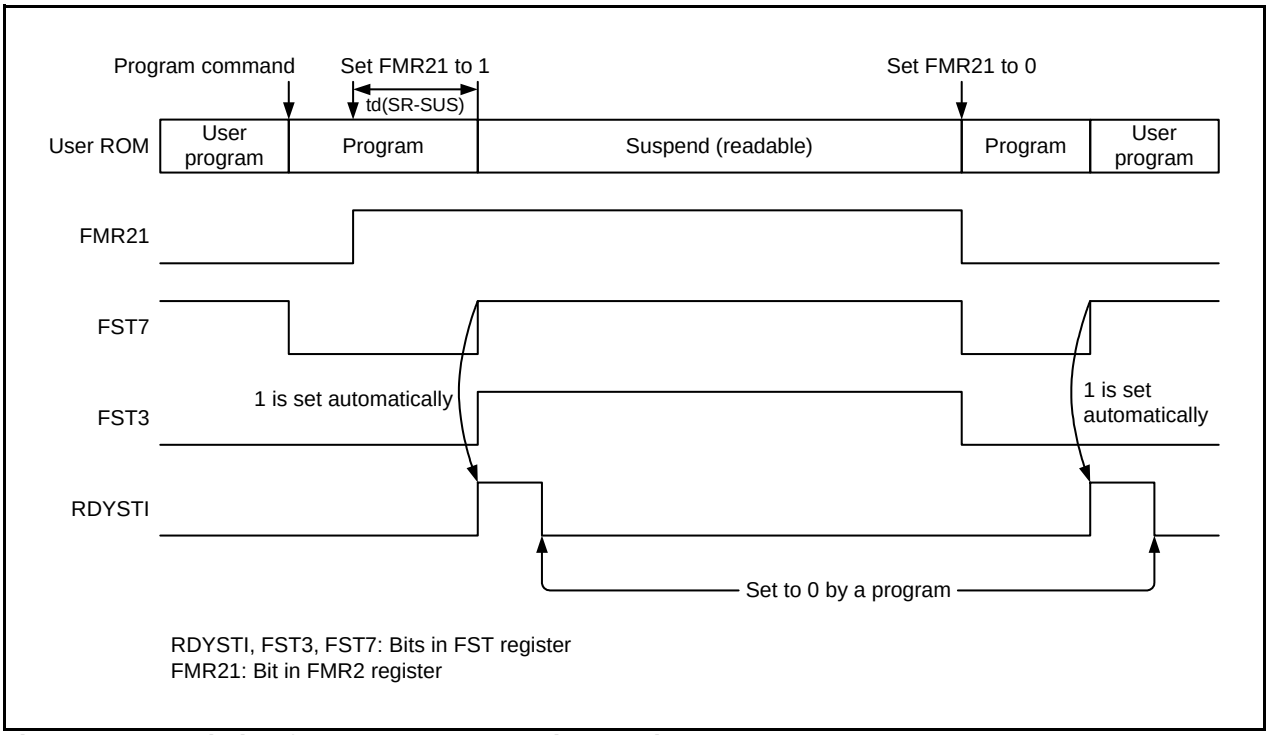


Figure 19.4 Timing for Program-Suspend Operation

19.6.4 Setting and Cancelling Each Mode

Figure 19.5 shows Setting and Cancelling EW0 Mode. Figure 19.6 shows Setting and Cancelling EW1 Mode.

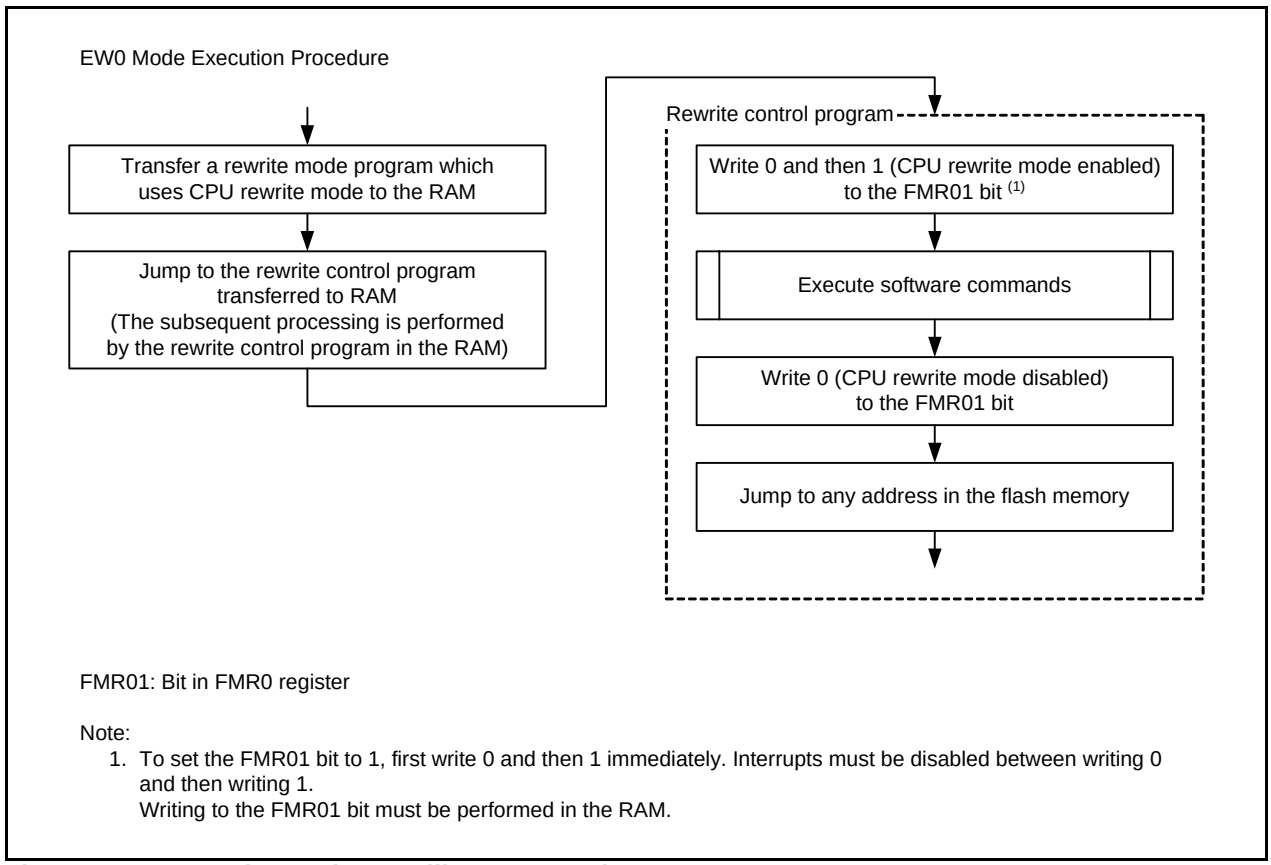


Figure 19.5 Setting and Cancelling EW0 Mode

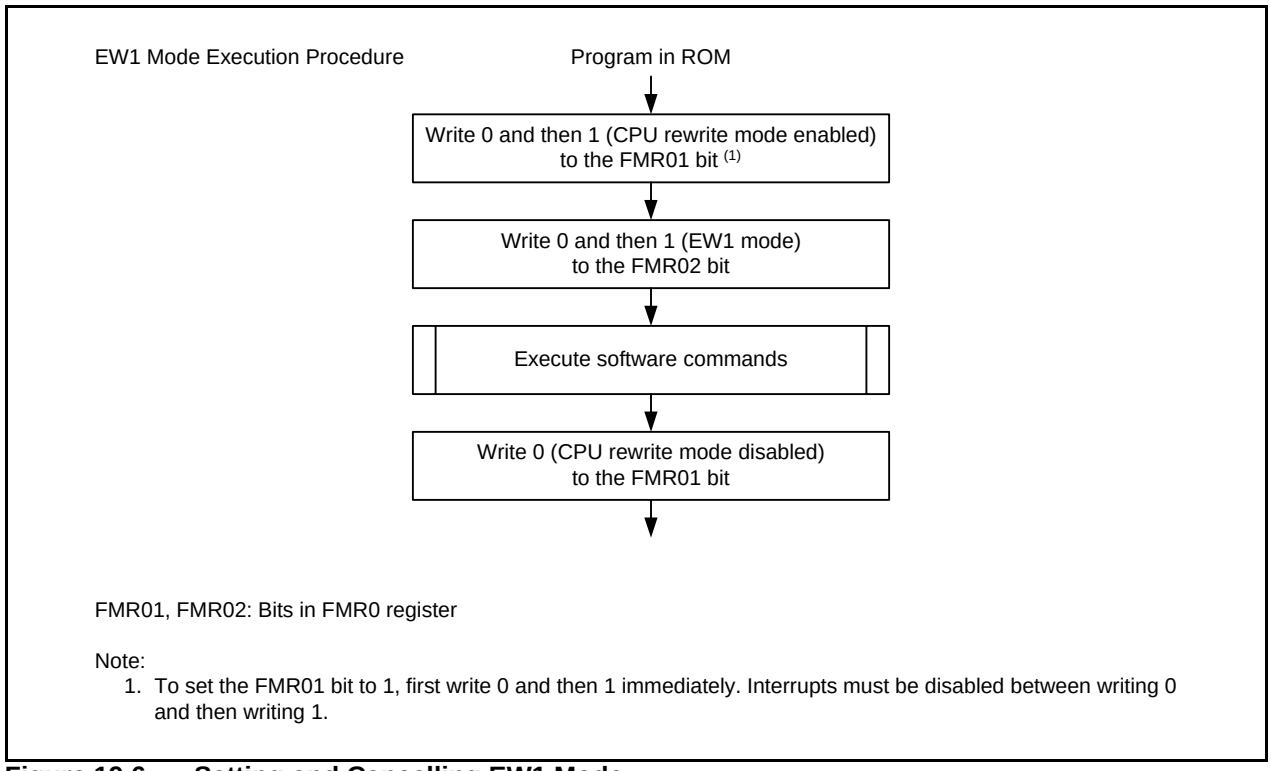


Figure 19.6 Setting and Cancelling EW1 Mode

19.6.5 Data Protect Function

Each block in the program ROM in the flash memory has a nonvolatile lock bit. The lock bit is enabled when the FMR13 bit in the FMR1 register is 0 (lock bit enabled). The lock bit can be used to disable (lock) programming/erasing each block. This prevents data from being written or erased inadvertently. The block status changes according to the lock bit as follows:

- When the lock bit data is 0: locked (the block cannot be programmed/erased)
- When the lock bit data is 1: not locked (the block can be programmed/erased)

The lock bit data is set to 0 (locked) when the lock bit program command is executed, and 1 (not locked) when the block is erased. There are no commands that can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and no blocks are locked. The lock bit data remains unchanged. When the FMR13 bit is set to 0 (lock bit enabled), the lock bit function is enabled. The lock bit data is retained.
When the block erase command is executed while the FMR13 bit is 1 (lock bit disabled), the target block is erased regardless of the lock bit status. The lock bit for the erase-target block is set to 1 after erase is completed. For details on individual commands, see **19.6.6 Software Commands**.
The FMR13 bit is set to 0 after auto-erase is completed. This bit is also set to 0 when one of the following conditions is met. To program/erase a block with a lock bit in a different state, set the FMR 13 bit to 1 (lock bit disabled) again and execute the program command or the block erase command.

- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and the program/erase command completes.
- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and program-suspend/erase-suspend is entered.
- When a command sequence error occurs.
- When the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- When the FMSTP bit in the FMR0 register is set to 1 (flash memory is stopped).
- When the CMDRST bit in the FMR0 register is set to 1 (erase/write sequence reset).

Figure 19.7 shows the Timing for FMR13 Bit Operation.

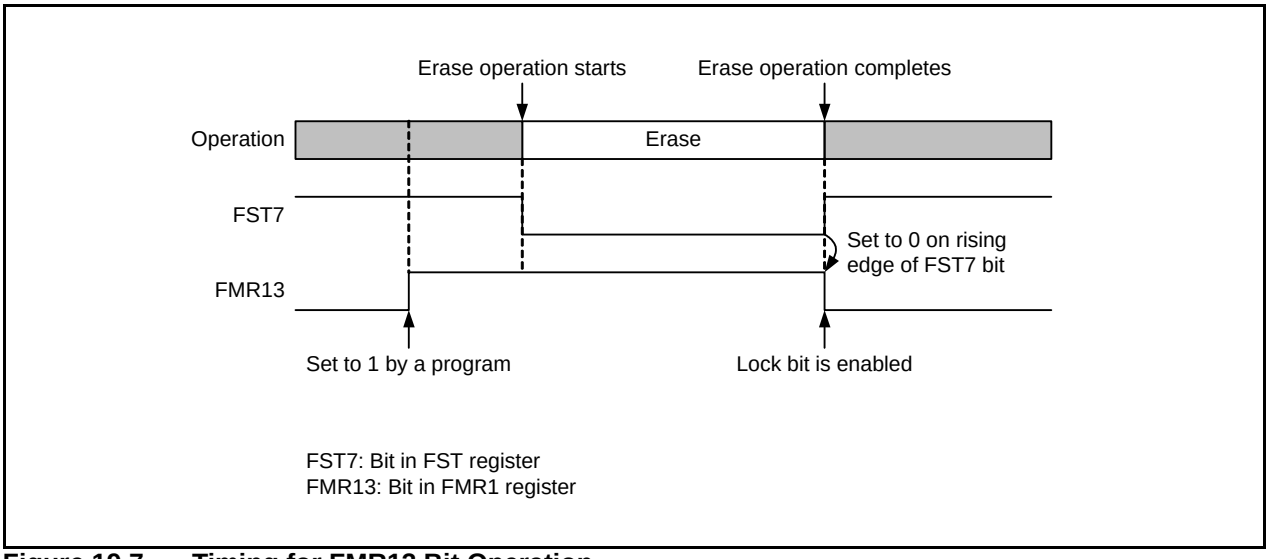


Figure 19.7 Timing for FMR13 Bit Operation

19.6.6 Software Commands

The software commands are described below. Commands must be read or written and data in 8-bit units. Do not input any command other than those listed in the table below.

Table 19.8 Software Commands

Command	First Command			Second Command (1)		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	x	FFh			
Clear status register	Write	x	50h			
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	x	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	x	71h	Write	BT	D0h
Block blank check	Write	x	25h	Write	BA	D0h

WA: Write address
WD: Write data
BA: Any address in the block
BT: Start address in the block
Block 2 → 0E000h
Block 1 → 0F000h
x: Any address in the user ROM area
Note:
1. For block erase, lock bit program, read lock bit status, and block blank check commands, if FFh is written as the second command, the command code written as the first command becomes invalid. A command sequence error does not occur.

The data flash does not have a lock bit, so the lock bit program and the read lock bit status commands are handled as illegal.

19.6.6.1 Read Array

This command is used to read the flash memory.
When FFh is written as the first command, the MCU enters read array mode. When the read address is input in the following cycles, the content of the specified address can be read in 8-bit units.
Since read array mode is retained until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering suspend.

19.6.6.2 Clear Status Register

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written as the first command, bits FST4 and FST5 in the FST register are set to 0.

19.6.6.3 Program

This command writes data to the flash memory in 1-byte units.
When 40h is written as the first command and data is written to the write address with the second command, auto-programming (a data program and verify operation) starts. The address value for the first command must be the same address as the write address specified with the second command.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (see **19.6.7 Full Status Check**).
Do not write additions to the already programmed addresses.
For each block in the program ROM, the program command can be disabled using the lock bit.
When the FMR16 bit in the FMR1 register is 1 (rewrite disabled), the program command for block A of data flash is not accepted. When the FMR17 bit is 1 (rewrite disabled), the program command for block B is not accepted.
Figure 19.8 shows the Program Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled). Figure 19.9 shows the Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled). Figure 19.10 shows the Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled). Figure 19.11 shows the Program Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command for any address where the rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled), a flash ready status interrupt is generated when auto-programming is completed.
When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled) and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (suspend request) and auto-programming is suspended. The result can be confirmed by reading the FST register in the interrupt routine.

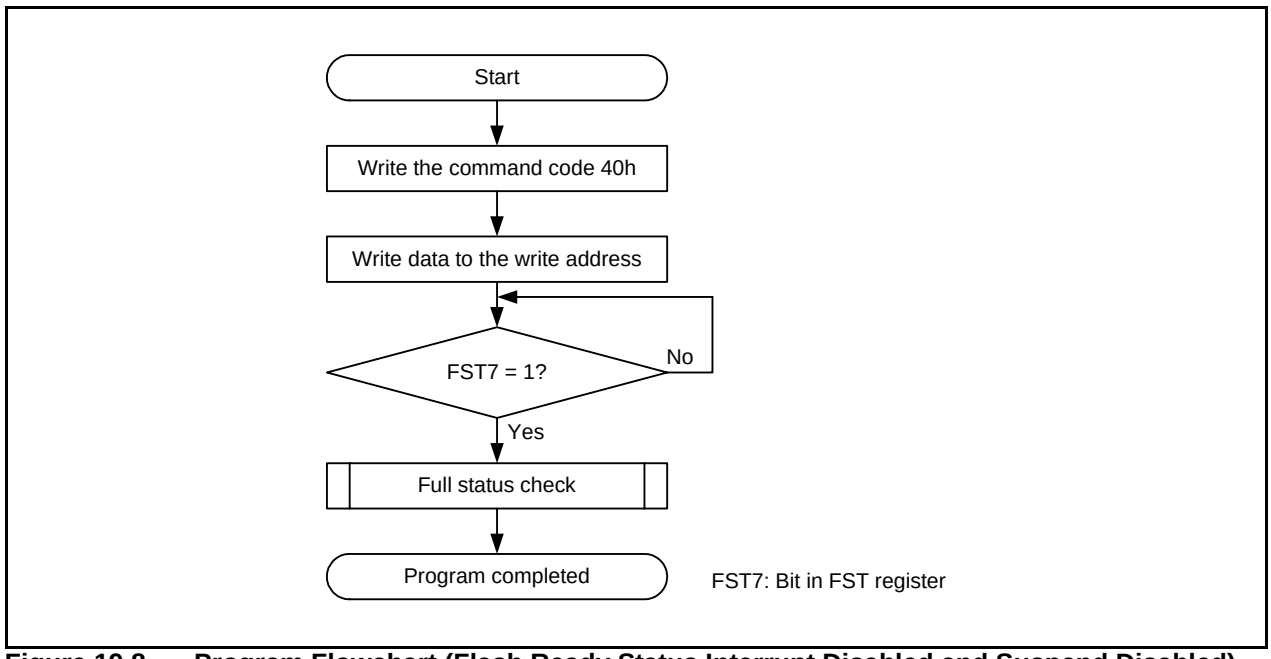
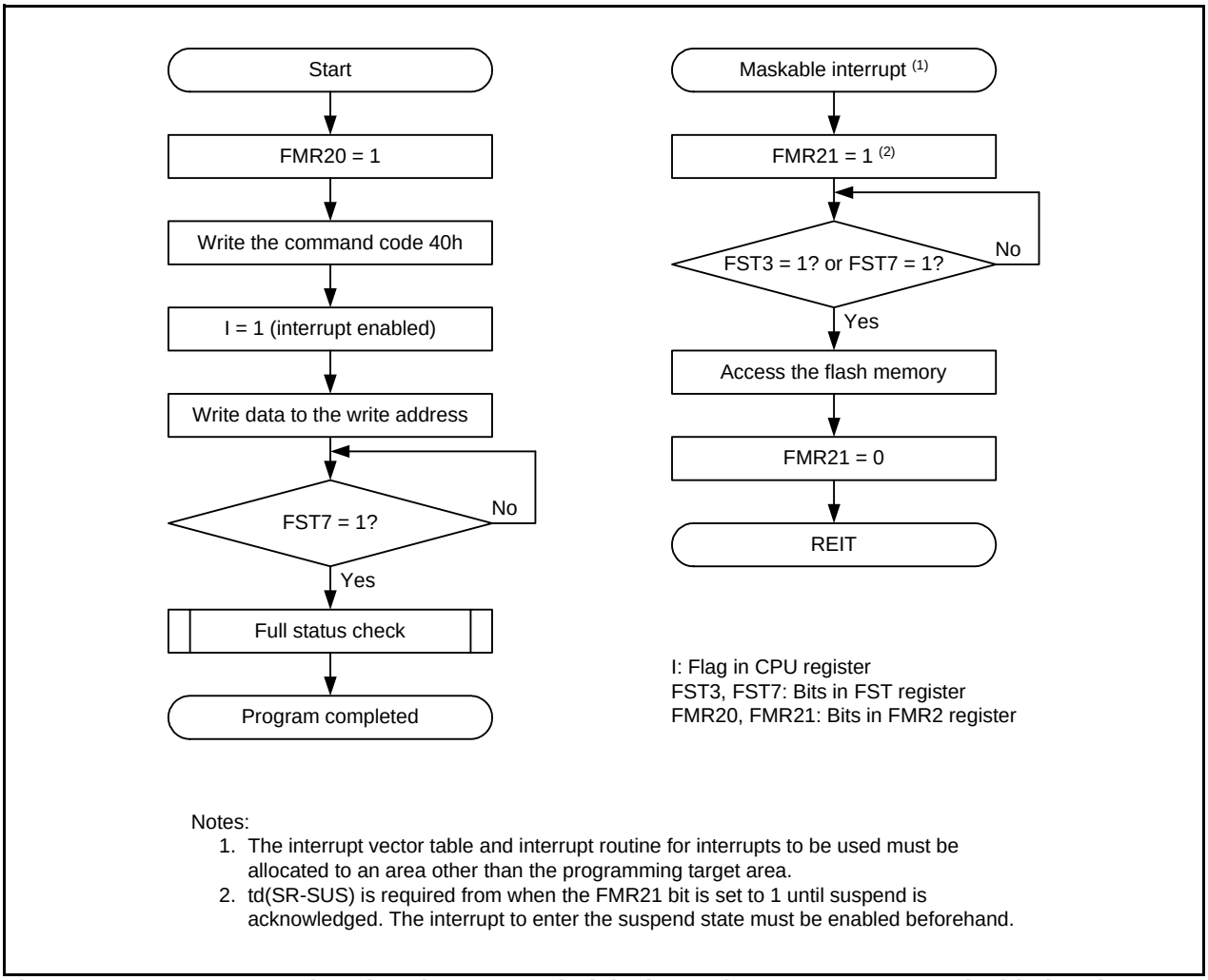
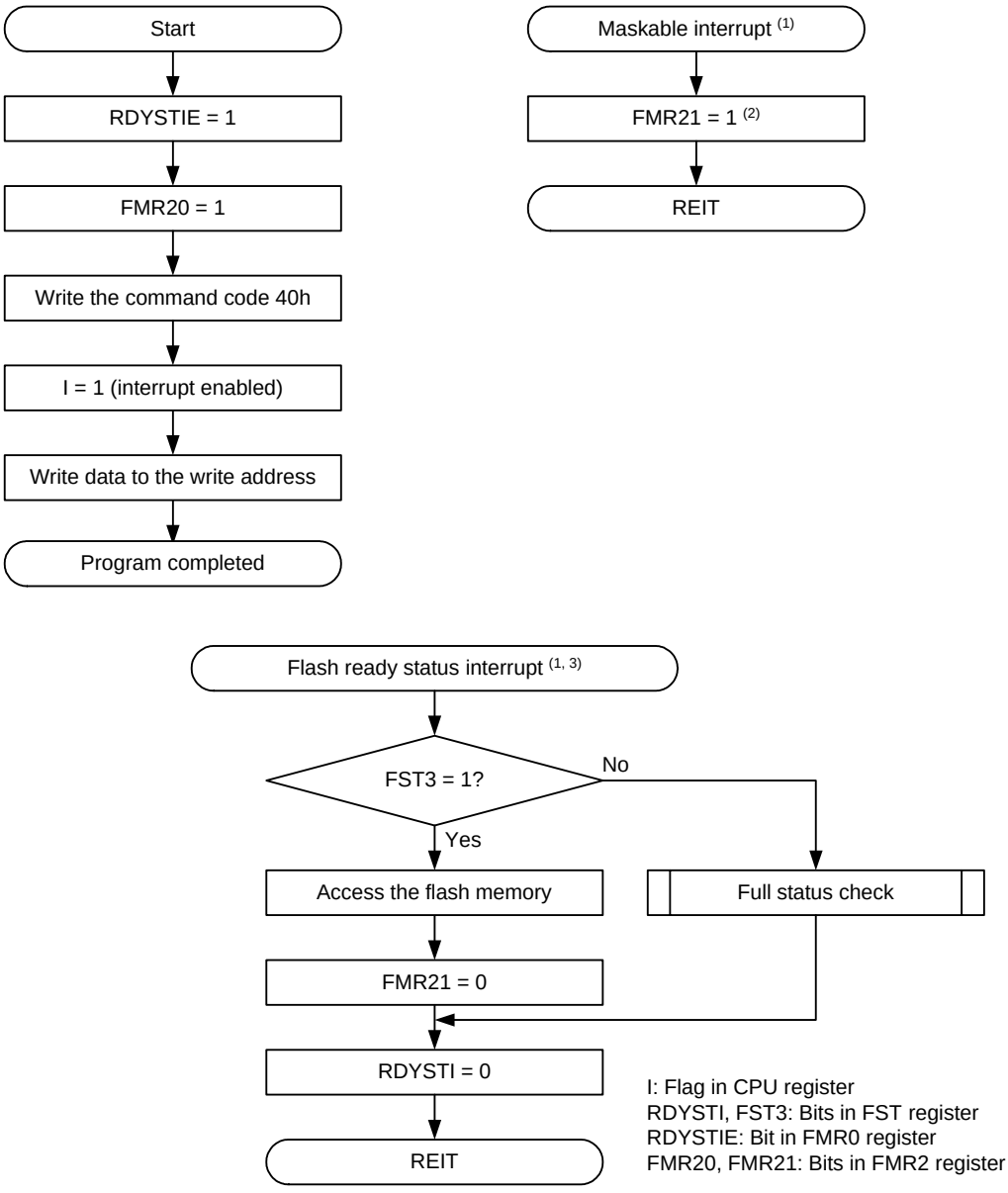


Figure 19.8 Program Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter the suspend state must be enabled beforehand.

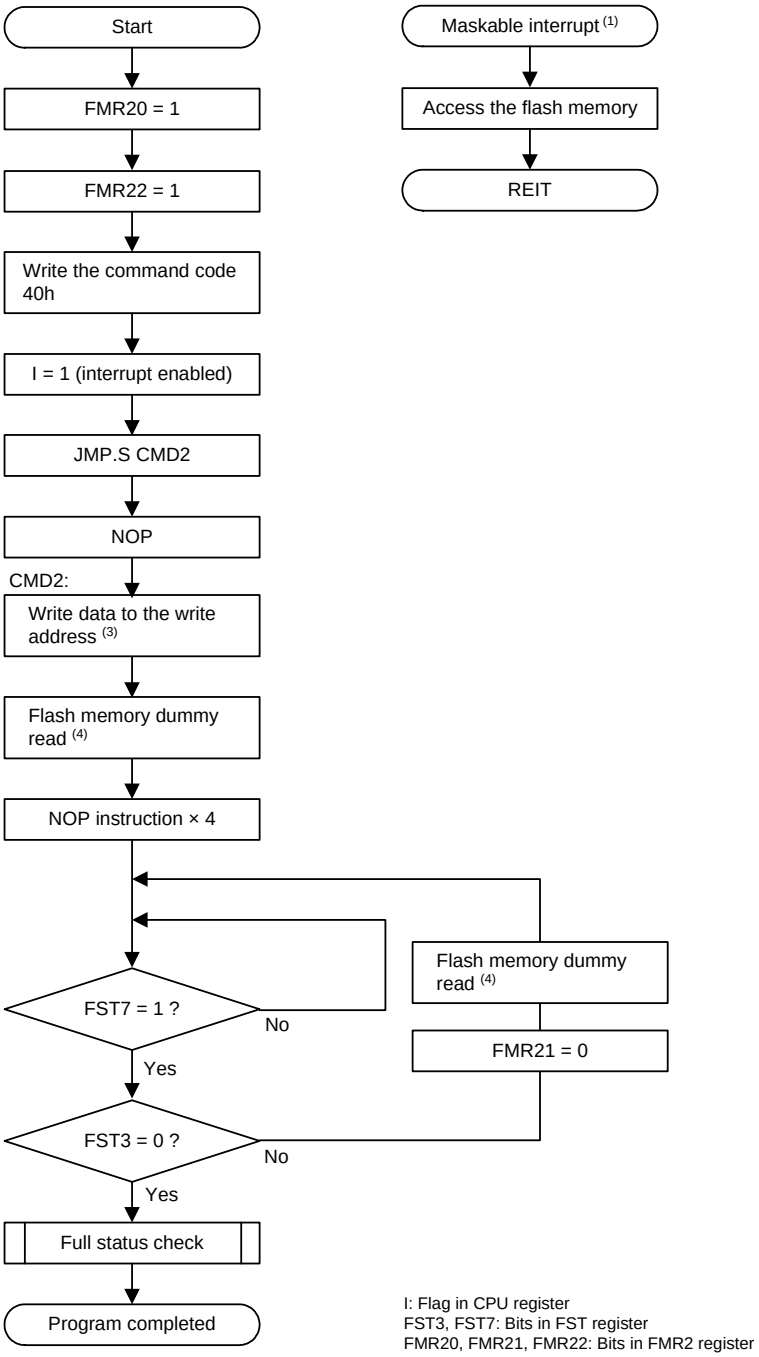
Figure 19.9 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter the suspend state must be enabled beforehand.
3. A flash ready status interrupt is generated when auto-programming is suspended.

Figure 19.10 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-programming. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.
3. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
4. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 19.11 Program Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

19.6.6.4 Block Erase

When 20h is written as the first command and then D0h is written to any address in the block with the second command, an auto-erase (erase and erase-verify operation) is started in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erase is completed. The FST7 bit is set to 0 during auto-erase and changed to 1 when auto-erase is completed. After auto-erase completes, all data in the block is set to FFh.
After auto-erase is completed, the result can be confirmed by the FST5 bit in the FST register (see **19.6.7 Full Status Check**).
For each block in the program ROM, the program erase command can be disabled using the lock bit.
When the FMR16 bit in the FMR1 register is 1 (rewrite disabled), the block erase command for block A of data flash is not accepted. When the FMR17 bit is 1 (rewrite disabled), the block erase command for block B is not accepted.
Figure 19.12 shows the Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled). Figure 19.13 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled). Figure 19.14 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled). Figure 19.15 shows the Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command for the block where the rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled), a flash ready status interrupt is generated when auto-erase is completed. When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled) and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (suspend request) and auto-erase is suspended. The result can be confirmed by reading the FST register in the interrupt routine.

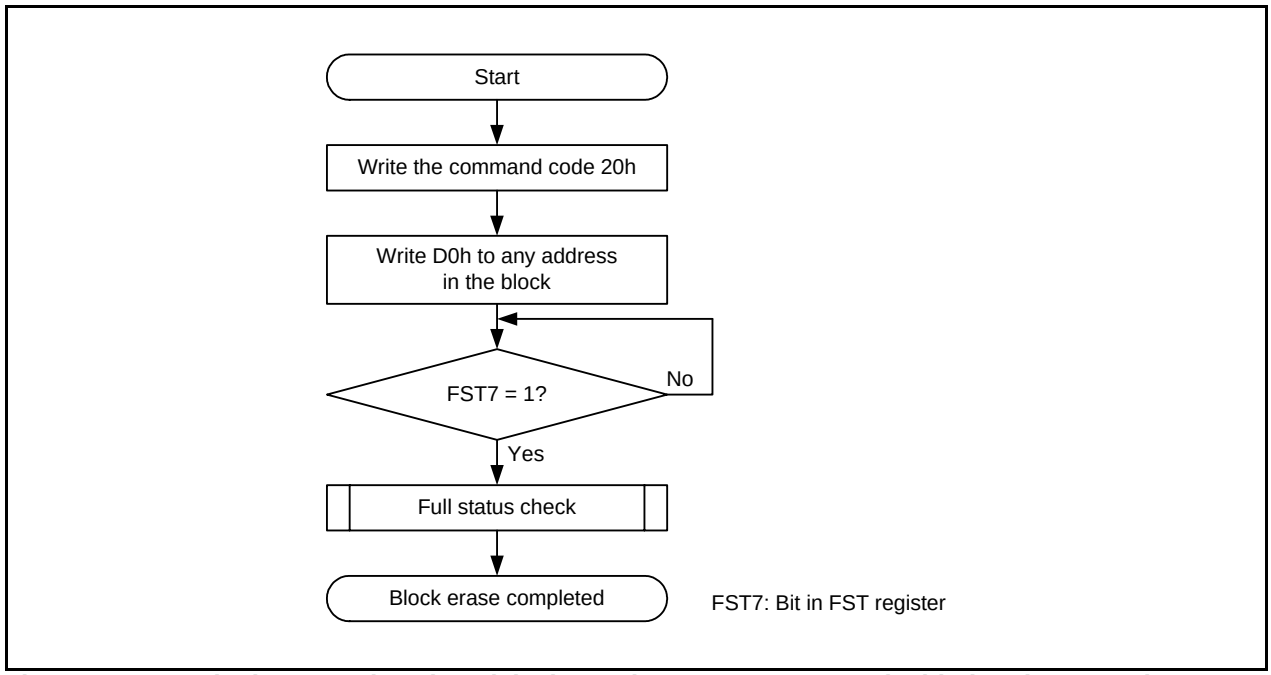
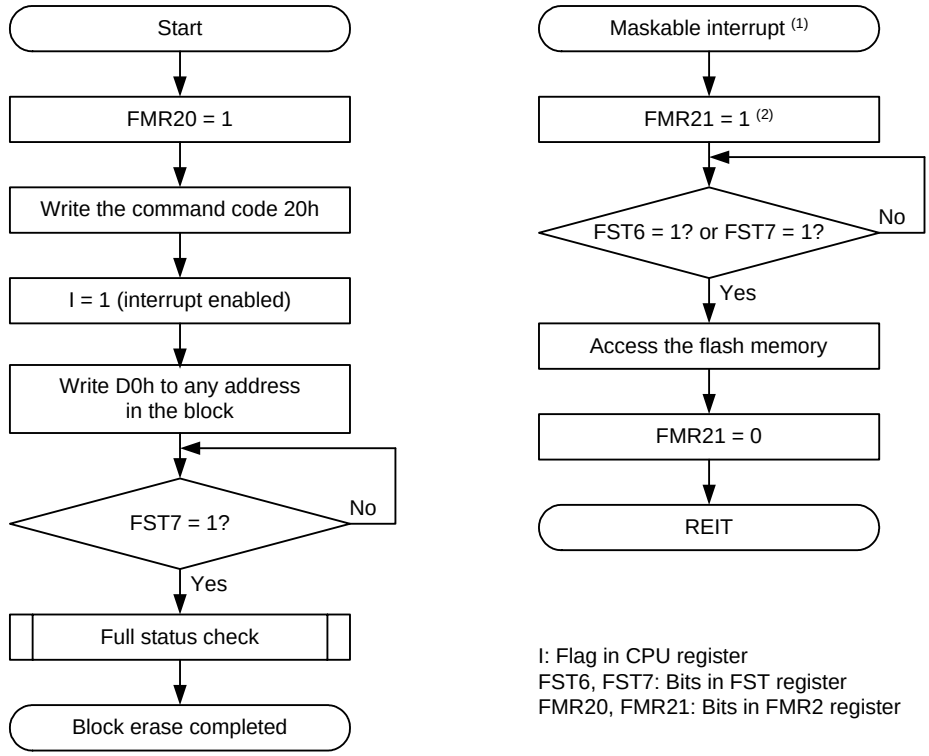
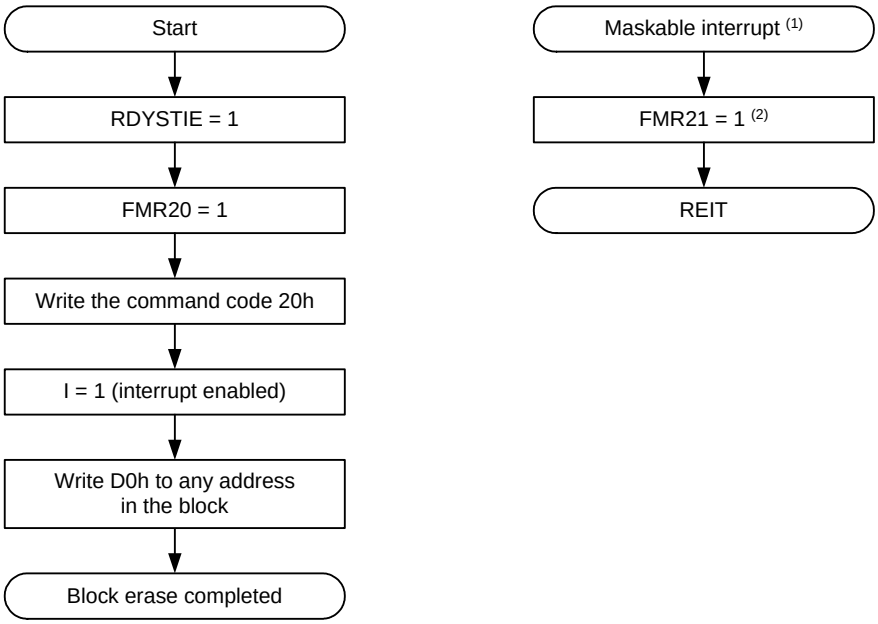


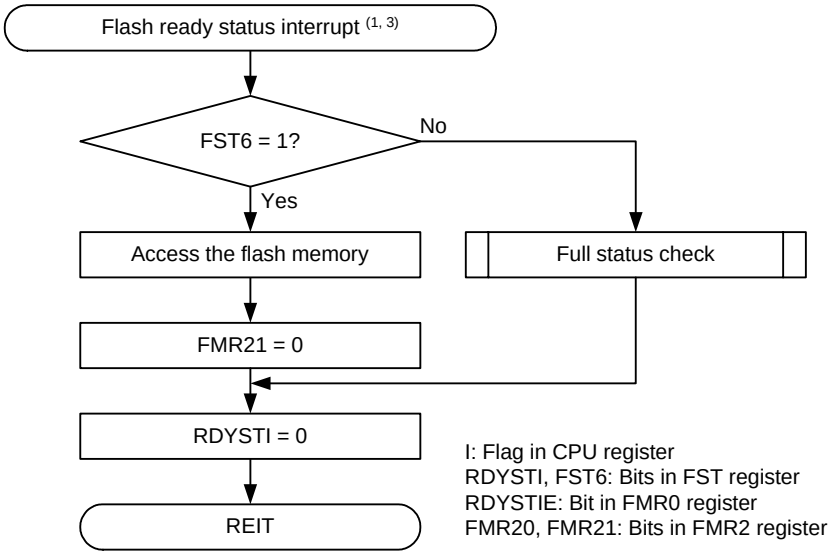
Figure 19.12 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled)



Notes:
1. The interrupt vector table and interrupt routine to be used must be allocated to an area other than the erase-target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

Figure 19.13 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

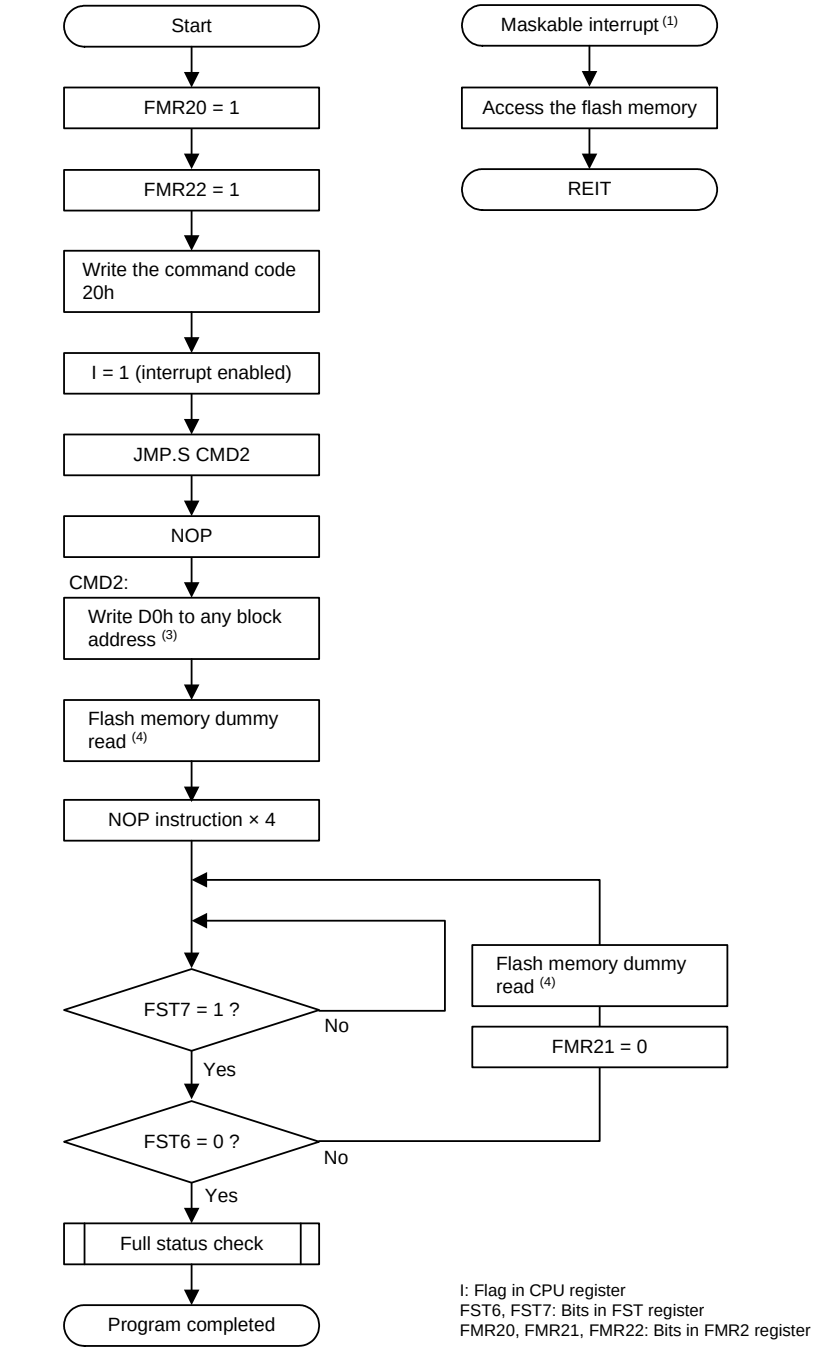




Notes:
1. The interrupt vector table and interrupt routine to be used must be allocated to an area other than the erase-target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.
3. A flash ready status interrupt is generated when auto-erase is suspended.

Figure 19.14 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erase. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.
3. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
4. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 19.15 Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

19.6.6.5 Lock Bit Program

This command is used to set the lock bit for any block in the program ROM area to 0 (locked).
When 77h is written as the first command and D0h is written to the start address in the block with the second command, 0 is written to the lock bit in the specified block. The address for the first command must be the same as that for the second which specifies the start address in the block.
Figure 19.16 shows the Lock Bit Program Flowchart.
The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit is completed.
For details on the lock bit function and how to set the lock bit to 1 (not locked), see **19.6.5 Data Protect Function**.

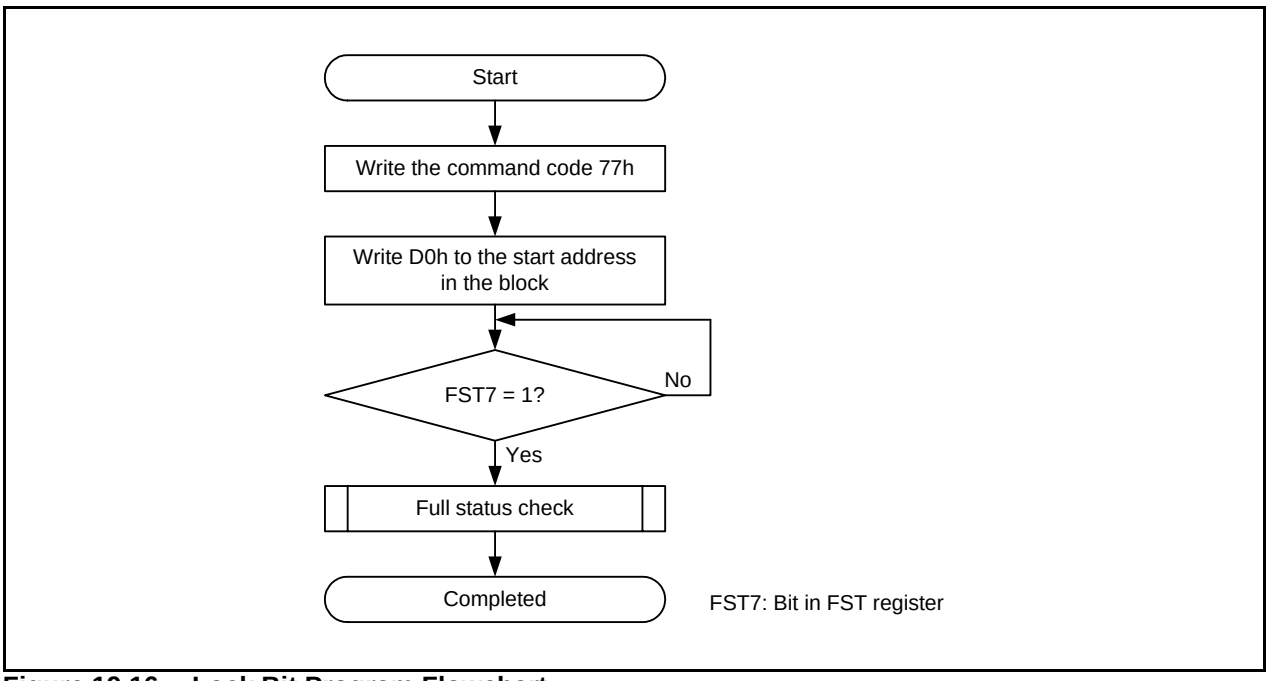


Figure 19.16 Lock Bit Program Flowchart

19.6.6.6 Read Lock Bit Status Command

This command is used to read the lock bit status for any block in the program ROM area.
When 71h written as the first command and D0h is written to the start address in the block with the second command, the lock bit status in the specified block is stored in the FST2 bit in the FST register. Read the FST2 bit after the FST7 bit in the FST register has changed to 1 (ready).
Figure 19.17 shows the Read Lock Bit Status Flowchart.

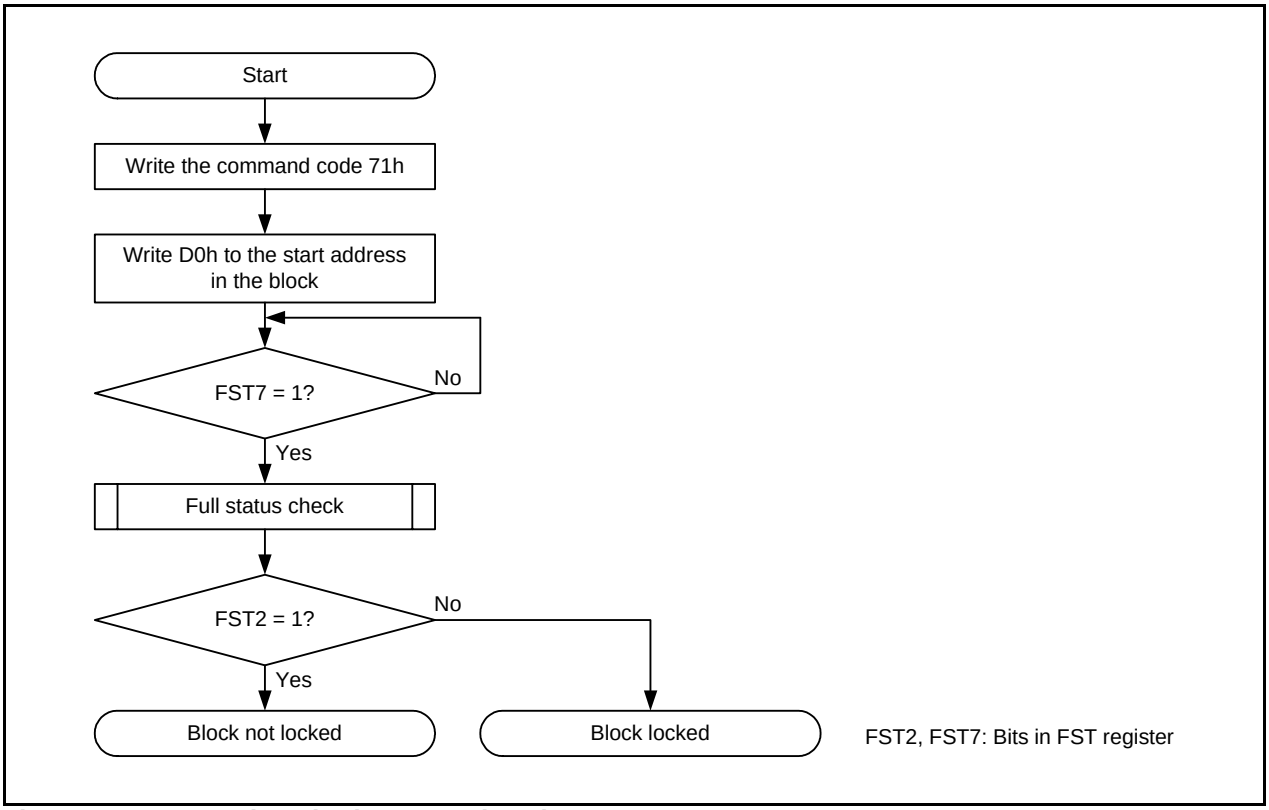


Figure 19.17 Read Lock Bit Status Flowchart

19.6.6.7 Block Blank Check

This command is used to confirm that all addresses in any block are blank data, FFh.
When 25h is written as the first command and D0h is written to any address in the block with the second command, a blank check is started for the specified block. The FST7 bit in the FST register can be used to confirm whether blank check is completed. The FST7 bit is set to 0 during the blank-check period and changed to 1 when the blank check has completed.
After the blank check has completed, the result can be determined by reading the FST5 bit in the FST register (see **19.6.7 Full Status Check**). This command is also used to verify the target block has not been written. To confirm whether erase has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit in the FST register is 1 (erase suspended) or the FST3 bit is 1 (program suspended).
Figure 19.18 shows the Block Blank Check Flowchart.

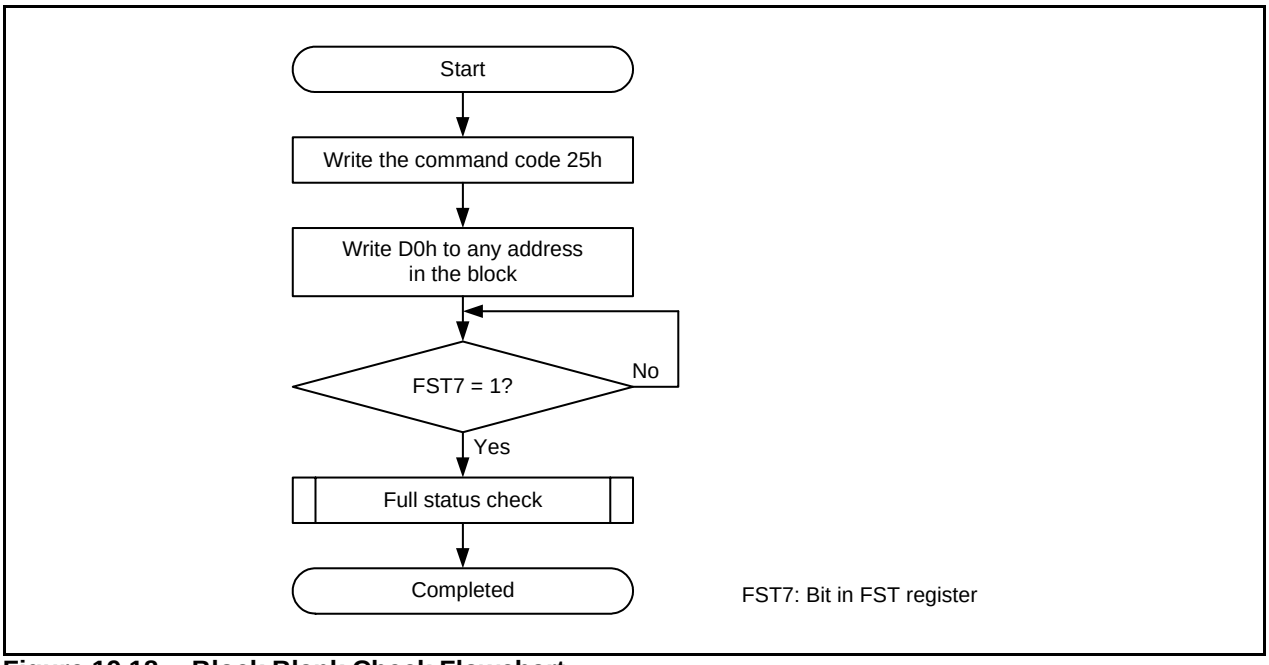


Figure 19.18 Block Blank Check Flowchart

This command is intended for programmer manufacturers, not for general users.

19.6.7 Full Status Check

If an error occurs, bits FST4 to FST5 in the FST register are set to 1, indicating the occurrence of the error. The execution result can be confirmed by checking these status bits (full status check).
Table 19.9 lists the Errors and FST Register States. Figure 19.19 shows the Full Status Check and Handling Procedures for Individual Errors.

Table 19.9 Errors and FST Register States

FST Register States		Error	Error Occurrence Condition
FST5 Bit	FST4 Bit		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written as the second command of the block erase, lock bit program, read lock bit status, or block blank check command (1). • The erase command is executed during erase-suspend or the block blank check command is executed. • The program, lock bit program, erase, or block blank check command is executed during program-suspend. • The program, lock bit program, erase, or block blank check command is executed to the block during suspend. • The lock bit program or read lock bit status commands are executed to the data flash.
1	0	Erase error	When the block erase command is executed and auto-erase does not complete normally.
		Blank check error	When the block blank check command is executed and data other than the blank data, FFh, is read.
0	1	Program error	When the program command is executed and auto-programming does not complete normally.
		Lock bit program error	When the lock bit command is executed, but the lock bit is not set to 0 (locked).

Note:
1. When FFh is written as the second command of these commands, the MCU enters read array mode. At the same time, the command code written as the first command becomes invalid.

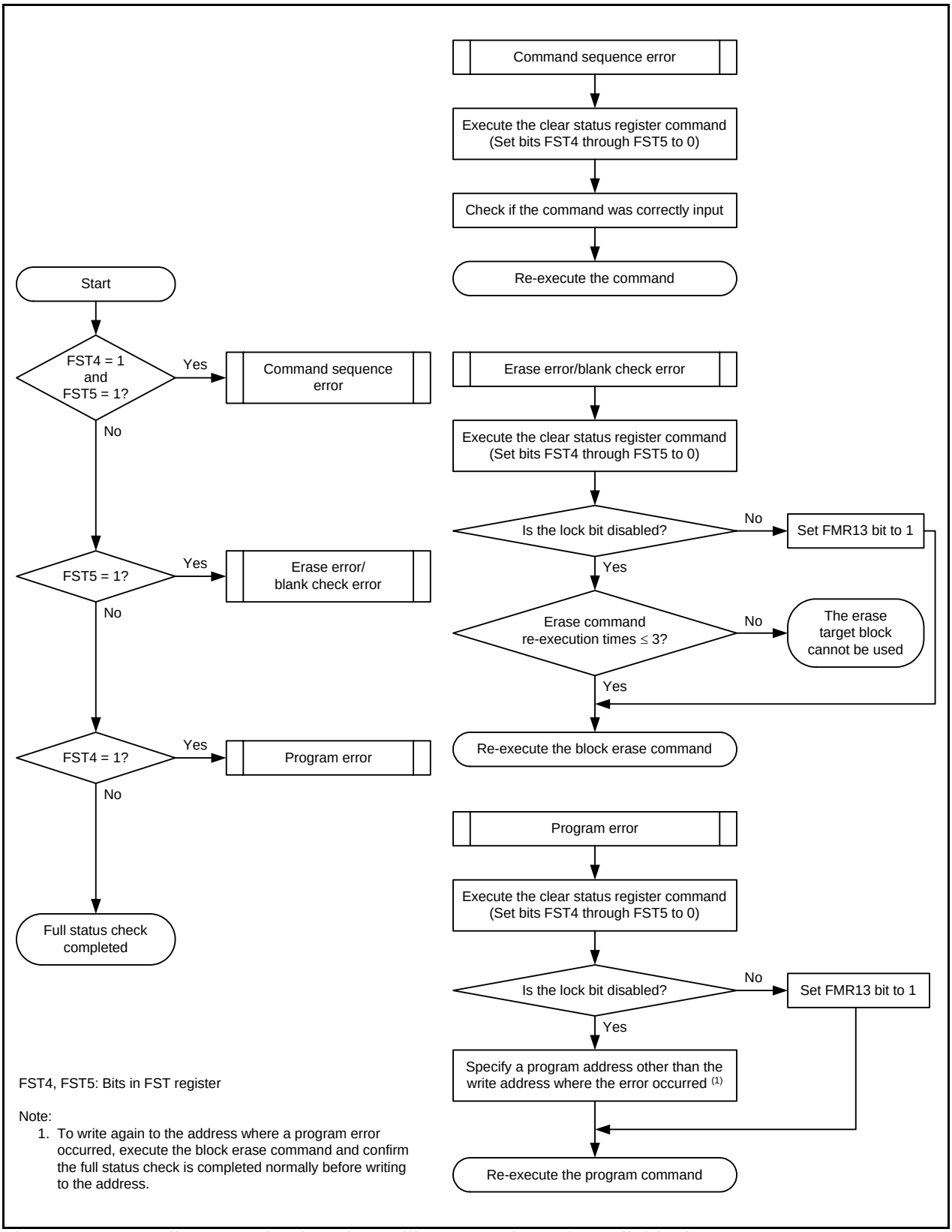


Figure 19.19 Full Status Check and Handling Procedures for Individual Errors

19.7 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer that supports the MCU can be used to rewrite the user ROM area with the MCU mounted on-board.
There are three standard serial I/O modes:
• Standard serial I/O mode 1: Connection to a serial programmer via clock synchronous serial I/O
• Standard serial I/O mode 2: Connection to a serial programmer via clock asynchronous serial I/O
• Standard serial I/O mode 3: Connection to a serial programmer via special clock asynchronous serial I/O

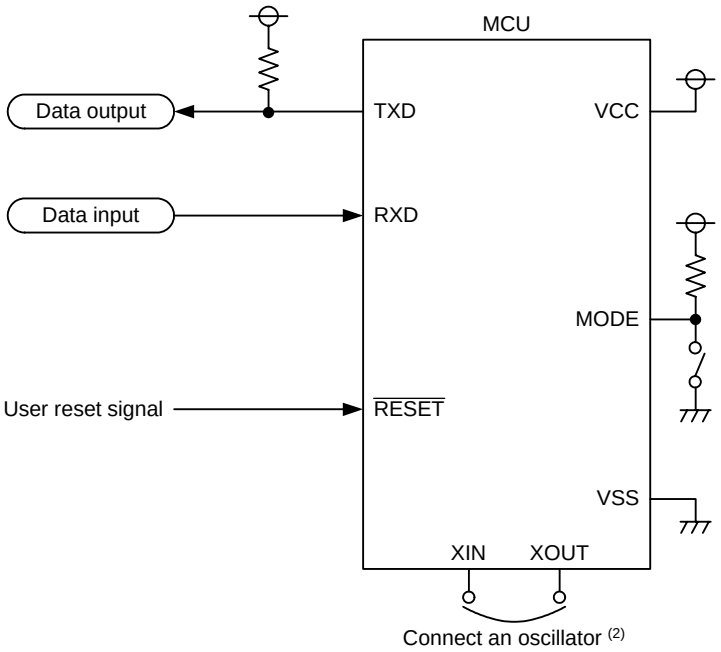
Standard serial I/O modes 2 and 3 can be used with the MCU.

See **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting a serial programmer. Contact the manufacturer for more information on the serial programmer. Also, see the user's manual for how to use the serial programmer.

Table 19.10 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2). Figure 19.20 shows a Pin Handling Example in Standard Serial I/O Mode 2. Table 19.11 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3). Figure 19.21 shows a Pin Handling Example in Standard Serial I/O Mode 3.
When a program in the flash memory is run in user mode after the pins are handled as shown in Table 19.11 and the flash memory is rewritten with the programmer, input a high level to the MODE pin and reset the hardware.
For details on the ID code check function, see **19.3 ID Code Check Function**.

Table 19.10 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin Name	Name	I/O	Description
VCC, VSS	Power supply input	—	Apply the guaranteed program/erase voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input.
P4_6/XIN	P4_6 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P4_7/XOUT	P4_7 input/clock output	I/O	
MODE	MODE	I/O	Input a low level.
P1_4	TXD output	O	Serial data output.
P1_6	RXD input	I	Serial data input.
Other pins			Input a low level or a high level, or leave the pin open.

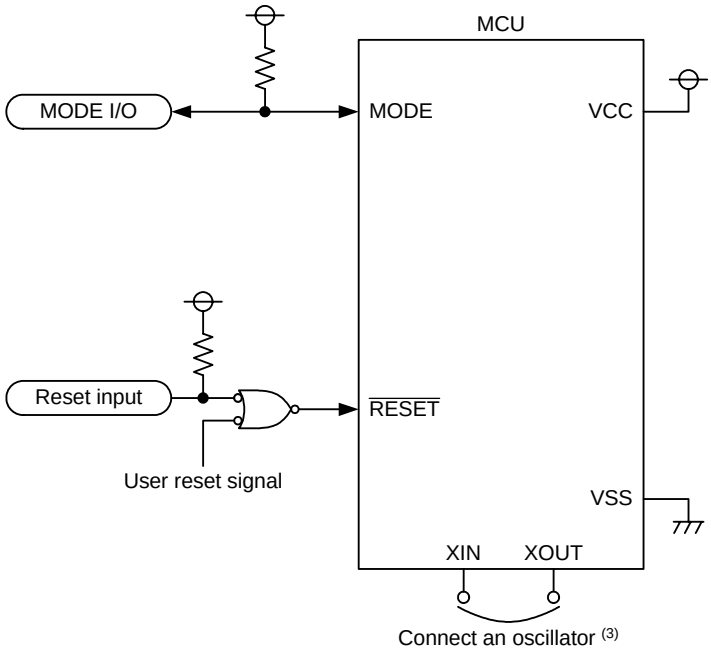


Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. See **Appendix Figures 2.1** and **2.2 MF Ten Nine Cable (M3A-0652CBL) Connection Examples**.

Figure 19.20 Pin Handling Example in Standard Serial I/O Mode 2

Table 19.11 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin Name	Name	I/O	Description
VCC, VSS	Power supply input	—	Apply the guaranteed program/erase voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input.
P4_6/XIN	P4_6 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P4_7/XOUT	P4_7 input/clock output	I/O	
MODE	MODE	I/O	Serial data I/O. Connect this pin to a flash programmer.
Other pins			Input a low level or a high level, or leave the pin open.



Notes:
1. Controlled pins and external circuits vary depending on the programmer. For details, see the programmer manual.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 19.21 Pin Handling Example in Standard Serial I/O Mode 3

19.8 Notes on Flash Memory

19.8.1 ID Code Area Setting Example

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set 55h in all of the ID code area

```
.org 00FFDCH
.lword dummy | (55000000h)      ; UND
.lword dummy | (55000000h)      ; INTO
.lword dummy                    ; BREAK
.lword dummy | (55000000h)      ; ADDRESS MATCH
.lword dummy | (55000000h)      ; SET SINGLE STEP
.lword dummy | (55000000h)      ; WDT
.lword dummy | (55000000h)      ; RESERVE
.lword dummy | (55000000h)      ; RESERVE
```

Programming formats vary depending on the compiler. Check the compiler manual.

19.8.2 CPU Rewrite Mode

19.8.2.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory:
UND, INTO, and BRK

19.8.2.2 Interrupts

Tables 19.12 and 19.13 list the Interrupt Handling during CPU Rewrite Operation.

Table 19.12 Interrupt Handling during CPU Rewrite Operation (EW0 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, interrupt handling is executed. (The interrupt vector is allocated in the RAM) The suspend state can be entered by either of the following: (1) When the FMR22 bit is 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS). (2) When the FMR22 bit is 0 (suspend request disabled by interrupt request) and suspend is required, set the FMR21 bit to 1 (suspend request) in the interrupt handling. The flash memory suspends auto-erase or auto-programming after td(SR-SUS). While auto-erase is suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. While auto-programming is suspended, any block other than the blocks being auto-programmed can be read. Auto-erase can be restarted by setting the FMR21 bit to 0 (restart).	Interrupt handling is executed with auto-erase or auto-programming executed (The interrupt vector is allocated in the RAM)
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register
Note:
1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

Table 19.13 Interrupt Handling during CPU Rewrite Operation (EW1 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, the FMR21 bit is automatically set to 1 (suspend request) if the FMR22 bit is 1 (suspend request enabled by interrupt request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS) and interrupt handling is executed. When auto-erase is being suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. When auto-programming is being suspended, any block other than the blocks being auto-programmed can be read. After interrupt handling completes, auto-erase or auto-programming can be restarted by setting the FMR21 bit is set to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.	Auto-erase or auto-programming has priority. Interrupt handling is executed after auto-erase or auto-programming.
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register

Note:

1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
   When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

19.8.2.3 Access Methods

To set one of the following bits to 1, first write 0 and then 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
• The FMR01 or FMR02 bit in the FMR0 register
• The FMR13 bit in the FMR1 register
• The FMR20, FMR22, or FMR27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Interrupts must be disabled between writing 1 and then writing 0.
The FMR16 or FMR17 bit in the FMR1 register

19.8.2.4 Rewriting User ROM Area

When EW0 mode is used and the supply voltage falls while rewriting a block where a rewrite control program is stored, the rewrite control program is not be rewritten correctly. As a result, it may not be possible to rewrite the flash memory afterwards. Use standard serial I/O mode to rewrite this block.

19.8.2.5 Programming

Do not perform even a single additional write to an already programmed address.

19.8.2.6 Entering Wait Mode or Stop Mode

Do not enter wait mode or stop mode during suspend.
When the FST7 bit in the FST register is 0 (busy) while programming or erasing the flash memory, do not enter wait mode or stop mode.
Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory is stopped).

19.8.2.7 Flash Memory Programming and Erase Voltages

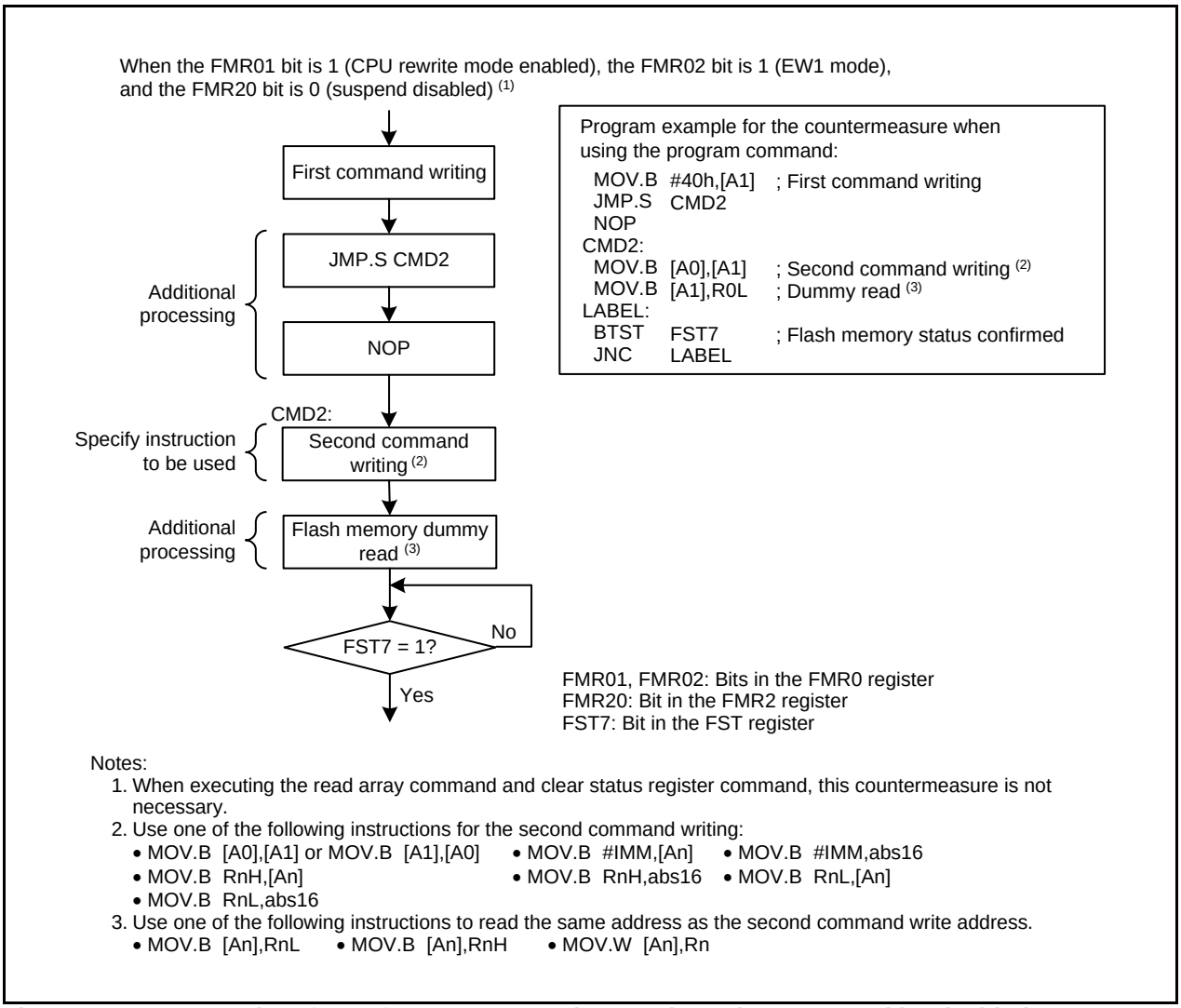
When performing a program/erase operation, use a VCC supply voltage in the range of 1.8 V to 5.5 V. Do not perform a program/erase operation at less than 1.8 V.

19.8.2.8 Block Blank Check

Do not execute a block blank check command during erase-suspend.

19.8.2.9 EW1 Mode

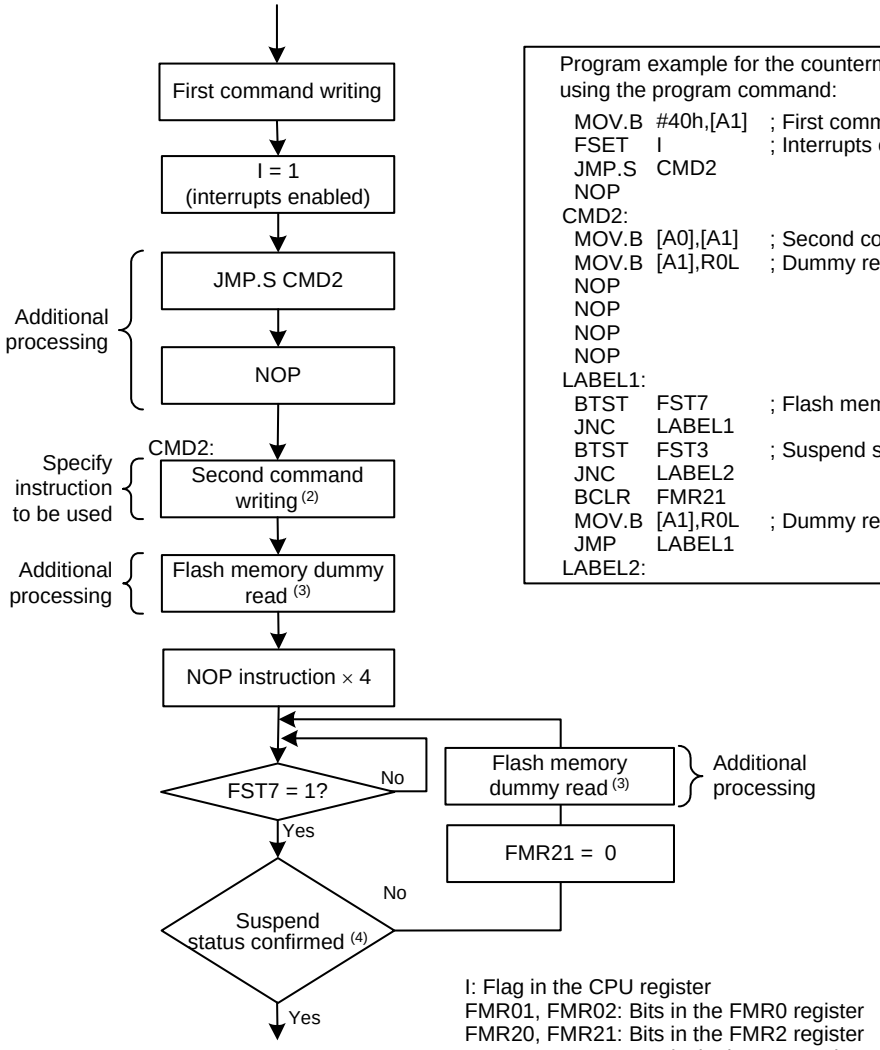
When setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and the FMR02 bit to 1 (EW1 mode) to execute CPU rewrite mode, follow the procedure below in EW1 mode. Figure 19.22 shows the Procedure for Software Command Execution When Suspend is Disabled. Figure 19.23 shows the Procedure for Software Command Execution When Suspend is Enabled.



Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 19.22 Procedure for Software Command Execution When Suspend is Disabled

When the FMR01 bit is 1 (CPU rewrite mode enabled), the FMR02 bit is 1 (EW1 mode), and the FMR20 bit is 1 (suspend enabled) (1)



Program example for the countermeasure when using the program command:

```
  MOV.B  #40h,[A1]   ; First command writing
  FSET   I           ; Interrupts enabled
  JMP.S  CMD2
  NOP
CMD2:
  MOV.B  [A0],[A1]   ; Second command writing (2)
  MOV.B  [A1],R0L    ; Dummy read (3)
  NOP
  NOP
  NOP
  NOP
LABEL1:
  BTST   FST7        ; Flash memory status confirmed
  JNC    LABEL1
  BTST   FST3        ; Suspend status confirmed (4)
  JNC    LABEL2
  BCLR   FMR21
  MOV.B  [A1],R0L    ; Dummy read (3)
  JMP    LABEL1
LABEL2:
```

I: Flag in the CPU register
FMR01, FMR02: Bits in the FMR0 register
FMR20, FMR21: Bits in the FMR2 register
FST3, FST6, FST7: Bits in the FST register

Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn
4. Confirm the suspend status using the FST3 bit for the program command, and the FST6 bit for the block erase command.

Figure 19.23 Procedure for Software Command Execution When Suspend is Enabled

19.8.3 Notes on Flash Memory Stop and Operation Transition

(1) Do not enter stop mode while the FMSTP bit is 1 (the flash memory is stopped).
(2) Do not enter wait mode while the FMSTP bit is 1 (the flash memory is stopped) and the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
(3) Do not enter flash memory stop state for 42 μs after entering from flash memory stop state to flash memory operation state. And do not rewrite the LOCODIS bit in the OCOCR register for 42 μs.

Conditions when entering flash memory operation state from flash memory stop state.
• Set the FMSTP bit to 0 (the flash memory operates).
• Return from wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Return from stop mode.

Conditions when entering flash memory stop state from flash memory operation state.
• Set the FMSTP bit to 1 (the flash memory is stopped).
• Enter wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Enter stop mode.

20. Electrical Characteristics

Table 20.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Power supply voltage			-0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
P_d	Power consumption		-40 °C ≤ Topr ≤ 85 °C	500	mW
T_{opr}	Operating ambient temperature			-20 to 85 (N version)/ -40 to 85 (D version)	°C
T_{stg}	Storage temperature			-60 to 150	°C

Note:
1. When the oscillation circuit is used: bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b
   When the oscillation circuit is not used: bits CKPT1 to CKPT0 in the EXCKCR register are set to any value other than 11b

Table 20.2 Recommended Operating Conditions

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Power supply voltage			1.8	—	5.5	V
V_{SS}/AV_{SS}	Power supply voltage			—	0	—	V
V_{IH}	Input high voltage	Other than CMOS input		0.8 Vcc	—	Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
V_{IL}	Input low voltage	Other than CMOS input		0	—	0.2 Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
$I_{OH(sum)}$	Peak sum output high current	Sum of all pins $I_{OH(peak)}$		—	—	-160	mA
$I_{OH(sum)}$	Average sum output high current	Sum of all pins $I_{OH(avg)}$		—	—	-80	mA
$I_{OH(peak)}$	Peak output high current		When drive capacity is low	—	—	-10	mA
			When drive capacity is high (5)	—	—	-40	mA
$I_{OH(avg)}$	Average output high current		When drive capacity is low	—	—	-5	mA
			When drive capacity is high (5)	—	—	-20	mA
$I_{OL(sum)}$	Peak sum output low current	Sum of all pins $I_{OL(peak)}$		—	—	160	mA
$I_{OL(sum)}$	Average sum output low current	Sum of all pins $I_{OL(avg)}$		—	—	80	mA
$I_{OL(peak)}$	Peak output low current		When drive capacity is low	—	—	10	mA
			When drive capacity is high (5)	—	—	40	mA
$I_{OL(avg)}$	Average output low current		When drive capacity is low	—	—	5	mA
			When drive capacity is high (5)	—	—	20	mA
$f_{(XIN)}$	XIN oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	2	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	2	—	5	MHz
	XIN clock input oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz
fHOCO	High-speed on-chip oscillator oscillation frequency (3)		1.8 V ≤ Vcc ≤ 5.5 V	—	20	—	MHz
fLOCO	Low-speed on-chip oscillator oscillation frequency (4)		1.8 V ≤ Vcc ≤ 5.5 V	—	125	—	kHz
—	System clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f_S	CPU clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz

Notes:
1. Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. For details, see **Table 20.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
4. For details, see **Table 20.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
5. The pins with high drive capacity are P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, and P3_7.

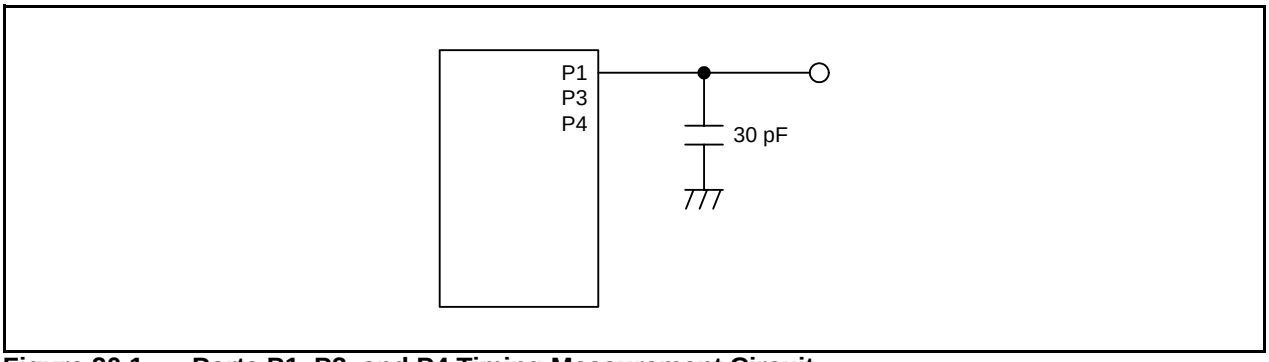


Figure 20.1 Ports P1, P3, and P4 Timing Measurement Circuit

Table 20.3 A/D Converter Characteristics

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
—	Resolution			—	—	10	Bit
—	Absolute accuracy	AVcc = 5.0 V	AN0 to AN4, AN7 input	—	—	±3	LSB
		AVcc = 3.0 V	AN0 to AN4, AN7 input	—	—	±5	LSB
		AVcc = 1.8 V	AN0 to AN4, AN7 input	—	—	±5	LSB
—	A/D conversion clock	4.0 V ≤ AVcc ≤ 5.5 V (2)		2	—	20	MHz
		3.2 V ≤ AVcc ≤ 5.5 V (2)		2	—	16	MHz
		2.7 V ≤ AVcc ≤ 5.5 V (2)		2	—	10	MHz
		1.8 V ≤ AVcc ≤ 5.5 V (2)		2	—	5	MHz
—	Permissible signal source impedance				3		kΩ
t_{CONV}	Conversion time	AVcc = 5.0 V, A/D conversion clock = 20 MHz		2.20	—	—	µs
t_{SAMP}	Sampling time	A/D conversion clock = 20 MHz		0.80	—	—	µs
V_{IA}	Analog input voltage			0	—	AVcc	V

Notes:
1. Vcc/AVcc = 1.8 V to 5.5 V and Vss = 0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in stop mode, or when the flash memory is in low-current-consumption read mode or stopped. Do not perform A/D conversion in these states. Do not enter these states during A/D conversion.

Table 20.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc - 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (2)	V_I = Vref ± 100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 20.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time (program/erase endurance ≤ 1,000 times)		—	80	—	µs
—	Byte programming time (program/erase endurance > 1,000 times)		—	160	—	µs
—	Block erase time		—	0.12	—	s
$t_{d(SR-SUS)}$	Transition time to suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = 0 °C to 60 °C, unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple programming operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

Table 20.6 Flash Memory (Blocks A and B of Data Flash) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time		—	150	—	µs
—	Block erase time		—	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		-20 (N version)	—	85	°C
			-40 (D version)	—	85	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple program operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

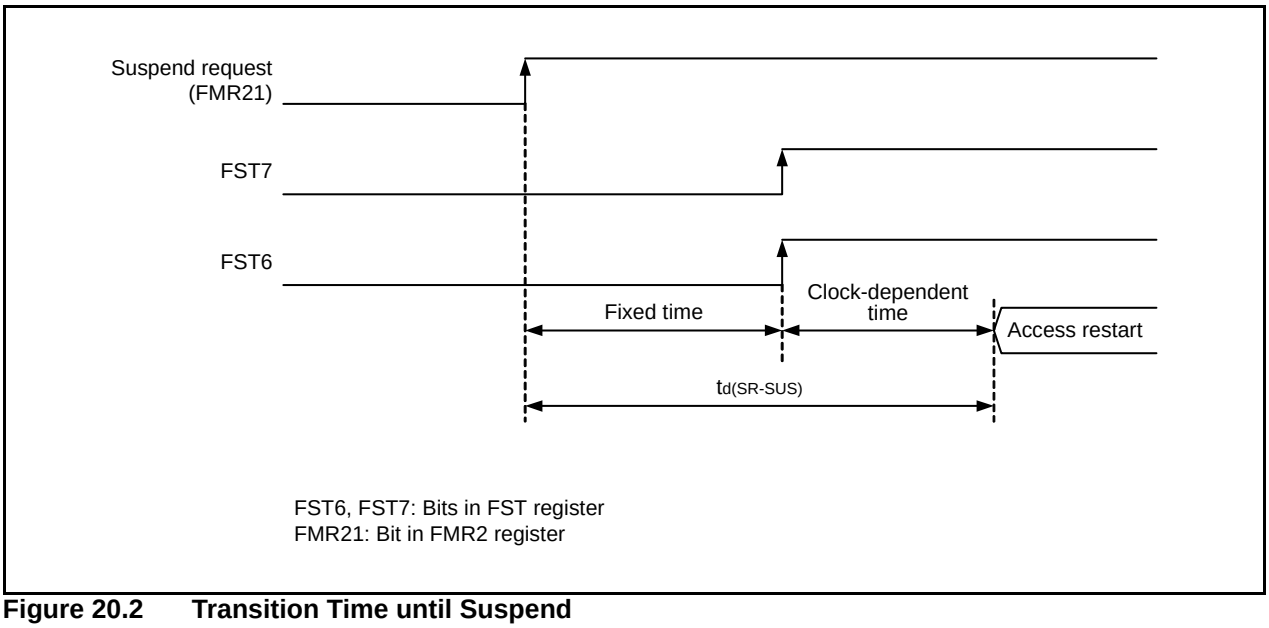


Figure 20.2 Transition Time until Suspend

Table 20.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	When Vcc decreases from 5 V to (Vdet0_0 - 0.1) V	—	30	—	µs
—	Self power consumption in voltage detection circuit	VC0E = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

Table 20.8 Voltage Detection 1 Circuit Electrical Characteristics

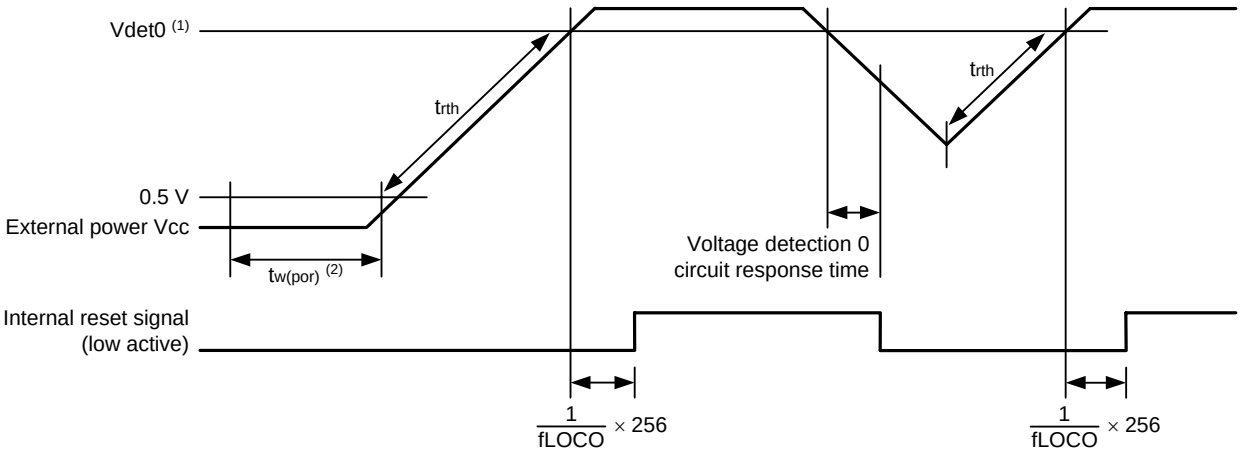
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_1 (2)	When Vcc decreases	2.15	2.35	2.55	V
	Voltage detection level Vdet1_3 (2)	When Vcc decreases	2.45	2.65	2.85	V
	Voltage detection level Vdet1_5 (2)	When Vcc decreases	2.75	2.95	3.15	V
	Voltage detection level Vdet1_7 (2)	When Vcc decreases	3.00	3.25	3.55	V
	Voltage detection level Vdet1_9 (2)	When Vcc decreases	3.30	3.55	3.85	V
	Voltage detection level Vdet1_B (2)	When Vcc decreases	3.60	3.85	4.15	V
	Voltage detection level Vdet1_D (2)	When Vcc decreases	3.90	4.15	4.45	V
	Voltage detection level Vdet1_F (2)	When Vcc decreases	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_1 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_7 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V	—	60	150	µs
—	Self power consumption in voltage detection circuit	VC1E = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.
3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.

Table 20.9 Power-On Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power Vcc rise gradient		0	—	50,000	mV/msec

Notes:
1. The measurement condition is Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. For details, see **7. Voltage Detection Circuit**.
2. $t_{w(por)}$ is required for a power-on reset to be enabled with the external power Vcc held below the valid voltage (0.5 V) to enable a power-on reset. When Vcc decreases with voltage monitor 0 reset disabled and then turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 20.3 Power-On Reset Circuit Electrical Characteristics

Table 20.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Package	Condition	Standard			Unit
				Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset is cleared	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	19.2	20.0	20.8	MHz
		14-pin DIP 20-pin DIP		19.0	20.0	21.0	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	19.0	20.0	21.0	MHz
	High-speed on-chip oscillator frequency when the FR18S0 register adjustment value is written into the FRV1 register and the FR18S1 register adjustment value into the FRV2 register (2)	14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	17.694	18.432	19.169	MHz
		14-pin DIP 20-pin DIP		17.510	18.432	19.353	MHz
		14-pin TSSOP 20-pin LSSOP	Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	17.510	18.432	19.353	MHz
—	Oscillation stabilization time	—		—	—	30	µs
—	Self power consumption at oscillation	—	Vcc = 5.0 V, Topr = 25 °C	—	530	—	µA

Notes:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0 % when the serial interface is used in UART mode.

Table 20.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stabilization time		—	—	35	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25 °C	—	2	—	µA

Note:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

Table 20.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25 °C.
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 20.13 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -20 mA	Vcc - 2.0	—	Vcc	V
			When drive capacity is low	I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 20 mA	—	—	2.0	V
			When drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 5 mA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 5 V		0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5 V, Vcc = 5.0 V		—	—	5.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 5.0 V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 4.0 V ≤ Vcc ≤ 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 20.14 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition							Standard			Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	125 kHz	No division	—		—	3	7.0	mA
			16 MHz	Off	125 kHz	No division	—		—	2.5	6.0	mA
			10 MHz	Off	125 kHz	No division	—		—	1.7	—	mA
			20 MHz	Off	125 kHz	Division by 8	—		—	1.5	—	mA
			16 MHz	Off	125 kHz	Division by 8	—		—	1.2	—	mA
			10 MHz	Off	125 kHz	Division by 8	—		—	1.0	—	mA
		High-speed on-chip oscillator mode	Off	20 MHz	125 kHz	No division			—	3.5	7.5	mA
			Off	20 MHz	125 kHz	Division by 8			—	2.0	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	270	µA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	100	µA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	90	µA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 5.0 V
4. Set the system clock to 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 5 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 20.15 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

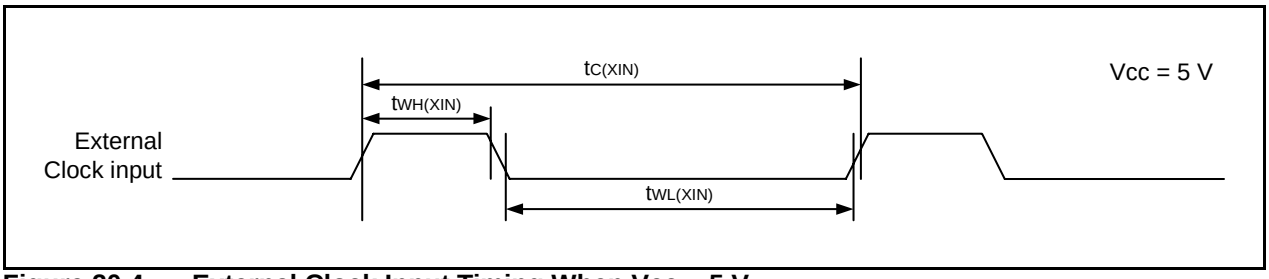


Figure 20.4 External Clock Input Timing When Vcc = 5 V

Table 20.16 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	40	—	ns

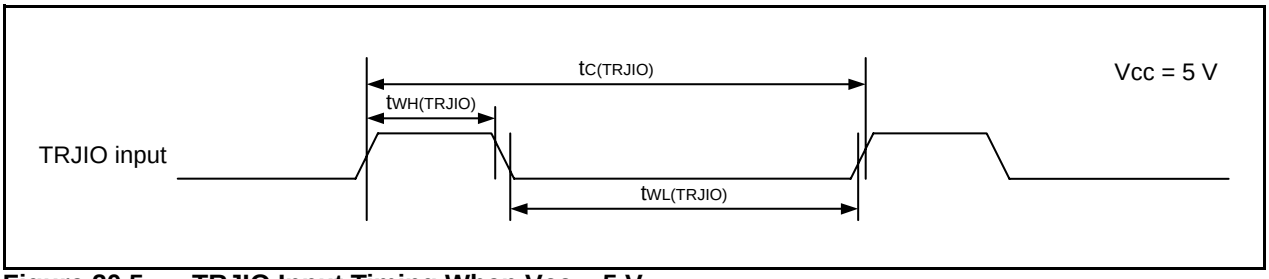


Figure 20.5 TRJIO Input Timing When Vcc = 5 V

Table 20.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	—	ns
$t_{W(CKH)}$	CLK0 input high width	100	—	ns
$t_{W(CKL)}$	CLK0 input low width	100	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	50	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

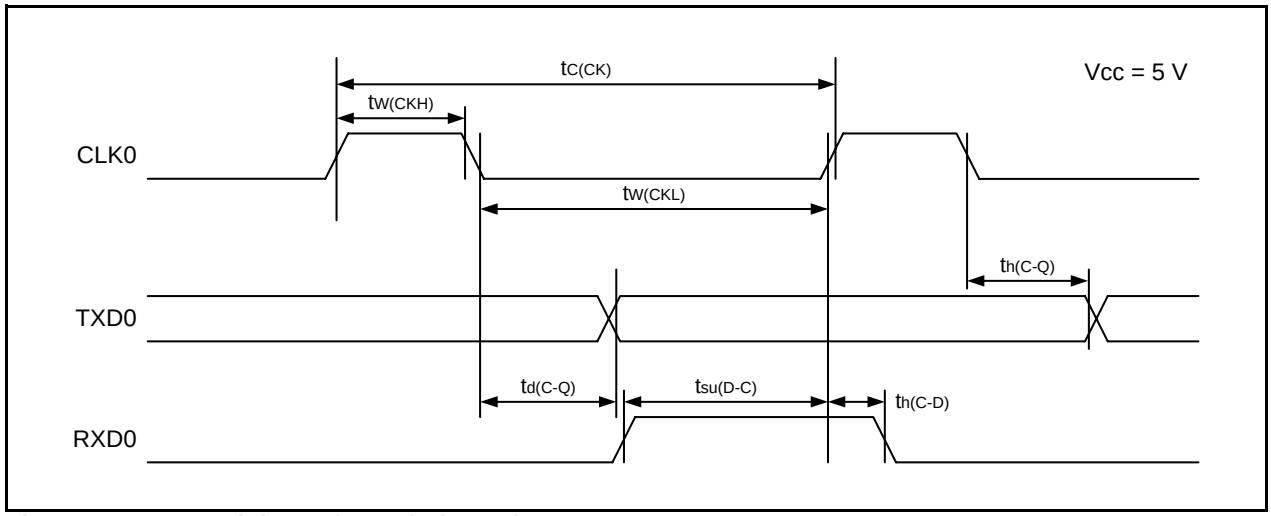


Figure 20.6 Serial Interface Timing When Vcc = 5 V

Table 20.18 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	250 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

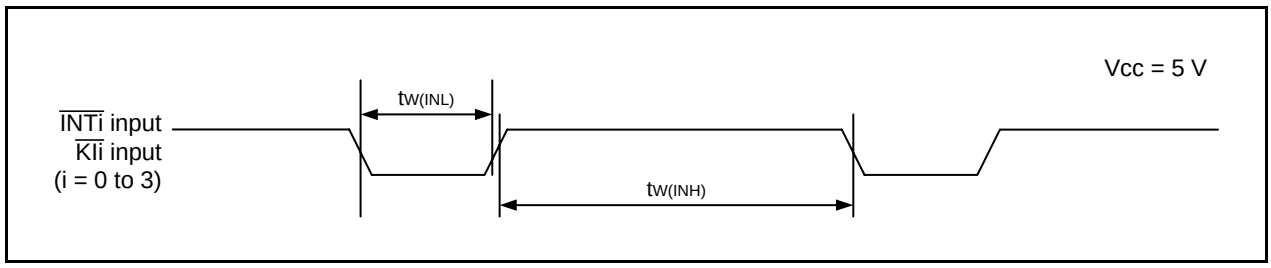


Figure 20.7 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 5 V

Table 20.19 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -5 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 3 V		0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3 V, Vcc = 3.0 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 3.0 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 2.7 V ≤ Vcc < 4.0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 10 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 20.20 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition							Standard			Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	125 kHz	No division	—		—	3.0	7.0	mA
			16 MHz	Off	125 kHz	No division	—		—	2.5	6.0	mA
			10 MHz	Off	125 kHz	No division	—		—	1.6	5.0	mA
			20 MHz	Off	125 kHz	Division by 8	—		—	1.5	—	mA
			16 MHz	Off	125 kHz	Division by 8	—		—	1.2	—	mA
			10 MHz	Off	125 kHz	Division by 8	—		—	0.9	4.5	mA
		High-speed on-chip oscillator mode	Off	20 MHz	125 kHz	No division			—	3.5	7.5	mA
			Off	20 MHz	125 kHz	Division by 8			—	2.0	—	mA
			Off	10 MHz (4)	125 kHz	No division			—	2.2	—	mA
			Off	10 MHz (4)	125 kHz	Division by 8			—	1.4	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	260	µA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	µA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	80	µA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 3.0 V
4. Set the system clock to 10 MHz or 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 3 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 20.21 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns

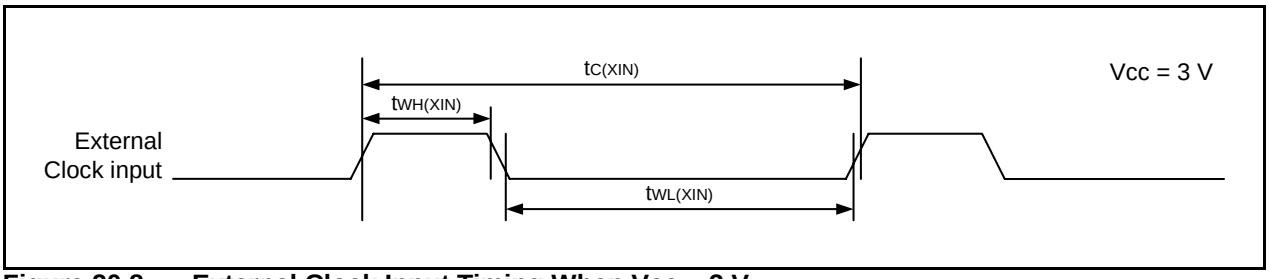


Figure 20.8 External Clock Input Timing When Vcc = 3 V

Table 20.22 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	ns

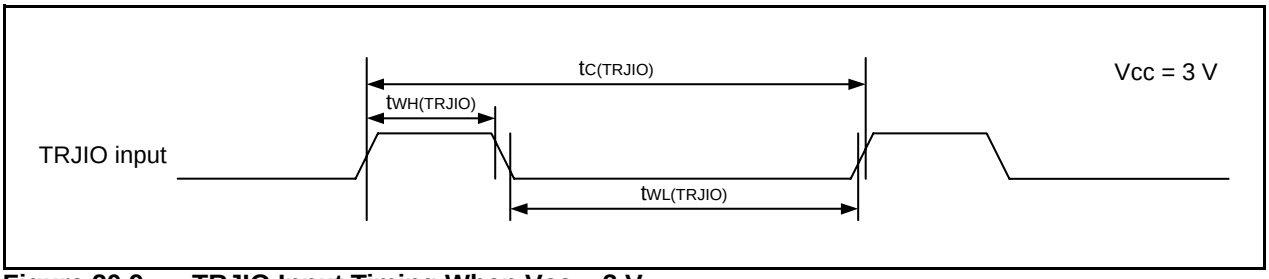


Figure 20.9 TRJIO Input Timing When Vcc = 3 V

Table 20.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{W(CKH)}$	CLK0 input high width	150	—	ns
$t_{W(CKL)}$	CLK0 input low width	150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	70	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

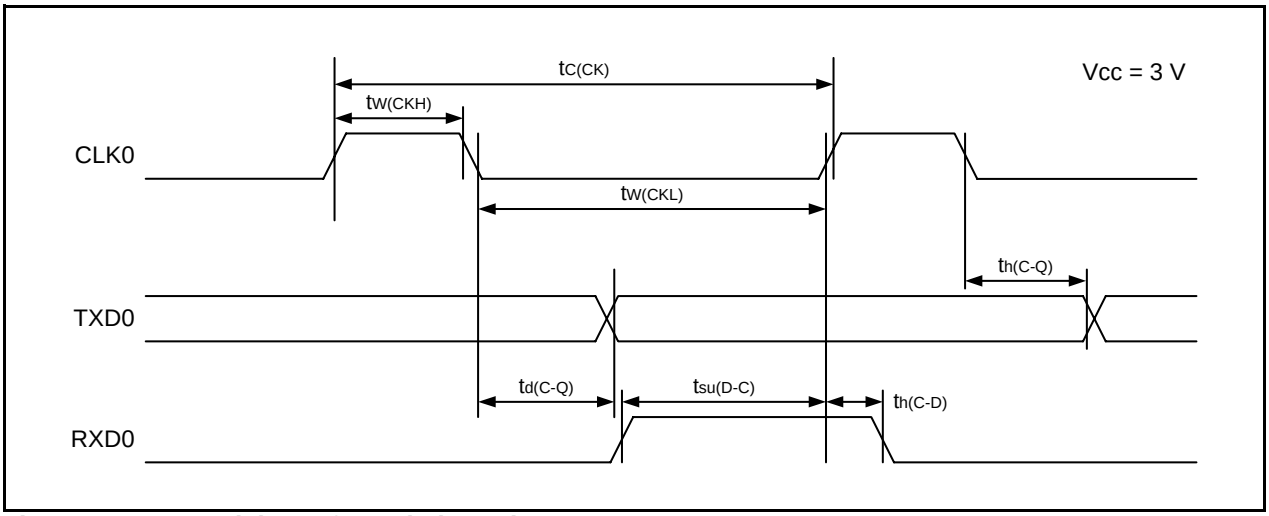


Figure 20.10 Serial Interface Timing When Vcc = 3 V

Table 20.24 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	380 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

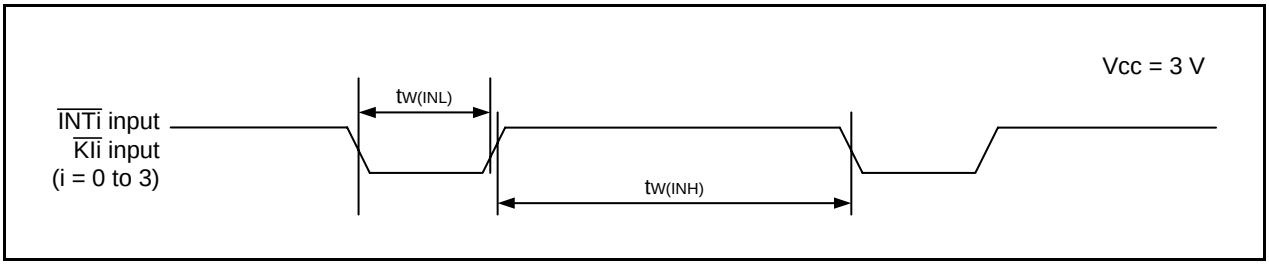


Figure 20.11 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 3 V

Table 20.25 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -2 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 2 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P1_0, P1_1, P1_6, P1_7, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 2.2 V		0.05	0.20	—	V
		$\overline{RESET}$	Vcc = 2.2 V		0.05	0.20	—	V
I_{IH}	Input high current		V_I = 2.2 V, Vcc = 2.2 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 2.2 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 1.8 V ≤ Vcc < 2.7 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 5 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 20.26 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition							Standard			Unit
			Oscillation Circuit	On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	125 kHz	No division	—		—	1.0	—	mA
			5 MHz	Off	125 kHz	Division by 8	—		—	0.6	—	mA
		High-speed on-chip oscillator mode	Off	5 MHz (4)	125 kHz	No division			—	1.6	6.5	mA
			Off	5 MHz (4)	125 kHz	Division by 8			—	1.1	—	mA
			Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	200	µA
		Wait mode	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	µA
			Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.0	80	µA
		Stop mode	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.5	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 2.2 V
4. Set the system clock to 5 MHz or 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 2.2 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified)

Table 20.27 External Clock Input (XIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	—	ns
$t_{WH(XIN)}$	XIN input high width	90	—	ns
$t_{WL(XIN)}$	XIN input low width	90	—	ns

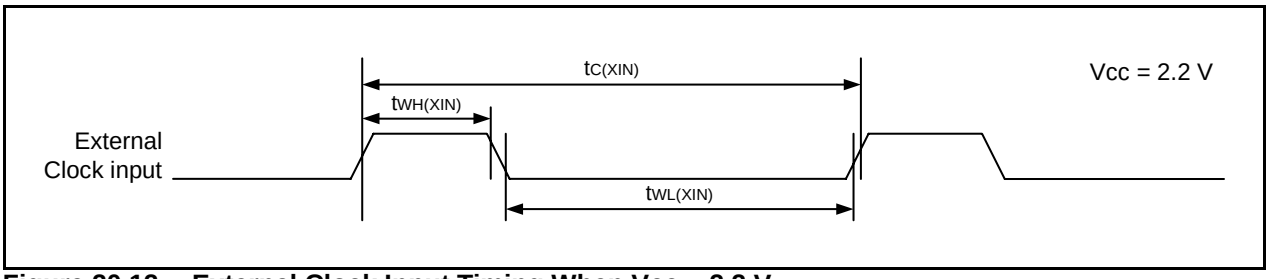


Figure 20.12 External Clock Input Timing When Vcc = 2.2 V

Table 20.28 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	500	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	200	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	200	—	ns

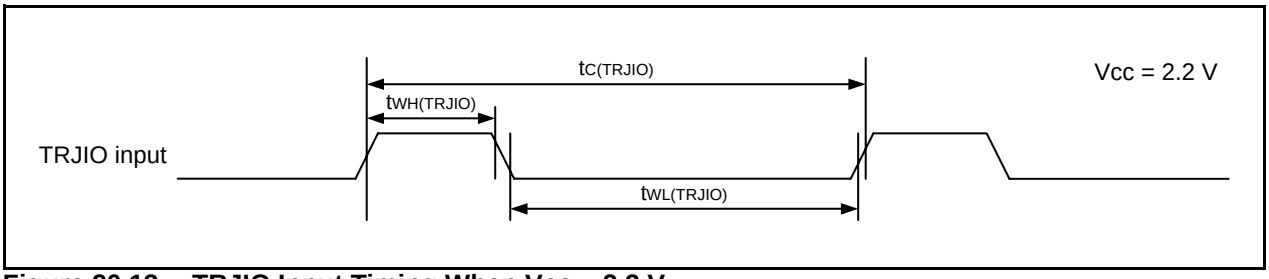


Figure 20.13 TRJIO Input Timing When Vcc = 2.2 V

Table 20.29 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	800	—	ns
$t_{W(CKH)}$	CLK0 input high width	400	—	ns
$t_{W(CKL)}$	CLK0 input low width	400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time	—	200	ns
$t_{h(C-Q)}$	TXD0 hold time	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time	150	—	ns
$t_{h(C-D)}$	RXD0 input hold time	90	—	ns

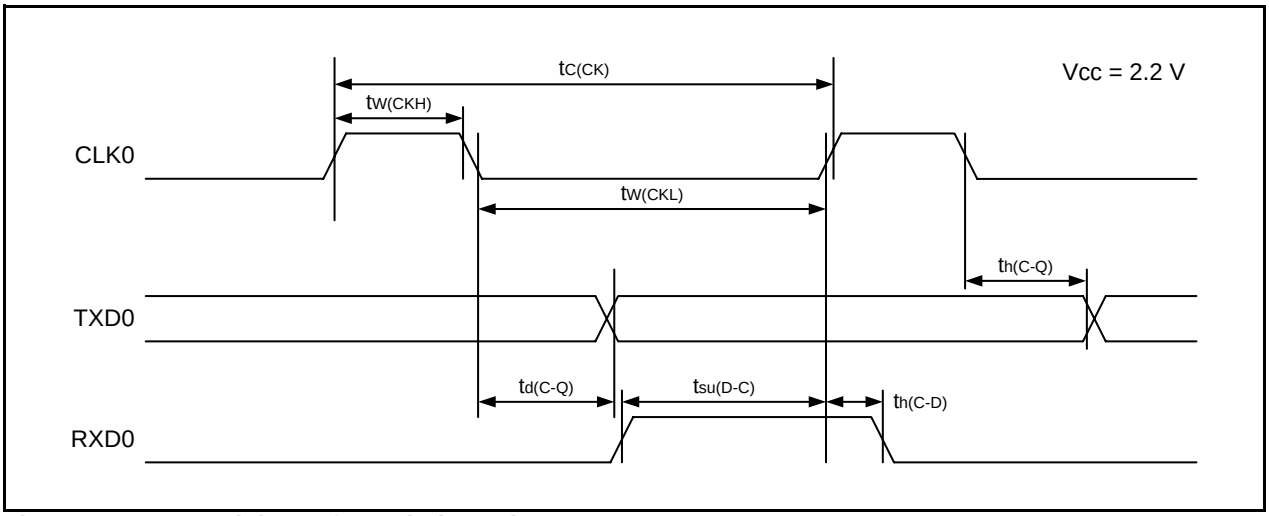


Figure 20.14 Serial Interface Timing When Vcc = 2.2 V

Table 20.30 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	1,000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	1,000 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

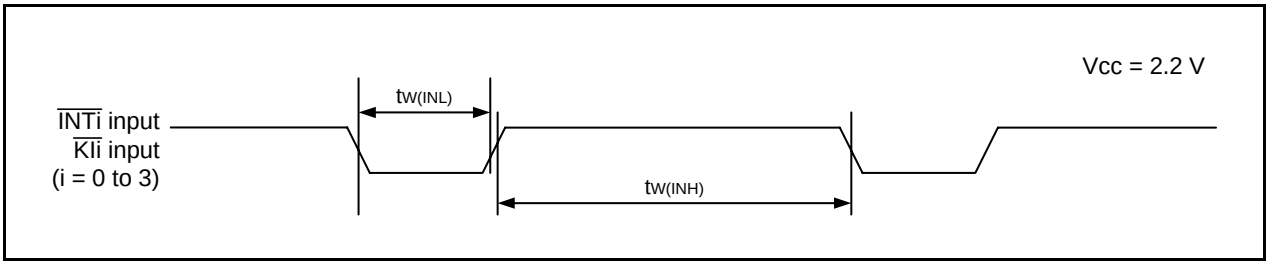


Figure 20.15 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 2.2 V

21. Usage Notes

21.1 Notes on System Control

21.1.1 Option Function Select Area Setting Example

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

Programming formats vary depending on the compiler. Check the compiler manual.

• To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)          ; RESET
```

Programming formats vary depending on the compiler. Check the compiler manual.

21.2 Notes on Watchdog Timer

- Do not switch the count sources during watchdog timer operation.
- There is a delay of two cycles of the count source from a write to the WDTR register until the initialization of the watchdog timer.
- Allow at least three cycles of the count source between the previous and the next initialization of the watchdog timer.

21.3 Notes on Clock Generation Circuit

21.3.1 Oscillation Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, so set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt disabled, oscillation stop detection function disabled).

21.3.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

21.4 Notes on Power Control

21.4.1 Program Restrictions When Entering Wait Mode

To enter wait mode by setting the WAITM bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the WAITM bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction. The 4 bytes of instruction data following the instruction that sets the WAITM bit to 1 (wait mode is entered) or the WAIT instruction are prefetched from the instruction queue and then the program stops. Insert at least four NOP instructions after the instruction that sets the WAITM bit to 1 (wait mode is entered) or after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        FSET    I               ; Interrupt enabled
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to set the WAITM bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to the SCKCR register enabled
        FCLR    I               ; Interrupt disabled
        BSET    5, SCKCR        ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to the SCKCR register disabled
        FSET    I               ; Interrupt enabled
```

21.4.2 Program Restrictions When Entering Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)). The 4 bytes of instruction data following the instruction that sets the STPM bit to 1 are prefetched from the instruction queue and then the program stops.
Insert at least four NOP instructions following the JMP.B instruction immediately after the instruction that sets the STPM bit to 1.

• Program example to enter stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CKSTPR register enabled
        FSET    I               ; Interrupt enabled
        BSET    0, CKSTPR       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

21.5 Notes on Interrupts

21.5.1 Reading Address 00000h

Do not read address 00000h by a program. When an external interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from address 00000h in the interrupt sequence. At this time, the corresponding bit in the IRR3 register for the acknowledged interrupt is set to 0.
If a program is used to read address 00000h, the corresponding bit in the IRR3 register for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

21.5.2 SP Setting

Set a value in the SP before any interrupt is acknowledged. The SP is 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

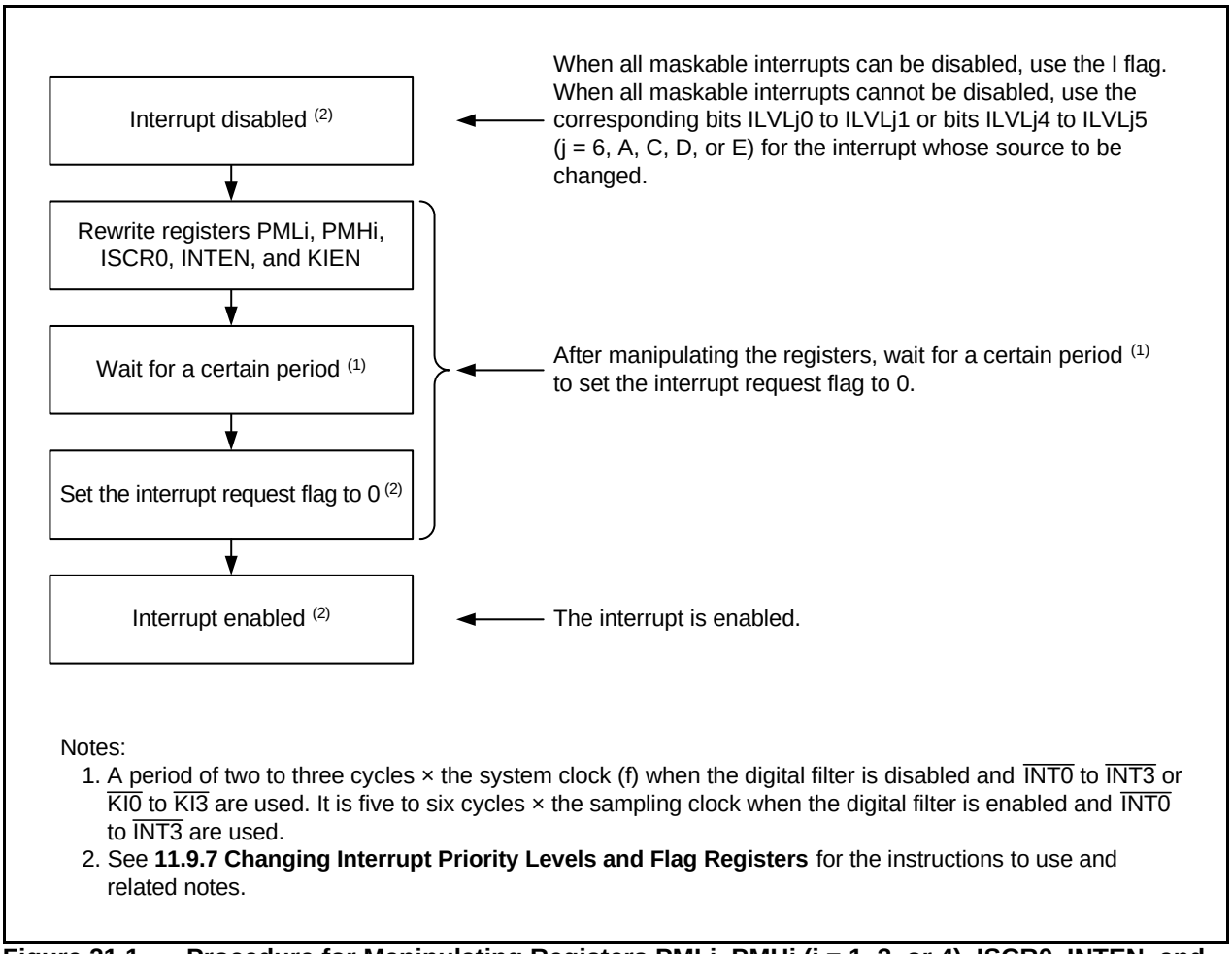
21.5.3 External Interrupt and Key Input Interrupt

Signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ must meet either the low-level width or the high-level width requirements shown in External Interrupt $\overline{\text{INTi}}$ Input (i = 0 to 3) in the Electrical Characteristics, regardless of the CPU operating clock. For details, see **Table 20.18** (Vcc = 5 V), **Table 20.24** (Vcc = 3 V), and **Table 20.30** (Vcc = 2.2 V) **External Interrupt $\overline{\text{INTi}}$ Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)**.

21.5.4 Rewriting Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN

When changing the functions of the $\overline{INT0}$ to $\overline{INT3}$ and $\overline{KI0}$ to $\overline{KI3}$ interrupts, an interrupt request flag may be set to 1 by rewriting registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN. When an interrupt function is switched, rewrite these registers with interrupt requests disabled, and wait for a certain period (1) before setting the interrupt request flag to 0.
Figure 21.1 shows the Procedure for Manipulating Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0.

Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.



Notes:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.
2. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers** for the instructions to use and related notes.

Figure 21.1 Procedure for Manipulating Registers PMLi, PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0

21.5.5 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) When Returning from Wait Mode or Stop Mode to Standard Mode

When a transition is made to wait mode or stop mode with the WCKSTP bit in the CKSTPR register set to 1 (system clock stopped in wait mode) while in use of the $\overline{\text{INTi}}$ input filter, the $\overline{\text{INTi}}$ interrupt cannot be used to return to standard operating mode.

When the $\overline{\text{INTi}}$ interrupt is used to return, set the WCKSTP bit to 1 and bits INTiF1 to INTiF0 in the INTF0 register to 00b (no filter) before a transition is made to wait mode or stop mode. When the $\overline{\text{INTi}}$ input filter is used again, select the sampling clock with bits INTiF0 to INTiF1 to enable the INTiEN bit in the INTEN register.

Figure 21.2 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used.

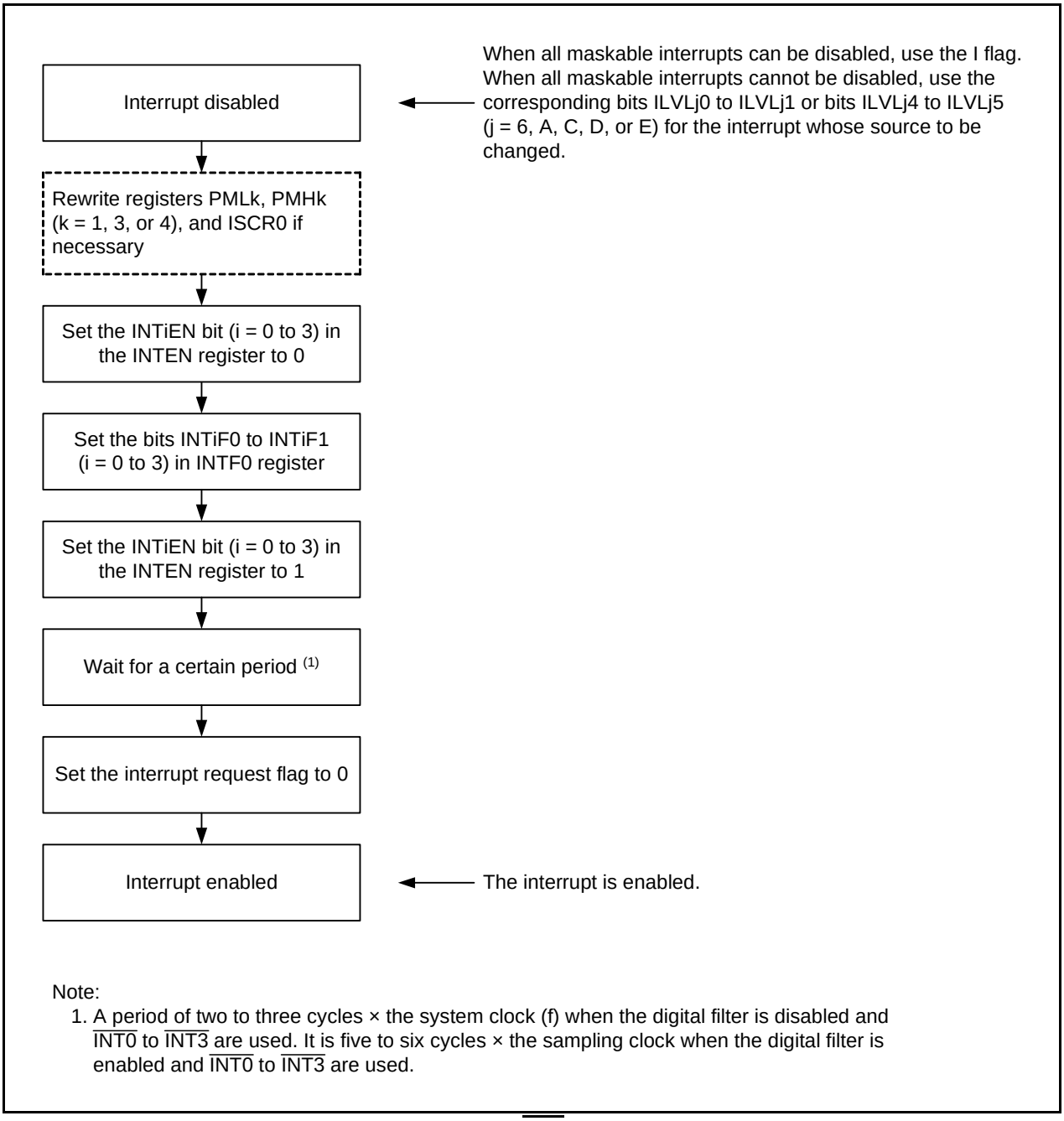
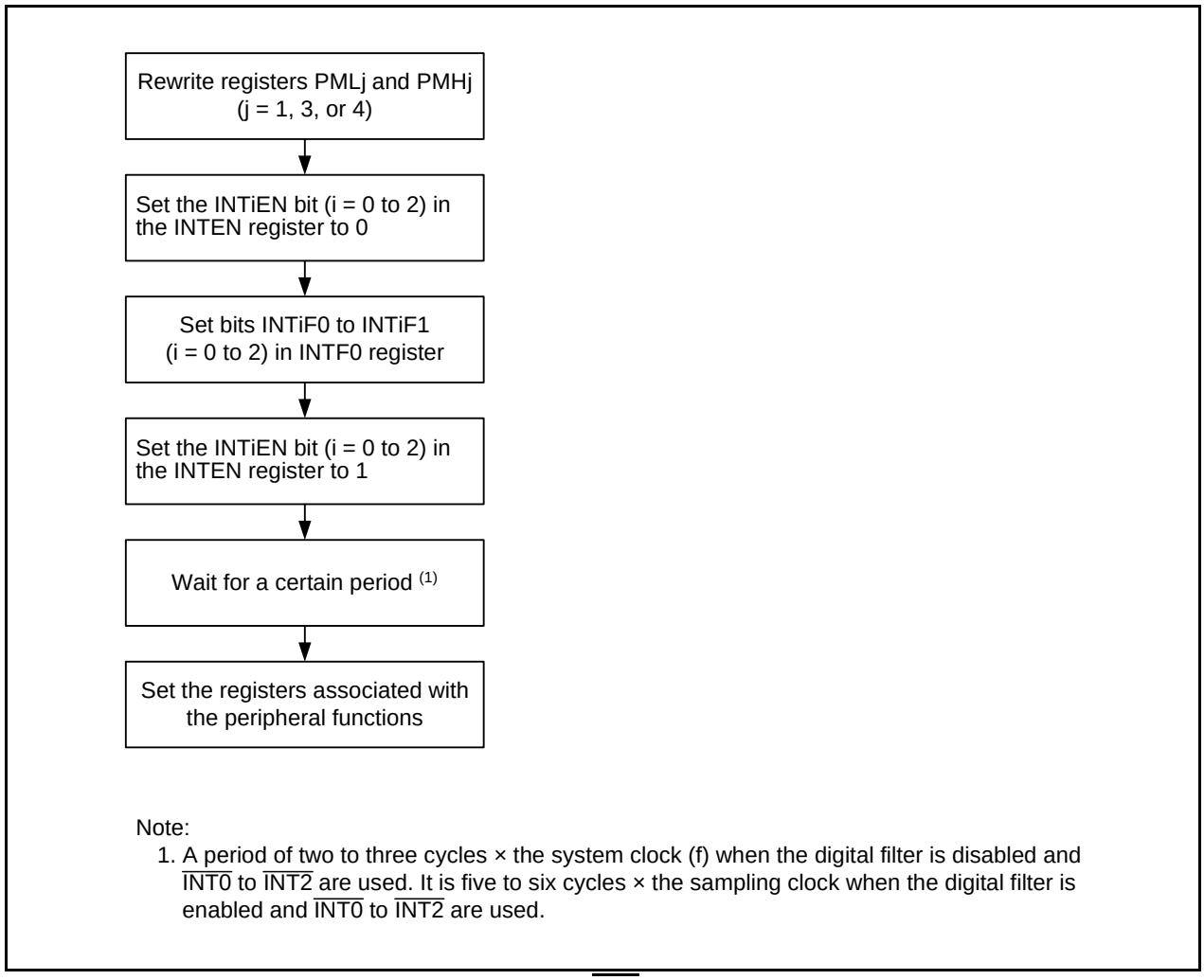


Figure 21.2 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used

21.5.6 Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions

Figure 21.3 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC).



Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used.

Figure 21.3 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC)

21.5.7 Changing Interrupt Priority Levels and Flag Registers

(a) The interrupt priority level and the flag register must be changed only while no interrupt requests are generated. If an interrupt may be generated, using the I flag to disable the interrupt before changing the interrupt priority level and the flag register.

(b) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the interrupt priority level and the flag register are changed due to effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instruction to separate the interrupt priority level and the flag register operation, and I flag operation.

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #0CFH, ILVLE    ; Set INT0 interrupt priority level 0
    POPC    FLG             ; Enable interrupts
```

21.6 Notes on I/O Ports

21.6.1 Notes on PA_0 Pin

The PA_0 pin is multiplexed with the hardware reset function ($\overline{\text{RESET}}$). The PA_0 pin functions as the $\overline{\text{RESET}}$ function after any reset (hardware reset, power-on reset, voltage monitor 0 reset by voltage detection circuit, watchdog timer reset, and software reset) occurs. After the reset is cleared, the PA_0 pin can be set to the I/O port function or the hardware reset function by the HWRSTE bit in the PAMCR register. When a low level is input to the $\overline{\text{RESET}}$ pin before a reset is cleared, the level will be recognized by the MCU as hardware reset and the reset state will not be cleared until a high level is input to the $\overline{\text{RESET}}$ pin.
When the HWRSTE bit is set to 0, the $\overline{\text{RESET}}$/PA_0 pin becomes the PA_0 I/O port. When this pin is used as an input port, an external pull-up resistor must be connected. When used as an output port, the open-drain output function must be enabled to avoid conflicting with an external reset signal accidently. See the following assembly language.

• Program example to set PA_0 as an output port

```
MOV.B    #00000000b, HRPR
MOV.B    #00000001b, HRPR      ; PAMCRE = 1, un-protect PAMCR register
;
MOV.B    #00000001b, PAMCR     ; HWRSTE = 0, PODA_0 = 1
MOV.B    #00000001b, PDA       ; PDA_0 = 1, PA_0 output L
;
...
MOV.B    #00000001b, PA        ; PA_0 become hiz output (open drain)
```

21.6.2 I/O Pins for Peripheral Functions

In this MCU, the pin assignment of the peripheral functions can be changed using the port function mapping register. However, multiple pins must not be assigned to the same peripheral function input at the same time. Otherwise, no signal can be input correctly.

21.7 Notes on Timer RJ2

(1) Timer RJ2 stops counting after a reset. Start the count only after setting the value in the timer.

(2) After 1 (count is started) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started from the first active edge of the count source after the TCSTF bit is set to 1. After 0 (count is stopped) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 0.
Note:
1. Registers associated with timer RJ2: TRJ, TRJCR, TRJIOC, and TRJMR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count is started) and then input an external pulse.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program but remain unchanged even if 1 is written to these bits. If a read-modify-write instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In this case, write 1 using the MOV instruction to the TEDGF or TUNDF bit which is not supposed to be set to 0.

(5) Insert NOP instructions between writing to and reading from registers associated with the TRJ counter while the counter is stopped.

(6) When the TSTART bit in the TRJCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), allow at least three cycles of the count source clock for each write interval when writing to the TRJ register successively.

(7) Note the following when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.
Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.
When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.
Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.
After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.

(8) When the TEDGSEL bit in the TRJIOC register is set to 0 (count on rising edge) and the external signal (TRJIO) is counted in event counter mode, the signal may not be counted correctly depending on the state of the TSTART bit in the TRJCR register (see Figure 21.4).
If the TRJIO pin is set to low before the TSTART bit is set to 1 (count is started) and a valid event is input after the TSTART bit is set to 1, the signal is not counted on the first rising edge of the TRJIO input.
Thus, the number of counted events is obtained as follows:
Number of counted events = {(initial value in the counter – value in the counter on completion of the valid event + 1) + 1}
To avoid this, set the TRJIO pin to low after setting the TSTART bit to 1 (count is started) (see Figure 21.5).

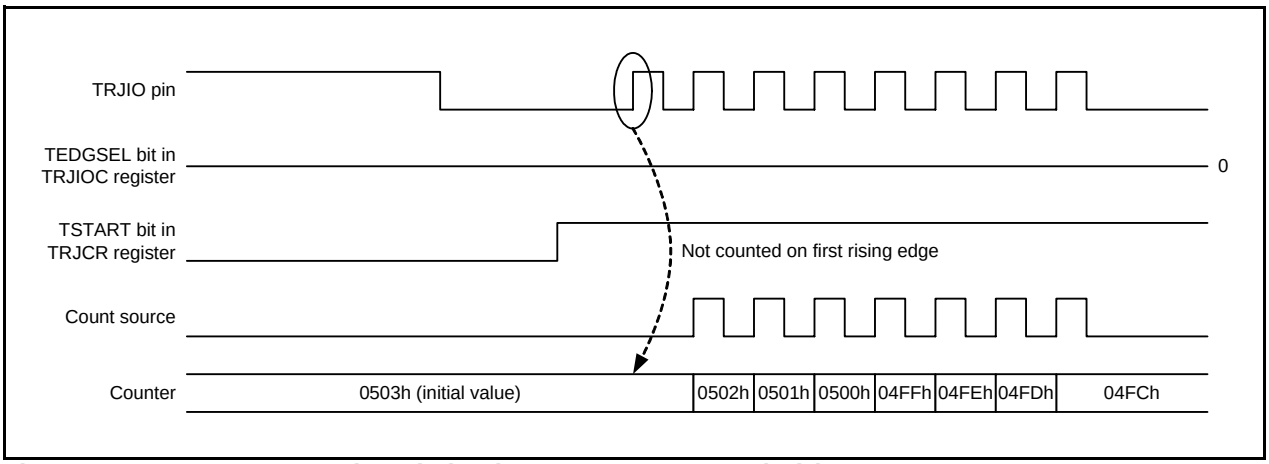


Figure 21.4 TSTART Setting Timing in Event Counter Mode (1)

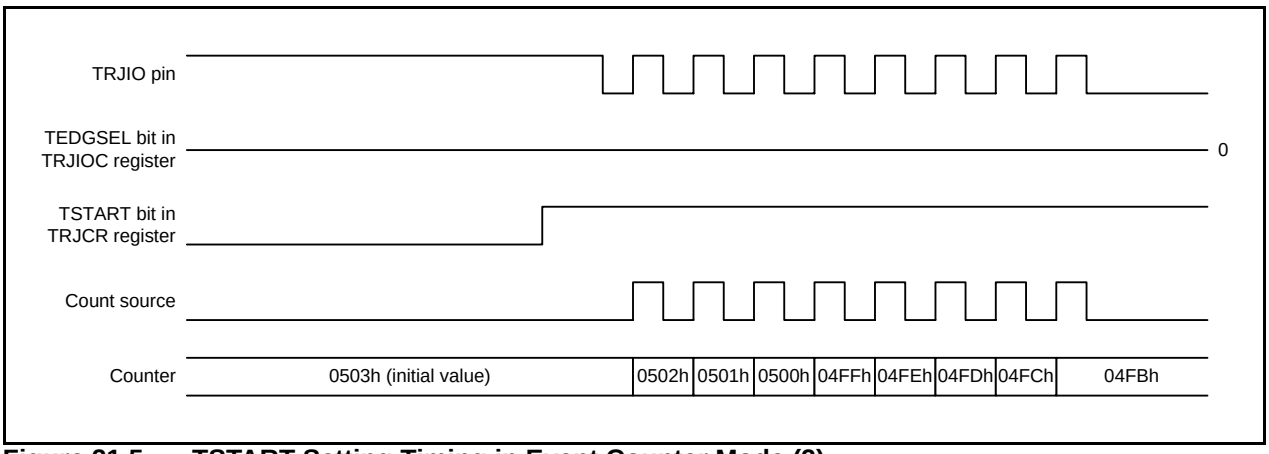


Figure 21.5 TSTART Setting Timing in Event Counter Mode (2)

(9) When the TEDGSEL bit in the TRJIOC register is set to 1 (count on falling edge) and the external signal (TRJIO) is counted in event counter mode, the signal may not be counted correctly depending on the state of the TSTART bit in the TRJCR register (see Figure 21.6).
Even if the TRJIO pin is set to low after the TSTART bit is set to 1 (count is started), the signal is not counted on the falling edge.
Thus, the number of counted events is obtained as follows:
Number of counted events = {(initial value in the counter – value in the counter on completion of the valid event + 1) + 1}
To avoid this, set the TSTART bit to 1 (count is started) and input a valid event after setting the TRJIO pin to low (see Figure 21.7).

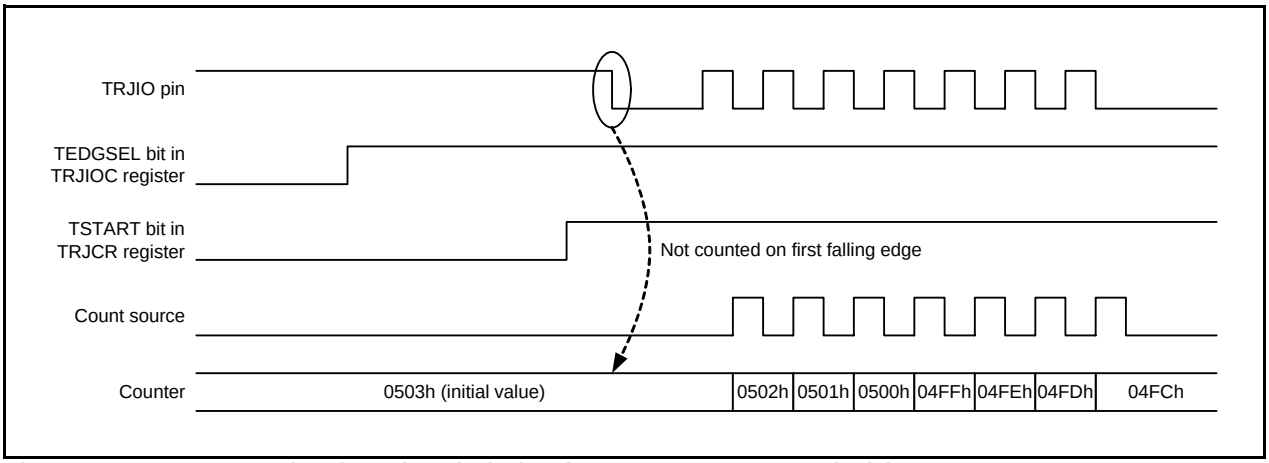


Figure 21.6 External Pulse Signal Timing in Event Counter Mode (1)

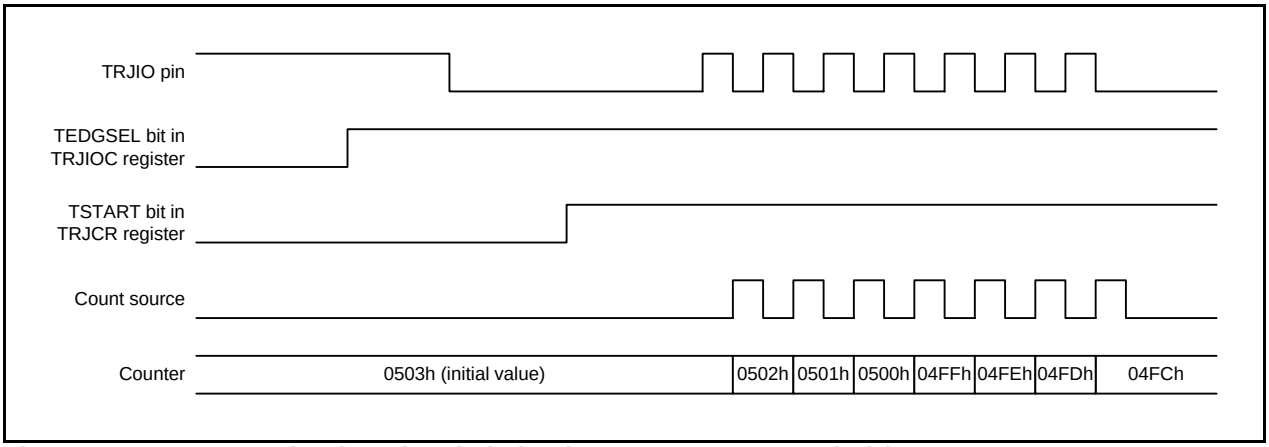


Figure 21.7 External Pulse Signal Timing in Event Counter Mode (2)

21.8 Notes on Timer RB2

- Timer RB2 stops counting after a reset. Start the count after setting the value in the timer and prescaler.
- In the 8-bit timer with 8-bit prescaler, even if the prescaler and timer are read in 16-bit units, they are actually read sequentially byte by byte in the MCU. This may cause the value in the timer to be updated during reading of these two registers.
  In the 16-bit timer, access the TRBPRE register first and then the TRBPR register. Read the TRBPRE register first to read the count value in the lower byte. The count value in the higher byte will be retained. Next, read the TRBPR register to read the retained value in the higher byte. The timer value is not updated during reading of these two registers.
- In programmable one-shot and programmable wait one-shot generation modes, when the TOSSP bit in the TRBOCR register is set to 1 and the one-shot is stopped, the timer reloads the reload register value and is stopped. The timer count value must be read before the timer is stopped.
- After 1 (count is started) is written to the TSTART bit in the TRBCR register while the count is stopped, the TCSTF bit in the TRBCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started on the first active edge of the counter source after the TCSTF bit is set to 1.
  After 0 (count is stopped) is written to the TSTART bit during count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 0.
  Note:
  1. Registers associated with timer RB2:
     TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBPR, and TRBSC
- In timer mode, do not set both the TRBPRE and TRBPR registers to 00h at the same time.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), change the values of registers TRBPRE, TRBPR, and TRBSC, then wait for at least two cycles of the system clock (f) before setting the TSTART bit in the TRBCR register to 1 (count is started).
- When the TSTART bit in the TRBCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), do not change the values in registers TRBIOC and TRBMR, and the TRBIE bit in the TRBIR register.
- Make sure the TCSTF bit in the TRBCR register is 1 (count is in progress) before writing 1 (one-shot count is started) to the TOSST bit in the TRBOCR register. When the TCSTF bit is 0 (count is stopped), writing 1 (one-shot count is started) to the TOSST bit is invalid.
- When writing to registers TRBPRE, TRBPR, and TRBSC during count operation (the TSTART bit is 1 or the TCSTF bit is 1), note the following points:
  - When writing to the TRBPRE register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBPR register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBSC register successively, allow at least three cycles of the count source for each write interval.
- When the TRBPR register is rewritten in programmable waveform generation mode, do not write to the TRBPRE, TRBPR, or TRBSC register during the secondary output period as described below after rewriting.
  - 8-bit timer with 8-bit prescaler:
    Two cycles of the prescaler underflow before the secondary output period ends.
  - 16-bit timer:
    Two cycles of the count source clock before the secondary output period ends.
- When the underflow signal from timer RJ2 is used as the count source for timer RB2, set timer RJ2 to timer mode, pulse output mode, or event counter mode.

- When 1 is written to the TOSST bit or the TOSSP bit in the TRBOCR register, the TOSSTF bit is changed after two to three cycles of the count source. If 1 is written to the TOSSP bit from when 1 is written to the TOSST bit until the TOSSTF bit is set to 1, the TOSSTF bit may be set to 0 or 1 depending on the internal state. Likewise, if 1 is written to the TOSST bit from when 1 is written to the TOSSP bit until the TOSSTF bit is set to 0, the TOSSTF may be set to 0 or 1 depending on the internal state.
- In programmable waveform generation mode and programmable wait one-shot mode, write to the TRBSC register before writing to the TRBPR register. At the underflow during the secondary period after the TRBPR register is written, the value written to the TRBPR register is transferred to the counter. If registers TRBPR and TRBSC are written two or more times after the TRBPR register is written until the underflow during the secondary period, the last written value is transferred to the counter at the underflow.
- When 1 is written to the TSTOP bit in the TRBCR register during count operation, timer RB2 is immediately stopped.
- If the count is forcibly stopped by writing 1 to the TSTOP bit during count operation, the TRBIF bit in the TRBIR register may be set to 1 (interrupt requested). Set the TRBIF bit to 0 (no interrupt requested) before restarting the count.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), wait for at least two cycles of the system clock (f) after writing the values of registers TRBPRE and TRBPR before reading them.

21.9 Notes on Timer RC

21.9.1 TRCCNT Register

The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A).

- When writing a value to the TRCCNT register by a program while the CTS bit in the TRCMR register is set to 1 (count is started), ensure that the write timing does not coincide with when the TRCCNT register is set to 0000h.
- If the timing when the TRCCNT register is set to 0000h and is written coincide with each other, the value is not be written and the TRCCNT register is set to 0000h.

If the TRCCNT register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.W   #XXXXh, TRCCNT      ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.W   TRCCNT, DATA        ; Read
```

21.9.2 TRCCR1 Register

To set bits CKS2 to CKS0 in the TRCCR1 register to 110b (fHOCO), set fHOCO to the clock frequency higher than the system clock frequency.

21.9.3 TRCSR Register

If the TRCSR register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.B   #XXh, TRCSR         ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.B   TRCSR, DATA         ; Read
```

21.9.4 Count Source Switching

When switching the count sources, stop the count before switching. After switching the count sources, wait for at least two cycles of the system clock before writing to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Write to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

When changing the count source from fHOCO to another source and stopping fHOCO, wait for at least two cycles of the system clock after changing the clock setting before stopping fHOCO.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Set the HOCOE bit in the OCOCR register to 0 (high-speed on-chip oscillator off).

21.9.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 15.1 Timer RC Specifications**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 15.19 Digital Filter Circuit Block Diagram**)

- The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

21.9.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (increment is stopped), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

21.9.7 MSTCR Register

After stopping the timer RC count, set the MSTTRC bit in the MSTCR register to 1 (standby).

21.9.8 Mode Switching

- When switching the modes during operation, set the CTS bit in the TRCMR register to 0 (count is stopped) before switching.
- After switching the modes, set each flag in the TRCSR register to 0 before operation is started.

21.9.9 Procedure for Setting Registers Associated with Timer RC

Set the registers associated with timer RC following the procedure below:
(1) Set timer RC operating mode (bits PWMB, PWMC, PWMD, and PWM2 in the TRCMR register).
(2) Set the registers other than that set in (1).
(3) Set the port output to be enabled (bits EA to ED in the TRCOER register).

21.10 Notes on Serial Interface (UART0)

Regardless of clock synchronous I/O mode or clock asynchronous I/O mode, read the U0RB register in 16-bit units.
When the U0RBH register is read, bits FER and PER in the U0RB register are set to 0 (no framing error, no parity error). Also, the RI bit in the U0C1 register is set to 0 (the U0RB register empty).
To check receive errors, use the data read from the U0RB register.

• Program example to read the receive buffer register

```
MOV.W    0086H, R0        ; Read the U0RB register
```

When the transfer data is 9 bits long in clock asynchronous I/O mode, write to the U0TB register in the order U0TBH first and then U0TBL in 8-bit units.

• Program example to write to the transmit buffer register

```
MOV.B    #XXH, 0083H      ; Write to the U0TBH register
MOV.B    #XXH, 0082H      ; Write to the U0TBL register
```

Do not set the MSTUART bit in the MSTCR register to 1 (standby) during communication. When setting the module to the standby state, confirm whether communication has completed. After communication has completed, set bits TE and RE in the U0C1 register to 0 (communication disabled) before setting the module to the standby state. After the module standby state is cleared, the initial settings for communication must be set again.

21.11 Notes on A/D Converter

21.11.1 A/D Converter Standby Setting

The A/D converter can be set to standby or active using the MSTAD bit in the MSTCR register.
Stop A/D conversion before setting to module standby. Register access is enabled by clearing the A/D converter standby state. For details, see **5. System Control**.

21.11.2 Sensor Output Impedance during A/D Conversion

To perform A/D conversion accurately, charging of the internal capacitor C shown in Figure 21.8 must be completed within the period of time specified as T (sampling time). Let the output impedance of the sensor equivalent circuit be R0, the internal resistance of the microcomputer be R, the accuracy (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in 10-bit mode).

$$\text{VC is generally } VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$$

$$\text{And when } t = T,\ VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

$$\text{Hence, } R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$$

Figure 21.8 shows the Analog Input Pin and External Sensor Equivalent Circuit. The user can obtain an impedance R0 that makes the pin-to-pin voltage VC increase from 0 to VIN – (0.1/1024) VIN within time T when the difference between VIN and VC becomes 0.1 LSB. The value, (0.1/1024) indicates a precondition for the calculation of R0 when the degradation due to insufficient capacitor charge is suppressed to 0.1 LSB during A/D conversion in 10-bit mode. The actual error, however, is the absolute accuracy plus 0.1 LSB.
A/D conversion clock = 20 MHz, T = 0.8 μs. Output impedance R0 through which an capacitor C is fully charged within T is obtained as follows:

T = 0.8 μs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.8 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 4.4 \times 10^{3}$$

Thus the maximum output impedance of a sensor circuit for an accuracy (error) of 0.1 LSB or less is 4.4 kΩ maximum.

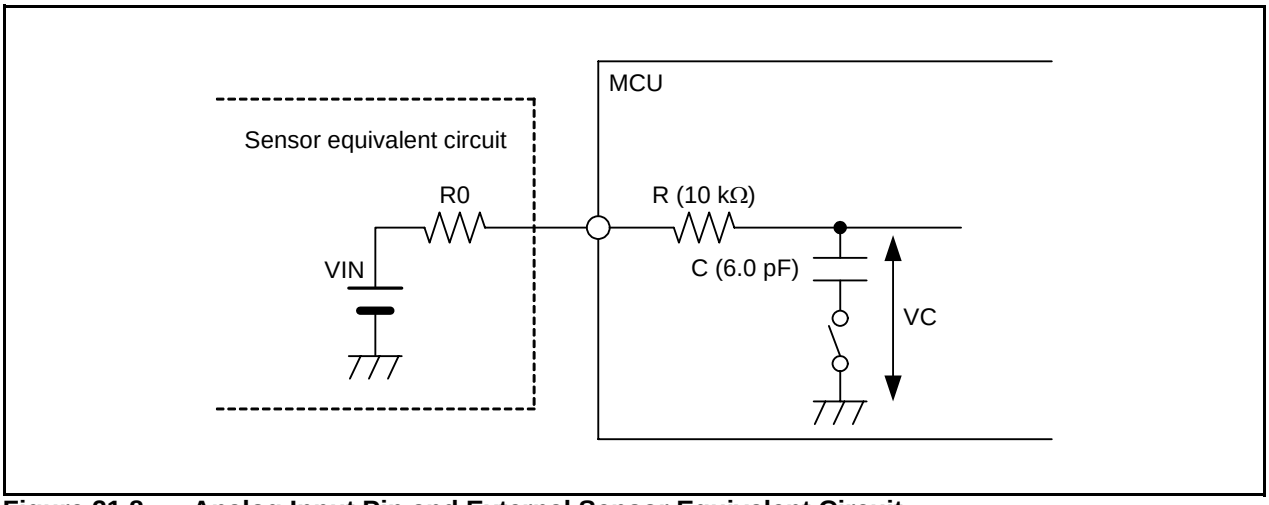


Figure 21.8 Analog Input Pin and External Sensor Equivalent Circuit

21.11.3 Register Setting

- Registers ADMOD and ADINSEL must be written only when A/D conversion is stopped.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion while the WCKSTP bit in the CKSTPR register is 1 (system clock is stopped in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) or the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) during A/D conversion.
- During A/D conversion, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate the conversion, the conversion result from the A/D converter will be undefined and no interrupt will be generated. The value of the ADi register (i = 0 or 1) which is not engaged in A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use any of the values of the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

21.12 Notes on Flash Memory

21.12.1 ID Code Area Setting Example

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set 55h in all of the ID code area

```
  .org 00FFDCH
  .lword dummy | (55000000h)      ; UND
  .lword dummy | (55000000h)      ; INTO
  .lword dummy                    ; BREAK
  .lword dummy | (55000000h)      ; ADDRESS MATCH
  .lword dummy | (55000000h)      ; SET SINGLE STEP
  .lword dummy | (55000000h)      ; WDT
  .lword dummy | (55000000h)      ; RESERVE
  .lword dummy | (55000000h)      ; RESERVE
```

Programming formats vary depending on the compiler. Check the compiler manual.

21.12.2 CPU Rewrite Mode

21.12.2.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory:
UND, INTO, and BRK

21.12.2.2 Interrupts

Tables 21.1 and 21.2 list the Interrupt Handling during CPU Rewrite Operation.

Table 21.1 Interrupt Handling during CPU Rewrite Operation (EW0 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, interrupt handling is executed. (The interrupt vector is allocated in the RAM) The suspend state can be entered by either of the following: (1) When the FMR22 bit is 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS). (2) When the FMR22 bit is 0 (suspend request disabled by interrupt request) and suspend is required, set the FMR21 bit to 1 (suspend request) in the interrupt handling. The flash memory suspends auto-erase or auto-programming after td(SR-SUS). While auto-erase is suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. While auto-programming is suspended, any block other than the blocks being auto-programmed can be read. Auto-erase can be restarted by setting the FMR21 bit to 0 (restart).	Interrupt handling is executed with auto-erase or auto-programming executed (The interrupt vector is allocated in the RAM)
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register
Note:
1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

Table 21.2 Interrupt Handling during CPU Rewrite Operation (EW1 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, the FMR21 bit is automatically set to 1 (suspend request) if the FMR22 bit is 1 (suspend request enabled by interrupt request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS) and interrupt handling is executed. When auto-erase is being suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. When auto-programming is being suspended, any block other than the blocks being auto-programmed can be read. After interrupt handling completes, auto-erase or auto-programming can be restarted by setting the FMR21 bit is set to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.	Auto-erase or auto-programming has priority. Interrupt handling is executed after auto-erase or auto-programming.
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register

Note:

1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
   When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

21.12.2.3 Access Methods

To set one of the following bits to 1, first write 0 and then 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
• The FMR01 or FMR02 bit in the FMR0 register
• The FMR13 bit in the FMR1 register
• The FMR20, FMR22, or FMR27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Interrupts must be disabled between writing 1 and then writing 0.
The FMR16 or FMR17 bit in the FMR1 register

21.12.2.4 Rewriting User ROM Area

When EW0 mode is used and the supply voltage falls while rewriting a block where a rewrite control program is stored, the rewrite control program is not be rewritten correctly. As a result, it may not be possible to rewrite the flash memory afterwards. Use standard serial I/O mode to rewrite this block.

21.12.2.5 Programming

Do not perform even a single additional write to an already programmed address.

21.12.2.6 Entering Wait Mode or Stop Mode

Do not enter wait mode or stop mode during suspend.
When the FST7 bit in the FST register is 0 (busy) while programming or erasing the flash memory, do not enter wait mode or stop mode.
Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory is stopped).

21.12.2.7 Flash Memory Programming and Erase Voltages

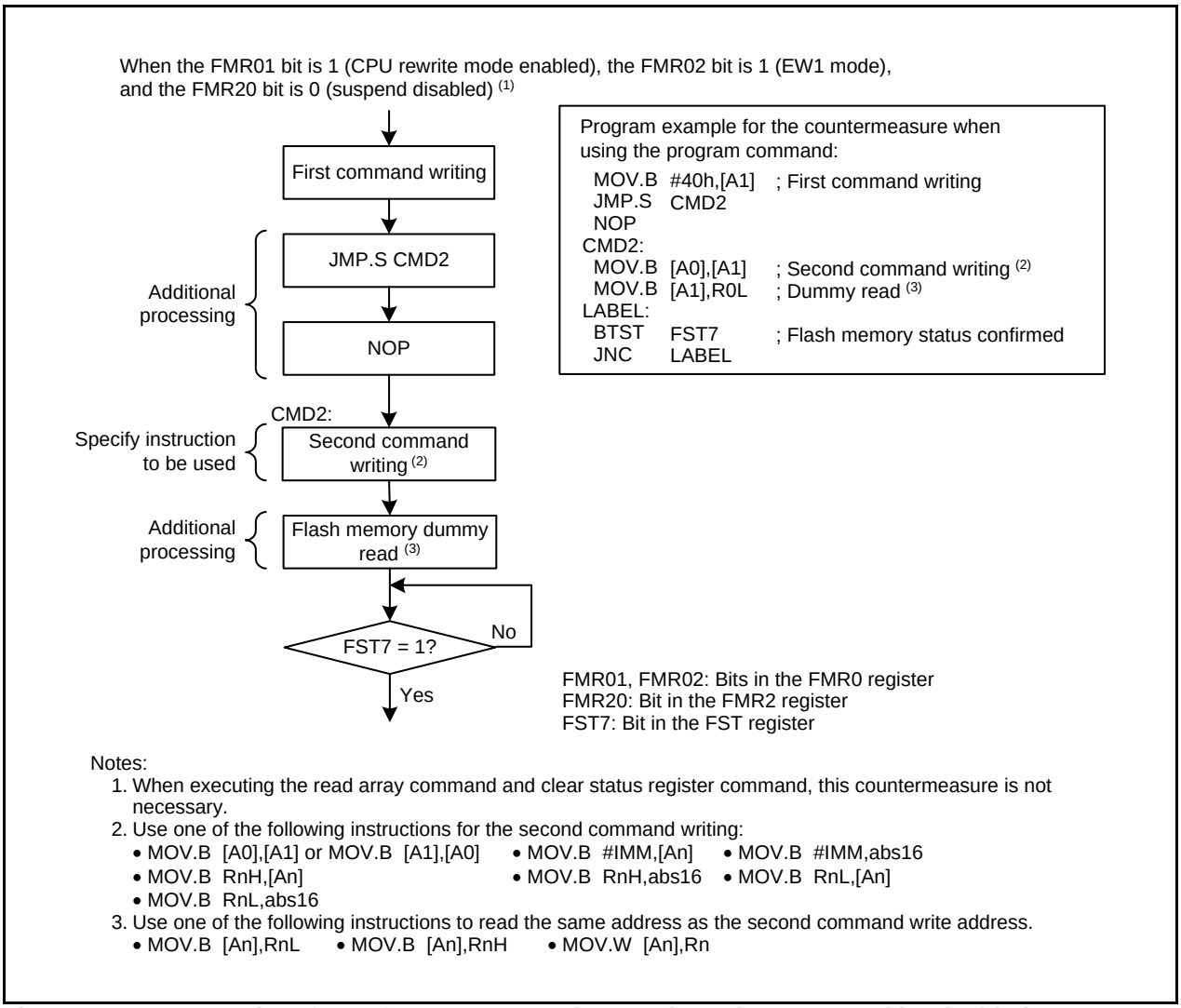
When performing a program/erase operation, use a VCC supply voltage in the range of 1.8 V to 5.5 V. Do not perform a program/erase operation at less than 1.8 V.

21.12.2.8 Block Blank Check

Do not execute a block blank check command during erase-suspend.

21.12.2.9 EW1 Mode

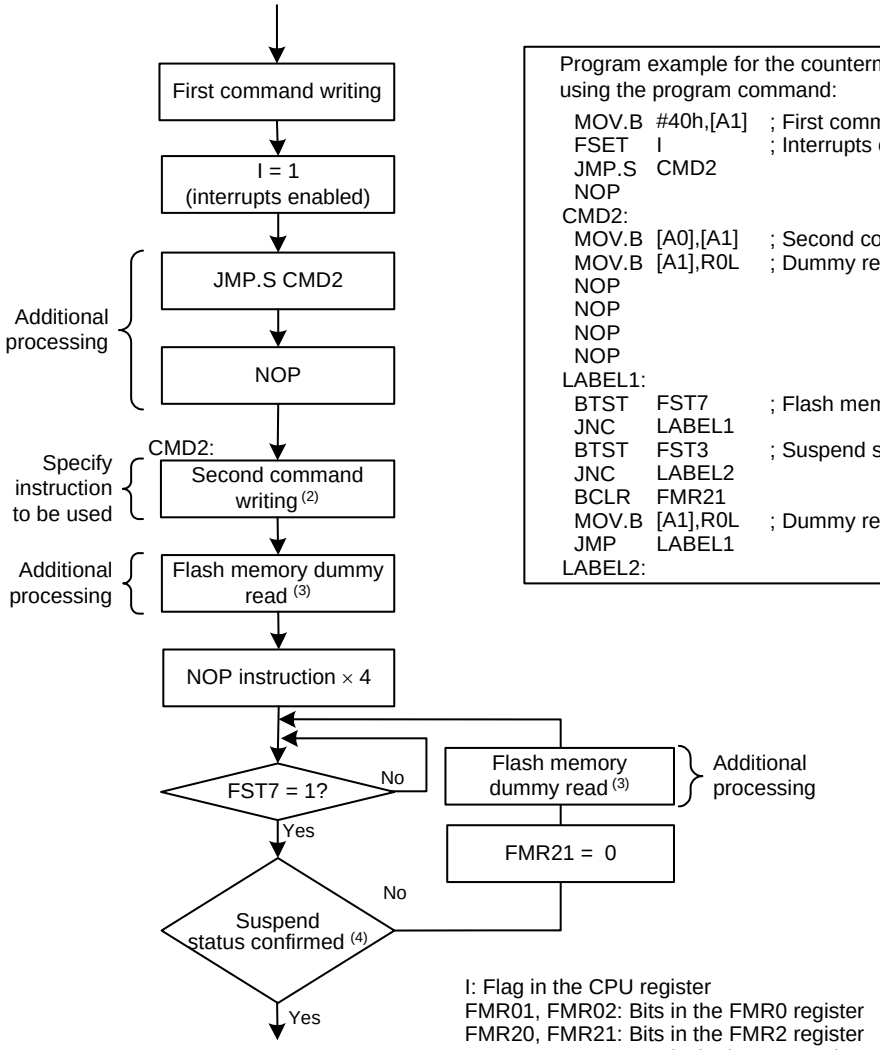
When setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and the FMR02 bit to 1 (EW1 mode) to execute CPU rewrite mode, follow the procedure below in EW1 mode. Figure 21.9 shows the Procedure for Software Command Execution When Suspend is Disabled. Figure 21.10 shows the Procedure for Software Command Execution When Suspend is Enabled.



Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 21.9 Procedure for Software Command Execution When Suspend is Disabled

When the FMR01 bit is 1 (CPU rewrite mode enabled), the FMR02 bit is 1 (EW1 mode), and the FMR20 bit is 1 (suspend enabled) (1)




```
Program example for the countermeasure when
using the program command:
  MOV.B  #40h,[A1]   ; First command writing
  FSET   I           ; Interrupts enabled
  JMP.S  CMD2
  NOP
CMD2:
  MOV.B  [A0],[A1]   ; Second command writing (2)
  MOV.B  [A1],R0L    ; Dummy read (3)
  NOP
  NOP
  NOP
  NOP
LABEL1:
  BTST   FST7        ; Flash memory status confirmed
  JNC    LABEL1
  BTST   FST3        ; Suspend status confirmed (4)
  JNC    LABEL2
  BCLR   FMR21
  MOV.B  [A1],R0L    ; Dummy read (3)
  JMP    LABEL1
LABEL2:
```

I: Flag in the CPU register
FMR01, FMR02: Bits in the FMR0 register
FMR20, FMR21: Bits in the FMR2 register
FST3, FST6, FST7: Bits in the FST register

Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn
4. Confirm the suspend status using the FST3 bit for the program command, and the FST6 bit for the block erase command.

Figure 21.10 Procedure for Software Command Execution When Suspend is Enabled

21.12.3 Notes on Flash Memory Stop and Operation Transition

(1) Do not enter stop mode while the FMSTP bit is 1 (the flash memory is stopped).
(2) Do not enter wait mode while the FMSTP bit is 1 (the flash memory is stopped) and the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
(3) Do not enter flash memory stop state for 42 μs after entering from flash memory stop state to flash memory operation state. And do not rewrite the LOCODIS bit in the OCOCR register for 42 μs.

Conditions when entering flash memory operation state from flash memory stop state.
• Set the FMSTP bit to 0 (the flash memory operates).
• Return from wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Return from stop mode.

Conditions when entering flash memory stop state from flash memory operation state.
• Set the FMSTP bit to 1 (the flash memory is stopped).
• Enter wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Enter stop mode.

21.13 Notes on Noise

21.13.1 Inserting a Bypass Capacitor between Pins VCC and VSS as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) across pins VCC and VSS using the shortest and thickest possible wiring.

21.13.2 Countermeasures against Noise Error in Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.
As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may occur between the reset routine and interrupt routines.

21.14 Note on Power Supply Voltage Fluctuation

After a reset is cleared, the supply voltage applied to the VCC pin must meet either or both of the allowable ripple voltage Vr(vcc) and the ripple voltage falling gradient dVr(vcc)/dt shown in Figure 21.11.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr(vcc)	Allowable ripple voltage			0.1 VCC	V
dVr(vcc)/dt	Ripple voltage falling gradient			10	V/ms

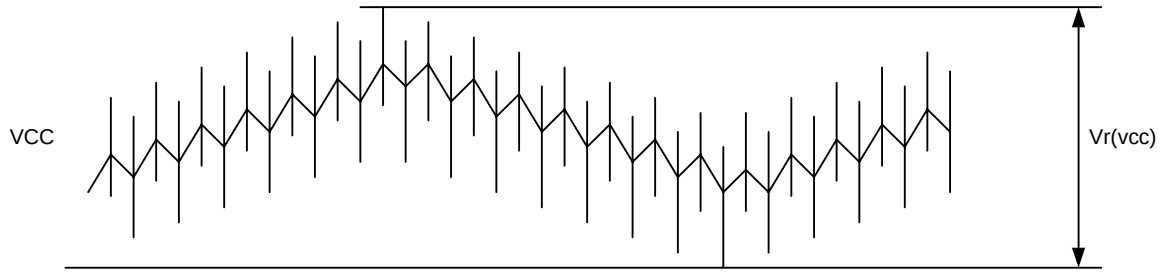


Figure 21.11 Ripple Voltage Definition

22. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/M11A Group and R8C/M12A Group, attention must be paid to the following restrictions:

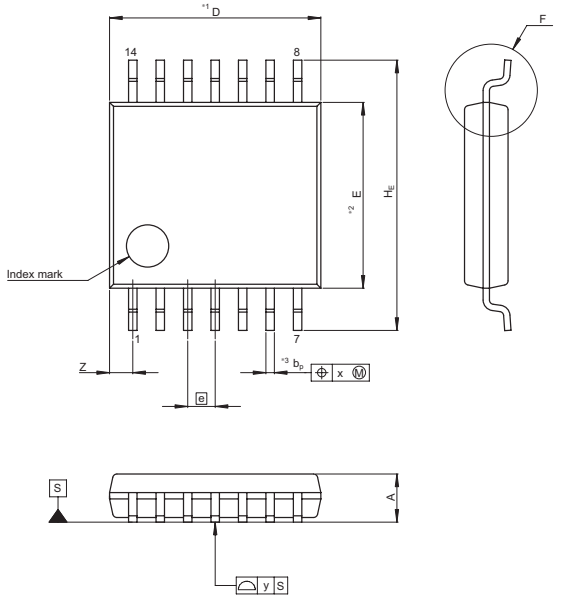
(1) Some of the user flash memory and RAM areas are used by the on-chip debugger. These areas cannot be accessed by the user.
See the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIENi and AIADRi (i = 0 or 1) and fixed vector table) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) The debugging is possible with VCC in the range of 1.8 V to 5.5 V. Set the supply voltage to 2.7 V or above for rewriting the flash memory.

There are some special restrictions on connecting and using the on-chip debugger. For details, see the on-chip debugger manual.

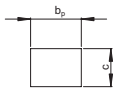
Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

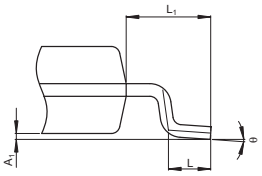
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP14-4.4x5-0.65	PTSP0014JA-B	TTP-14DV	0.05g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



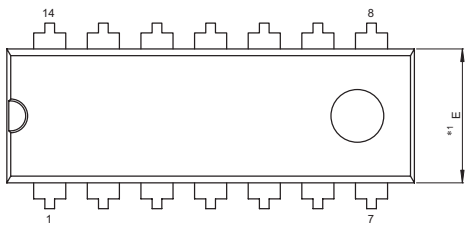
Terminal cross section
(Ni/Pd/Au plating)

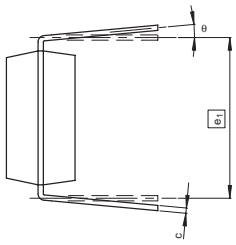


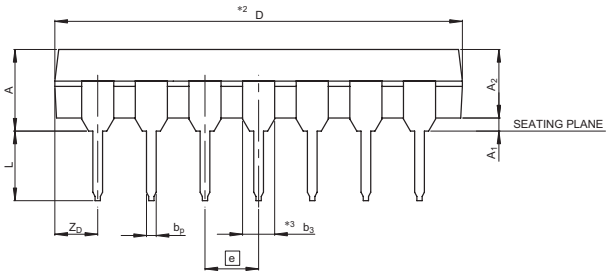
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.83
L	0.4	0.5	0.6
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.35x19.3-2.54	PRDP0014AC-A	14P4X-A	0.94g



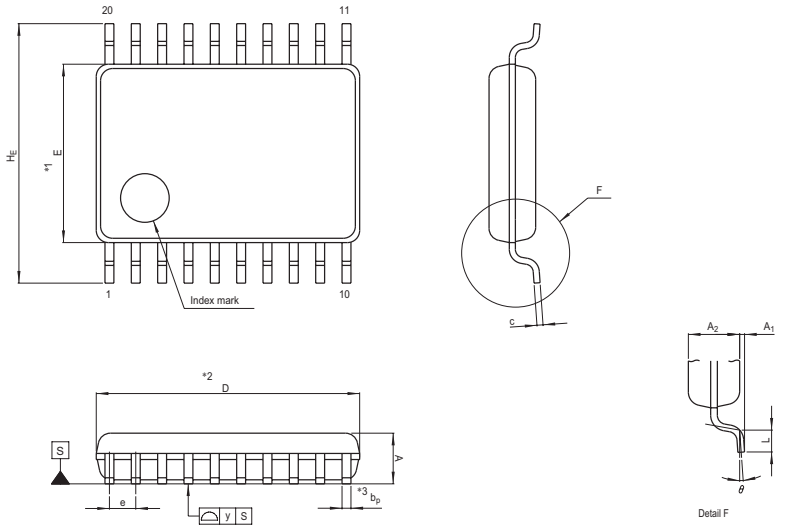




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	—	7.69	—
D	19.2	19.3	19.4
E	6.25	6.35	6.45
A	—	—	4.8
A_1	0.5	—	—
A_2	3.05	3.25	3.45
b_p	0.38	—	0.55
b_3	1.47	1.52	1.57
c	0.21	—	0.35
θ	0°	—	15°
e	—	2.54	—
Z_D	—	2.03	—
L	2.92	—	—

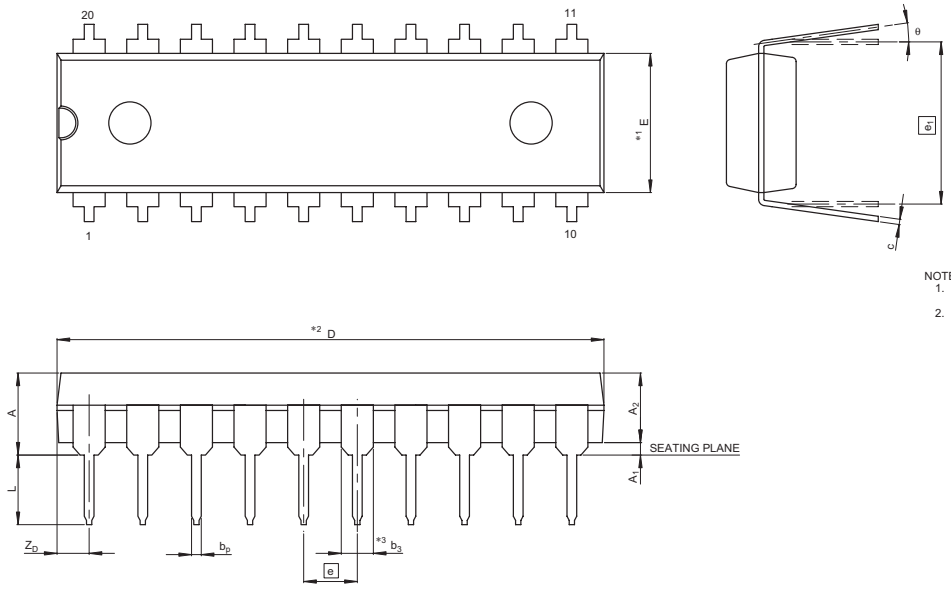
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP20-6.6x25.9-2.54	PRDP0020AD-A	20P4X-A	1.39g

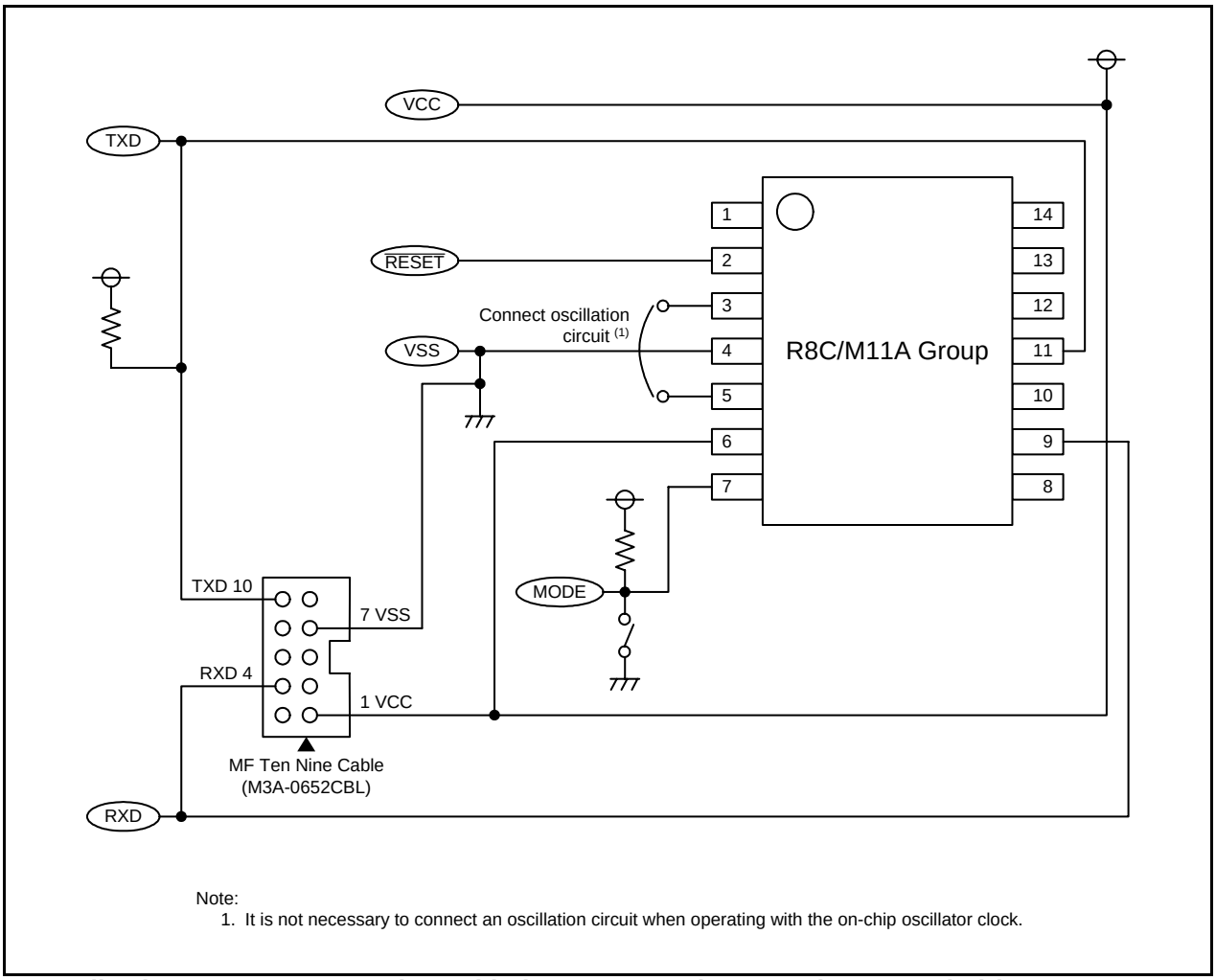


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	—	7.69	—
D	24.9	25.9	26.9
E	6.1	6.6	7.1
A	—	—	5.33
A_1	0.38	—	—
A_2	3.1	3.3	3.5
b_p	0.36	0.46	0.56
b_3	1.32	1.52	1.72
c	0.21	—	0.35
θ	0°	—	15°
e	—	2.54	—
Z_D	—	1.52	—
L	2.9	—	—

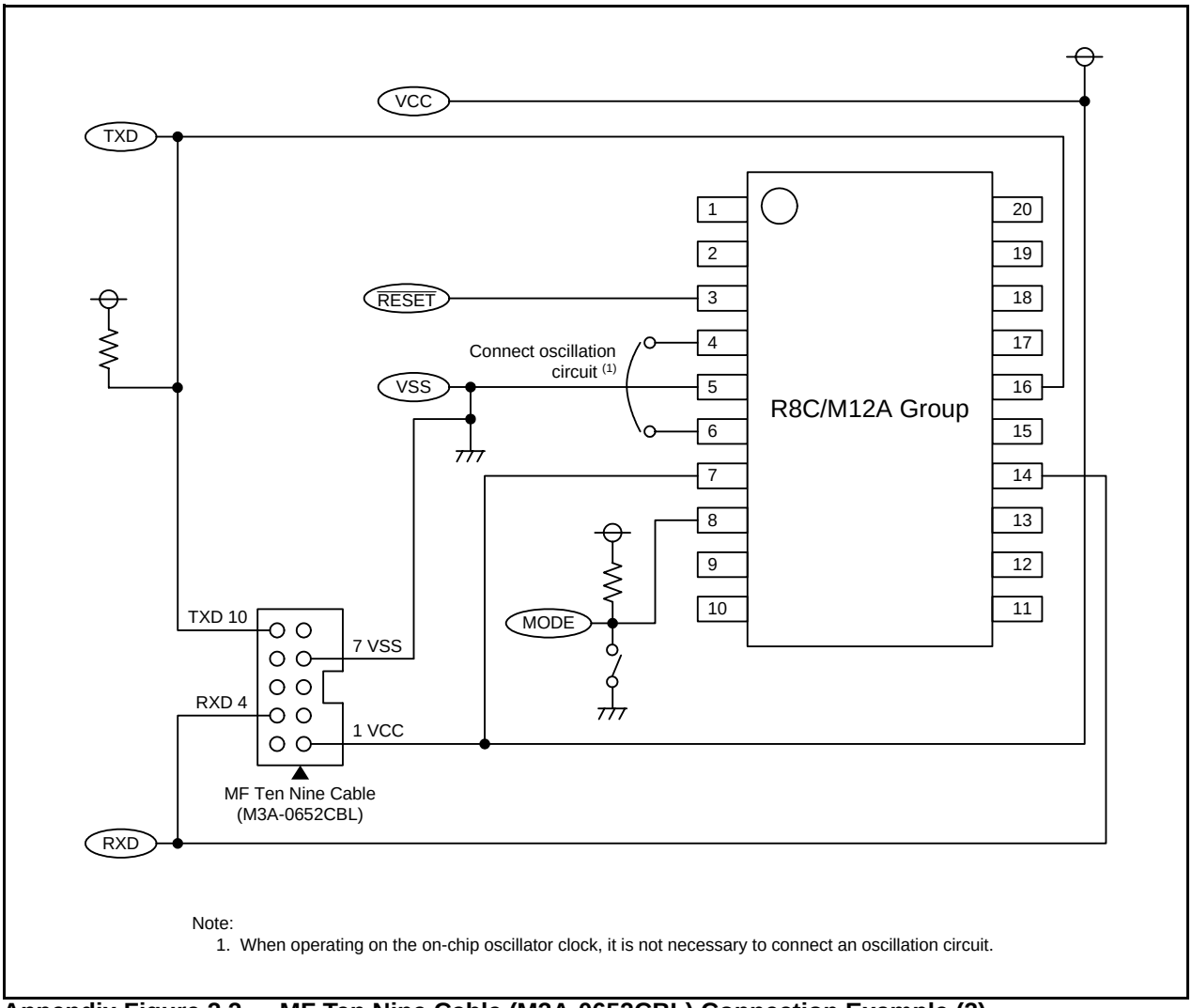
Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figures 2.1 and 2.2 show MF Ten Nine Cable (M3A-0652CBL) Connection Examples. Appendix Figures 2.3 and 2.4 show E8a Emulator (R0E00008AKCE00) Connection Examples.



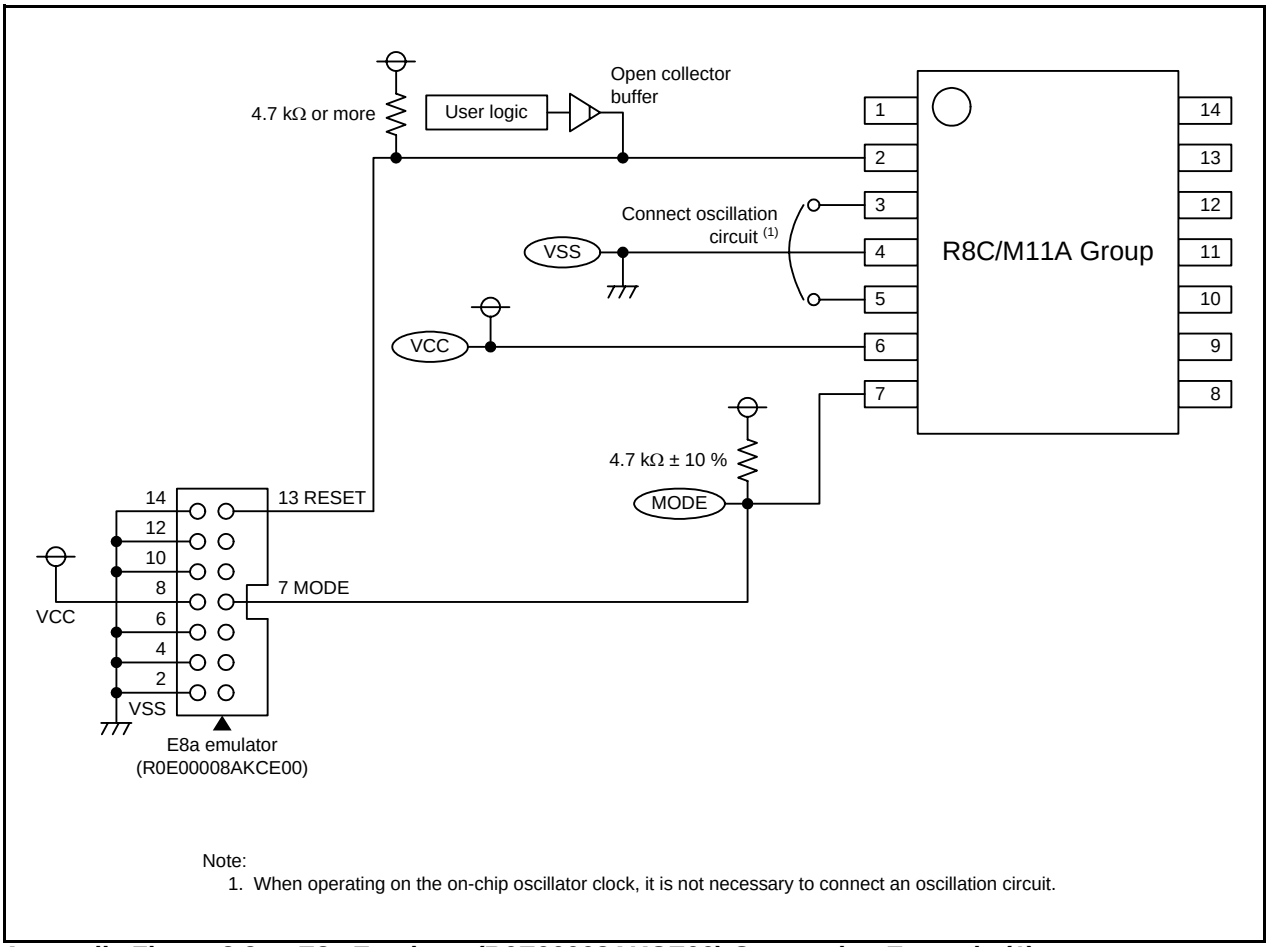
Note:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.

Appendix Figure 2.1 MF Ten Nine Cable (M3A-0652CBL) Connection Example (1)



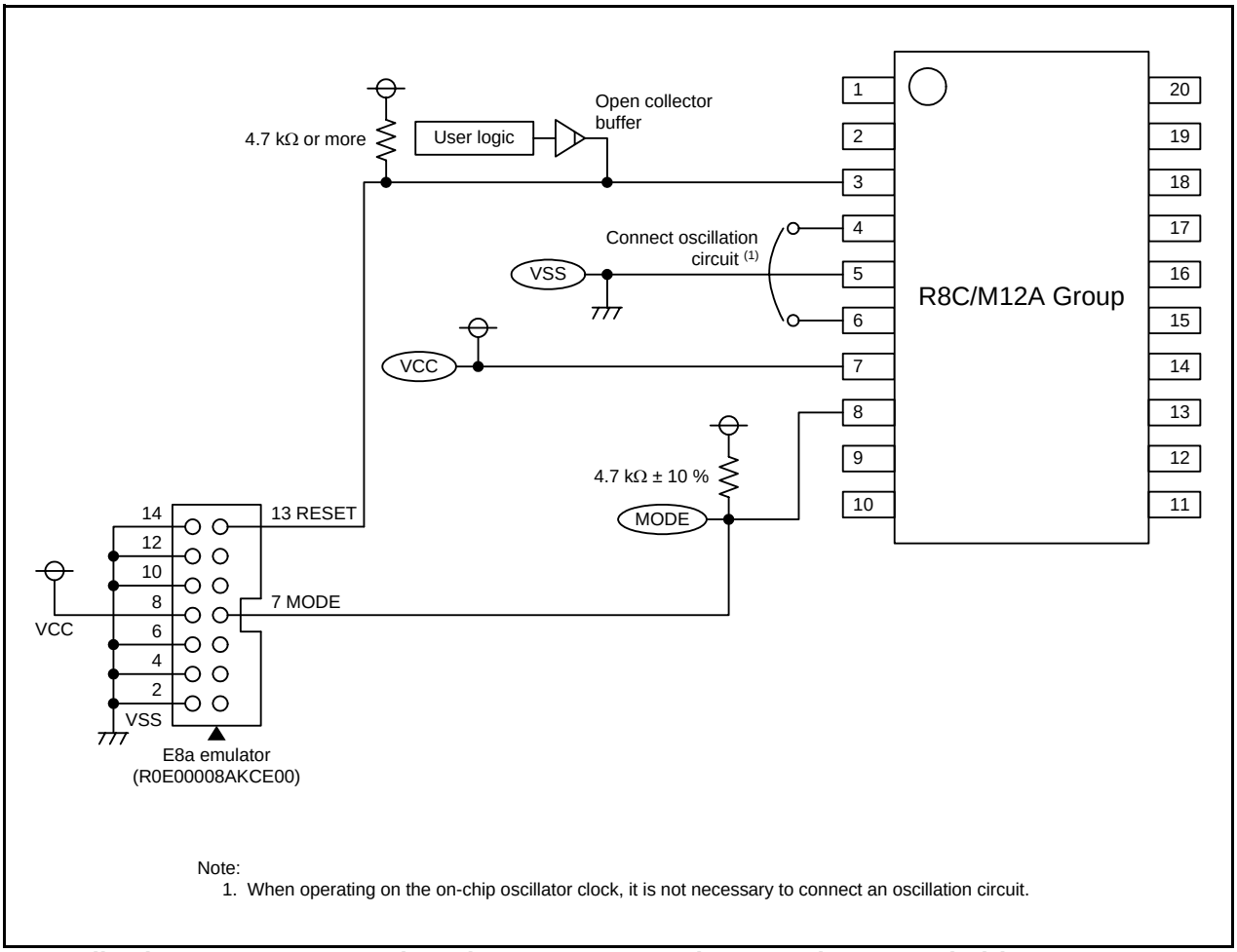
Note:
1. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Appendix Figure 2.2 MF Ten Nine Cable (M3A-0652CBL) Connection Example (2)



Note:
1. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Appendix Figure 2.3 E8a Emulator (R0E00008AKCE00) Connection Example (1)

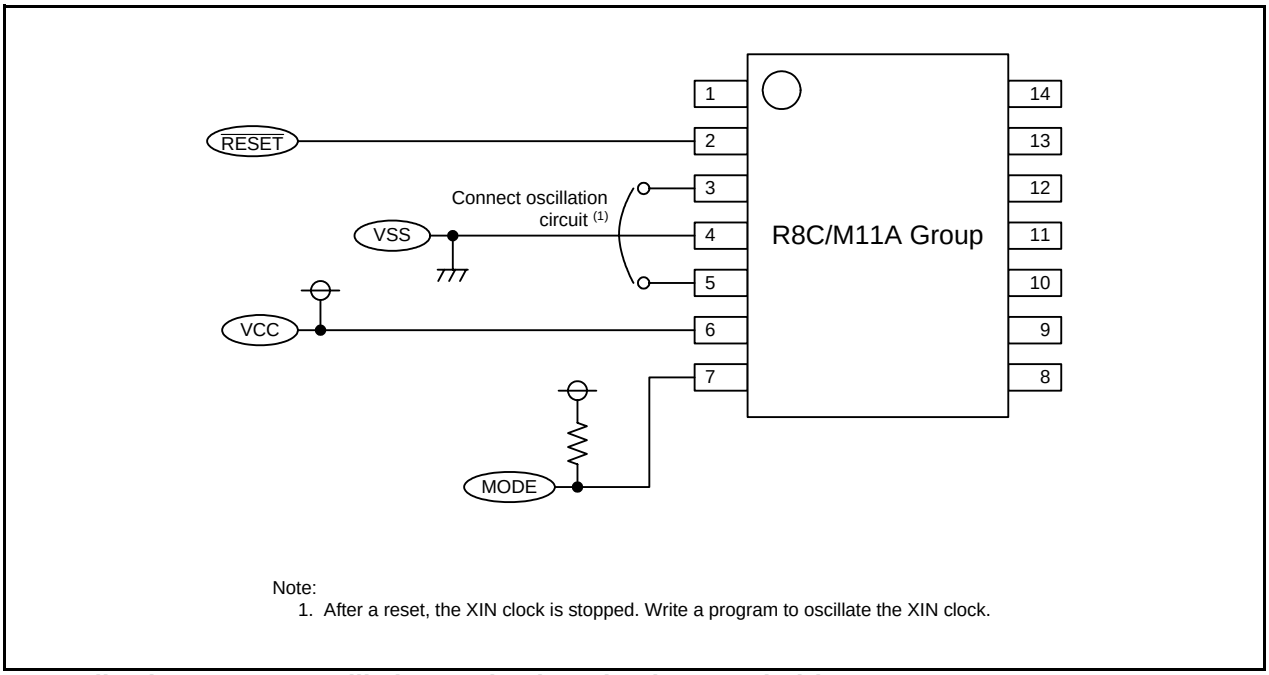


Note:
1. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Appendix Figure 2.4 E8a Emulator (R0E00008AKCE00) Connection Example (2)

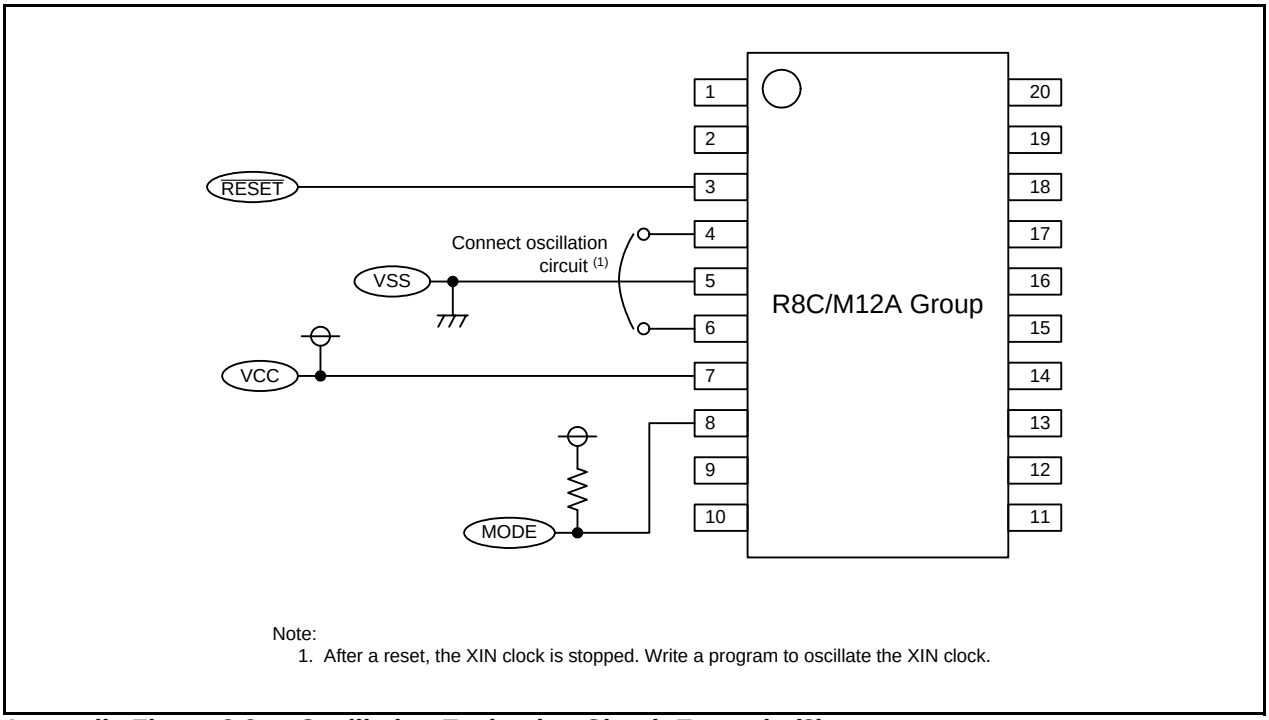
Appendix 3. Oscillation Evaluation Circuit Example

Appendix Figures 3.1 and 3.2 show Oscillation Evaluation Circuit Examples.



Note:
1. After a reset, the XIN clock is stopped. Write a program to oscillate the XIN clock.

Appendix Figure 3.1 Oscillation Evaluation Circuit Example (1)



Note:
1. After a reset, the XIN clock is stopped. Write a program to oscillate the XIN clock.

Appendix Figure 3.2 Oscillation Evaluation Circuit Example (2)

Appendix 4. Comparison between R8C/M12A Group and R8C/M13B Group

Appendix Table 4.1 lists Specification Comparison between R8C/M12A Group and R8C/M13B Group.
For details on the R8C/M13B Group specifications, refer to the R8C/M13B Group User's Manual: Hardware.

Appendix Table 4.1 Specification Comparison between R8C/M12A Group and R8C/M13B Group

Item	Function	R8C/M12AGroup	R8C/M13B Group
Memory	ROM	2 KB, 4 KB, 8 KB	4 KB, 8 KB, 16 KB
	RAM	256 bytes, 384 bytes, 512 bytes	384 bytes, 512 bytes, 1K byte
Clock generation circuit	XCIN clock generation circuit	Not available	Available
I/O port	Number of pins	20	32 Added ports: P2_2/TRCIOD/TRKI/SSO/SDA P2_1/TRCIOC/TRKO/SSCK/SCL P2_0/TRCIOB/TRKO/INT1 P3_1/XIN/TRBO P0_7/TRCIOC/TRKO P0_6/TRCIOD P0_5/TRCIOB P0_4/TRCIOB/TREO P0_3/TRCIOB/CLK1 P0_2/TRCIOA/TRCTRG/RXD1/IrRXD P0_1/TRCIOA/TRCTRG/TXD1/IrTXD P0_0/TRCIOA/TRCTRG
	Number of CMOS I/O ports	17	29 Added ports: P2_2, P2_1, P2_0, P3_1, P0_7, P0_6, P0_5, P0_4, P0_3, P0_2, P0_1, P0_0
Timer	Timer RE2	Not available	Available
	Timer RK	Not available	Available
Serial interface	UART1	Not available	Available
Clock synchronous serial interface	IIC/SSU	Not available	Available
IrDA interface		Not available	Available
A/D converter	Number of A/D channels	6 channels	8 channels Added channels: AN5, AN6
Package		20-pin LSSOP 20-pin DIP	32-pin LQFP

Appendix Tables 4.2 and 4.3 list the Register Comparison between R8C/M12A Group and R8C/M13B Group. For details on the R8C/M13B Group registers, refer to the R8C/M13B Group User's Manual: Hardware.

Appendix Table 4.2 Register Comparison between R8C/M12A Group and R8C/M13B Group (1)

Related Function	Register	Address	Bit	Remarks
System Control	MSTCR	00012h	MSTTRE	Functions added
	MSTCR1	00017h	MSTUART1, MSTTRK, MSTICSU, MSTIRDA	Register added
Clock	EXCKCR	00020h	CKPT1, CKPT0	Functions changed
			XCRCUT, XCINNC1, XCINNC0, CKPT3, CKPT2	Functions added
	SCKCR	00022h	LSCKSEL	Functions added
Interrupt	ILVL1	00041h	ILVL11, ILVL10	Register added
	ILVL5	00045h	ILVL51, ILVL50	Functions added
	ILVL7	00047h	ILVL75, ILVL74	Functions added
	ILVL9	00049h	ILVL95, ILVL94	Functions added
	ILVLA	0004Ah	ILVLA1, ILALA0	Functions added
	IRR0	00050h	IRS1R, IRS1T, IRTE	Functions added
	IRR1	00051h	IRTK, IRIS	Functions added
P0	PD0	000A8h		Register added
	P0	000AEh		Register added
	PUR0	000B4h		Register added
	POD0	000C0h		Register added
	PML0	000C6h		Register added
	PMH0	000C7h		Register added
P1_0, P1_2, P1_4, P1_5, P1_6	PML1	000C8h	P12SEL1, P12SEL0, P10SEL1, P10SEL0	Functions changed
	PMH1	000C9h	P16SEL1, P16SEL0, P15SEL1, P15SEL0, P14SEL1, P14SEL0	Functions changed
P2_0, P2_1, P2_2	PD2	000AAh	PD2_2, PD2_1, PD2_0	Register added
	P2	000B0h	P2_2, P2_1, P2_0	Register added
	PUR2	000B6h	PU2_2, PU2_1, PU2_0	Register added
	POD2	000C2h	POD2_2, POD2_1, POD2_0	Register added
	PML2	000CAh	P22SEL1, P22SEL0, P21SEL1, P21SEL0, P20SEL1, P20SEL0	Register added
P3_1, P3_3, P3_4	PD3	000ABh	PD3_1	Functions added
	P3	000B1h	P3_1	Functions added
	PUR3	000B7h	PU3_1	Functions added
	POD3	000C3h	POD3_1	Functions added
	PML3	000CCh	P33SEL1, P33SEL0	Functions changed
			P31SEL1, P31SEL0	Functions added
	PMH3	000CDh	P34SEL1, P34SEL0	Functions changed
P4_2, P4_5, P4_6, P4_7	PML4	000CEh	P42SEL1, P42SEL0	Functions changed
	PMH4	000CFh	P47SEL1, P47SEL0, P46SEL1, P46SEL0, P45SEL1, P45SEL0	Functions changed
AN5, AN6	ADINSEL	0009Dh	ADGSEL1, ADGSEL0	Functions changed

Appendix Table 4.3 Register Comparison between R8C/M12A Group and R8C/M13B Group (2)

Related Function	Register	Address	Bit	Remarks
Timer RK	TMKM	00188h		Registers added
	TMKCR	00189h		
	TMKLD	0018Ah		
	TMKCMP	0018Bh		
	TMKIR	0018Ch		
Timer RE2	TRESEC (TRECNT)	00130h		Registers added
	TREMIN	00131h		
	TREHR	00132h		
	TREWK	00133h		
	TREDY	00134h		
	TREMON	00135h		
	TREYR	00136h		
	TRECR	00137h		
	TRECSR	00138h		
	TREADJ	00139h		
	TREIFR	0013Ah		
	TREIER	0013Bh		
	TREAMN	0013Ch		
	TREAHR	0013Dh		
	TREAWK	0013Eh		
	TREPRC	0013Fh		
UART1	U1MR	00190h		Registers added
	U1BRG	00191h		
	U1TBL	00192h		
	U1TBH	00193h		
	U1C0	00194h		
	U1C1	00195h		
	U1RBL	00196h		
	U1RBH	00197h		
	U1IR	00198h		
IrDA	IRCR	0019Ch		Register added
IIC/SSU	IICCR	00160h		Registers added
	SSBR	00161h		
	SITDR	00162h		
	SIRDR	00164h		
	SICR1	00166h		
	SICR2	00167h		
	SIMR1	00168h		
	SIER	00169h		
	SISR	0016Ah		
	SIMR2	0016Bh		

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REVISION HISTORY	R8C/M11A Group, R8C/M12A Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.01	Jan 29, 2010	—	First Edition issued
0.10	Jun 14, 2010	All pages	Revised
0.11	Jun 29, 2010	180	13.4.1 "... next count source" → "... next system clock (f)"
		231	15.2.11 revised
		232	15.2.12 revised
		233	15.2.13 Note 1 revised
0.12	Jul 06, 2010	400, 401	Appendix Figures 2.3 and 2.4 Connection line between E8a emulator and VCC revised
1.00	Nov 30, 2010	All pages	"Preliminary" and "Under development" deleted
		B-1	00021h, 00025h, 00030h and 00035h revised
		B-2	000DEh and 000E7h revised
		1	1.1 revised
		3	Table 1.2 IRR3 and IRR2 revised
		4	Table 1.3 Watchdog timer revised
		5	Table 1.4 Note 1 revised
		6	Table 1.5 revised
		10	Table 1.7 revised
		11	Figure 2.1 revised
		15	Table 3.1 00021h, 00025h, 00030h to 00033h, and 00035h revised
		18	Table 3.4 000DEh and 000E7h revised
		23	Table 3.9 Notes 1 and 2 revised
		24	4 revised
		25	Table 5.1 Notes 3 and 4 revised
		26, 37	5.2.1, 6.2.1 SRST Bit revised
		27	5.2.2 After Reset, Note 3 revised, "When changing ... peripheral function beforehand." added
		29, 38	5.2.5, 6.2.2 revised
		31, 40	5.2.6, 6.2.3 Note 1 revised
		32, 41	5.2.7, 6.2.4 Note 1 revised
		33	"Table 5.3 ... 5.2.4 Hardware Reset Protect Register (HRPR)" and Table 5.3 added
		37	Table 6.2 Notes 2 and 3 revised
		42	Figure 6.2 Note 1 revised
		43	6.3.2 revised, the last Figure 6.3 deleted
		53	7.2.2 Note 1 revised
		61	7.6 and Figure 7.6 added
		62	Table 8.1 revised, Note 1 deleted
		63	Figure 8.1 revised
		64	Table 8.2 and 8.2.1 revised
		65	8.2.2 to 8.2.4 After Reset revised
		66	8.2.6 revised
		67	8.3.1.1 and Figure 8.2 revised

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		Page	Summary
1.00	Nov 30, 2010	68	Table 8.3 revised, Notes 2 and 3 deleted
		69	Table 8.4 Notes 1 to 3 deleted
		70	Table 8.5 revised, Note 1 added, and Figure 8.3 revised
		71	8.4 revised
		72 to 90	"9. Clock Generation Circuit" revised
		91, 379	9.6, 21.3 revised
		92 to 106	"10. Power Control" revised
		107, 380	10.6, 21.4 revised
		108	Table 11.1 revised
		111	11.2.1 Note 1 added
		113	11.2.4 Note 1 revised
		115	11.2.6 and 11.2.7 revised
		116	11.2.8 revised
		118	11.2.10 and 11.2.11 "The resister remains ... or software reset." added
		119	Table 11.5 "0FFE7h" → "0FFE6h"
		121	11.4.2 revised, Table 11.7 added
		122	11.4.3 revised
		123	11.4.4 (1) revised
		125	11.4.7 revised
		128	Figure 11.8 Note 1 deleted
		129	11.5.1 revised
		130	11.5.2 and Figure 11.9 revised
		131	Figure 11.11 revised
		132	11.7 revised
		133	Figure 11.12 revised
		135, 382	11.9.4,21.5.4, Figure 11.13, and Figure 21.1 revised
		136, 383	11.9.5, 21.5.5 revised, Figure 11.14, Figure 21.2 added
		137, 384	11.9.6, 21.5.6, Figure 11.15, Figure 21.3 added
		140	12.2 and 12.2.1 revised
		142	12.3.2 revised
		143	12.3.4 Note 1 added
		148	Tables 12.9 and 12.10 revised
		150	12.4.2 revised
		151	12.4.4 Note 1 added
		154	Table 12.15 revised
		156	12.5.2 revised
		160	Table 12.16, Table 12.18, and Table 12.19 revised
		162	12.6.2 revised
		163	12.7 added
		166	Figure 12.6 revised, Figure 12.7 added
		167	Figure 12.9 revised
		168	Figure 12.10 revised

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		Page	Summary
1.00	Nov 30, 2010	169	Figure 12.11 revised
		172	Figures 12.15 and 12.16 revised
		173	Figure 12.17 revised
		175, 385	12.11.2, 21.6.2 added
		176	13 and Table 13.1 revised
		177	Figure 13.1 and Table 13.2 revised
		178	Table 13.3 and 13.3.1 revised
		181	TOPCR Bit and Table 13.6 revised
		183	13.3.6 revised
		186	13.4.3 revised
		187	13.4.4 revised
		191, 386	13.5, 21.7 revised
		193, 388	Figures 13.10, 13.11, 21.6, and 21.7 revised
		195	14.2 revised
		196	Table 14.3 revised
		197	14.3.1 Notes 2 and 3 deleted
		217	Tables 14.6 and 14.7 revised
		228	Table 15.2 revised
		230	15.2.1 revised
		231	15.2.2 revised
		232	15.2.3 revised
		233	15.2.4 revised
		238	15.2.9 revised
		244	15.3.1 revised
		252	Figure 15.12 revised
		259	Figure 15.19 revised
		262	"toggle output from TRCIOD pin ..." → "toggle output from TRCIOB pin ..."
		263	Figure 15.23 revised
		264	Figures 15.24 and 15.25 revised
		265	Figure 15.26 revised
		266	Figure 15.27 revised
		271, 391	15.6.2, 15.6.4, 15.6.7, 21.9.2, 21.9.4, and 21.9.7 revised
		275	Figure 16.2 revised
		280	16.2.6 revised
		289	Figure 16.6 revised
		291	Table 16.8 Note 1 revised
		295	Table 17.1 revised
		296	Figure 17.1 and Table 17.2 revised
		298	17.2.1 revised
		299	17.2.2 revised
		300	17.2.3 revised
		301	17.2.4 revised

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		Page	Summary
1.00	Nov 30, 2010	302	17.2.5 revised
		303	17.3, 17.3.1.1, and Figure 17.2 revised
		304	Table 17.6 revised, the last Table 17.7 deleted, 17.3.1.2 and Figure 17.3 revised
		305	17.3.2 and Figure 17.4 revised
		306	17.3.3 and Figure 17.5 revised
		307	17.3.4 and Figure 17.6 revised
		308	17.3.5 and Figure 17.7 revised
		309	17.4 revised, the last 17.5, and the last Figures 17.8 to 17.9 deleted
		310, 394	17.5.1, 17.5.2, 21.11.1, 21.11.2 revised, the last Figure 17.10, the last Figure 21.6 deleted
		311, 395	17.5.3, 21.11.3 revised
		313	Table 18.2 Note 1 added
		318	Table 18.4 revised
		332	19.5.5 revised
		339	19.6.6.2 and Figure 19.8 revised
		340	Figure 19.9 revised
		341	Figure 19.10 revised
		342	"When the FMR22 bit is ... in EW1 mode." and Figure 19.11 added
		343	19.6.6.3 and Figure 19.12 revised
		344	Figure 19.13 revised
		345	Figure 19.14 revised
		346	"When the FMR22 bit is ... in EW1 mode." and Figure 19.15 added, the last Figures 19.20 and 19.21 moved to 10. Power Control
		353	Figure 19.20 revised
		361	Table 20.3 revised
		366	Tables 20.10 and 20.11 revised
		402 to 403	Package Dimensions added
		404	Appendix Figure 2.1 revised
		405	Appendix Figure 2.2 revised
2.00	May 18, 2012	4	"Under development" deleted
		9	Table 1.6"Voltage detection circuit" deleted
		24	4. Description revised
		28	5.2.3 b3: Function revised, 5.2.4 Note 1 added
		29	5.2.5 and 6.2.2 CWR Bit Description revised
		33	Table 5.2 revised
		78	9.2.3 Bits PHISSEL0 to PHISSEL2 Description revised
		79	9.2.4 b7 to b0: Bit Name revised
		80	9.2.5 STPM and WCKSTP Bit Description revised
		81	9.2.6 Note 2 added
		82	9.2.6 Bits CKST0 to CKST3: Description revised
		85	9.3.1 Description, Figure 9.3 revised
		88	9.4.5 Description revised

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		Page	Summary
2.00	May 18, 2012	90	Figure 9.6 revised
		97	10.3 Description revised
		99	Figure 10.2 title revised
		106	Figure 10.6 revised
		108, 389	10.6.1, 10.6.2, 21.4.1, and 21.4.2 revised
		115, 118	11.2.5 and 11.2.9 Description revised
		119	11.2.10 and 11.2.11 Description revised
		130	11.5.1 Description and Table 11.11 "Assigned Pin" revised
		131	Figures 11.9 and 11.10 revised
		136, 391	Figures 11.13 and 21.1 Note 2 added
		139, 394	"11.9.7 Changing Interrupt Priority Levels and Flag Registers" and "21.5.7 Changing Interrupt Priority Levels and Flag Registers" added
		177, 395	12.11.2 and 21.6.2 Description revised
		179	Figure 13.1 revised
		180	13.3.1 Note 2 revised, Note 3 added
		181	13.3.2 Note 2 revised, Description added
		182	13.3.3 b6 and b7: Function revised
		183	13.3.3 Bits TIOGT0 to TIOGT1: Description added
		184	13.3.4 Note 1 deleted, Description added
		186	13.4.1 and Figure 13.2 revised
		187	Figure 13.3 revised
		188	Figure 13.4 revised
		191	13.4.6 Description, Figure 13.7 revised
		193, 396	13.5 and 21.7 (3) revised, (5) deleted, (13) added
		199	14.3.1 Note 1 revised
		200	14.3.2 b0 and b1: Function revised, description added
		201	Table 14.4 "Timer mode" revised
		202	14.3.4 Note 2 revised
		204	14.3.6 Note 1 added
		205	14.3.7 Description revised
		207	14.4.1 Description revised
		209	14.4.2 Description revised
		212	14.4.3 Description revised
		215	14.4.4 Description revised
		220	14.5.2 Description revised
		221 to 224	Figures 14.10 to 14.13 revised
		227, 228, 399, 400	14.8 and 21.8 revised
		229	Table 15.1 "Operating clock" added
		232	15.2.1 Description revised
		233, 234	15.2.2 Description deleted, Tables 15.5 to 15.8 added
		235	15.2.3 Notes 1 and 2 revised

Rev.	Date	Description	
		Page	Summary
2.00	May 18, 2012	236	15.2.4 b7: Function revised, Note 3 added
		238	15.2.6 Note 1 added, Table 15.9 Note 2 added
		239	15.2.7 b0, b1, b4, b5 : Function revised, Note 1 revised
		240, 241	15.2.8 b0, b1, b4, and b5: Function revised, Note 8 added
		242	15.2.10 Description deleted, b0 to b4: Function revised, Notes 1 and 2 added.
		243	15.2.11 Note 3 added
		246	Table 15.10 revised
		251	15.3.2 Description revised
		253	Figure 15.10 and title revised
		255	15.3.3 Description revised
		257	Figure 15.14, 15.3.3 Description revised
		262	Figure 15.19 revised
		264	15.4.3 Description revised
		266	15.4.4 Description revised
		267	Figure 15.24 revised
		271	Figure 15.31 revised
		273	15.5.8, Figure 15.34 revised
		274	"15.6 Timer RC Interrupt" added
		275, 276, 556, 557	15.7.4, 15.7.5, 25.9.4, and 25.9.5 revised
		277	16.1 Description revised
		280	16.2.1 Notes 1 and 2 added
		284	16.2.6 b0 to b8: Bit Name, Note 1 revised, Note 2 added
		288, 293, 294	Figures 16.3, 16.6, and 16.7 revised
		291	16.3.2 Note 2 added
		297	16.4 Description revised
		299	Table 17.1 revised
		308	Table 17.6, Notes 1 and 2 revised
		309 to 312	Figures 17.4 to 17.7 revised
		314, 404	17.5.2 and 21.11.2 Description revised
		328	19.3.2.1 and 19.3.2.2 Description revised
		329	19.4 Description, Table 19.5 revised
		330	19.5.1 "After Reset" revised, Notes 1 to 4 added
		331	19.5.1 RDYSTI and BSYAEI: Description revised
		332	19.5.1 Bits FST2 to FST6: Description revised, FST7 bit: Description added
		333	19.5.2 Notes 2 to 4, FMSTP bit description revised, FMR01 and FMR02 bit description added
		334	19.5.2 CMDRST, CMDERIE, BSYAEIE, and RDYSTIE bit description revised
		335	19.5.3 FMR13 bit description revised, FMR16 and FMR17 bit description added
		336	19.5.4 Note 2 and FMR22 bit revised, FMR20 bit description added
		337	19.5.4 FMR27 bit description revised

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		Page	Summary
2.00	May 18, 2012	339	19.6.1 Description revised
		340	Table 19.7 Notes 1 to 3 added, Figure 19.3 revised
		341	Figure 19.4 revised
		343	19.6.5 Description revised
		344	19.6.6 Description revised and "19.6.6.1 Read Array" added
		345	19.6.6.2 and 19.6.6.3: Description revised
		348	Figure 19.11 revised
		349	19.6.6.4 Description revised
		352	Figure 19.15 revised
		355	Figure 19.18 revised
		356	Table 19.9 revised
		359	Table 19.10 revised
		360	Table 19.11 revised
		362, 363, 407, 408	Tables 19.12, 19.13, 21.1, and 21.2 revised
		364, 409	19.8.2.6 and 21.12.2.6 revised
		365, 366, 410, 411	"19.8.2.9 EW1 Mode" and "21.15.2.9 EW1 Mode" added
		367, 412	"19.8.3 Notes on flash memory stop and operation transition" and "21.15.3 Notes on flash memory stop and operation transition" added
		370	Table 20.3 revised
		417	Appendix Figure 2.1 Note 1 revised
		422 to 424	"Appendix 4. Comparison between R8C/M12A Group and R8C/M13B Group" added

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