ISL6844 Reference Design: ISL6844EVAL3Z

Introduction

This document focuses on Intersil's solution for the flyback converter. An inexpensive approach with discrete circuitry has been adopted instead of an integrated solution. Low cost and optimal performance are the prime objectives.

Intersil's superior industry-standard ISL684x family of PWM controllers would best serve the needs of this design. Some key features of this family of parts include:

- 40ns peak current sensing
- 1A MOSFET driver

ISL6844 was selected for its large UVLO hysteresis, UVLO start threshold, and the fact that the converter has been designed for a maximum operational duty cycle of 50%, thus protecting the IC by limiting the duty cycle in case of extreme fault conditions.

Specifications

- Operating Input Voltage: 24V DC ±10%
- Output Voltage: ±15V
- Output Current: 100mA
- Ripple: 50mV$_{P-P}$
- Switching Frequency: 300kHz
- Topology: DCM Flyback

Design Procedure

Figure 1 shows a simplified circuit of the solution. It is assumed that loads are balanced for both positive and negative outputs. The turn ratio of the auxiliary winding is chosen to be the same as the secondary winding. Figure 2 shows typical operational waveforms of a flyback converter in discontinuous conduction mode.

Determine the Maximum Duty Cycle and Transformer Turn Ratio

ISL6844 clamps the duty cycle to 50%. However, in this converter design, it is assumed that the operating maximum duty cycle, d_{max}, will be 35% at the minimum input voltage of 21.6V.

Given the power level, the flyblack converter is designed to operate in discontinuous conduction mode. The magnitizing inductance can be calculated using Equation 1:

$$L_M = \eta \cdot \frac{V_{IN,MIN}^2 \cdot d_{max}^2}{2 \cdot P_{out} \cdot F_{sw}} \quad \text{(EQ. 1)}$$

$$= 0.75 \cdot \frac{21.6^2 \cdot 0.35^2}{2 \cdot 3 \cdot 300 \times 10^3} = 23.8\mu H$$

Where:

η = Converter's efficiency, assuming 75%

P_{OUT} = Total output power

F_{sw} = Switching frequency

As a result, the peak magnitizing current = 1.06A

The transformer's turn ratio can be determined from:

$$n = \frac{(V_{out} + V_F) \cdot (1 - d_2)}{V_{IN,MIN} \cdot d_{MAX}} \quad \text{(EQ. 2)}$$

$$d_{MAX} + d_2 < 1$$

Where:

n = Turns ratio between the primary and the secondary windings

V_F = Forward drop across the diode, assuming 0.6V

d_2 = Duty cycle of diode conduction time

d_2T_{sw} is the magnitizing current reset time. Setting d_2 to 0.5, Equation 2 yields the transformer's turn ratio of 1.

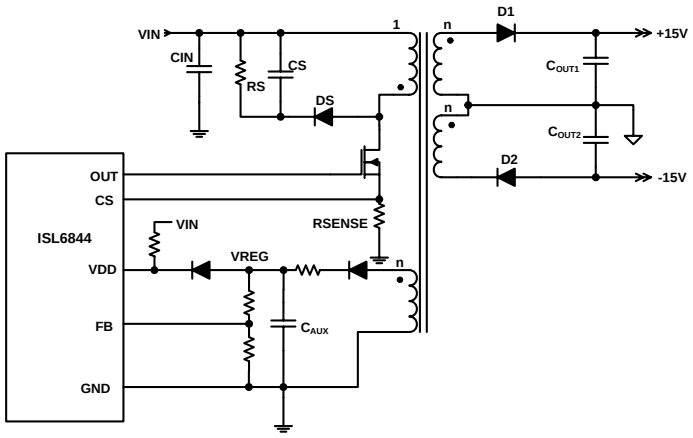


FIGURE 1. SIMPLIFIED CIRCUIT

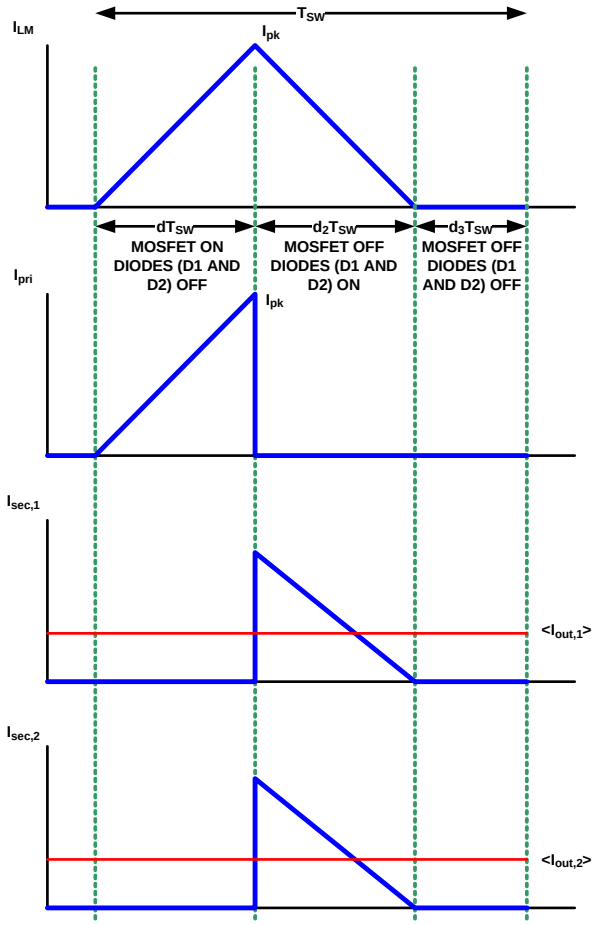


FIGURE 2. TYPICAL OPERATIONAL CURRENT WAVEFORMS

Transformer Core Selection

From Figure 2, the RMS current in the transformer primary side can be calculated from:

$$I_{rms,pri} = I_{pk} \cdot \sqrt{\frac{d}{3}} \quad \text{(EQ. 3)}$$

$$= 1.06 \cdot \sqrt{\frac{0.35}{3}} = 0.362A$$

The RMS current in each transformer secondary side can also be computed from:

$$I_{rms,sec} = \frac{I_{pk}}{2} \cdot \sqrt{\frac{d_2}{3}} \quad \text{(EQ. 4)}$$

$$= \frac{1.06}{2} \cdot \sqrt{\frac{0.5}{3}} \cdot = 0.216A$$

The transformer used in this design is Pulse's PA3374Nl. It is a gapped ferrite toroid core, which has the following parameters:

- $A_e = 4.3mm^2$
- $A_L = 35nH/n^2$
- $l_e = 13.1mm$
- $V_e = 56.5mm^3$

This section provides general guideline to calculate the number of turn and wire size. For more details on designing transformer parameters, please contact a Pulse representative.

The number of turns on the primary side, Np, can be determined from:

$$N_p = \sqrt{\frac{L[uH] \times 1000}{A_L}} \quad \text{(EQ. 5)}$$

$$= \sqrt{\frac{23.8 \times 1000}{35}} = 26.07$$

Therefore, the primary side has 26 turns. With the turn ratio of 1, the secondary side and the auxiliary primary side also have 26 turns.

Next the calculate the maximum flux density to make sure that it is below the saturation limit.Where:

$$B_{max} = \frac{L_M \cdot I_{M,max}}{N_p \cdot A_e} \quad \text{(EQ. 6)}$$

$$= \frac{23.8 \times 10^{-6} \cdot 1.06}{26 \cdot 4.3 \times 10^{-2}} \times 10^4 = 0.226T$$

For the operating power level, the wire sizes of the primary, secondary, and auxiliary windings are selected such that the current density in each winding is about 0.25335 cm^2/A (50 circular mil/A).

$$A_{w,pri} \geq 0.25335 \cdot 0.362 = 0.0917cm^2 \quad \text{(EQ. 7)}$$

To simplify transformer winding, AWG#37 is used for all primary, secondary and auxiliary windings.

Primary MOSFET Selection

The primary MOSFET needs to be able to handle the voltage stress, given by:

$$V_{DSFET} = V_{IN,MAX} + [n \times (V_{out} + V_f)] \quad \text{(EQ. 8)}$$

$$= 26.4 + [1 \times (15 + 0.6)] = 42V$$

As a good design practice, some margin is provided to this peak stress voltage to accommodate transient spikes and for a good reliable performance over time. Providing a 30% design margin as a rule of thumb, the minimum rating on the primary MOSFET needs to be 54.6V.

The RMS current through the MOSFET can be calculated from:

$$I_{rms,FET} = I_{pk} \cdot \sqrt{\frac{d}{3}} = 1.06 \cdot \sqrt{\frac{0.35}{3}} = 0.362A \quad \text{(EQ. 9)}$$

Selecting the conduction loss in the MOSFET to 1% of total output power, 0.03W. The required MOSFET's $r_{DS(ON)}$ to achieve the required conduction loss is shown in Equation 10.

$$r_{DS(ON)} = \frac{P_{FET,cond-loss}}{I^2_{FET,rms}} = \frac{0.03}{0.362^2} = 0.229\Omega \quad \text{(EQ. 10)}$$

Vishay's SI4436DY is selected in this design.

Output Diode Selection

Schottky diodes are recommended for the output diode due to their low forward voltage drop. The voltage stress across the output diode can calculated by:

$$V_{Diode} = n \times V_{IN,MAX} + V_{OUT} = 1 \times 26.4 + 15 = 41.4V \quad \text{(EQ. 11)}$$

Diodes Inc's B180 are employed in this design.

Output Filter

The output capacitance needs to meet the ripple and noise requirements, and also be able to handle the ripple current. Assuming ceramic capacitors are used as the output filter, the voltage ripple from the capacitor's ESR is negligible. The minimum capacitance required to meet specifications can be approximately calculated from Equation 12.

$$C_{OUT} > \frac{\Delta V_{PP}}{2} \cdot \frac{(1-d_2) \cdot T_{SW}}{I_{OUT}} > \frac{50\times10^{-3}}{2} \cdot \frac{(1-0.5)}{0.1 \cdot 300\times10^{3}} > 0.42\mu F \quad \text{(EQ. 12)}$$

10µF ceramic capacitors are selected for each output. Design margin has been provided to account for noise spikes.

Snubber Circuit

When the MOSFET switches off, it interrupts the current that flows through the transformer leakage inductance. An RCD snubber circuit is typically used in flyback converters to clamp voltage spikes on the MOSFET.

Assuming that the transformer leakage inductance is 2% of the magnitizing inductance, the energy stored in the leakage inductance during MOSFET's on-time is:

$$W_L = \frac{1}{2} \cdot L_L \cdot I^2_{LM} = \frac{1}{2} \cdot 0.02 \cdot 23.8\times10^{-6} \cdot (1.06)^2 = 267.4nJ \quad \text{(EQ. 13)}$$

Average power transferred to the snubber circuit is:

$$P_L = W_L \cdot F_{SW} = 267.4\times10^{-9} \cdot 300\times10^{3} = 0.08W \quad \text{(EQ. 14)}$$

To limit peak voltage spikes across the MOSFET to 50V, the snubber voltage is set to:

$$V_S = peakV_{MOSFET} - V_{IN,MIN} = 50 - 21.6 = 28.4V \quad \text{(EQ. 15)}$$

The average power transferred to the snubber circuit in Equation 14 is dissipated by the snuuber resistor, so R_S is determined by:

$$R_S = \frac{V_S^2}{P_I} = \frac{28.4^2}{0.08} = 10.08k\Omega \quad \text{(EQ. 16)}$$

So R_S = 10kΩ is selected. Cs is selected such that the R_SC_S time constant is substantially longer than the switching period to keep low ripple voltage on the snubber circuit. A time constant of 10 times the switching period is used for calculation:

$$C_S \approx 10 \cdot \frac{T_{SW}}{R_S} = 10 \cdot \frac{3.33\times10^{-6}}{10\times10^{3}} = 3.33nF \quad \text{(EQ. 17)}$$

C_S = 3.33nF is used in the design.

Feedback Network

The feedback is being tapped off of the primary auxiliary winding. This is one of the advantages of selecting the flyback topology, since the auxiliary winding voltage follows the output. This scheme was fully exploited, since the load fluctuation is minimal, and that load regulation does not suffer much at these power levels. For tighter regulation requirements, an opto-coupled solution would need to be used, which leads to additional cost.

Referring to the schematic on page 8, the output voltage can be set by:

$$\frac{R_{22}}{R_{23}} = \frac{V_{OUT} + V_F}{V_{ref}} - 1 = \frac{15 + 0.6}{2.514} - 1 = 5.2 \quad \text{(EQ. 18)}$$

R_{23} = 1kΩ and R_{22} = 5.23kΩ are selected.

The control-to-output transfer function of the DCM flyback converter is [1]:

$$G_{vc} = K \cdot \sqrt{\frac{R_E \cdot L_M \cdot F_{SW}}{2}} \cdot \frac{1 + s \cdot ESR \cdot C}{(1 + s \cdot 0.5 \cdot R_E \cdot C_E)} \quad \text{(EQ. 19)}$$

Where:

R_E = Equivalent load resistor reflected to the auxiliary output.

C_E = Equivalent capacitor reflected to the auxiliary output.

ESR = Equivalent series resistance of the output capacitor.

$K = I_{SPK(MAX)}/V_{C(MAX)}$.

The equivalent load reflected to the auxiliary output can be estimated from:

$$R_E = \frac{V_{aux}^2}{P_{OUT(Total)}} = \frac{(15V)^2}{3W} = 75\Omega \quad \text{(EQ. 20)}$$

The equivalent capacitor reflected to the auxiliary output can be estimated from:

$$C_E = C_{aux} + \frac{N_{S1}}{N_{aux}} \cdot C_{OUT1} + \frac{N_{S2}}{N_{aux}} \cdot C_{OUT2} = 1\mu F + \frac{15}{15} \cdot 10\mu F + \frac{15}{15} \cdot 10\mu F = 21\mu F \quad \text{(EQ. 21)}$$

The value of $I_{SPK(MAX)}$ can be determined by assuming that the auxiliary output delivers all of the output power.

$$I_{SPK(MAX)} = \frac{2 \cdot \frac{P_{OUT(MAX)}}{V_{AUX}}}{D_2} = \frac{2 \cdot \frac{4W}{15V}}{0.5} = 1.067A \quad \text{(EQ. 22)}$$

$P_{OUT(MAX)}$ = The maximum power allowed = 4W

$V_{C(MAX)}$ has value of 1.1V, clamped by ISL6844's internal circuit. Along with the result from Equation 22, K has a value of 0.97.

Replaces K and the results from Equation 21 and Equation 22 into Equation 19, yields

$$G_{vc} = 15.87 \cdot \frac{1}{(1 + s \cdot 7.875 \times 10^{-4})} \quad \text{(EQ. 23}$$

Note that with the low ESR values of the output ceramic capacitor, the zero due to their ESR is located at the frequency significantly higher than the switching frequency. As the result, the impact of capacitor's ESR is neglected for compensator design.

From Equation 20, it shows that when the total output power reduces, the equivalent load resistor increases. This increases the DC-gain in Equation 19, also the pole is moved to the lower frequency.

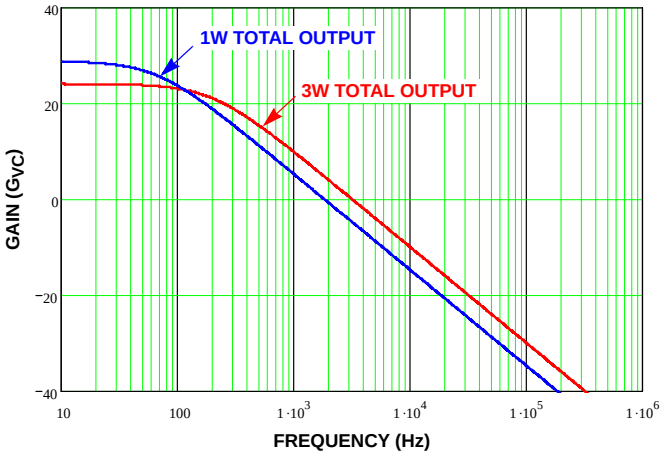


FIGURE 3. GAIN OF G_{VC}

From Equation 23, the pole of the control-to-output transfer function for 3W output is located at 202Hz. Setting the closed-loop's bandwidth of 10kHz, the feedback compensation must have a mid-band gain of 3.11 (10dB). The mid-band gain is determined by

$$A_{mid-band} = \frac{R_{24}}{R_{22}} \quad \text{(EQ. 24)}$$

Therefore, R_{24} is selected to be 16.2kΩ.

The first zero of compensation is set at 1/3 of the crossover frequency, 3.33kHz. C_9 can be calculated from:

$$C_9 = \frac{1}{2 \cdot \pi \cdot 3.33 \times 10^3 \cdot 16.2 \times 10^3} = 2.95nF \quad \text{(EQ. 25)}$$

2.7nF is used for C_9.

The second zero of compensation is set at half of the switching frequency. C_{10} can be calculated from:

$$C_{10} = \frac{1}{2 \cdot \pi \cdot 150 \times 10^3 \cdot 16.2 \times 10^3} = 65.5pF \quad \text{(EQ. 26)}$$

68pF is used for C_{10}.

Printed Circuit Board

The fixture of the PCB is a 2-layer board with dimensions of 4 by 6 centimeters. All components are surface-mount packages and are placed in the top layer.

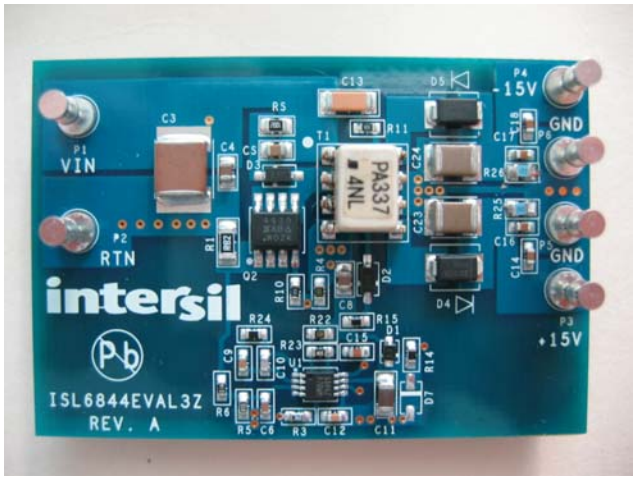


FIGURE 4. EVALUATION BOARD PHOTO (TOP SIDE)

FIGURE 5. EVALUATION BOARD PHOTO (BOTTOM SIDE)

TABLE 1. TERMINAL

TERMINALS	SIGNALS
P1	VIN (Input voltage)
P2	RTN (Input ground return)
P3	+15V (+15V output voltage)
P4	+15V(-15V output voltage)
P5,P6	GND (Output ground)

Reference

[1] Dixon, Lloyd H., “Closing the Feedback Loop”, Unitrode Power Supply Design Seminar, slup068, 1984.

Typical Performance Curves

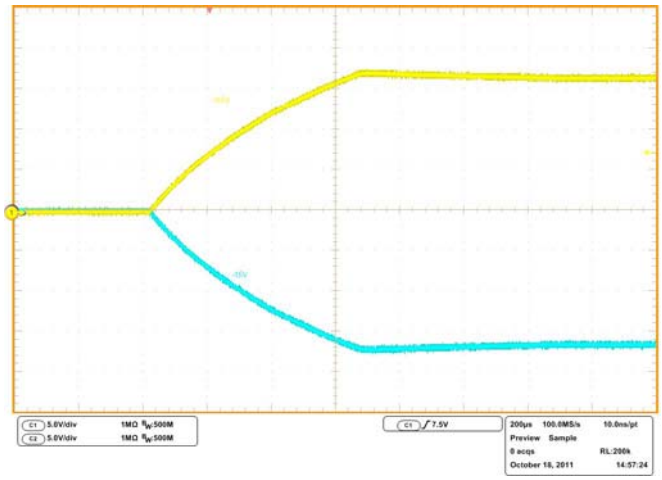


FIGURE 6. START UP AT NO LOAD

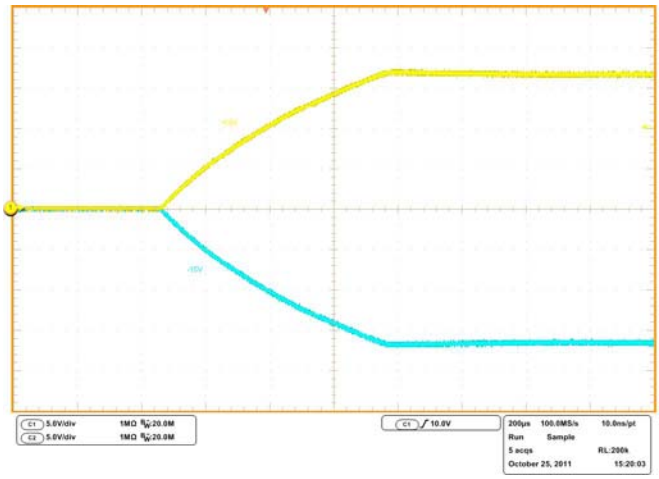


FIGURE 7. START UP AT FULL LOAD

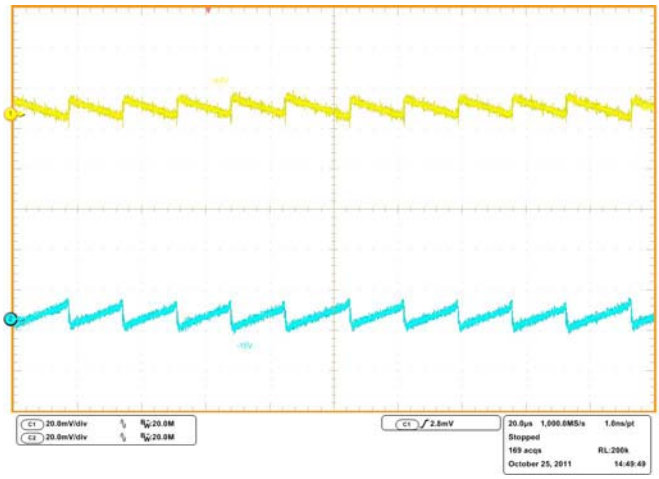


FIGURE 8. OUTPUT RIPPLES AT NO LOAD

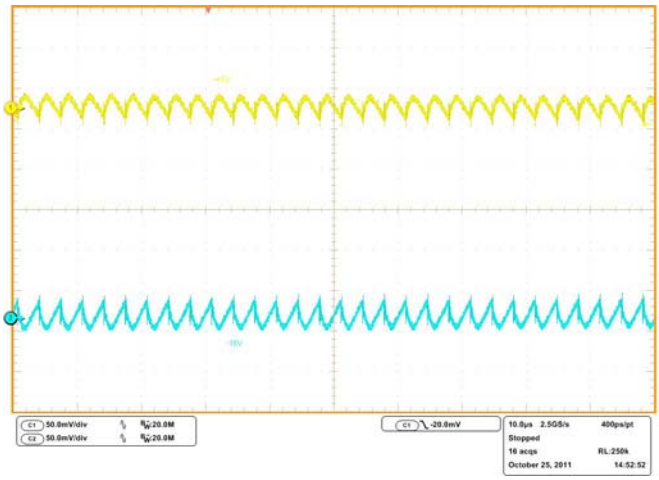


FIGURE 9. OUTPUT RIPPLES AT FULL LOAD

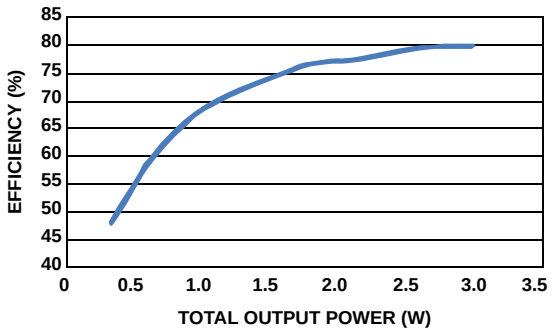


FIGURE 10. EFFICIENCY

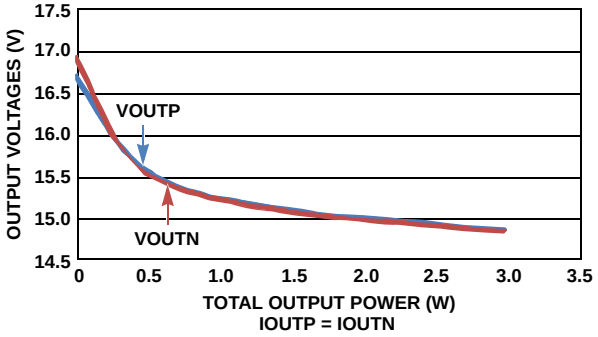


FIGURE 11. OUTPUT VOLTAGE REGULATIONS

Typical Performance Curves (Continued)

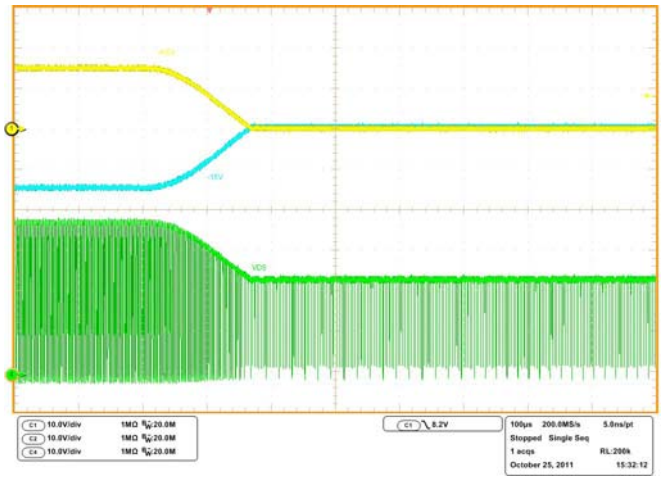
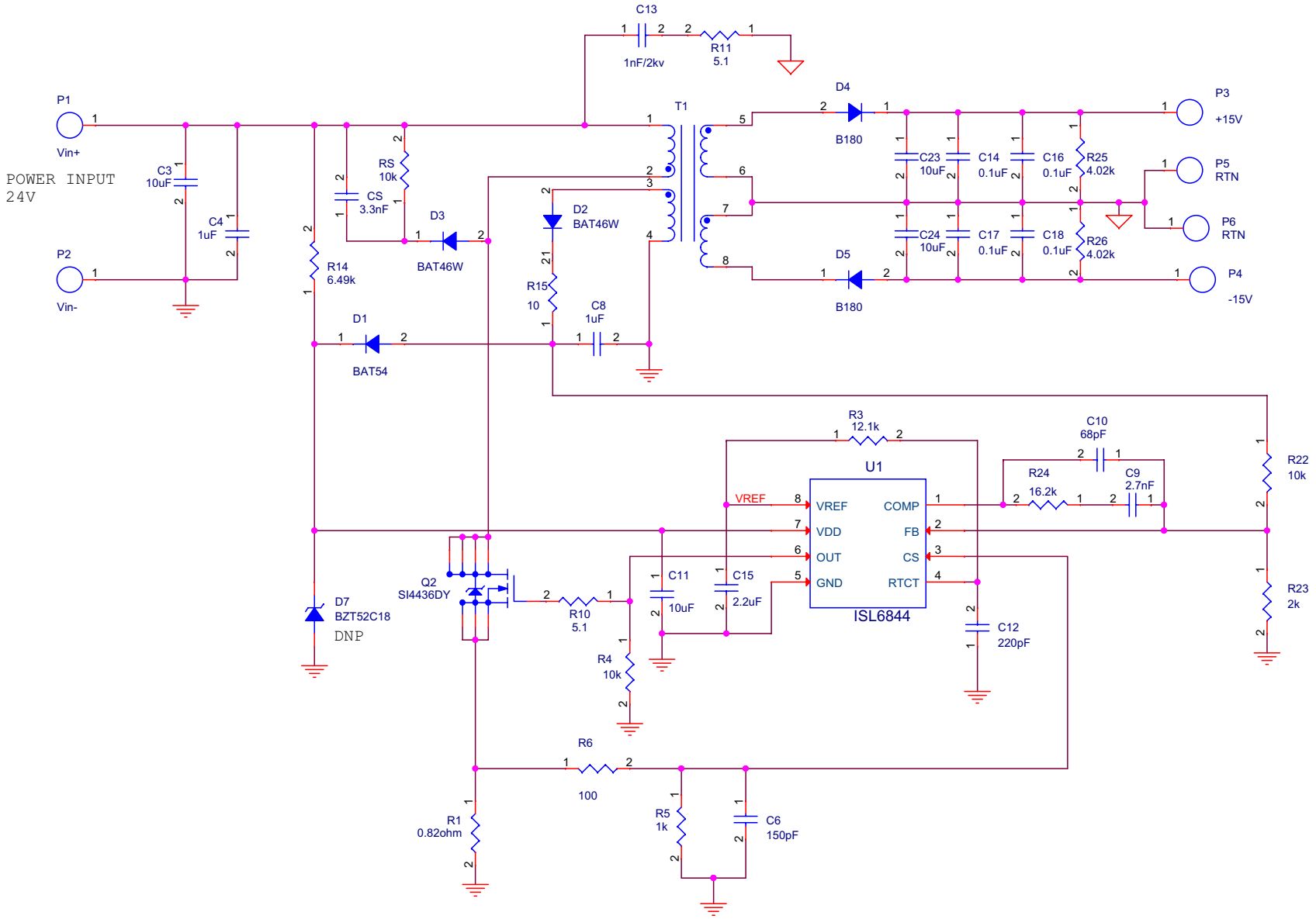


FIGURE 12. OVER CURRENT RESPONSE

Schematic


C13
1nF/2kv
R11
5.1
P1
Vin+
POWER INPUT
24V
P2
Vin-
C3
10uF
C4
1uF
RS
10k
CS
3.3nF
D3
BAT46W
R14
6.49k
D1
BAT54
T1
D4
B180
D5
B180
D2
BAT46W
R15
10
C8
1uF
C23
10uF
C14
0.1uF
C16
0.1uF
R25
4.02k
C24
10uF
C17
0.1uF
C18
0.1uF
R26
4.02k
P3
+15V
P5
RTN
P6
RTN
P4
-15V
R3
12.1k
U1
VREF
VDD
OUT
GND
COMP
FB
CS
RTCT
ISL6844
C10
68pF
R24
16.2k
C9
2.7nF
R22
10k
R23
2k
C12
220pF
Q2
SI4436DY
R10
5.1
C11
10uF
C15
2.2uF
D7
BZT52C18
DNP
R4
10k
R6
100
R1
0.82ohm
R5
1k
C6
150pF

Bill of Materials

REF DES	QTY	PART NUMBER	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL6844IUZ	IC, PWM Controller	MSOP-8	Intersil
Q2	1	SI4436DY	MOSFET, N-channel, 60V	SOP-8	Vishay
D1	1	BAT54WS	Schottky Diode, 30V	SOD323F	Diodes Inc.
D2, D3	2	BAT46W	Schottky Diode, 100V	SOD123	Diodes Inc.
D4, D5	2	B180	Schottky Diode, 80V, 1A	SMA	Diodes Inc.
D7	DNP	BZT52C18	Zener Diode 18V	SMA	Diodes Inc.
T1	1	PA3374NL	Transformer, Custom		Pulse
C3	1	C5750X7R1H106K	Capacitor, ceramic, X7R, 10µF, 20%, 50V	SM_2210	Generic
C4	1		Capacitor, ceramic, X7R, 1.0µF, 20%, 50V	SM_0805	Generic
C6	1		Capacitor, ceramic, X5R, 150pF, 20%, 50V	SM_0603	Generic
C8	1		Capacitor, ceramic, X5R, 1.0µF, 20%, 25V	SM_0805	Generic
C9	1		Capacitor, ceramic, X5R, 2.7nF, 20%, 50V	SM_0603	Generic
C10	1		Capacitor, ceramic, X5R, 68pF, 20%, 50V	SM_0603	Generic
C11	1		Capacitor, ceramic, X5R, 10µF, 20%, 25V	SM_1206	Generic
C12	1		Capacitor, ceramic, X7R, 220pF, 20%, 50V	SM_0603	Generic
C13	1	C4520X7R3D102K	Capacitor, ceramic, X7R, 1000pF, 10%, 2kV	SM_1808	TDK
C14, C16, C17, C18	4		Capacitor, ceramic, X7R, 100nF, 10%, 50V	SM_0603	Generic
CS	1		Capacitor, ceramic, X7R, 3.3nF, 20%, 50V	SM_0805	Generic
C15	1		Capacitor, ceramic, X7R, 2.2µF, 20%, 10V	SM_0603	Generic
C23, C24	2		Capacitor, ceramic, X5R, 10µF, 10%, 25V	SM_1812	Generic
R1	1		Resistor, 0.82Ω, 1%, 1/4W	SM_1206	Generic
R3	1		Resistor, 12.1kΩ, 1%, 1/16W	SM_0603	Generic
R4, R22	2		Resistor, 10kΩ, 5%, 1/16W	SM_0603	Generic
R5	1		Resistor, 1kΩ, 1%, 1/16W	SM_0603	Generic
R6	1		Resistor, 100Ω, 1%, 1/16W	SM_0603	Generic
R10, R11	2		Resistor, 5.1Ω, 1%, 1/16W	SM_0603	Generic
R14	1		Resistor, 6.49kΩ, 1%, 1/16W	SM_0603	Generic
R15	1		Resistor, 10Ω, 1%, 1/16W	SM_0603	Generic
RS	1		Resistor, 10kΩ, 5%, 1/4W	SM_1206	Generic
R23	1		Resistor, 2kΩ, 1%, 1/16W	SM_0603	Generic
R24	1		Resistor, 16.2kΩ, 5%, 1/16W	SM_0603	Generic
R25, R26	2		Resistor, 4.02kΩ, 5%, 1/16W	SM_0603	Generic

ISL6844EVAL3Z Printed Circuit Board Layers

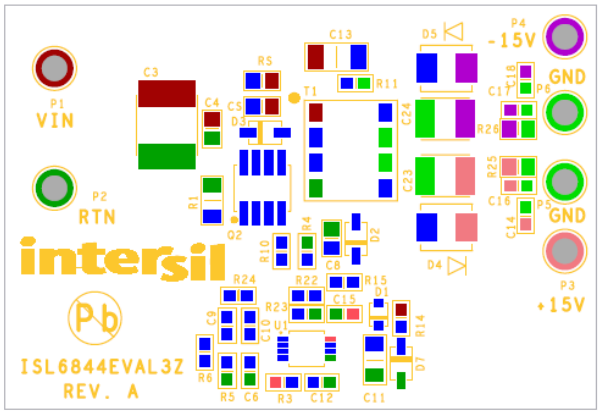


FIGURE 1. ISL6844EVAL3Z - TOP LAYER (SILKSCREEN)

FIGURE 2. ISL6844EVAL3Z - TOP LAYER (COMPONENT SIDE)

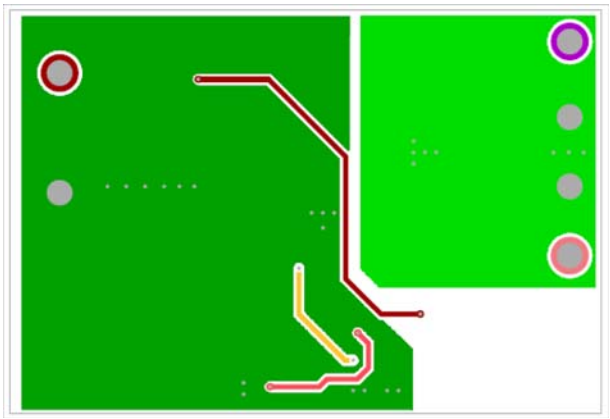


FIGURE 3. ISL6844EVAL3Z - BOTTOM LAYER (SOLDER SIDE)

FIGURE 4. ISL6844EVAL3Z - BOTTOM LAYER (SILKSCREEN)