FEMTOCLOCK™ CRYSTAL-TO-3.3V, 2.5V LVPECL CLOCK GENERATOR

ICS843001CI

GENERAL DESCRIPTION

The ICS843001CI is a Fibre Channel Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS843001CI uses either a 26.5625MHz or a 23.4375MHz crystal to synthesize 106.25MHz, 187.5MHz or 212.5MHz, using the FREQ_SEL pin. The ICS843001CI has excellent <1ps phase jitter performance, over the 637kHz – 10MHz integration range. The ICS843001CI is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- One differential LVPECL output pair
- Crystal oscillator interface designed for 23.4375MHz or 26.5625MHz, 18pF parallel resonant crystal
- Selectable 106.25MHz, 187.5MHz or 212.5MHz output frequencies
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.31ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
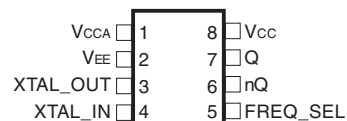- Available in lead-free (RoHS 6) package

FUNCTION TABLE

Inputs		Output Frequencies
Crystal Frequency	FREQ_SEL	
26.5625MHz	0	106.25MHz (Default)
26.5625MHz	1	212.5MHz
23.4375MHz	1	187.5MHz

BLOCK DIAGRAM
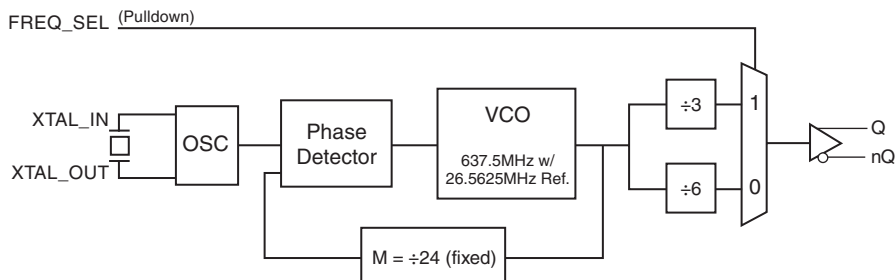
PIN ASSIGNMENT

ICS843001CI
8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin.
2	V_{EE}	Power		Negative supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

NOTE: *Pulldown* refers to an internal input resistor. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA} 8 Lead TSSOP	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} - 0.21	3.3	V_{CC}	V
I_{CCA}	Analog Supply Current	included in I_{EE}			21	mA
I_{EE}	Power Supply Current				72	mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} - 0.16	2.5	V_{CC}	V
I_{CCA}	Analog Supply Current	included in I_{EE}			16	mA
I_{EE}	Power Supply Current				67	mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	FREQ_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	FREQ_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

TABLE 3D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 3E. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		23.4375		26.5625	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5A. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 1	186.67		226.66	MHz
		FREQ_SEL = 0	93.33		113.33	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1	212.5MHz, (637kHz to 10MHz)		0.27		ps
		187.5MHz, (1.875MHz to 20MHz)		0.20		ps
		106.25MHz, (637kHz to 10MHz)		0.31		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		450	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plots.

TABLE 5B. AC CHARACTERISTICS, V_{CC} = 2.5V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 1	186.67		226.66	MHz
		FREQ_SEL = 0	93.33		113.33	MHz
$t$jit(Ø)	RMS Phase Jitter, (Random); NOTE 1	212.5MHz, (637kHz to 10MHz)		0.37		ps
		187.5MHz, (1.875MHz to 20MHz)		0.23		ps
		106.25MHz, (637kHz to 10MHz)		0.39		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		450	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plots.
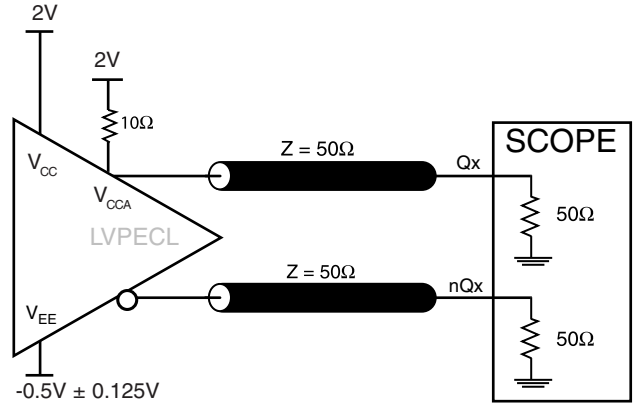
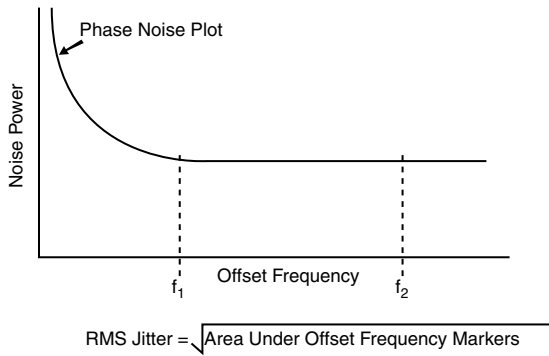## TYPICAL PHASE NOISE AT 106.25MHz
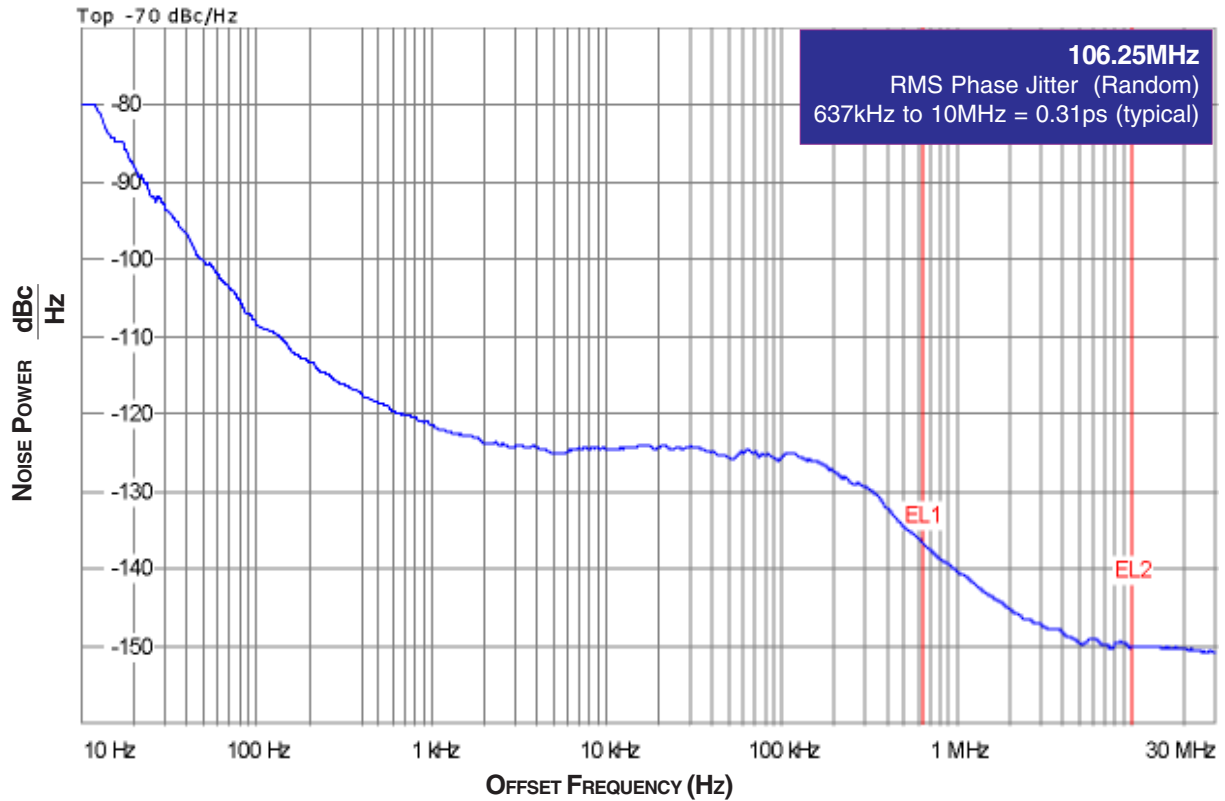
TYPICAL PHASE NOISE AT 212.5MHz
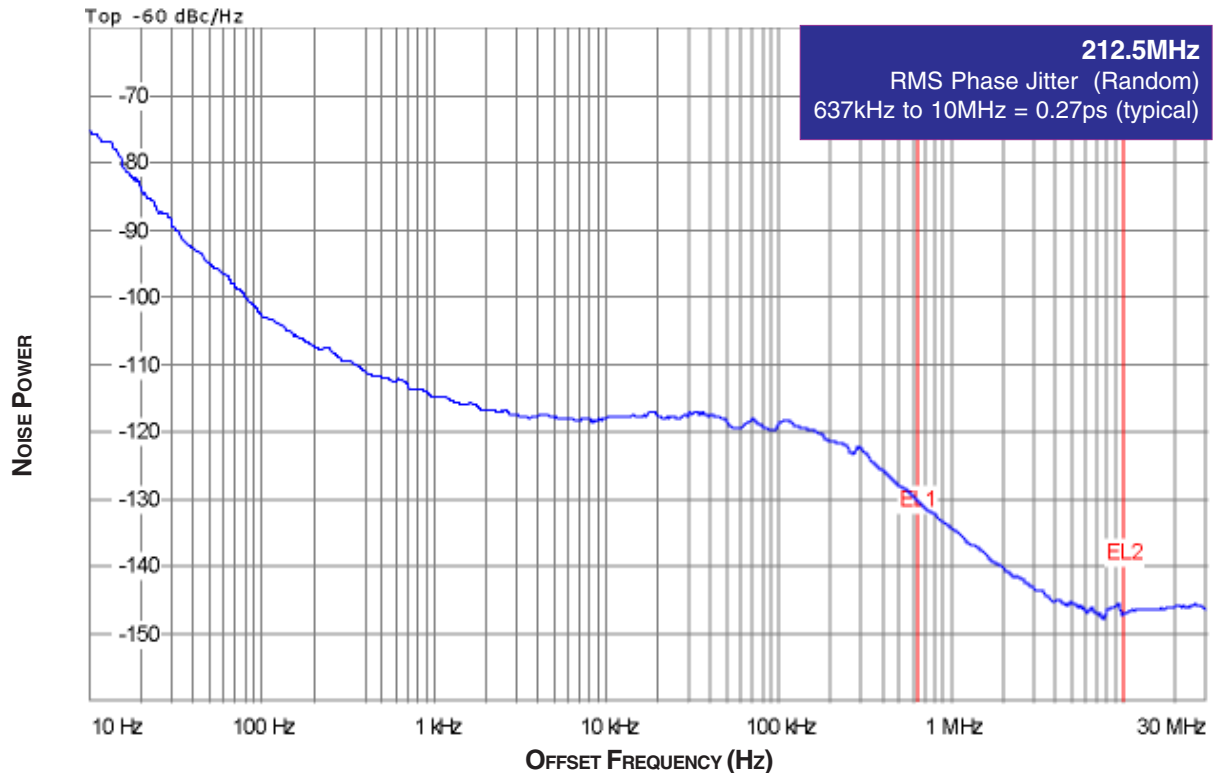
PARAMETER MEASUREMENT INFORMATION
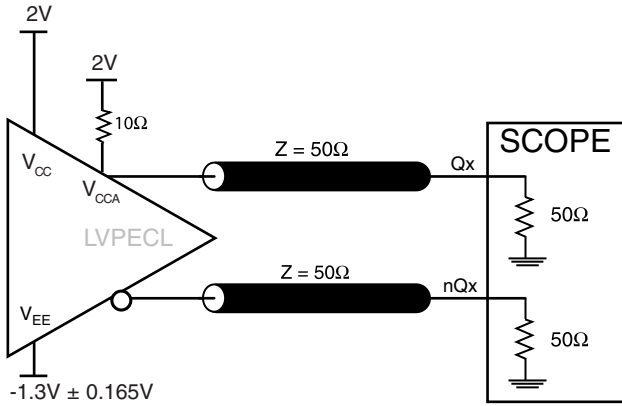
3.3V OUTPUT LOAD AC TEST CIRCUIT

2.5V OUTPUT LOAD AC TEST CIRCUIT

$$\text{RMS Jitter} = \sqrt{\text{Area Under Offset Frequency Markers}}$$

RMS PHASE JITTER
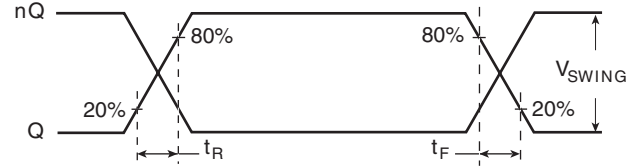
OUTPUT RISE/FALL TIME

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
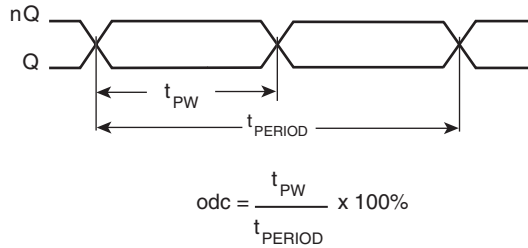
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843001CI provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.
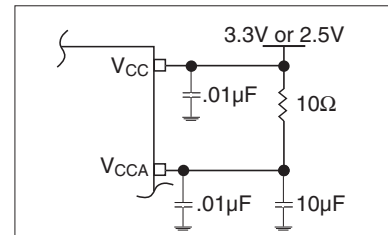
FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843001CI has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel reso- nant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
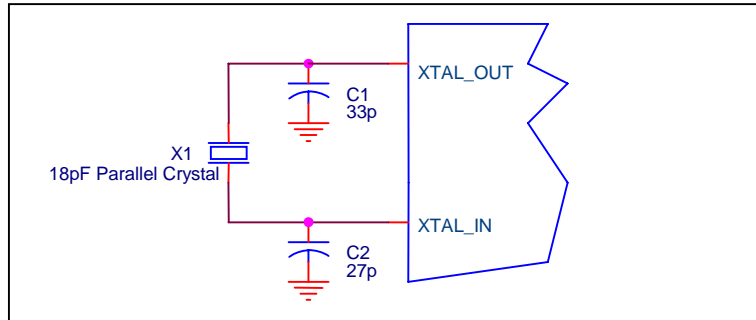

FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.
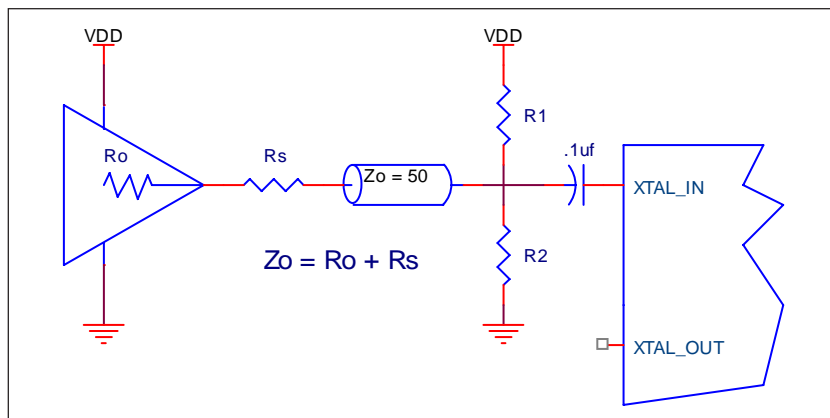

FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.
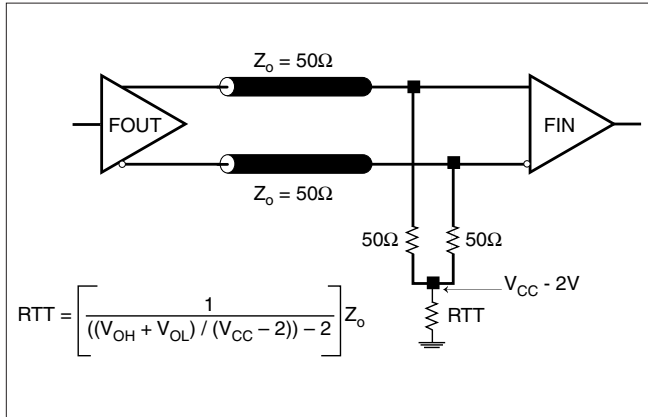

$$RTT = \left[\frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2} \right] Z_o$$

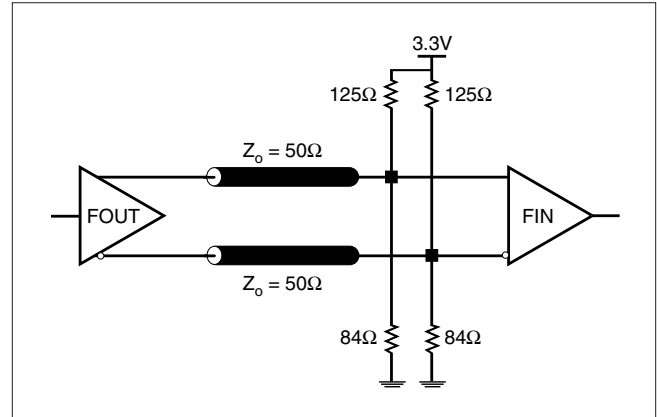**FIGURE 4A. LVPECL OUTPUT TERMINATION**

FIGURE 4B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*
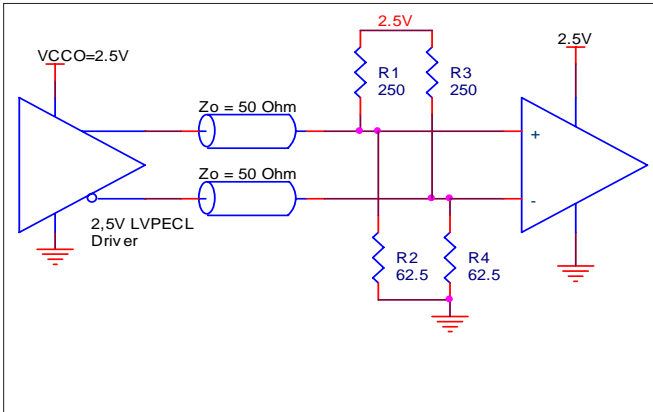

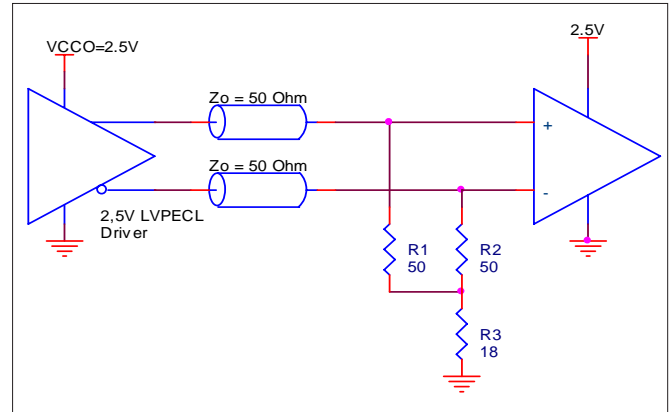**FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**

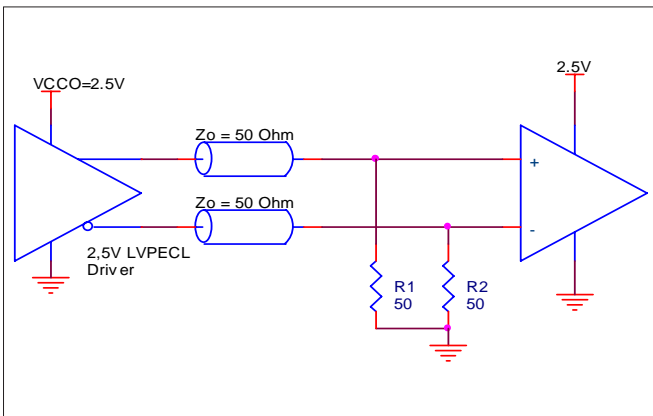**FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**

FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

LAYOUT GUIDELINE

Figure 6A shows a schematic example of the ICS843001CI. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel resonant crystal is used. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. The C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.
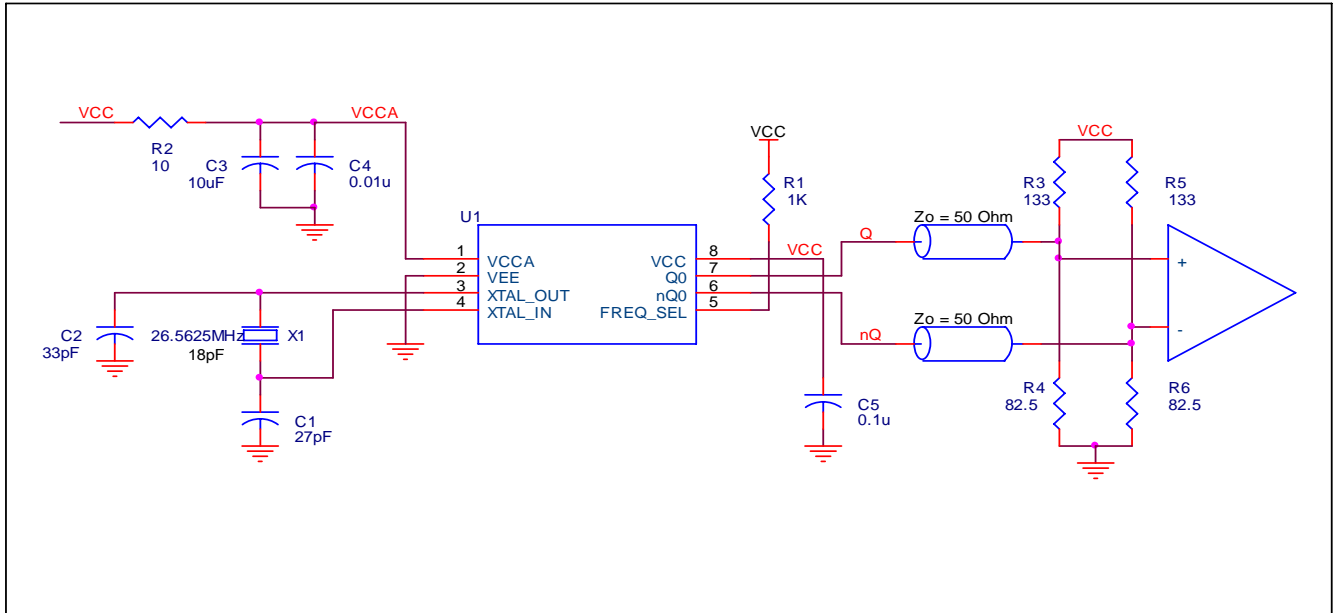

FIGURE 6A. ICS843001CI SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 6B shows an example of ICS843001CI P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.
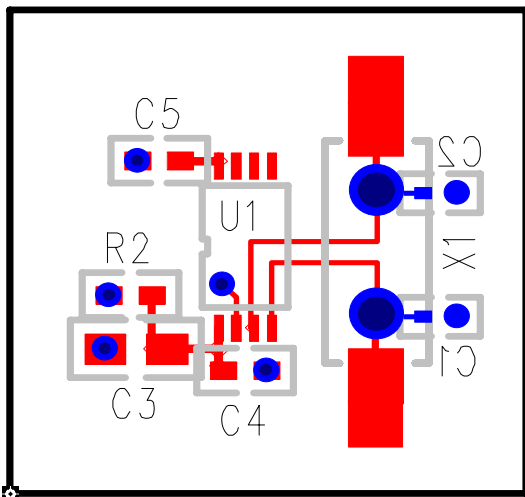

FIGURE 6B. ICS843001CI PC BOARD LAYOUT EXAMPLE

TABLE 6. FOOTPRINT TABLE

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2	0603

NOTE: Table 6, lists component sizes shown in this layout example.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843001CI.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843001C is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 72mA = **249.48mW**

- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

   Total Power $_{MAX}$ (3.465V, with all outputs switching) = 249.48mW + 30mW = **279.48mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

   The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

   Tj = Junction Temperature

   θ_{JA} = Junction-to-Ambient Thermal Resistance

   Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
   T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
   85°C + 0.279W * 129.5°C/W = 121.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)		
0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards 129.5°C/W	125.5°C/W	123.5°C/W

3. Calculations and Equations.
The purpose of this section is to derive the power dissipated into the load.
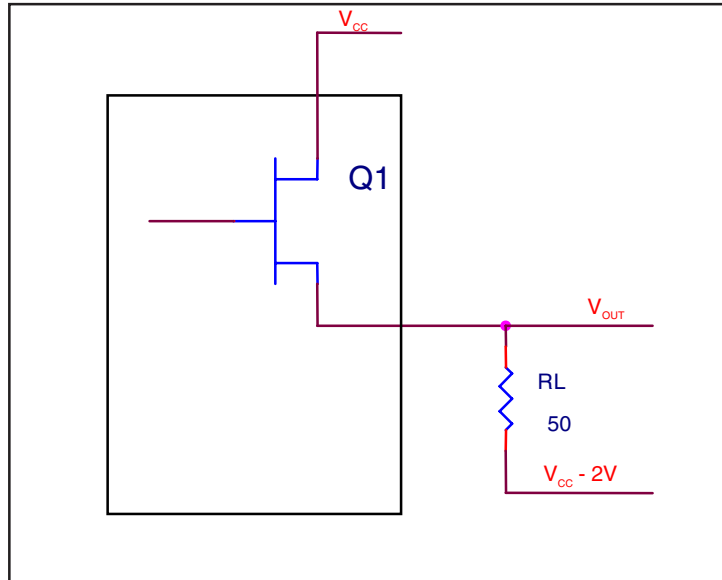LVPECL output driver circuit and termination are shown in *Figure 7.*

FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V = \mathbf{19.8mW}$

Pd_L = $[(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters Per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

TRANSISTOR COUNT

The transistor count for ICS843001CI is: 1764

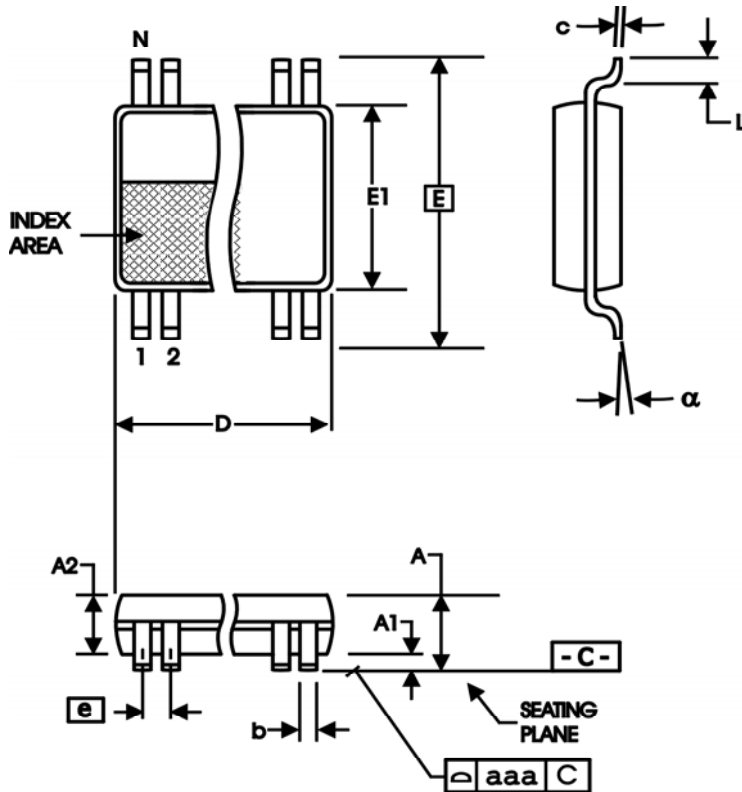# PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE - G SUFFIX 8 LEAD TSSOP

TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	**Maximum**
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843001CGILF	01CIL	8 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
843001CGILFT	01CIL	8 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

For Tech Support
netcom@idt.com
+480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)

IDT™

www.IDT.com