Z02201

V.22BIS DATA PUMP WITH INTEGRATED AFE

Product Specification

PS000904-0107

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Features

Device	Data Pump	AFE	Speed (MHz)
Z02201	16-Bit	Integrated	12.288

- Combined data pump and Analog Front-End (AFE)
- Full duplex data modem throughput to 2400 bps
  - ITU V.22bis, V.23, V.22, V.21
  - Bell 212A and Bell 103
- FSK (V.23 1200/75 bps, V.21/Bell 103 300 bps), DPSK (V.22/Bell 212A 1200 bps), or QAM encoding (V.22bis 2400 bps)
- Automatic handshake plus full manual control over handshake timings
- Scrambler/descrambler functions plus selectable control over internal data pump functions
- Programmable Bi-Quad tone detectors for call-progress tone detection
- Adaptive equalization to compensate for a wide variety of line conditions
- Programmable transmit attenuation and selectable receive threshold
- Fully programmable call-progress detectors, signal quality detectors, tone detectors, tone generators, and transmit signal levels which aid in rapid country qualifications
- Simultaneous tone generation and detection
- Host port allows direct parallel interface to standard 8-bit microprocessors
- HDLC framing at all speeds
- On-chip peripherals
  - Full-duplex voice band AFE with 12-bit resolution
  - Synchronous Serial Interface port
  - Eye pattern interface
- Low power consumption: 50 mA typical
- 44-Pin PQFP and PLCC packages
- Single +5 VDC power supply
- 0 °C to +70 °C commercial temperature range

Note: International Telecommunications Union (ITU), formerly CCITT.

General Description

The Z02201 is a synchronous single-chip modem solution that provides a means to construct a V.22bis modem capable of 2400 bps full duplex over dial-up lines. The Z02201 is specifically designed for use in embedded modem applications where space, performance, and low power consumption are key requirements.

Operating over the Public Switched Telephone Network (PSTN), the Z02201 meets the modem standards for V.22bis, V.22, V.23, V.21, Bell 212A, and Bell 103.

A typical modem application can be made by simply adding a control microprocessor (host), phone-line interface, and DTE interface.

The Z02201 performs HDLC framing at all speeds. This capability eliminates the requirement for an external Serial Input/Output (SIO) device for Data Terminal Equipment (DTE) in products incorporating error control.

All modulation, demodulation, filtering, A/D and D/A conversion functions for transmit and receive are provided on-chip. Automatic and selectable compromise equalizers are included to optimize performance over a wide range of line types.

The Z02201 device compensates for a wide variety of adverse line conditions by using a combination of fixed link, fixed cable, and adaptive equalizers.

The Z02201 provides comprehensive selectable and programmable tone generation and detection.

All digital I/O signals are TTL compatible. The parallel interface is compatible with standard 8-bit microprocessors, allowing direct access to eight I/O registers and indirect access to the modem RAM.

The RAM access capability allows the host to retrieve diagnostic data, modem/line status and control data, and set programmable coefficients. The serial interface is used for data transfers. All control and status information is transferred by means of the parallel interface.

The Z02201 transmit drivers and receive amplifiers can be connected directly to a Data Access Arrangement (DAA) by means of a transformer. Completing this connection reduces the external circuits to a minimum.

In addition, the Z02201 offers further system level savings by providing built-in filters for both the Transmitter Analog Output and the Receiver Analog Input, thus eliminating the need for external filtering components.

The Z02201 device operates on a single +5 VDC power supply. During periods of no traffic, the host can place the modem into SLEEP mode, reducing power consumption to less than 1 percent of full load power.

Note: All signals with an overline, are active Low. For example, B/$\overline{W}$, in which WORD is active Low; or $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

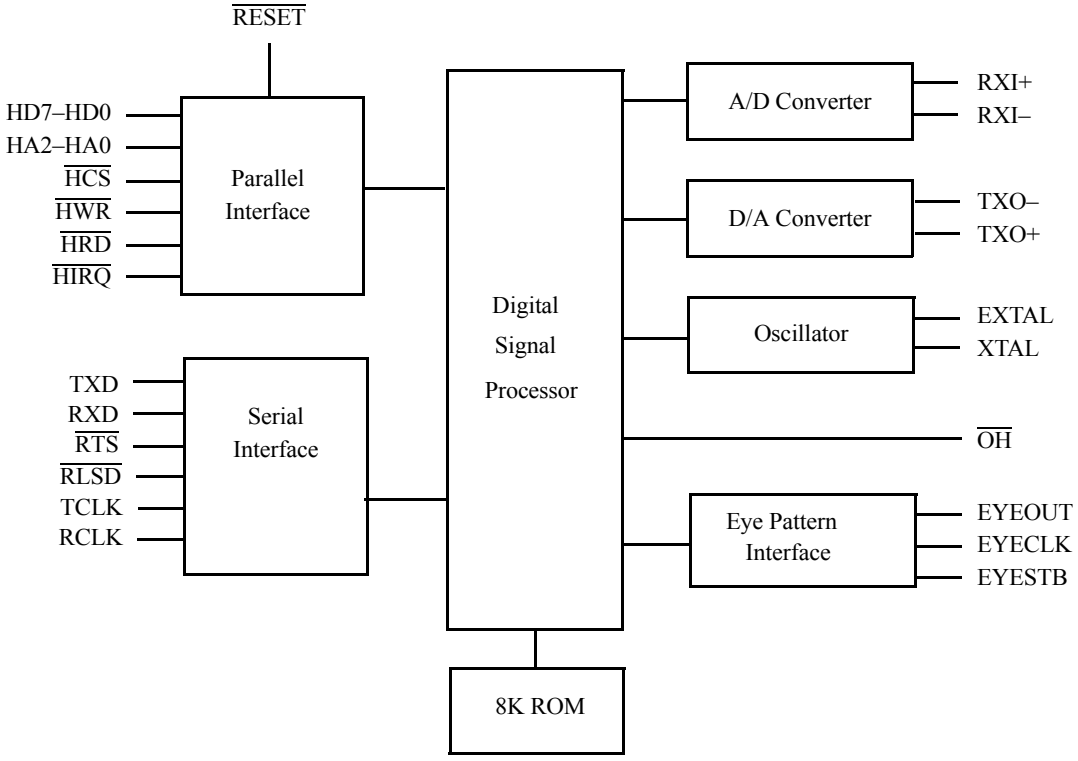


Figure 1. Z02201 Block Diagram

User Information

The ZiLOG Z02201 data pump can be selected for either parallel or serial synchronous data transfer under software control. Figure 2 indicates a block diagram of the general modem chip interface. The hardware and software configurations can be customized for a particular modem application. The parallel interface allows direct access to 7 I/O registers, indirect access to the modem RAM, and is compatible with the Z8, Z80, Z18X family, and other 8-bit microprocessors. The serial interface is used for data transfer. Controls and status information are transferred via the parallel interface. The RAM access capability allows indirect access to diagnostic data, additional status control, and programmable coefficients. The hardware and software interfaces are presented in the subsequent sections.

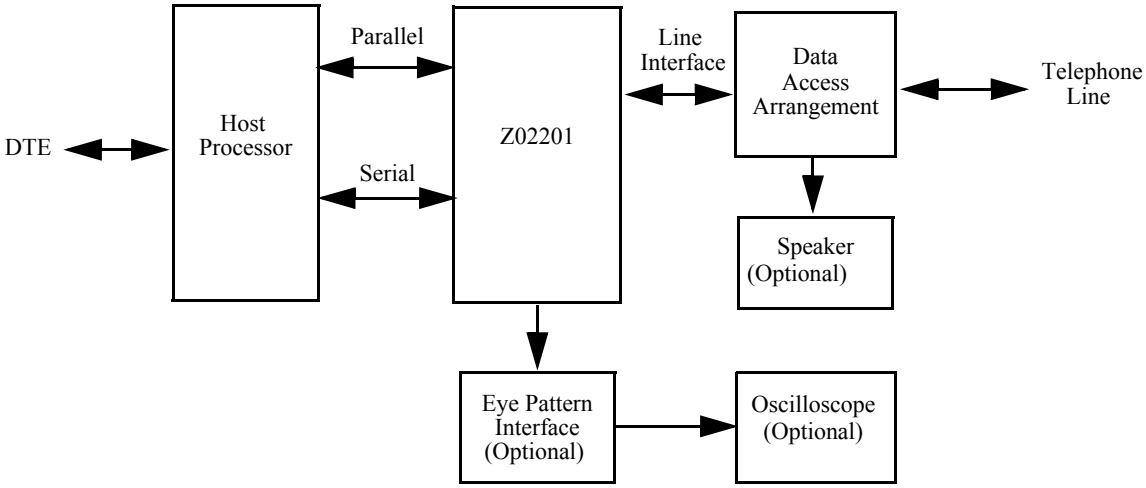


Figure 2. Z02201 System Block Diagram

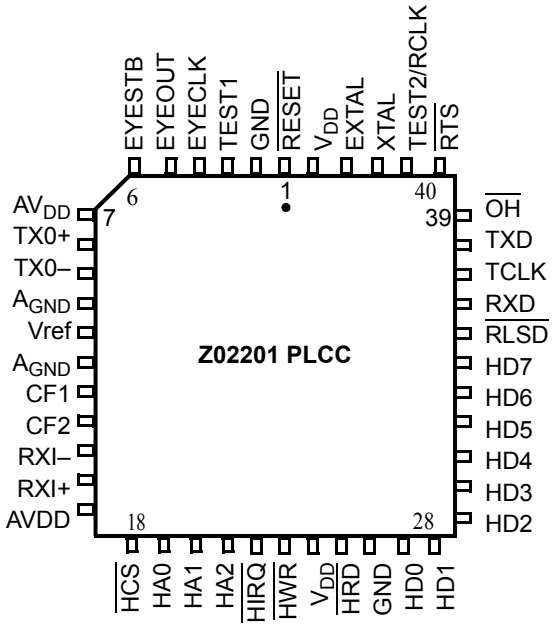


Figure 3. Z02201 44-Lead PLCC Pin Identification

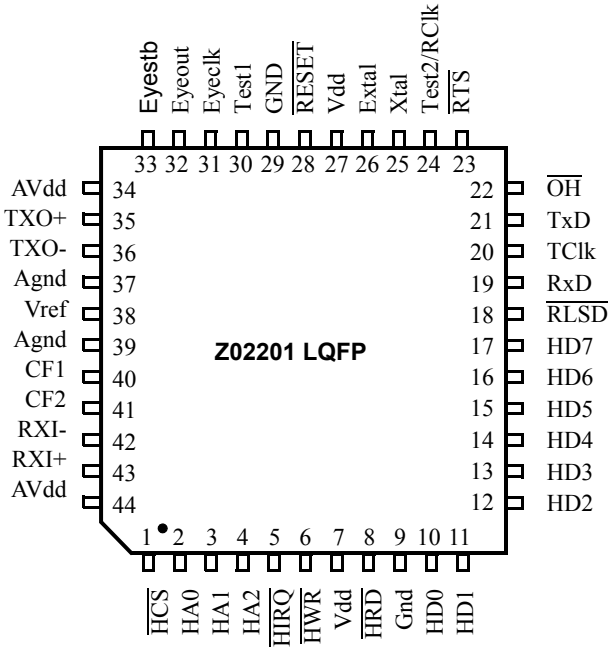


Figure 4. Z02201 44-Lead LQFP Pin Identification

Pin Description

Table 1. Z02201 Pin Assignments

PLCC Pin	LQFP Pin	Signal	Direction
1	28	RESET	
2	29	Gnd	
3	30	Test1	Input
4	31	Eyeclk	Output
5	32	Eyeout	Output
6	33	Eyestb	Output
7	34	AVdd	
8	35	TXO+	Output
9	36	TXO-	Output
10	37	Agnd	
11	38	Vref	Output
12	39	Agnd	
13	40	CF1	Input
14	41	CF2	Input
15	42	RXI-	Input
16	43	RXI+	Input
17	44	AVdd	
18	1	HCS	Input
19	2	HA0	Input
20	3	HA1	Input
21	4	HA2	Input
22	5	HIRQ	Output
23	6	HWR	Input
24	7	Vdd	
25	8	HRD	Input
26	9	Gnd	
27	10	HD0	Input/Output
28	11	HD1	Input/Output

Table 1. Z02201 Pin Assignments (Continued)

PLCC Pin	LQFP Pin	Signal	Direction
29	12	HD2	Input/Output
30	13	HD3	Input/Output
31	14	HD4	Input/Output
32	15	HD5	Input/Output
33	16	HD6	Input/Output
34	17	HD7	Input/Output
35	18	RLSD	Output
36	19	RxD	Output
37	20	TClk	Output
38	21	TxD	Input
39	22	OH	Output
40	23	RTS	Input
41	24	Test2/RClk	Input/Output
42	25	Xtal	Output
43	26	Extal	Input
44	27	Vdd	

Pin Functions

HD7–HD0 *Host Data Bus* (Bidirectional, Active High)—HD0–HD7 constitutes an 8-bit bidirectional data bus used for the transfer of control and status information.

$\overline{\text{HCS}}$ *Host Chip Select* (Input, Active Low)—When $\overline{\text{CS}}$ is Low, data transfer between the data pump and the host is enabled. Data transfers to the data pump registers are 8 bits wide.

$\overline{\text{HWR}}$ *Host Write Enable Strobe* (Input, Active Low)—The write enable strobe is an active Low signal that is used to initiate a write operation to the data pump. During a write operation, data is sent to the data pump by the host via the host data bus.

$\overline{\text{HRD}}$ *Host Read Enable Strobe* (Input, Active Low)—The read enable strobe is an active Low signal that is used to initiate a read operation from the data pump. During a read operation, data is transferred out of the data pump by the host via the host data bus.

$\overline{\text{HIRQ}}$ *Host Interrupt Request* (Output, Active Low)—The $\overline{\text{HIRQ}}$ is an open-drain output that can be tied through an external pull-up resistor to the digital power

supply V_{DD}. The $\overline{HIRQ}$ active Low data pump output can be activated when the host selects this option or requests by setting the RXIE or TXIE bits in the data pump Host Register. This pin can be connected to the host interrupt request pin to initiate host service.

$\overline{RESET}$ *Reset* (Input, Active Low)—The $\overline{RESET}$ signal places the device into its reset state.

HA2–HA0 *Host Address* (Input, Active High)—These three register select lines (pins) are used for addressing the controller-accessible internal registers of the data pump. When $\overline{HCS}$ is active, the state of the HA2–HA0 is used as the internal data pump interface register address. HA2 is the most significant bit; HA0 is the least significant bit.

$\overline{RLSD}$ *Receive Line Signal Detect* (Output, Active Low)—This pin indicates when an input signal has been detected.

RXD *Receive Data* (Output)—The data pump serial receive data is presented by the data pump to the local DTE on the RXD output.

TCLK *Transmit Serial Data Clock* (Output)—The serial data output clock is a synchronous data clock used to transfer serial data via synchronous serial interface between the data pump and the host. The clock frequencies are 2400, 1200, and 300 Hz, corresponding to the supported data bit rates.

TXD *Transmit Data* (Input)—The data pump accepts the serial transmit data from the local DTE on the TXD input when the data pump is configured to the serial transmit data mode. The serial transmit data mode is selected when the TDPM bit (bit 4) of the RAM CONTROL/DATA PUMP STATUS register (Register 6) is reset to 0.

$\overline{OH}$ *Off Hook Relay Control* (Output, Active Low)—This pin is activated to drive a relay which engages the modem with the phone line (the modem equivalent of picking up the receiver).

$\overline{RTS}$ *Request To Send* (Input, Active Low)—The logical OR of this pin and the RTSP bit (bit 3 of register 4), determines the data pump mode of operation. When the result of the logical OR of these two bits is logic 1, the data pump is in transmit mode at the selected speed, thereby placing the data pump in receive mode. In STANDBY mode, the state of this pin is insignificant.

EYECLK *Eye Pattern Clock* (Output, Active High)—Data is valid at the rising edge of the clock. The EYECLK can be used to clock an external Digital-to-Analog (D/A) converter shift register for eye pattern display.

EYEOUT *Eye Pattern Data* (Output, Active High)—This pin controls the serial 16-bit eye pattern output data. The first 8 bits is the EYEX data, and the next 8-bits are the EYEY data. This data can be used for display on an oscilloscope X and Y-axis following D/A conversion.

EYESTB ***Serial Eye Pattern Strobe*** **(Output, Active High)—**This signal is used for loading an external D/A converter.

TXO+ ***Transmit Differential Analog Output Positive*** **(Analog Output)—**The TXO+, TXO– is capable of driving a 600-ohm resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA). The TXO– and TXO+ can be configured either as a differential or single-ended output driver.

TXO– ***Transmit Differential Analog Output Negative*** **(Analog Output)—**The TXO–, TXO+ is capable of driving a 600-ohm resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA).

RXI– ***Receive Differential Analog Input Negative*** **(Analog Input)—**

RXI+ ***Receive Differential Analog Input Positive*** **(Analog Input)—**

TEST1 ***Test Pin 1*** **(Input, Active High)—**This pin is a test pin and must be tied to digital ground.

TEST2/RCLK ***Test Pin 2, Receive Data Clock*** **(Output, Active High)—**This pin is a test pin and must be tied to digital ground through a pull-down resistor. The resistor should be Low enough to ensure this pin floats below 0.8V when the part is in the $\overline{\text{RESET}}$ state. After $\overline{\text{RESET}}$, this pin becomes the Receive Data Clock Output. The resistor should be high enough such that the output can be driven to logic `1`. This pin is a synchronous data clock used to transfer serial data between the data pump and the host. The clock frequencies are 2400, 1200, and 300 Hz corresponding to the supported data bit rates.

Vref ***Reference Voltage*** **(Output, Active High—**An internally generated reference voltage.

XTAL ***Crystal*** **(Output, Active High)—**Crystal oscillator connection. This pin must be left open if an external clock is used instead of a crystal. The data pump chip can be connected to an external crystal circuit consisting of 24.576-MHz (parallel resonant) crystal, a resistor, and two capacitors.

EXTAL External Clock/ ***Crystal*** **(Input, Active High)—**Crystal oscillator connection. An external clock can be input to the Z02280 on this pin when a crystal is not used. The oscillator input is not a TTL level (see DC characteristics in Table 4).

CF1 and CF2 ***Integration Capacitor Pins 1 and 2*** **(Analog Input)—**Connect an 82pF capacitor between CF2 and CF1 to complete the internal feedback integration filter for improved Analog-to-Digital (A/D) conversion performance.

GND ***Digital ground***–0 Volts**—**

V_{DD} ***Digital Power***–5 Volts**—**

AV_{DD} ***Analog Power***–5 Volts**—**

AGND ***Analog Ground***–0 Volts**—**

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	+7.0	V
T_{OPR} (com)	Operating Temperature	0	+70	°C
T_{STG}	Storage Temperature	–65	+150	°C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The DC Parameters were tested as per Table 6. The Z02201 tester has active loads which are used to test the loading for I_{OH} and $I_{OR.}$

Available operating temperature range is: where: S = Standard Temperature Range

S = 0°C to +70°C

Voltage Supply Range:

+4.5 V ≤ V_{CC} ≤ + 5.5 V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus, and 100 pF for address and control lines.

Environmental and power requirements

The modem power and environmental requirements are indicated in Table 3 and Table 4.Table 5 provides the crystal specifications.

Table 3. Power Requirements

Voltage	Current Typical @ 25°C	Current Maximum @ 0°C
+5 V_{DC}, Operating	50 mA	<=100 mA
+5 V_{DC}, Sleep	25 µA	<=125 µA

Note: All voltages are ±5% DC and must have ripple less than 0.1V peak to peak. If switching supply is used, the frequency may be between 20 kHz and 150 kHz. No component of the switching frequency should be present outside of the supply greater than 500 µV peak.

Table 4. Environmental Requirements

Parameter	Value
Ambient Temperature Under Bias (Commercial Temp Range)	0°C to +70°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin to V_{SS}	–0.3V to +7V
Power Dissipation	250 mW
Soldering Temperature 0.5 sec	+230°C

Table 5. Z02201 Crystal Specifications

Parameter	Value
Temperature Range (Commercial)	0°C to +70°C
Nominal Frequency @ 25°C	24.576 MHz
Frequency Tolerance @ 25°C	±20 ppm
Temperature Stability @ 0°C to 70°C	±25 ppm
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF max.

Table 5. Z02201 Crystal Specifications (Continued)

Parameter	Value
Load Capacitance	32 ± 0.3 pF
Drive Level	1.0 mW max.
Aging, per Year Max.	± 5 ppm
Oscillation Mode	Fundamental
Series Resistance	60 ohms max.
Max. Frequency Variation with 28.8 or 35.2 pF load	±30 ppm

DC Characteristics

Table 6. TDC Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Test Conditions
Pin Types I and I/O: Input and Input-Output						
V_{IH}	Input High Voltage	2	–	V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	0	–	0.8	V	
I_L	Input Leakage Current	–10	–	10	µA	GND <V0<V_{DD}
Pin Types O and IO: Output and Input-Output						
V_{OH}	Output High Voltage	2.4	–	–	V	$I_{OH=}$ –200 µA
V_{OL}	Output Low Voltage	0	–	0.4	V	$I_{OI=}$ –2.2 mA
I_{OZ}	Tri-state Leakage Current	–10	–	10	µA	GND<V0<V_{DD}
Pin Types I-PU and I-PD: Input with Internal Pull-up/Pull-down Resistor						
V_{IH}	Input High Voltage	2		V_{CC} +0.3	V	$I_{OI=}$ –2.2 mA
V_{IL}	Input Low Voltage	0		0.8	V	
I_{IL}	Input Current	–10		10	µA	GND <V0<V_{DD}
Pin Type XI: Crystal Input						
V_{IH}	Input High Voltage	V_{DD} x0.8		V_{DD}	V	
V_{IL}	Input Low Voltage	0				
Pin Type O-OD: Output with Open-Drain						
V_{OL}	Output Low Voltage	0	–	0.4		I_{OI}=2.2 mA
I_{OZ}	Tri-state Leakage Current	–10	–	10	µA	GND<V0<V_{DD}
Pin Type XO: Crystal Output						
V_{OH}	Output High Voltage	V_{DD} –1		V_{DD}	V	I_{OH}=1.0 mA
V_{OL}	Output Low Voltage	0		1	V	I_{OI}=–1.0 mA
Pin Type AI: Analog Input						
V_{DC}	Input Bias Offset	V_{REF} –15	V_{REF}	V_{REF} +15	mV	
I_L	Input Current	–100	–	100	µA	
C_{IN}	Input Capacitance	–	10	–	pF	
R_{IN}	Input Resistance	–	20	–	Kohm	
Pin Type AO: Analog Output						

Table 6. TDC Pin Characteristics (Continued)

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_O	Analog Output Voltage	V_{REF} – 1.163	V_{REF}	V_{REF} +1.163	mV	
V_{OFF}	Output DC Offset	V_{REF} –40	V_{REF}	V_{REF} +40	mV	
R_O	Output Resistance	–	0.8	–	Ohm	
C_O	Output Capacitance	–	10	–	pF	
Z_I	Load Impedance	400	600	Infinite	Ohm	
Pin Type PWR: Power and Ground						
V_{DD}	Digital Supply Voltage	4.75	5	5.25	V	Voltage
GND	Digital Ground	–	–	0	–	
AV_{DD}	Analog Supply Voltage	V_{DD}	V_{DD}	V_{DD}	V	
AGND	Analog Ground	GND	GND	GND	V	
I_{DD1}	Digital Supply Current	–	45	90	mA	Operating
I_{ADD1}	Analog Supply Current	–	5	10	mA	Operating
I_{DD2}	Digital Supply Current	–	20	100	µA	Sleep Mode
I_{ADD2}	Analog Supply Current	–	5	25	µA	Sleep Mode

AC Characteristics

Timing Diagrams

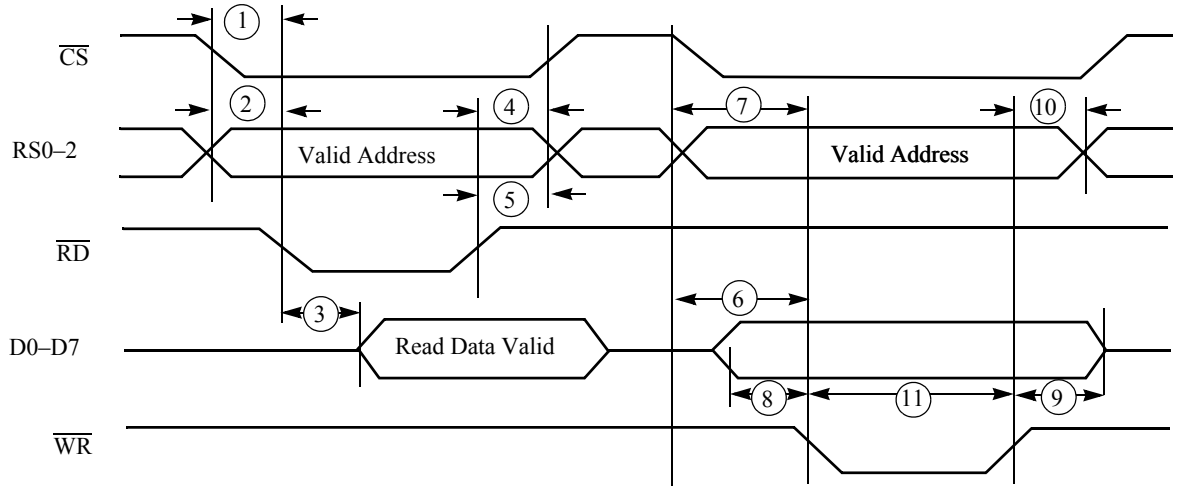


Figure 5. Microprocessor Interface Read/Write Diagram

Table 7. Microprocessor Interface Timing

Description	Parameter	Min	Typ	Max	Units
Read Timing					
HA0–2 and $\overline{HCS}$ to $\overline{HRD}$ Setup Time	1	0	–	–	ns
HA0–2 to $\overline{HRD}$ Setup Time	2	0	–	–	ns
$\overline{HRD}$ to Data Access Time	3	—	25	85	ns
$\overline{HRD}$ Data Hold	4	0	10	–	ns
HA0–2 and $\overline{HCS}$ Hold From $\overline{HRD}$	5	0	–	–	ns
Write Timing					
HA0–2 and $\overline{HCS}$ to $\overline{HWR}$ Setup Time	6	70	–	–	ns
$\overline{HCS}$ to $\overline{HWR}$ Setup Time	7	70	–	–	ns
Data to $\overline{HWR}$ Setup Time	8	0	–	–	ns
$\overline{HWR}$ Data Hold	9	10	–	–	ns
HA0–2 and $\overline{HCS}$ Hold from $\overline{HWR}$	10	10	–	–	ns

Table 7. Microprocessor Interface Timing (Continued)

Description	Parameter	Min	Typ	Max	Units
$\overline{\text{HWR}}$ Pulse Width	11	25	–	–	ns
Reset Timing					
Reset Pulse Width		1.0	–	–	µs
Reset Rise Time			–	100	ns

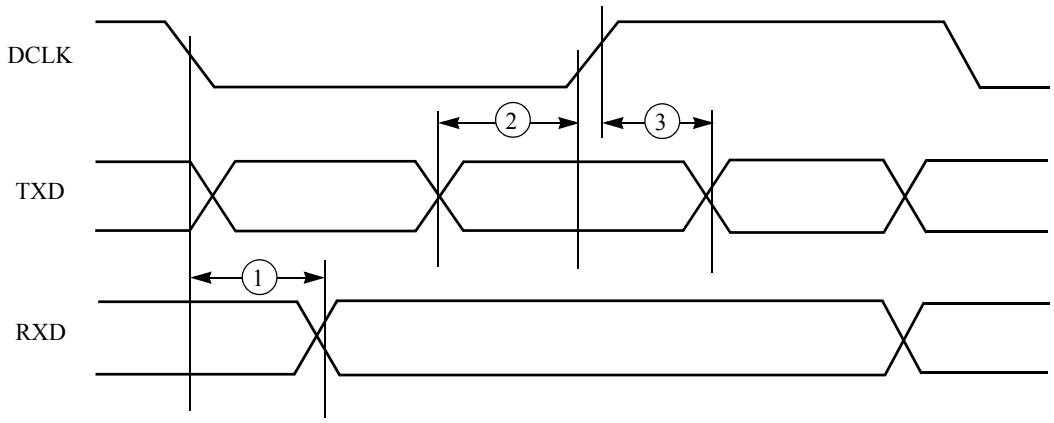


Figure 6. Serial Port Timing Diagram

Table 8. Serial Interface Timing

Description	Parameter	Min	Typ	Max	Units
RXD Data Valid Delay Time	1	–	12	–	ns
TXD Data Setup Time	2	100	–	–	ns
TXD Data Hold Time	3	100	–	–	ns

Timing Diagrams

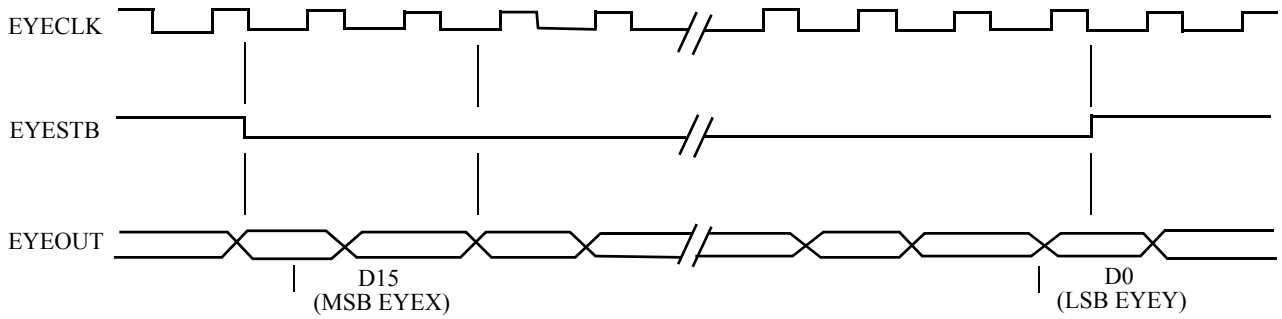


Figure 7. Eye Pattern Port Timing Diagram

Table 9. Analog Characteristics Table

Description	Parameter	Min	Typ	Max	Units
Input impedance of transformer interface	1	400	1200	–	Ohm
3 dB point of interface	2	21	26.5	32.5	kHz
External integration capacitance Type NPO (COG)	3	73	82	90	pF

Analog Inputs: Type AI

Table 10. Analog Inputs, Type AI

AC Characteristics	Sym	Min	Typ	Max	Units
Input Impedance (DC to V_{REF})	Z_{IN}	15K	25K	–	Ω
Power Supply Rejection	P_{SRRi}	40	–	–	dB
Input Current	I_i	–80	–	80	µA
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNi}	–	–	–72	dBm
Signal to Distortion	S_{TDi}	30	–	–	dB

The characteristics below are provided for information only. They are not tested

except in the functional test vectors.

Characteristics	Sym	Min	Typ	Max	Units
Input Capacitance	C_{IN}	–	10	–	pF
Input Bias	V_{DCOFF}	–	+2.5	–	V
Analog Input Voltage (Peak Differential), (23)	V_{PKI}	–2.362	–	+2.362	V
Analog Input Voltage (Per RXI+. RXI- Pin)	V_{PKIP}	–1.181	–	+1.181	V

Analog Outputs: Type A0

Table 11. Analog Inputs Type A0

AC Characteristics	Sym	Min	Typ	Max	Units
Power Supply Rejection	P_{SRRO}	40	–	–	dB
Signal to Distortion	S_{TD0}	35	–	–	dB
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNO}	–	–	–72	dBm
Out of Band Noise	N_{qo}				dBm
4–8 kHz	–	–	–20		dBm
8–12 kHz	–	–	–40		dBm
12 kHz and Above in 4 kHz Bandwidths	–	–	–55		dBm

Characteristics	Sym	Min	Typ	Max	Units
Output Impedance	Zout	–	0.80	–	Ω
Output Capacitance	Cout	–	10	–	pF
Analog Output Voltage (peak differential), (24)	Vpko	–2.375	–	+2.375	V
Load Impedance (25)	ZI	400	600	–	–

Hardware Interface Signals

The Z02201 interface consists of the Synchronous Serial Interface Port, 8-bit Host Microprocessor Interface, Eye Pattern Interface, Voice Band AFE, System Signals, and Overhead Signals. The Z02201 functional interconnect diagram is indicated in Figure 8. Any signal that is active Low is represented by a line over the signal name.

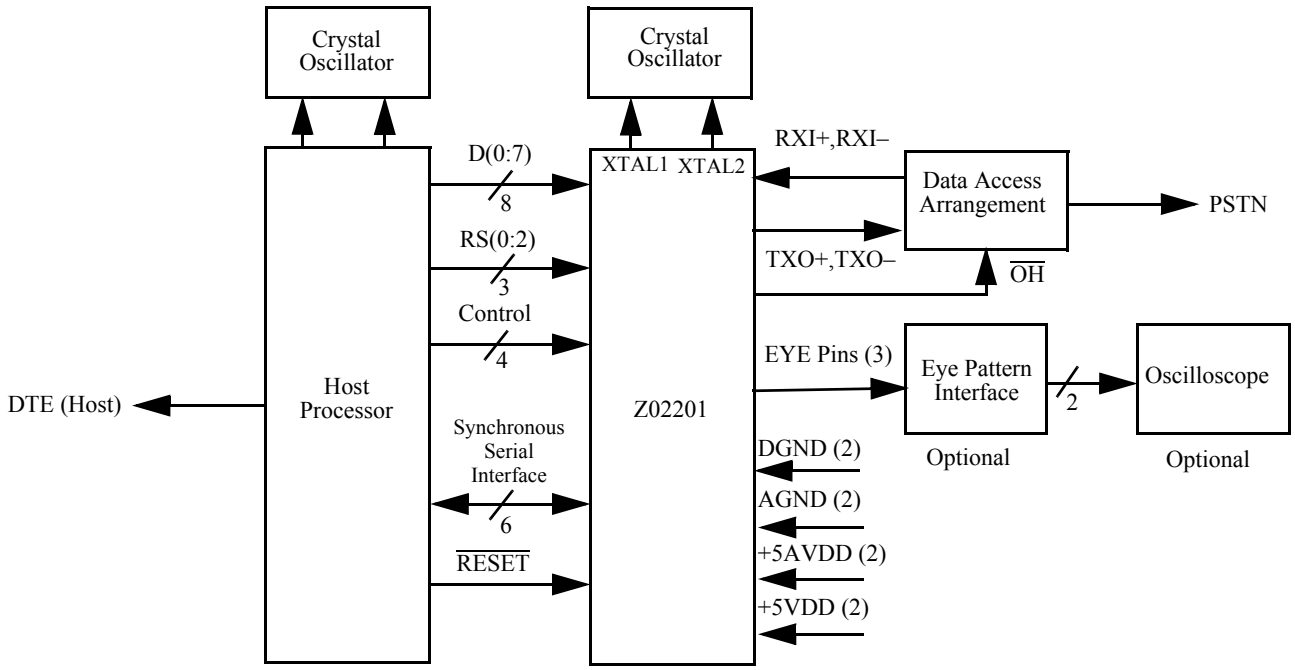


Figure 8. Modem Functional Interconnect Diagram

Synchronous Serial Interface Port

The Synchronous Serial Interface Port provides no parallel-to-serial/serial-to-parallel conversion hardware. The synchronous serial interface port consists of six signal pins as shown in Table 12.

Table 12. Synchronous Serial Interface Port

Pin	Signal Name
TxD	Transmit Data
RxD	Receive Data
RTS	Request To Send
RLSD	Receive Line Signal Detect
TCLK	Transmit Data Clock
RCLK	Receive Data Clock

Host Port Interface

The host parallel port interface consists of 15 signal pins: 8-bit bidirectional data bus pins (HD7–HD0), 3-bit Address bus (HA2–HA0), four control lines, which include the HoST READ ($\overline{\text{HRD}}$), HOST WRITE ($\overline{\text{HWR}}$), HOST CHIP SELECt ($\overline{\text{HCS}}$), and HOST INTERRUPT REQUEST ($\overline{\text{HIRQ}}$). Multiple interrupt sources are provided in the Z02201, each of which can be masked under host control.

The host parallel interface allows the host to access the data pump RAM address and data bits, transmit and receive data, control the RAM and status bits, and read data pump status bits. The host can access eye pattern functions, transmit and receive tones, and access adaptive equalizer coefficients in modem-type applications.

The host parallel interface is compatible with standard 8-bit microprocessors, which include the Z8 and Z80 bus.

Eye Pattern Interface

The eye pattern interface consists of three pins: EYE PATTERN DATA (EYEOUT), EYE PATTERN CLOCK (EYECLK), and EYE PATTERN STROBE (EYESTB). Sixteen bits of data are serially transmitted via EYEOUT, under control of EYESTB and EYE-CLK. The first byte is the X-coordinate and the second byte is Y-coordinate of the sample. The least significant bit is presented first for both the X and Y coordi-nates. A schematic of an eye pattern circuit is found in Figure 16 at the end of this specification.

The EYE PATTERN DATA, EYEOUT, outputs a serial bit stream containing data for display of the eye pattern on an oscilloscope after D/A conversion. 8 bits of the X-axis data and 8 bits of the Y-axis are output as a single 16-bit data stream with the

X-axis data first. EYEOUT is synchronous with the rising edge of EYECLK. EYEOUT is valid only while the EYESTB is Low. Data is shifted out MSB first.

Data on eyeout is shifted out on each rising edge of the 1.536MHz EYECLK. EYEOUT data is valid on the following edge of the EYE PATTERN CLOCK, EYECLK.

The EYEOUT data is valid when the EYE PATTERN STROBE, EYESTB, is Low. EYESTB changes state on the rising edge of EYECLK.

Technical Specifications

Configurations and Data Rates

Table 13 provides the selectable options, supported data rate, baud rate, and the modulation method.

Tone Generation and Tone Detection

The Z02201 provides comprehensive and flexible tone generation and detection, including all tones required to establish a circuit connection and to setup and control a communication session. The tone generation furnishes the DTMF tones for PSTN auto dialing, and the supervisory tones for call establishment. The tone detection provides support for call-progress monitoring. The detector can also be user-programmed to recognize up to 16 tones.

Data Encoding

The data encoding for the Z02201 meets both ITU–T recommendations and Bell standards.

Table 13. Selectable Configurations

Configuration[1]	Modulation[2]	Carrier Freq.	Data Rate (bps)	Symbol Rate (baud)	Bits Per Symbol	Constellation Points
V.22 bis 2400	QAM	1200/2400	2400	600	4	16
V.22 bis 1200	DPSK	1200/2400	1200	600	2	4
V.22 1200	DPSK	1200/2400	1200	600	2	4
V.23 1200/75	FSK	1700/420	1200/75	1200/75	1	—

Notes:
1. Configuration is selected through the RAM location Config.
2. QAM=Quadrature Amplitude Modulation FSK=Frequency Shift Keying, DPSK=Dual Phase Shift Keying

Table 13. Selectable Configurations (Continued)

V.21	FSK	1080/1750	300	300	1	—
Bell 212A	DPSK	1200/2400	1200	600	2	4
Bell 103	FSK	1170/2125	300	300	1	—

Notes:
1. Configuration is selected through the RAM location Config.
2. QAM=Quadrature Amplitude Modulation FSK=Frequency Shift Keying, DPSK=Dual Phase Shift Keying

Transmitted Data Spectrum

The transmitted data spectrum, with compromise equalization disabled, is shaped in the baseband by the finite impulse response (FIR) filter. Table 14 reflects the spectrum characteristics.

Table 14. Spectral Shaping

Mode	Carrier Freq	Spectral Power Shaping Function
V.22	1200	sqrt 75% Raised Cosine at 600 baud
V.22bis	2400	sqrt 75% Raised Cosine at 600 baud

Note: The carrier and the spectral shaping are selected automatically according to the configuration.

Transmit Levels

The transmit output level of the Z02201 is programmable in 1 dBm decrements from –6 dBm to –43 dBm. With a default value of –10 dBm, the Z02201 is measured differentially across pins TX0+ and TX0– with a sinusoidal waveform.

Note: To avoid saturation, the Tx level should be set to –6 dBm or lower by the host. If a higher transmit level is required, additional op amps may be added during operation.

Receiver Levels

The timing recovery circuit can track a ±0.01% (100 ppm) frequency error in the associated transmit timing source with less than 1.0 dB degradation in performance.

Clamping

Received Data (RXD) is clamped to a constant mark whenever $\overline{\text{RLSD}}$ is OFF.

Carrier Recovery

The recovery circuit can track a ±7 Hz frequency offset in the receiver carrier with less than 1.0 dB degradation in performance.

Software Interface

Note: This section refers to the **Version 0x48** of the datapump firmware. For various versions of the datapump and the differences in firmware refer to the addendum of the product specification.

The host microprocessor communicates with the Z02201 via the parallel microprocessor bus interface. Access is provided to a set of seven 8-bit Interface Registers, and through these registers, to Z02201 RAM memory locations. This interface allows the host to request modem status information and receive data, control the configuration, and load data for transmit. Table 15 is the Parallel Interface Register map.

Table 15. Parallel Interface Register Map

Function	Register Number	RS2–0 b2b1b0	MSB Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0	Access Method
RAM Access Low	0	000	RAMDL								R/W
RAM Access High	1	001	RAMDH								R/W
RAM Access Address	2	010	RAMAL								W
Parallel Data	3	011	DATAP								R/W
RAM Control & Status	4	100	TXIE	RXIE	RAMIE	TPDM	RTSP	RAMRW	RAMRQ	RAMAH	R/W
Modem Status	5	101	TXI	RXI	RAMI	DPBUSY	Reserved	RTRND	CDET	RES	R
HDLC	7	111	0	0	0	0	0	TEND	RXERR	EOF	R/W

Microprocessor Interface Register and Bit Definitions:

Reg0, Reg1 RAMDL, RAMDH—DATA PUMP RAM DATA REGISTERS—In this case, RAMDL is the least significant byte, and RAMDH is the most significant byte. After a data pump RAM read operation has completed, these registers contain the requested data. When a data pump RAM write operation is started, these registers contain the data written to data pump RAM.

Reg2 RAMAL—DATA PUMP RAM DATA ADDRESS—When a data pump RAM read or write operation is started, this byte contains the lower 8 bits of the RAM address. Register 4 (RAMAH) is the high bit of the RAM address.

Reg3 DATAP—DATA PUMP PARALLEL DATA—This register contains data transferred to or from the remote modem during the parallel modem (see register Register 4, bit 4). At any reset, when Config register bits 0–6 (MODE) is 0 (STANDBY), the data pump places its firmware version number in register DATAP.

Bit	7	6	5	4	3	2	1	0
	TXIE	RXIE	RAMIE	TPDM	RTSP	RAMRW	RAMRQ	RAMAH

Table 16. REG4: RAM Control Register

SYMBOL	POSITION	NAME AND DESCRIPTION
RAMAH	REG 4, bit 0	RAM Address High Bit. The most significant bit of the data pump RAM address. This bit is set to 1 when accessing a data pump RAM address that is greater than 255, or set to 0 for any value below 255.
RAMRQ	REG 4, bit 1	Data Pump RAM Access Request Bit. Set this bit to 1 to request a read or write of the data pump RAM. The data pump sets this bit to 0 when the request has been fulfilled.
RAMRW	REG 4, bit 2	Data Pump RAM Read/Write Bit. Set this bit to 0 to request a read of the data pump RAM or a 1 to request a write of data pump RAM.
RTSP	REG 4, bit 3	Register Request to Send Bit. A logical OR operation is executed using the value of the hardware RTS signal received by the data pump on the RTS pin. The host sets RTS or RTSP to 1 to inform the data pump the host is transmitting data. To control the data pump using the RTS signal, set RTSP to 0. To control the data pump using RTSP, hold RTS High.
TPDM	REG 4, bit 4	Select Parallel Data Mode. Setting this bit selects the parallel data mode. Resetting it selects the serial data mode.

Note: All the bits in this register (REG 4) default to logic 0 at power-up or after reset sequences are completed.

Table 16. REG4: RAM Control Register (Continued)

SYMBOL	POSITION	NAME AND DESCRIPTION
RAMIE	REG 4, bit 5	RAM Interrupt Enable Bit. Setting this bit allows the data pump to interrupt the host when a RAM read/write request has been completed.
RXIE	REG 4, bit 6	Receive Data Interrupt Enable Bit, Parallel Data Mode Only. This bit, when set, causes the data pump to generate an interrupt whenever the RXI bit is set.
TXIE	REG 4, bit 7	Transmit Data Interrupt Enable Bit, Parallel Data Mode Only. This bit, when set, causes the data pump to generate an interrupt whenever the TXI bit is set.
Note: All the bits in this register (REG 4) default to logic 0 at power-up or after reset sequences are completed.		

Bit	7	6	5	4	3	2	1	0
	TXI	RXI	RAMI	DPBUSY	Reserved	RTRND	CDET	RES

Table 17. REG5: Data Pump Status Register

SYMBOL	POSITION	NAME AND DESCRIPTION
RES	REG 5, bit 0	Data Pump in RESET Mode. This bit is set whenever the data pump is in RESET mode because of a hardware reset or power-on. The data pump sets RES to 0 when it completes the reset cycle.
CDET	REG 5, bit 1	Carrier Detect. The data pump sets CDET to 1 when it enters any data mode and is ready to transmit data. The data pump sets CDET to 0 during retrains (see Reg5, bit 2, RTRND), and when no signal is detected from the remote modem. See locations RLSDOnThresh and RLSDOffThresh for more information. CDET is inverted and reflected on the data pump's RLSD pin. If CDET is 1, RLSD is Low (asserted). At any reset, or when the host sets Config register, bits 0–6 (MODE) to 0 (STANDBY), the data pump sets CDET to 0.
RTRND	REG 5, bit 2	Retrain Detect, 2400 bps (V.22bis data mode only). The Retrain sequence is detected when this bit is set. The data pump has detected a retrain request sequence from the remote modem.
Reserved	REG 5, bit 3	Reserved bit location.
DPBUSY	REG 5, bit 4	Data Pump Busy. This bit is set whenever the data pump starts transmitting data and RTSP is 1. When the link is to be terminated, setting RTSP to 0 causes this bit to be reset after the data pump has finished transmitting the most recent data in its internal buffers. When this bit has been reset, it is safe to set Config. register, bits 0–6 (MODE) to standby mode (0) and hang up the telephone, terminating the connection. This bit also indicates when digits are being dialed during timed dialing operation. At any reset, or when the host sets Config register, bits 0–6 (MODE) to 0 (STANDBY) the data pump sets DPBUSY to 0. This bit is not valid during HDLC operation.
RAMI	REG 5, bit 5	Data Pump RAM Interrupt Status. This bit is set when the data pump has processed a RAM read/write request.
RXI	REG 5, bit 6	Receive Interrupt Status. This bit is set when the data pump is in parallel data transfer mode (TPDM is 1) and the data pump has written a new octet to the DATAP register. A read from the DATAP register clears this bit.
TXI	REG 5, bit 7	Transmit Interrupt Status. This bit is set when the data pump is in parallel data transfer mode (TPDM is 1) and the data pump has read the DATAP register. A write to the DATAP register clears this bit.

Note: The RXI bit is set to 1 after the reset sequences. All other bits in this register (Reg. 5) default to 0 at power up or after reset sequences are completed.

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	TEND	RXERR	EOF

Table 18. REG7: HDLC Register

SYMBOL	POSITION	NAME AND DESCRIPTION
EOF	REG 7, bit 0	Receive End of Frame. The data pump sets EOF to 1 when an HDLC frame has been completely received (that is, when frame data has been received and a closing HDLC flag or HDLC Abort condition is received). If the frame was correctly received, the data pump also sets Reg5, bit 1 (RXERROR) to 0, Reg5, bit 6 (RXI) to 1, and DATAP to 7EH. See Reg7, bit 1 (RXERROR) for a description of CRC errors and HDLC Aborts. EOF reflects whether the current register DATAP value indicates the end of receipt of an HDLC frame. When the first data byte of the next HDLC frame is received, or if an HDLC ABORT condition is received when no HDLC frame data was received, the data pump sets EOF to 0. This condition may occur only 8 bit times after the data pump sets EOF to 1.
RXERR	REG 7, bit 1	Receive Error. If an HDLC frame contains a CRC error, or an HDLC Abort condition is received, the data pump sets RXERROR to 1, Reg5, bit 6 (RXI) to 1, and DATAP to the value of 7EH or FFH. If the frame had a CRC error, DATAP has the value of 7EH. If an HDLC Abort condition was received, DATAP is FFH. RXERROR reflects whether the current register DATAP contains an error. When the first data byte of the next HDLC frame is received, the data pump sets RXERROR to 0. This condition may occur only 8 bit times after the data pump set RXERROR to 1.
TEND	REG 7, bit 2	Transmit End of Frame. The data pump sets TEND to 1 when it closes an HDLC frame that is transmitted. The data pump sets TEND to 0 after transmitting the CRC bytes, when it starts transmitting the closing flag of the HDLC frame. The data pump closes an HDLC frame when the host does not provide data to transmit (see DATAP) in time to be included in the HDLC frame.
0	REG 7, bits 3–7	Unused. Set these bits to 0.

Notes:
1. All the bits in this register (REG 7) default to 0 at power up or after reset.
2. All undefined bits of this register are reserved. The host writes a 0 to all reserved bit positions when writing this register. The host ignores the reserved bits when reading this register.

Reg7 Data Pump Register 7—These bits represent the state of HDLC frames when the data pump is in the HDLC FRAMING mode. These bits are valid only if BUFCTRL. bit 7 (HDLC) is 1. The host should refrain from writing Reg7 to avoid changing

the values of bit fields set by the data pump. Bits not defined above are reserved or not available for use.

The host reads register Reg7 immediately before DATAP. The two CRC checksum bytes in received HDLC frames are provided to the host.

At any reset, or when the host sets Config register, bits 0–6 (MODE) to 0 (STANDBY) the data pump sets TEND to 0, RXERROR to 0, and EOF to 0.

RAMI, RXI, and TXI Interrupts

The three most significant bits in the RAM Control and data pump status registers define the interrupt masks for RAMI, RXI, and TXI. A logical AND operation is performed with the RAMIE, RXIE, and TXIE enable bits of the RAM Control register and the corresponding interrupt bits in the DATA PUMP STATUS register. A logical OR operation is performed on the outputs driving the $\overline{\text{HIRQ}}$ pin, providing an interrupt to the host interrupt (See Figure 9).

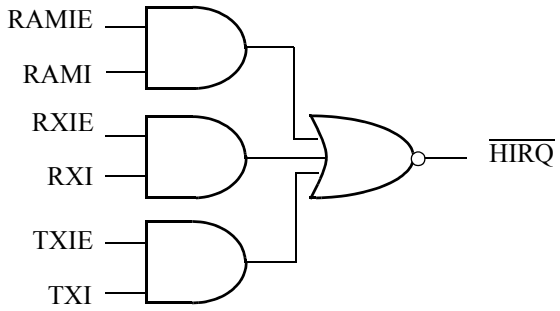


Figure 9. Host Interrupt Circuit Diagram

Interface RAM

The interface RAM is used by the data pump for normal operations. All writes to the interface RAM should be Read-Modify-Write, where only the bits that must be changed are affected. All undocumented bits are reserved and must be left intact.

Notes: 1. Data pump RAM reads or writes requires approximately 0.1 msec to complete.

2. Data pump RAM writes take effect at different times, depending upon the location being written to. During data modes, writes typically take effect at the end of the next baud period. During other modes of operation, writes take effect in 0.1 msec.
3. Writing Reg4, for example, to set Reg4, bit 7 (TXIE) to 0 in an interrupt handler while waiting for the data pump to set Reg4, bit 1 (RAMRQ) to 0 in the background, may cause unwanted side effects. Setting Reg4, bit 1 (RAMRQ) to 1 may cause the data pump to repeat the read/write request if the data pump had just set Reg4, bit 1 (RAMRQ) to 0; however, setting Reg4, bit 1 (RAMRQ) to 0 may abort the RAM read/write request.

Data Pump Interface RAM Access Method

To write to the data pump RAM:

1. Write data to RAMDL & RAMDH.

2. Write the lower 8 bits of the address of the data pump RAM location to register RAMAL.
3. With one write operation to register R4, set the high bit of the data pump RAM address in R4, RAMAH, set R4, bit 2 (RAMRW) to 1, and set R4, bit 1 (RAMRQ) to 1.
4. Wait until the data pump sets R4, bit 1 (RAMRQ) to 0.

To read from data pump RAM:

1. Write the lower 8 bits of the address of the data pump RAM location to register RAMAL.
2. With one write operation to register R4, set the high bit of the data pump RAM address in R4, RAMAH, set R4, bit 2 (RAMRW) to 0, and set R4, bit 1 (RAMRQ) to 1.
3. Wait until RAMRQ is reset to 0 by the data pump or until RAMIE is set to 1.
4. Read data from RAMDL and RAMDH.

Reads and writes to the data pump RAM may require 105 µs to complete.

Modem Data Pump RAM Map

Table 19. Modem Data Pump RAM Map

Mnemonic	Address (Hex)	Access Mode	Description
Config	01FF	R/W	Data Pump Configuration
Trnctrl	01FE	R/W	Training Control
Bufctrl	01FD	R/W	Buffer Control
ToneStatus	01FC	R/W	DTMF and Tone Control Status
Dpctrl	01FA	R/W	Data Pump Miscellaneous Controls
MStatus	01F7	R/W	Modem Control and Status
EQMMaxThresh	01F6	R/W	MSE Maximum Threshold
RLSDOffThresh	01F5	R/W	RLSD Off Threshold
RLSDOnThresh	01F4	R/W	RLSD On Threshold
CONN_Mode	01F0	R/W	Connection Speed After Handshake is Complete
Notch	01A2–01A6	R/W	Notch Filter Coefficients
DTMFh_lev	01A1	R/W	DTMF High Band Transmit Level
DTMFl_lev	01A0	R/W	DTMF Low Band Transmit Level
ToneGenA	0191	R/W	Tone Generator A
ToneGenB	0196	R/W	Tone Generator B
TxLevel	0185	R/W	Modem Transmit Level
Seq3Count	18E	R/W	Dial Timer Inter-Pulse Count
Seq2Count	18D	R/W	Dial Timer Off Count
Seq1Count	18C	R/W	Dial Timer On Count
BiquadA	0155–015E	R/W	Biquad A Coefficient
BiquadB	015F–0168	R/W	Biquad B Coefficient
DTD0–DTD15	0145–0154	R/W	Tone Detector Coefficients
EQMlev	092	R/W	Eye Quality Monitor Level
BiQuadOffThresh	052	R/W	Biquad Detectors Off Point
BiQuadOnThresh	051	R/W	Biquad Detectors On Point

Table 19. Modem Data Pump RAM Map (Continued)

Mnemonic	Address (Hex)	Access Mode	Description
DTD0Lev–DTD15Lev	026–035	R/W	Tone Detector Levels
DTDThresh	03	R/W	Tone Detector Threshold
DTDStatus	00	R/W	Discrete Tone Detector Status

Interface RAM Definitions

Table 20. Modem Data Pump Word Definitions

Register & Address (hex)		Default Value	Function and Explanation
Config	01FF	0H	Data pump Config register
		b15	Unused. Set this bit to 0.
		b14	ORG (Set Originate Mode: all modes) If ORG is 1, the modem is in Originate Mode. Otherwise, it is in answer mode. Be sure to set ORG before or at the same time as Config register, bits 0–6 (MODE), not afterwards.
		b13	ERROR (Data Pump Error: all modes) This bit is set to 1 when the data pump detects an internal error condition such as an invalid Config code. The host should reset the data pump.
		b12	RESERVED
		b11	RESERVED
		b10	MCUCTRL (Manual Handshake: V.22/V.22bis/B212A) This bit allows the host to control the handshake process in V.22bis. (See Manual Handshake Procedures on page 59 for more information).
		b9	RESERVED
		b8	SRESET (Soft Reset: all modes) Set this bit to soft reset the data pump. The data pump sets SRESET to 0 when the software reset completes.
		b7	Unused. Set this bit to 0.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation	
	b0–6	MODE (Data Mode Configuration: selects a mode) Selects the data pump operation mode. All modes unlisted below should be considered Reserved. The host should read MODE, one time after writing it, to allow the data pump enough time to begin operation in the new mode. Setting MODE to 0 (STANDBY) starts the IDLE mode of operation, not the power-saving SLEEP mode.	
			Data Mode Specified
		0	Standby
		1	Transmit tones using both generators simultaneously
		2	Detect tones/BiQuads using all discrete tone detectors and biquad tone detectors simultaneously
		3	Dial
		4	Simultaneous transmission of tones (mode 0X01) and detection of tones (mode 0x02)
		8	V.22bis 2400 bps/1200 bps mode
		9	V.22 1200 bps mode
		B	Bell 212A 1200 bps mode
		10	V.21 300 bps mode
		11	Bell 103 300 bps mode
		13	V.23 1200 bps Tx/75 bps Rx mode
		14	V.23 75 bps Tx/1200 bps Rx mode

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
Trnctrl	01FE	0H	Training Control Register The data pump sets this location to its default value at any reset and when the host sets Config register, bits 0–6 (MODE) to 0 or to any data mode. This RAM location controls the handshake process during a manual training process (see Manual Handshake Procedures on page 59 for an example on the use of this interface). This RAM location has no effect when data mode is entered (Trnctrl is set to 5 or 6).

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation	
		b7	SB1DET–Scrambled Binary 1 Detected (1200 bps or 2400 bps). Debounced through 30 ms.
		b6	S1DET–S1 Detected. Debounced through 27 ms
		b5	USB1DET–Unscrambled Marks Detected (1200 bps)
		b4	SB0DET–Scrambled Binary 0 Detected (1200 bps or 2400 bps)
		b3	V22bis Force 16 Way Decisions.
		b0–2	TXCTRL Transmitter Control. Set TXCTRL to control the output of the data pump, using the table below as a guide. The default frequency for the transmitted tone (TXCTRL is 7) is 2225 Hz, and may be changed after setting TXCTRL by changing ToneGenA appropriately. The tone level is controlled by TxLevel.
			Value: V.22/Bell 212A/V.22bis Sequence Transmitted
			0: Silence: squelch transmitter
			1: Transmit unscrambled binary 1 at 1200 bps
			2: Transmit S1 signal
			3: Transmit scrambled binary 1 at 1200 bps
			4: Transmit scrambled binary 1 at 2400 bps
			5: Begin V.22, or Bell212A, 1200 bps data mode
			6: Begin V.22bis 2400 bps data mode
			7: Transmit tone. The default frequency for the transmitted tone is 2225 Hz, and may be changed after setting TXCTRL to 7 by changing ToneGenA approximately. The tone level is controlled by TxLevel.
			Value: FSK (V.21/ Bell 103/ V.23) Sequence Transmitted
			0: Silence: squelch transmitter
			1: Transmit marks (binary 1)
			2: Transmit spaces (binary 0)
			5: Begin FSK Data Mode
			7: Transmit tone. Set the frequency to be transmitted by changing ToneGenA after setting TXCTRL is 7. The tone level is controlled by TxLevel.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
Bufctrl	01FD	0h	Buffer Control Register

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation	
		b15.. b8	Set these bits to 0 when setting Bufctrl.HDLC to 1.
		b7	HDLC (Set HDLC Mode: all data modes) Set HDLC mode. When parallel data transfer mode is selected (TPDM is 1) and HDLC is set, the data pump transfers data using the synchronous HDLC mode. In serial mode (TPDM is 0), this bit has no effect. The host should set bits 8–15 to 0 when it sets this bit to 1.
		b3	SCRDIS (Scrambler Disable: V.22, V.22bis, Bell 212A) Set this bit to disable the transmitter scrambler. This action takes precedence over TRNCTRL/TXCTRL.
		b2	TXMHLD (Hold Tx Output to Marks: all modes) Set this bit to force the data pump to transmit only marks to the remote modem, disregarding data received from the host.
		b1	DSCRDIS (Descrambler Disable: V.22, V.22bis, Bell 212A). Set this bit to disable the receiver descrambler.
		b0	RXMHLD (Hold Rx Output to Marks: all modes) Set RXMHLD to 1 to cause the data pump to transmit only marks to the host, disregarding data received from the remote modem.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
ToneStatus	01FC	080h	**Biquad Tone Detector Control and Status, Dial Control** The data pump sets this location to its default value at any reset.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation
		b15 TONEA (Tone A Detected) The tone frequency programmed in biquad detector A is detected if this bit is set.
		b14 TONEB (Tone B Detected) The tone frequency programmed in biquad detector B is detected if this bit is set.
		b13 Cascade Biquad Tone Detectors A & B The two 4th-order biquad tone detectors can be cascaded to form a single 8th-order biquad tone detector if this bit is set by the host. The result of the cascaded biquad tone detector is available in ToneStatus, bit 15.
		b7 TONEDIAL (Use DTMF to Dial) This bit causes the data pump to use DTMF tone dialing when in dialing mode (Config register, bits 0–6 (MODE) is 3).
		b5 SQRDIS (Squarer Disable) Set SQRDIS to 1 to cause the data pump to provide the output of biquad detector A directly to the input of biquad detector B, without first squaring it. SQRDIS is valid only when the biquad tone detectors are cascaded (see ToneStatus, bit 13).
		b4 TIMEDIAL (Timed Dialing) Set TIMEDIAL to 1 to cause the data pump to generate timed DTMF tones or pulse dialing. If TIMEDIAL to 0, continuous dialing is used.
		b0–b3 DIAL DIGIT The DTMF digit to be dialed is set here before Config is set for DTMF transmit. See the table below to determine how to set this parameter. For pulse dialing, only digits 0 through 9 are valid:

Digit	Value
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
Dpctrl	01FA	0H	Data Pump Miscellaneous Controls Do not modify this location during automatic handshake or retrain. The data pump sets this location to its default value at any reset.
			b15 TXSQLCH (Squelch Transmitter: all modes)
			b14 AGCFRZ (Freeze Autogain Control: V.22/V.22bis/Bell 212A) Set to 1 to freeze AGC adaptation.
			b13 Reserved for Internal Use Set to 0 when Dpctrl is written by the host.
			b12 Reserved for Internal Use Set to 0 when Dpctrl is written by the host.
			b10–11 LEQTYPE (Link Equalizer Type) Set LEQTYPE to 0 for a flat line equalizer, or LEQTYPE to 1 for a 3002 line equalizer.
			b9 GTEN (Guard Tone Enable: V.22/V.22bis/Bell 212A) This bit controls if a V.22/V.22bis/Bell 212A link has a guard tone or not. If ia guard tone is set, the tone is transmitted along with the carrier. This bit must not be enabled in modes other than V.22, V.22bis, and Bell 212A. This bit must be set prior to selecting the mode in the Config. register.
			b8 GTSEL (Guard Tone Select: V.22/V.22bis/Bell212A) This bit selects the guard tone frequency: 0 is 550 Hz, and 1 is 1800 Hz. This bit must be set prior to selecting the mode in the Config. register.
			b4 EQE (EQMlev > EQMMaxThresh: V.22, V.22bis, BELL 212A)—The data pump sets EQE to 1 when EQMlev exceeds the threshold set in EQMMaxThresh.
			b3 EQFRZ (Freeze Equalizer: all modes) Set to 1 to freeze adaptive equalizer (AEQ) adaptation. AEQ coefficients are lost when a mode change (in the Config. register) occurs.
			b2 TSPACE (Select T-spaced vs. T/2-spaced Equalizer) This bit, when set, selects a T-spaced AEQ. When reset, it selects a T/2 spaced AEQ. V.22/V.22bis/Bell 212A modes always use a T/2-spaced equalizer.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
MStatus	01F	0H	Modem Control and Status
			b11 RETRAIN (Force a Retrain: V.22bis) When set, this bit forces a retrain if the data pump has a V.22bis connection. The CDET (Register 5 bit 1) bit is set to 0 when the retrain begins. The CDET bit is set to 1 when the retrain is complete. The data pump sets RETRAIN to 0 when the retrain procedure begins and when the host sets Config register, bits 0–6 (MODE) to any data mode.
			b2 OFFHOOK (Enable Off-Hook Relay) The data pump sets the $\overline{OH}$ signal to the inverted value of this bit. For example, when OFFHOOK is 1, the data pump sets $\overline{OH}$ Low. When $\overline{OH}$ is Low, the off-hook relay closes for the signal from the telephone line to be presented to the data pump. The data pump sets OFFHOOK to 1 when the host sets Config register, bits 0–6 (MODE) to 3 (dial), or to any data mode. The data pump sets OFFHOOK to 0 at any reset. Modify OFFHOOK only when Config register, bits 0–6 (MODE) is set to 0 (STANDBY) to avoid interference with the data pump's use of this bit.
EQM MaxThresh	01F6	400H	EQM Maximum Threshold
			The upper acceptable limit for the Eye Quality Monitor (EQM). During V.22, V.22bis or Bell 212A data mode, the EQMlev exceeds EQMMaxThresh, and the data pump sets Dpctrl, bit 4 (EQE) to 1. The data pump sets this location to its default value at any reset. Changes in value take effect at the end of the next baud period.
RLSDOffThresh	01F5	–48 dBm	Received Line Signal Detect OFF Threshold
RLSDOnThresh	01F4	–43 dBm	Received Line Signal Detect ON Threshold

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation
		This register represents the upper and lower thresholds of the received telephone line energy. If Reg5, bit 1 (CDET) to 1, and the telephone line energy falls below RLSDOffThresh, the data pump sets Reg5, bit 1 (CDET) to 0. If Reg5, bit 1 (CDET) is 1 and the telephone line energy rises above RLSDOnThresh the data pump sets Reg5, bit 1 (CDET) to 1. These thresholds stabilize Reg5, bit 1 (CDET) by hysteresis when RLSDOffThresh is set to a lower value than RLSDOnThresh. Use the following formula when thresh is specified in dBm and is less or equal to 0: $$RLSDval = 10^{(power)/20}30(32767)$$ The data pump sets this location to its default value at any reset. Changes in value take effect after the next baud period.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
CONN_Mode	01F0	—	Connection Mode Register
			This RAM location reports the connection type and speed established after handshake is completed. The values for this location are the same as those for Config register, bits 0–6 (MODE):

Value	Data mode specified
8	V.22bis 2400 bps mode
9	V.22 1200 bps mode
B	Bell 212A 1200 bps mode
10	V.21 300 bps mode
11	Bell 103 300 bps mode
13	V.23 1200 bps Tx/75 bps Rx mode
14	V.23 75 bps Tx/1200 bps Rx mode

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
Notch	01A2-1A6	below	Notch Filter Coefficients

These RAM locations contain the notch filter coefficients. The notch filter is a biquad section (2nd-order IIR) used during simultaneous transmission and detection of tones (Config register, bits 0–6 (MODE) is 4) to remove a single transmitted tone from the received signal used by the tone detectors. See the section Simultaneous Transmission and Detection of Tones on page 56 for more information.

The default values for these locations are 0, 0, 0, 0, and 0x4000 respectively. The default values cause the notch filter to not modify the received signal used by the tone detectors. The data pump sets these locations to their default values when the host sets Config register, bits 0–6 (MODE) to 4 to begin simultaneous transmission and detection of tones.

The host must not modify these locations unless Config register, bits 0–6 (MODE) is 4.

To calculate the coefficients to remove a frequency **f** from the received signal, use these following formulae where,

r = pole radius (0£r<1), 0.9 is recommended

q = 2p**f**/9600, **f** is the frequency (Hz) to be removed, (0£**f**<4800)

a= $(1-2r\cos(q)+r^2)/(2-2\cos(q))$

Location	*0x1A2*	*0x1A3*	*0x1A4*	*0x1A5*	*0x1A6*
Name	*b2*	*b1*	*a3*	*a2*	*a1*
Formula	$-r^2$	$2r\cos(q)$	a	$-2a\cos(q)$	a

The cosine function is calculated in radians, not degrees.

Before writing the coefficients to data pump RAM, convert them to the format used by the data pump by multiplying each coefficient by 16,383, and round to the nearest 16-bit signed integer. For example, 2.0 becomes 32,766 (0x7FFE), -1.0 becomes -16,383 (0xC001), -2.0 becomes -32,766 (0x8002).

These formulae determine the coefficients of a biquad section with symmetric zeroes, a zero radius of 1.0, a pole radius of r, and pole and zero frequencies of f Hz.

See Simultaneous Transmission and Detection of Tones on page -56 for more detail and notch filter coefficients for the default frequencies detected by the discrete tone detectors.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value	Function and Explanation
DTMFh_lev	01A1	–6 dBm	DTMF Transmit Level — High Band
DTMFl_lev	01A0	–9 dBm	DTMF Transmit Level — Low Band
			These are the transmit levels for the DTMF low band (DTMFl_lev) and DTMF high band (DTMFh_lev) frequencies. The levels are set by the following formula where lev is specified in dBm and less or equal to 0: $$DTMFlev = 10^{(lev)/20} \cdot 32767$$ Change in value takes effect in 0.1 msec. The data pump sets these locations to their default values at any reset.
ToneGenA	0191	—	Tone Generator A
ToneGenB	0196	—	Tone Generator B
			The data pump has two independent tone generators, each simultaneously generating a pure tone with its own transmit level when Config register, bits 0–6 (MODE) is 1 (transmit tones). The outputs of the tone generators are mixed together. The generated frequencies are set by writing a coefficient to location ToneGenA or ToneGenB. The coefficient is defined as the following: where f is the frequency of the tone to be generated: $$coeff_x = \frac{2\pi \cdot f}{9600} \cdot 4096$$ The transmit levels for tone generators A and B are set in locations DTMFl_lev and DTMFh_lev, respectively. See “Transmitting Tones” for more information including a description of setting the tone transmission levels.
TxLevel	0185	–10 dBm	*Transmit Power Level* To sets the transmit power level, use the following formula where power is specified in dBm and less than or equal to –6: $$TxLevel = 10^{(power)/20} \cdot 2048$$ Change in value takes effect at the end of the baud period.
Seq3Count	18E	None	Dial Timer Inter-Pulse Count See Seq1Count
Seq2Count	18D	95 msec	Dial Timer Off Count See Seq1count

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation
Seq1Count 18C	95 msec	Dial Timer On Count
		Seq1Count, Seq2Count, and Seq3Count are timer counts in units of 1/9600 of a second, for DTMF and pulse dialing. For DTMF dialing, Seq1Count is the length of the digit on-time, and Seq2Count is the length of the digit off-time. For pulse dialing, Seq1Count is the length of the break period, Seq2Count is the length of the make period, and Seq3Count is the length of the pause after dialing a digit. The data pump sets these locations to their default values when the host sets Config register, bits 0–6 (MODE) to 3 (dial).
Biquad A Coefficients 0155–015E	—	Biquad A and B Coefficients
Biquad B Coefficients 015F–0168	—	
		These locations program the frequency range for the biquad tone detectors. The coefficients are in the following order: b2, b1, a3, a2, a1, B2, B1, A3, A2, A1. See the section on Call-Progress Monitoring Using Biquad Tone Detectors on page -54 for more information.
DTD0–DTD15 0145–0154	—	Tone Detector Coefficients
		These locations set the tone detector coefficients for the 16 detectors in the system. The coefficients are set by using the following formula where (2 pi x ftone/9600) is measured in radians: $$coeff_{tone} = \cos\left(\frac{2\pi \cdot f_{tone}}{9600}\right) \cdot 32767$$ See “Tone Detectors” for more information.
EQMlev 092	—	Eye Quality Monitor (EQM)
		This register provides a measure of line quality during V.22, V.22bis, or Bell 212A, while computing a running average of the mean square error (MSE) of the received point and decision point. When EQMlev exceeds EQMMaxThresh, Dpctrl.EQE is set to 1; otherwise, it is set to 0.

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation
BiQuadOffThresh 052	–42 dBm	Biquad Tone Detectors OFF Point The data pump sets this location to its default value when Config register, bits 0–6 (MODE) is set to 2 by the host.
		This location can be used to set the off point for the Biquad tone detectors. If the power level is below this value, the detector turns off the detection status bit. Use the following formula to set the threshold where the level is in dBm: $$Threshold = 10^{(level)/20} \cdot 32767$$ The data pump sets this location to its default value when the host sets Config register, bits 0–6 (MODE)=2 (detect tones).
BiQuadOnThresh 051	–35 dBm	Biquad Tone Detectors ON Point The data pump sets this location to its default value when Config register, bits 0–6 (MODE) is set to 2 by the host.
		This location can be used to set the ON point for the Biquad tone detectors. If the power level is above this value, the detector turns the detection status bit ON. Use the following formula to set the threshold where level is in dBm: $$Threshold = 10^{(level)/20} \cdot 32767$$ The data pump sets this location to its default value when the host sets Config register, bits 0–6 (MODE) is 2 (detect tones).
DTD0Lev–DTD15Lev 26–35	—	Discrete Tone Detector Levels
		These locations represent the tone detector levels when in the Tone Detect mode (Config register, bits 0–6 (MODE) has the value of 02h). These areas may be used by the host to determine which tone is dominant if multiple tones are detected. These particular locations have no default.
DTDThresh 03	–24 dBm	Discrete Tone Detector Threshold

Table 20. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value	Function and Explanation
		This location programs the threshold for all discrete tone detectors. Any signal whose signal strength is above this threshold turns on the detection bit for that tone. Any signal below this threshold turns off the detection bit for that tone. This location can be programmed using the following formula: $Threshold = 10^{(level)/20} \cdot 32767$ This location must be programmed after Config register, bits 0–6 (MODE) is set to detect tone (02h), because the data pump resets this location to its default when Config register, bits 0–6 (MODE) is set to tone detect mode. See “Tone Detectors” for more information.
DTDStatus	00 —	Discrete Tone Detector Status
		This location contains the status of the tone detectors when in tone detect mode (Config register, bits 0–6 (MODE) is 02h). Bit 0 contains the status of detector 0, bit 1 (the status of detector 1), and so on. This location is only valid when in tone detection mode. The response time of the tone detectors is dependent upon the frequency of the tone being detected and sampling rate of the data pump. When the host sets Config register, bits 0–6 (MODE) to 0 (STANDBY), or resets the data pump, the data pump writes its part number into this location.

Transmitting Tones

The data pump has two tone generators, each with their own transmit level. The outputs are mixed together. The frequency of the tones are programmed by writing coefficients to locations TONEGENA and TONEGENB. The transmit levels are programmed by writing values to locations DTMF_LEV and DTMFH_LEV. If only one tone is to be transmitted, the other tone generator’s transmit level is set to 0 to disable it.

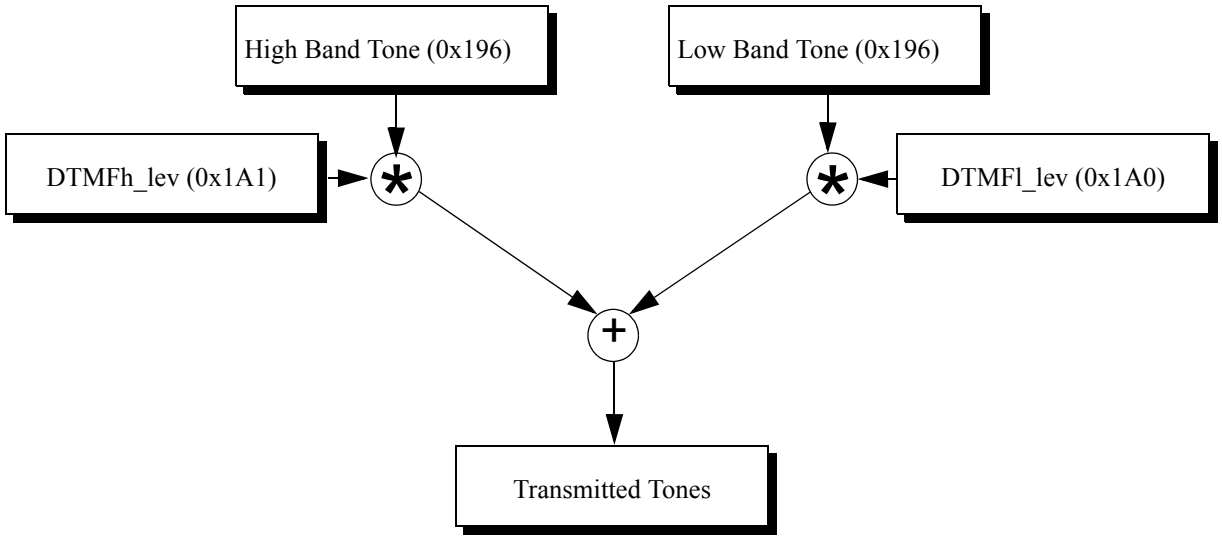


Figure 10. Transmitting Tones

For example, to generate a 2100 Hz Answer Tone for 3.3 seconds at –10dBm:

1. Set location TONEGENA to `015FEh`.
2. Set location DTMFL_LEV to `0287h`.
3. Set location DTMFH_LEV to `0`, disabling TONEGENB.
4. Set CONFIG register, bits 0–6 (MODE) to `1` (transmit tone).
5. Wait 3.3 seconds before setting CONFIG register, bits 0–6 (MODE) to `0` (STANDBY).

Tone Detectors

There are 16 tone detectors in the data pump. They are programmed by setting up one word for each tone detector. There is one global threshold setting for all 16 tone detectors. The address for the tone detectors are as follows:

- Tone Detector Coefficients—`0145–0154h` (Tone0–Tone15)
- Tone Detector Receive Levels—`026h–035h` (DTD0lev–DTD15lev)
- Tone Detector Threshold–`03h`

- Tone Detector Status–00h
- The tone coefficients are calculated as follows:

$$coeff_{tone} = \cos\left(\frac{2\pi \cdot f_{tone}}{9600}\right) \cdot 32767$$

- The default values on reset are represented in Table 21:

Table 21. Tone Detector Default Values

Tone Detector	Frequency Detected (Hz)
0	697
1	770
2	852
3	941
4	1209
5	1336
6	1477
7	1633
8	1750
9	1800
10	1650
11	2225
12	2250
13	1300
14	2100
15	600

- The threshold is calculated as follows:

$$Threshold = 10^{(level)/20} \cdot 32767$$

where level is in dBm. The default value for the threshold is –24 dBm. This value is set every time CONFIG register, bits 0–6 (MODE) is set up to detect tones. If the user wishes a different value, it should be reloaded *after* CONFIG register, bits 0–6 (MODE) is set to detect tones.

To use the tone detectors, perform the following steps:

1. Set up the tone detector coefficients (0145–0154h).
2. Set CONFIG register, bits 0–6 (MODE) to tone detect mode (02h).

Note: Tone detect mode is the same mode used for Biquad tone detectors, because both Biquad tone detectors and tone detectors run concurrently. As a result, the host is allowed to look for individual answer tones as well as call-progress tones.

3. Set up the tone detector threshold DTDTHRESH.
4. Inspect the tone detector status.
5. When the detection phase is complete, set CONFIG register, bits 0–6 (MODE) to STANDBY (00h).

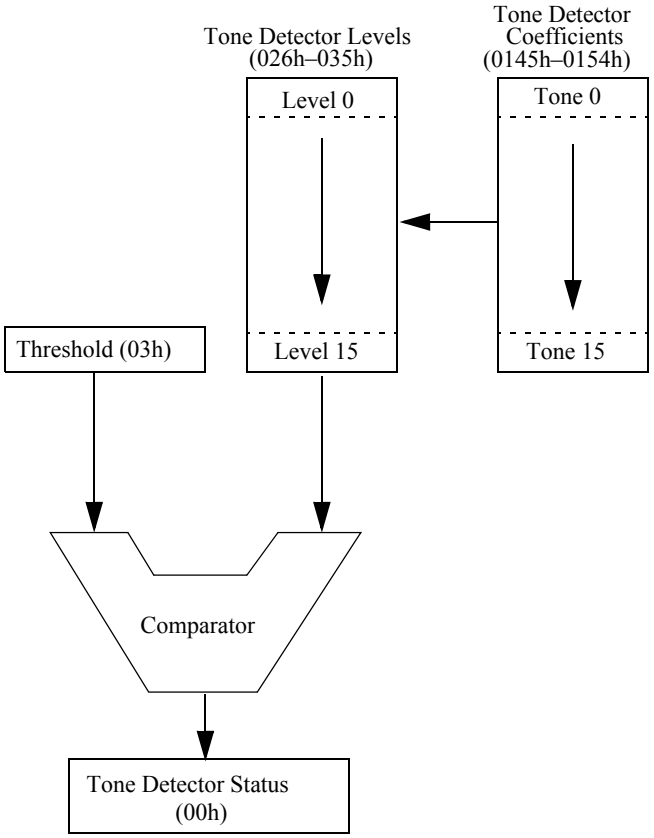


Figure 11. Tone Detectors

Call-Progress Monitoring Using Biquad Tone Detectors

The data pump contains two biquad tone detectors that are capable of detecting energy in a frequency band. These detectors are useful for call-progress monitoring, where the exact frequency of the incoming signal is not known. Each biquad tone detector is composed of two cascaded, independently programmable, biquad sections. The order of biquad coefficients in RAM is:

b2, b1, a3, a2, a1, B2, B1, A3, A2, A1

The addresses for the coefficients for the two sections start at 0155H (TONEA) and 015FH (TONEB). The sample rate is 9600 Hz.

The transfer equation for each section of the biquad tone detector is of the form:

$$H_n = \frac{2(a_1 + a_2 Z^{-1} + a_3 Z^{-2})}{(1 - 2b_1 Z^{-1} - 2b_2 Z^{-2})}$$

There are two threshold settings affecting both biquad tone detectors. The locations BIQUADOFFTHRESH and BIQUADONTHRESH define the on and off hysteresis points where level is in dBm:

1. BIQUADOFFTHRESH–052h–OFF point.
2. BIQUADONTHRESH–051h–ON point.

Use the following formula to set the thresholds:

$$Threshold = 10^{(level)/20} \cdot 32767$$

The default values are –35 dBm (BiQuadOnThresh) and –42dBm (BiQuadOffThresh).

The biquad tone detector status is contained in TONESTATUS, bit 15 (TONEA) and TONESTATUS, bit 14 (TONEB). The response time of the biquad tone detectors depends on the coefficients and the input signal frequency.

The biquad tone detectors can be cascaded to form one tone detector with 4 biquad sections (an 8th order IIR filter) by setting ToneStatus.CASCADE. In this case, TONESTATUS, bit 15 (TONEA) contains the status of the cascaded tone detector, and TONESTATUS, bit 5 (SQRDIS) controls whether the output of biquad tone detector B is squared before being input to biquad tone detector A.

The default settings for the biquad tone detector coefficients are indicated in Table 22 and Table 23, where the first row is TONEA and the second row is TONEB. The data pump sets the biquad tone detector coefficients to their default settings at any reset.

Table 22. Biquad Section 1 Coefficients (Hex)

Band (Hz)	b2	b1	a3	a2	a1
245–650	C774	7601	0716	F5FB	0716
360–440	C148	7A66	FF5C	0000	00A4

Table 23. Biquad Section 2 Coefficients (Hex)

Band (Hz)	B2	B1	A3	A2	A1
245–650	C63E	6FE1	F8EA	0000	0716
360–440	C7CD	7438	01AA	FEBC	01AA

To use the Biquad tone detectors to perform Call-Progress Monitoring, execute the following:

1. Set the coefficients. Coefficients which are changed remain valid until the next reset.
2. Set CONFIG register, bits 0–6 (MODE) to `2` (detect tones). The biquad tone detectors and the discrete tone detectors operate simultaneously to allow the host to look for call-progress tones and individual answer tones at the same time.
3. Set the BIQUADONTHRESH and BIQUADOFFTHRESH values.
4. If the two biquad tone detectors are to be cascaded, set TONESTATUS, bit `13` (CASCADE) to `1`. If required, set TONESTATUS, bit `5` (SQRDIS) to `1` to disable the squarer when the tone detectors are cascaded.
5. Inspect TONESTATUS, bit `15` (TONEA) and TONESTATUS, bit `14` (TONEB) for the detection status. If TONESTATUS, bit `13` (CASCADE) is set, only inspect TONESTATUS, bit `15` (TONEA).
6. Time the ON time and the OFF time of the tone(s) to provide the cadence, which is used to identify the type of call-progress tone detected.After call-progress monitoring is complete, set CONFIG register, bits 0–6 (MODE) to `0` (STANDBY).

Simultaneous Transmission and Detection of Tones

Setting CONFIG register, bits 0–6 (MODE) to 4 enables the simultaneous operation of all Discrete Tone Detectors, Biquad Tone Detectors, and Tone Generators. Please refer to the sections Transmitting Tones on page 50, and Tone Detectors on page 51 for descriptions of how to use each of these features by itself.

The host uses simultaneous transmission and detection of tones when it needs to detect tones while generating a single tone. An example during the call establishment phase of a special purpose modem.

To prevent a single generated tone from interfering with the tone detectors the host programs data pump RAM locations 0x1A2 through 0x1A6 with coefficients for a notch filter to remove a single tone from the received signal used by the tone detectors.

The notch filter coefficients are set to their default values when the host sets CONFIG register, bits 0–6 (MODE) to 4, so the host writes new values to these locations after setting CONFIG register, bits 0–6 (MODE) to begin simultaneous transmission and detection of tones. The default notch filter coefficient values cause the notch filter to not change the received signal used by the tone detectors.

The notch filter is a biquad section (2nd-order IIR filter). The values of the coefficients determine the frequency to be removed. Refer to the description of RAM location “Notch” for the formulae used to compute these commonly used coefficient values:

Table 24. Notch Filer Coefficients

f (Hz)	0x1A2	0x1A3	0x1A4	0x1A5	0x1A6
default	0x0	0x0	0x0	0x0	0x4000
600	0xCC2A	0x6A6D	0x3DCD	0x8DCF	0x3DCD
1300	0xCC2A	0x4BF4	0x3A89	0xB2CF	0x3A89
1650	0xCC2A	0x364D	0x3A34	0xC921	0x3A34
1750	0xCC2A	0x2F8A	0x3A24	0xD002	0x3A24
1800	0xCC2A	0x2C15	0x3A1D	0xD385	0x3A1D
2100	0xCC2A	0x1679	0x39FE	0xE95F	0x39FE
2225	0xCC2A	0x0D2A	0x39F5	0xF2C1	0x39F5
2250	0xCC2A	0x0B4A	0x39F4	0xF4A4	0x39F4

Notes: Failing to program the notch filter to the same frequency as the transmitted tone when CONFIG register, bits 0–6 (MODE) is 4 seriously reduces the accuracy and sensitivity of the data pump's tone detectors.

It is not possible to generate two tones simultaneously when CONFIG register, bits 0–6 (MODE) is 4 without seriously reducing the accuracy and sensitivity of the data pump's tone detectors, even if the notch filter is programmed to remove one of the generated tones.

The notch filter attenuates received signals at frequencies close to the notched frequency. For the commonly used coefficient values shown, signals within 100 Hz of the notch frequency are attenuated by 6 dB or more, signals 320 Hz or more from the notch frequency are attenuated by less than 1 dB.

Dialing

The data pump may be programmed to dial using either DTMF tones, or make/break pulses. By default, the data pump is configured for tone (DTMF) dialing.

Tone Dialing

Tone dialing may be either continuous or timed. Continuous dialing generates the required tone until the host specifically shuts it OFF. Timed dialing allows the host to specify the on/off timing of the digit dialed.

The following example assumes the host controls the data pump's RTS through Reg4, bit 3 (RTSP). To perform tone dialing:

1. Set Reg4, bit 3 (RTSP) to 0, TONESTATUS, bit 4 (TIMEDIAL) to 1 for timed dialing, or to 0 for continuous dialing. Set CONFIG register, bits 0–6 (MODE) to 3 (DIAL). If timed dialing is required, set the timer locations SEQ1COUNT and SEQ2COUNT to 1.
2. Control the twist by setting locations DTMFH_LEV and DTMFL_LEV to specify the transmit levels of the high tone and the low tone, respectively.

3. Set up the digit to be dialed in TONESTATUS bits 0–3 (DIGIT) according to the following table:

Table 25. Tone Dialing

Digit	Value
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
*	10
#	11
A	12
B	13
C	14
D	15

1. For continuous operation, set Reg4, bit 3 (RTSP) to 1 to start transmitting the DTMF tone, and to 0 to stop.
2. For timed operation, set Reg4, bit 3 (RTSP) to 1 to dial the digit. The data pump sets Reg5, bit 4 (DPBUSY) to 1 while it dials the digit. Set Reg4, bit 3 (RTSP) to 0 after the digit has been dialed. The data pump sets Reg5, bit 4 (DPBUSY) to 0 when the dial sequence is completed.
3. To dial additional digits, repeat the procedure starting at step 3.
4. When dialing is complete, set CONFIG register, bits 0–6 (MODE) to 0 (STANDBY).

The Z02922 data pump exhibits limited maximum output power. This feature applies not only to data mode, but also to DTMF and other tone generation. During DTMF or tone generation, if the sum of the transmit levels programmed

into DTMFh_lev and DTMFl_lev exceeds 30720 (0x7800) the data pump may not properly transmit the tones.

When transmitting DTMF with a required twist (power difference between high and low bands), use this formula to determine the maximum DTMF transmit levels where x is the DTMF low band (DTMFL_LEV) transmit level in dBm, and x+b is the DTMF high band (DTMFH_LEV) transmit level in dBm (*b* is the twist in dBm):

```
10^(x/20) + 10^((x+b)/20) <= 30720/32768
```

The values for maximum transmit levels (*DTMFl_lev + DTMFh_lev* = 30720) at common twist values are described in the following table:

Table 26. Maximum Transmit Levels

DTMFl_lev	DTMFh_lev	x	x+b	b
14,477	16,243	-7.10	-6.10	1
13,599	17,121	-7.64	-5.64	2
12,733	17,987	-8.21	-5.21	3

Pulse Dialing

Pulse dialing is very similar to timed dialing, with the exception that the *tone* generated is a cadence of pulses output on the $\overline{OH}$ pin and mirrored in RAM location MSTATUS, bit 2 (OFFHOOK). To implement pulse dialing, follow the instructions for timed tone dialing, except:

1. Select pulse instead of tone dial mode by setting location TONESTATUS, bit 7 (TONEDIAL) to 0 TONESTATUS, bit 4 (TIMEDIAL) has no effect. Pulse dialing is always timed.
2. After setting CONFIG register, bits 0–6 (MODE) to 3 (DIAL), set SEQ1COUNT, SEQ2COUNT, and SEQ3COUNT to the required make and break times, pausing after each digit is dialed. For North American applications requiring a 100 msec cadence, a 39%/61% make/break ratio, and a 0.75 second pause, set locations SEQ1COUNT to 024Ah, SEQ2COUNT to 0176h, and SEQ3COUNT to 01C20h.

Manual Handshake Procedures

The V.22bis data pump software allows the host to control every aspect of the handshake procedure. The host instructs the data pump which signal to send at which time. The data pump sets status bits when it receives signals from the remote modem.

The host begins a manual handshake by setting CONFIG register, bit 10 (MCUCTRL) to 1 to prevent the data pump from transmitting its own handshake signals.

The host monitors the receive signal status bits in location TRNCTRL and transmits its own responding signals by setting TRNCTRL, bits 0–2 (TXCTRL) transmits the following values:

Table 27. Signal Transmit Values

Trnctrl Value	Signal Transmitted
0	Silence
1	1200 bps Unscrambled Binary 1
2	S1
3	1200 bps Scrambled Binary 1
4	2400 bps Scrambled Binary 1
5	1200 bps data mode or FSK
6	2400 bps data mode
7	2225 Hz tone

In the following section, certain acronyms are used to denote the various V.22bis handshake signals. These are:

Table 28. Handshake Acronyms

Name	Meaning
USB1	Unscrambled Binary 1
SB1	Scrambled Binary 1
S1	S1 Signal

Originating Modem

1. Take the telephone line off-hook and dial.
2. Program the discrete tone detectors and the biquad tone detectors for answer tones (2100 Hz) and call-progress tones (200–600 Hz). Look for both the answer tone and call-progress tones (such as busy tones, ring back and so on).
3. Upon receiving the 2100 Hz answer tone, set CONFIG to 4409h (V.22, V.22bis originate, manual handshake).

4. Wait for TRNCTRL, bit 5 (USB1DET) to be set to 1 (USB1 DETECTED) continuously for 155 msec.
5. Wait for 456 msec.
6. Set TRNCTRL, bits 0–2 (TXCTRL) to 2 (TRANSMIT S1 SIGNAL) for 100 msec.
7. Set TRNCTRL, bits 0–2 (TXCTRL) to 3 (TRANSMIT SB1), and inspect TRNCTRL, bit 6 (S1DET) and TRNCTRL, bit 7 (SB1DET) repeatedly for either a received S1 signal or SB1. If SB1 is received for 270 msec, proceed to step 11. If S1 is received, wait for the S1 to end. Wait for an additional 450 msec.
8. Set TRNCTRL, bit 3 (V22BIS) to 1 (force a 16-way receive decision). Wait for 150 msec.
9. Set TRNCTRL, bits 0–2 (TXCTRL) to 4 (transmit SB1 at 2400 bps). Wait for 200 msec.
10. Set TRNCTRL, bits 0–2 (TXCTRL) to 6 (2400 bps DATA mode). Data is now being transmitted and received at 2400 bps.
11. In step 7, if SB1 is detected instead of the S1 signal, wait for 765 msec. Proceed to set TRNCTRL, bits 0–2 (TXCTRL) to 5 (1200 bps DATA mode). Data is now being transmitted and received at 1200 bps.

Answering Modem

1. At a ring signal or a command from the host, take the phone off-hook and transmit silence for 1.8 to 2.5 seconds.
2. If required, use the tone generators to transmit a 2100 Hz tone for 2.6 to 4 seconds. This tone is the V.25 answer tone.
3. Set CONFIG register, bits 0–6 (MODE) to 0 (STANDBY) and transmit silence for 75 msec.
4. Set CONFIG to 8 (ANSWER MODE, MANUAL HANDSHAKE). After setting Config, the host is ready to receive data from the remote modem. The data pump holds the received data to marks (that is, receives nothing) until the modem is able to receive data from the remote modem.
5. Set TRNCTRL, bits 0–2 (TXCTRL) to 1 (transmit USB1).
6. Inspect TRNCTRL, bit 6 (S1DET) and TRNCTRL, bit 7 (SB1DET) repeatedly for either a received S1 signal or SB1. If SB1 is received continuously for 270 msec, proceed to step 12. If an S1 signal is received (TRNCTRL, bit 6 (S1DET) is 1) wait for the S1 to end.
7. Set TRNCTRL, bits 0–2 (TXCTRL) to 2 (transmit S1 signal) for 100 msec.
8. Set TRNCTRL, bits 0–2 (TXCTRL) to 3 (transmit SB1) for 350 msec.

9. Set TRNCTRL, bit 3 (V22BIS) to 1 (force 16-way receive decisions). Wait for 150 msec.
10. Set TRNCTRL, bits 0–2 (TXCTRL) to 4 (transmit SB1 at 2400 bps). Wait for 200 msec.
11. Set TRNCTRL, bits 0–2 (TXCTRL) to 6 (2400 bps data mode). Data is now being transmitted and received at 2400 bps.
12. If in step 6., SB1 is received instead of an S1 signal, set TRNCTRL, bits 0–2 (TXCTRL) to 3 (Transmit SB1) for 765 msec. From that point, set TRNCTRL, bits 0–2 (TXCTRL) to 5 (1200 bps DATA mode). Data is now transmitted and received at 1200 bps.

Making a V.22bis Connection

In the following example, all timing is performed by the host.

Originating Modem

1. Take the telephone line OFF-HOOK and dial.
2. Program the discrete tone detectors and the biquad tone detectors for answer tones (2100 Hz) and call-progress tones (200–600 Hz). Look for the answer tone and call-progress tones (busy tones, ring back, etc.)
3. Upon receiving the 2100 Hz answer tone, set CONFIG to 4008h (V.22bis originate). After setting Config, the host should be prepared to receive data from the remote modem. The data pump holds the received data to marks (that is, receives nothing) until the modem is able to receive data from the remote modem.
4. When the data pump establishes a V.22bis connection, and is ready to transmit data to the remote modem, it sets Reg5, bit 1 (CDET) to 1. Data may now be transmitted or received between the modems.

Answering Modem

1. Upon a ring signal or command from the terminal, take the phone off-hook and transmit silence for 1.8–2.5 seconds.
2. If required, use the tone generators to transmit a 2100 Hz tone for 2.6–4 seconds. This tone is the V.25 answer tone.
3. Set CONFIG register, bits 0–6 (MODE) to 0 (STANDBY) and transmit silence for 75 msec.

4. Set CONFIG to 8 (V.22BIS ANSWER). After setting Config, the host should be prepared to receive data from the remote modem. The data pump holds the received data to marks (receives nothing) until the modem is able to receive data from the remote modem.
5. When the data pump establishes a V.22bis connection, and is ready to transmit data to the remote modem, it sets Reg5, bit 1 (CDET) to 1. Data may now be transmitted or received between the modems.

Notes: The data pump sets Reg5, bit 1 (CDET) to 0 during carrier dropouts, retrains, and when the remote modem hangs up the telephone line. Depending on the data mode, the host may use Reg5, bit 1 (CDET), Reg5, bit 2 (RTRND), Dpctrl.EQE, EQMlev and EQMMaxThresh to determine when the remote modem has initiated a retrain, or has hung up the telephone line.

During 2400 bps V.22bis data mode, the host may use Dpctrl.EQE and EQMMaxThresh or EQMlev, to determine when to initiate a retrain (see Table 20, Mstatus.RETRAIN) to improve the quality of the connection.

Using HDLC

The data pump includes HDLC firmware operating in all data modes. The HDLC firmware performs all the necessary operations to frame host-supplied data into HDLC format, including automatic opening and closing flag generation, zero insertion and deletion, flag and abort detection, and CRC checksum computation and checking.

HDLC Operation

During HDLC operation, the data pump frames host-supplied asynchronous data into a synchronous data stream in the transmitter, and extracts the same asynchronous data from the received synchronous data stream in the receiver. The inclusion of 16-bit cyclic redundancy check (CRC) information in the frames allows the receiving host to check whether the data has been correctly received.

HDLC data is sent in frames. A frame consists of a number of bytes, each composed of 8 data bits. A frame contains an opening flag, frame data bytes, two CRC checksum bytes, and a closing flag, respectively. Opening flags and closing flags indicate the start and the end of a frame, respectively.

A flag, byte value 07Eh, is one of two HDLC control symbols. The other is an abort, which is any sequence of consecutive binary 1s more than six bits long. If the frames do not use the bandwidth of the data mode (for example, when there is no host data to transmit), the modem fills the remaining bandwidth by sending flags between frames.

Frame data bytes for transmission are supplied by the host to the data pump's DATAP register. These bytes are modified by the data pump to ensure that no more than five consecutive binary 1 bits are sent. To accomplish this modification, the transmitting modem inserts a single 0 bit after every five consecutive binary 1 bits in the host supplied data. This zero insertion process allows the receiving modem's data pump to distinguish between frame data, flags, and aborts. The receiving modem's data pump uses a zero deletion process to remove each inserted 0 bit before returning the data to the receiving modem's host.

When a frame is to be closed, the frame's two CRC checksum bytes are sent immediately following the frame data. The CRC checksum is computed without the inserted zeroes. The frame's closing flag is transmitted following the CRC. This flag may also serve as the opening flag of the next frame, saving bandwidth.

Enabling HDLC Operation

The data pump's HDLC firmware is disabled at power-up and any reset, and can be enabled only in parallel mode (Reg4., bit 4 (TPDM) is 1). To enable HDLC, set BUFCTRL, bit 7 (HDLC) to 1, and bits 8–15 of BUFCTRL to 0 prior to beginning data mode operation. The host also reads register DATAP just before starting data mode to clear DATAP.

These examples demonstrate the use of the data pump in parallel mode to transmit and receive HDLC data frames. The examples assume that the data pump has just been put in data mode, and HDLC operation is enabled. The data to be sent or received is the sequence of N bytes (Byte1–ByteN), where Byte1 is sent (or received) first.

Transmitting

1. When Reg5, bit 7 (TXI) is 1, write Byte1 to DATAP. Repeat this step for each byte to be transmitted. If Reg4, bit 7 (TXIE) is 1, the data pump generates an interrupt when it is ready to transmit the next byte, for example, when the byte sets Reg5, bit 7 (TXI) to 1.
2. When the last byte, ByteN, has been sent, wait for the data pump to set Reg7, bit 2 (TEND) to 1. This function indicates the data pump has closed the current frame. The data pump now computes and transmits the CRC checksum and closing flag for the frame. The data pump does not set Reg7, bit 7 (TEND) to 1

until at least 8 bit times after it has set Reg4, bit 7 (TXI) to 1, indicating the data pump is ready to transmit another data byte. To transmit another frame, repeat steps 1–2.

3. When the data pump begins sending the frame's closing flag, it sets Reg7, bit 2 (TEND) to 0. Transmission of the frame is complete 8 bit times after the data pump sets Reg7, bit 7 (TEND) to 0.

Receiving

1. Prepare to receive a new frame.
2. When Reg5, bit 6 (RXI) is 1, the data pump has received a byte. First read register Reg7, followed by DATAP. Register 7 (Reg7) is read first, because the data pump may change it any time after DATAP is read. If Reg4, 6 (RXIE) is 1, the data pump generates an interrupt when it sets Reg5, bit 6 (RXI) 1.

   Act on the value of Reg7 read in step 2 as follows:

- If RXERROR is 0 and EOF is 0, the DATAP value read in step 2 is an HDLC frame byte. Repeat step 2 to receive all remaining frame bytes.
- If RXERROR is 0 and EOF is 1, an HDLC frame with a correct checksum has been received.
- If Byte1–ByteN+3 have been read, with ByteN+3 being the DATAP value just read, then the two previous bytes (ByteN+1 and ByteN+2), are the frame checksum bytes; the remaining bytes (Byte1–ByteN) are the frame data bytes.

3. Continue from step 1 to receive the next frame. If RXERROR is 1, discard any received frame bytes and continue from step 1 to receive the next frame.
4. If DATAP was 0FF, an HDLC abort sequence was received. If DATAP was 07Eh, an HDLC frame with an incorrect checksum was received.

Data Pump Firmware Version Number and Part Number

The data pump code version can be obtained any time the RAM location CONFIG register, bits 0–6 (MODE) is set to 0. The data pump writes the part number to data pump RAM location 0 and the code version number to the DATAP register. To obtain the version and part number from the data pump, the following steps must be performed:

1. Set CONFIG register, bits 0–6 (MODE) to 0 (STANDBY), then read location Config to provide the data pump enough time to begin standby operation.

2. Read the DATAP register. This register returns the code release version number (an 8 bit value, for example, 030h indicates version 30).
3. Read RAM location 0. This location returns the part number (for example, 02201h for a Z02201 part).

Sleep Mode

The data pump incorporates a low-power sleep mode. In this mode, the data pump clock is shut down, effectively stopping the part. To enter SLEEP mode, the controller can set Config to mode 7. To exit SLEEP mode, the controller can either reset the data pump (asserting the $\overline{\text{RESET}}$ signal) or write any value to the DATAP register. The host must wait at least 2 msec before accessing the data pump registers.

Typical Performance Data

The Bit Error Rate (BER) and Block Error Rate (BLER) curves in Figure 12 and Figure 13 represent typical performance over a variety of signal to noise conditions (SNR).

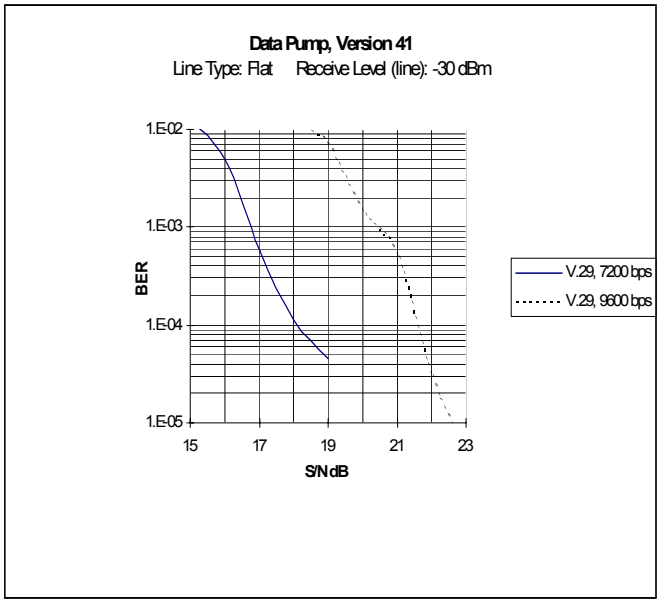


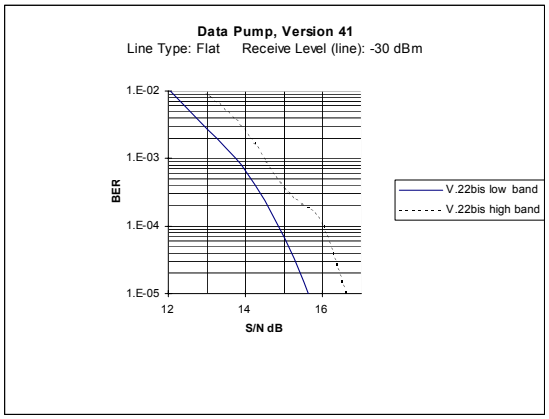
Figure 12. Bit Error Rate

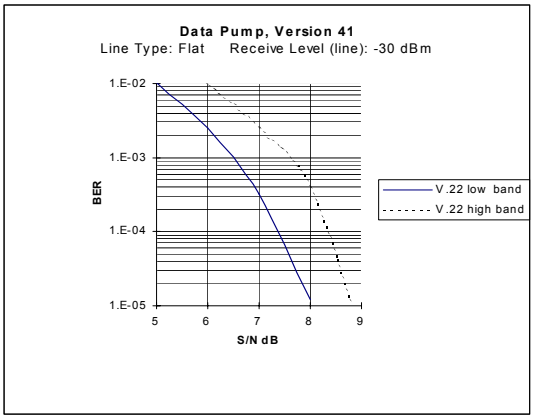
Note: Modems usually exhibit lower bit error rates receiving in the low band as opposed to the high band.

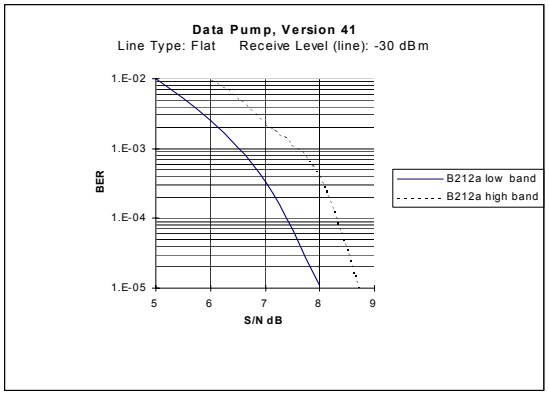
When an analog link is completed, the Adaptive Equalizer (AEQ) is frozen. The noise level is increased without making new links. These tests were conducted using a Consultronics TCS500 Telephone Line Simulator, and a Hewlett Packard 4951B protocol analyzer/BERT tester under the following conditions:

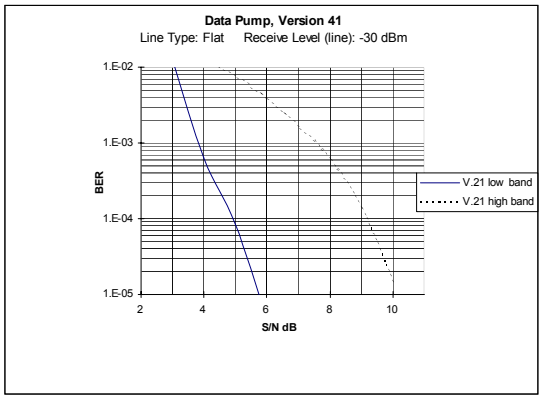
Table 29. Performance Testing Conditions

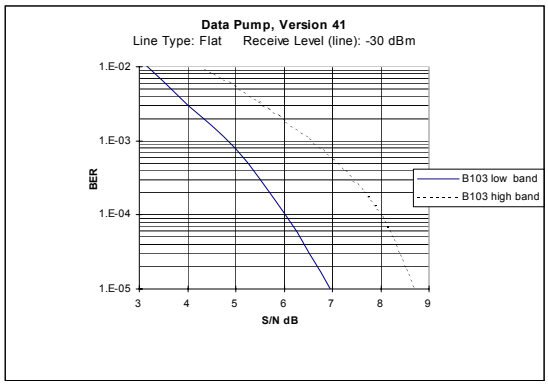
Line Simulation	Flat
Transmit Level	–10 dBm
Receive Level	–16.0 dBm
Data Transmitted	511 pseudo-random pattern
Number of Bits Sent	1,000,000
Number of Blocks Sent	1,000
Bits per Block	1,000
AEQ	Frozen after link establishment
Noise Calibration	C-message











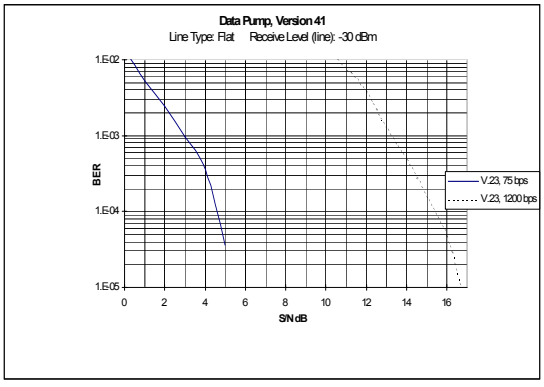


Figure 13. Typical Performance Data

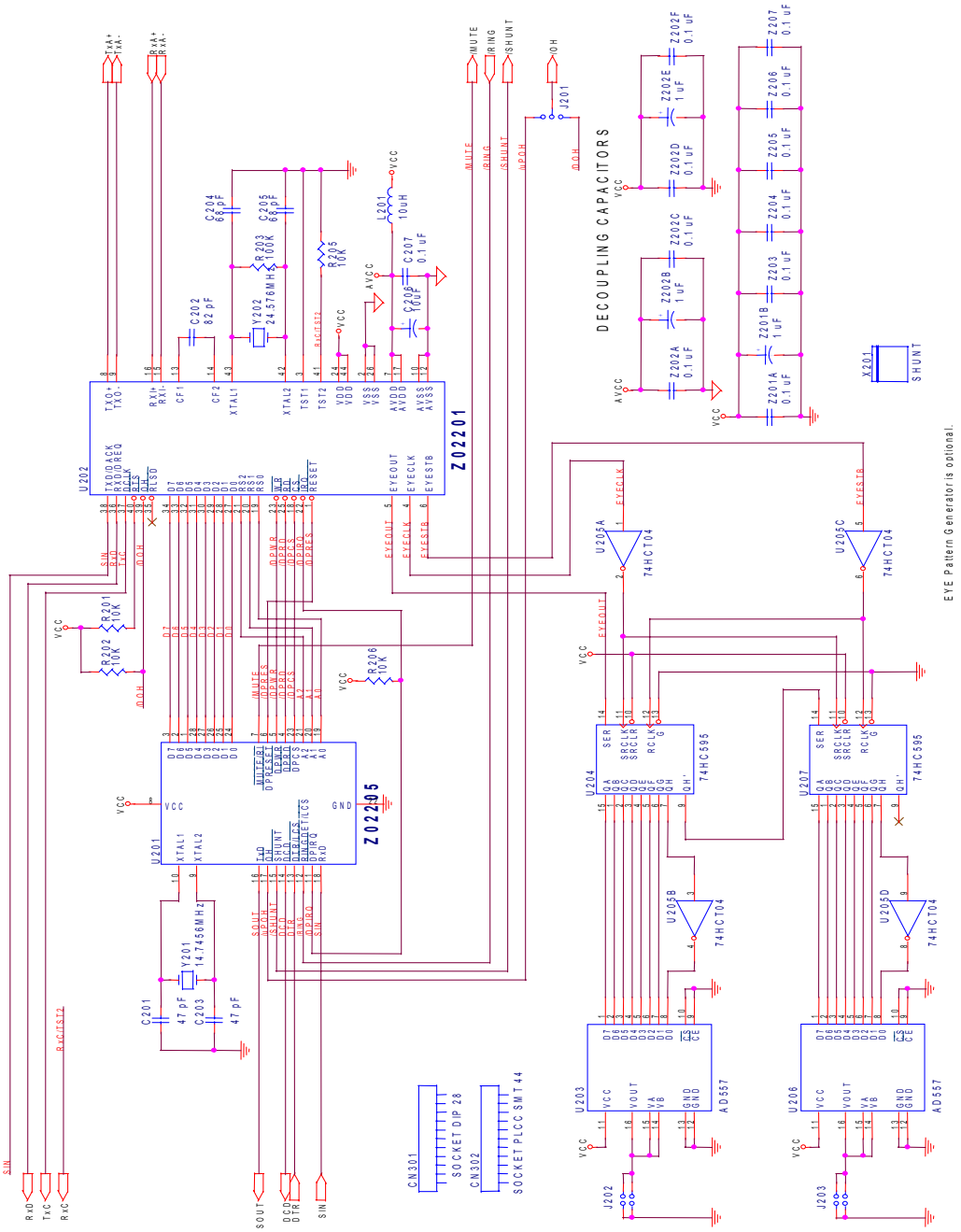


Figure 14. Typical Modem Using Z02201 and a Z02205 Controller

Example DAA

Figure 15 indicates an example DAA configuration for North America. Isolation transformer, T1, couples the primary (line) and secondary (modem) sides, while providing high voltage isolation. This *wet* transformer (allowing DC current) simplifies the circuit, while reducing the cost of the DAA.

On the Secondary side, the transmit (TxA+ and TxA–) and receive (RxA+ and RxA–) are combined in the 4-wire to 2-wire hybrid circuit. This hybrid can be either passive or active. The more complex active hybrid allows operation to lower signal levels. It cancels out most of the transmit signal from the receive signal.

On the Primary side, the off-hook relay switches the phone line between a local handset (PHONE) or the modem. The ring detect circuit consists of DC blocking capacitor C4, current limiting resistor R2, zener diodes CR3 and CR4, optocoupler U3, and its reverse protection diode D3. Protection elements RV1, F1, C1, and C2 (and transformer T1's isolation) provide higher voltage capability for approval in some foreign markets. C1 and C2, for example, may must be replaced by Metal Oxide Varistors (MOV's) or Gas Discharge Tubes (GDTs). The shunt relay reduces the DAA impedance during pulse dialing. This operation is required for some country regulations

.

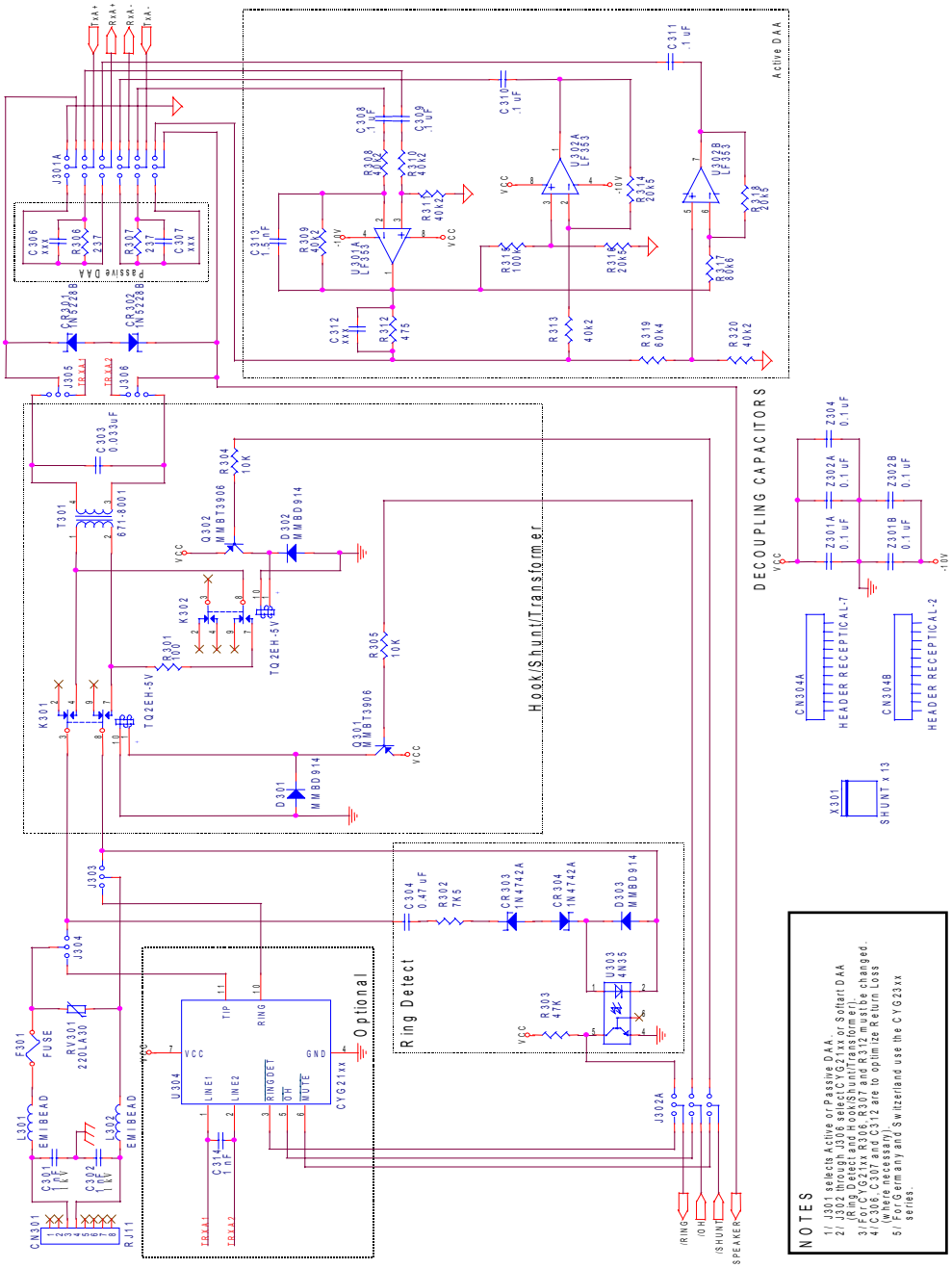


Figure 15. Example DAA

Eye Pattern Circuit

Figure 16 is the eye pattern circuitry used in the Z0220100ZCO modem evaluation board, and can be used with modem components such as the ZiLOG Z02201 and Z02201 that have an eye pattern interface. The Z02201 Eye Pattern port consists of 3 signals:

Data (EYEOUT)—The most significant and least significant bytes of this 16 bit word are the X and Y coordinates respectively for the eye pattern display. Each byte is most significant bit first.

Clock (EYECLK)—Data is set on the rising edge of the EYECLK, and should be read on the falling edge.

Strobe (EYESTB)—This signal is active Low when the data is valid.

Data is shifted through a pair of 8 bit serial-in parallel-out shift registers (74HC594) in response to the falling edge of EYECLK, then latched into a pair of 8 bit DACs on the rising edge of EYESTB. The output of these DACs can be viewed on an oscilloscope in X–Y mode to see the received signal quality.

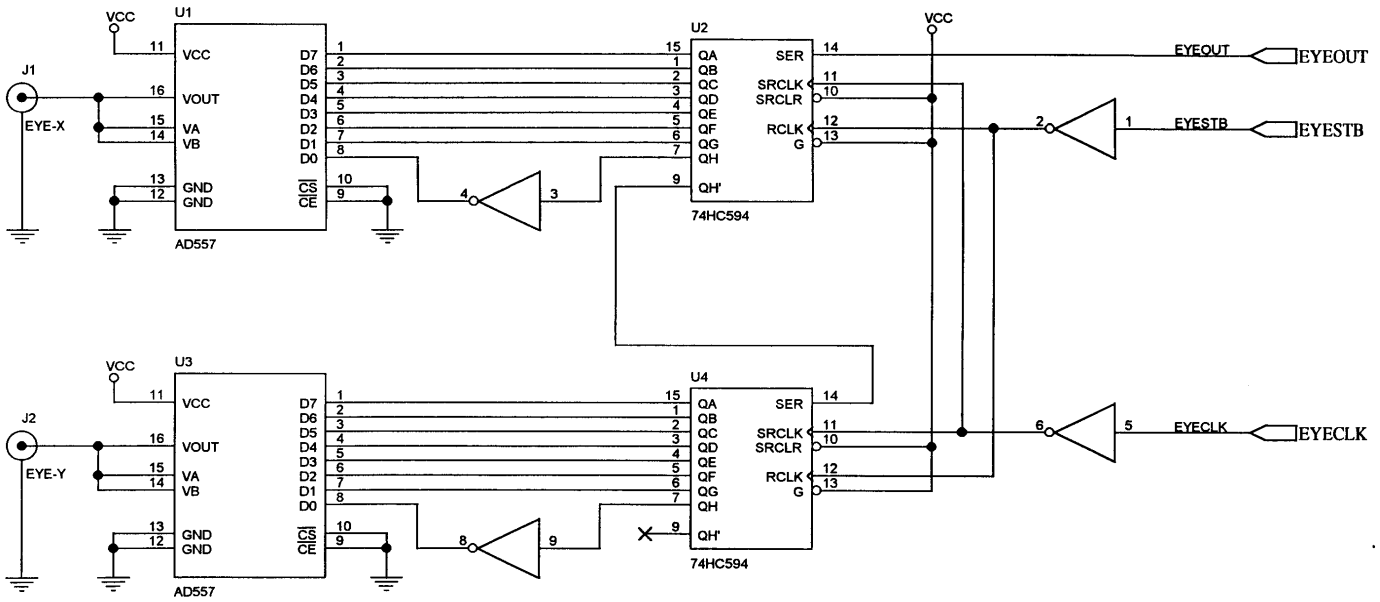
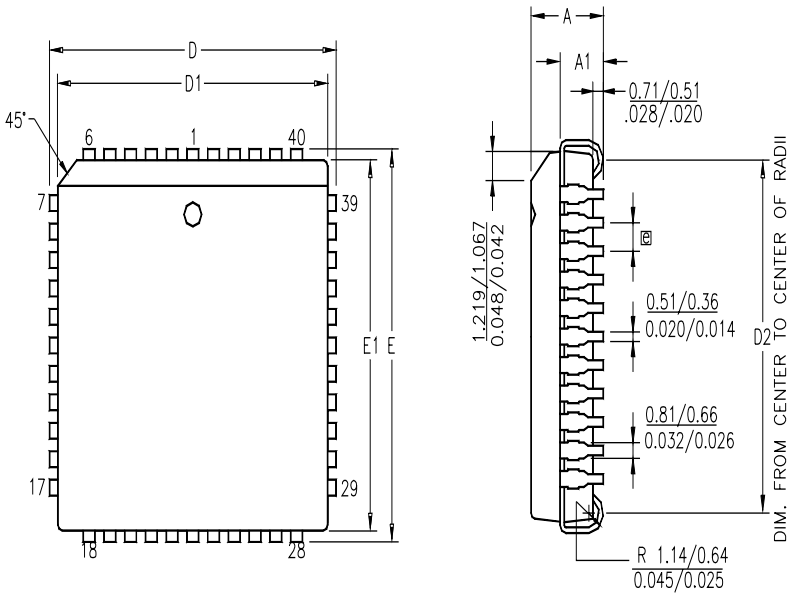


Figure 16. Eye Pattern Circuit

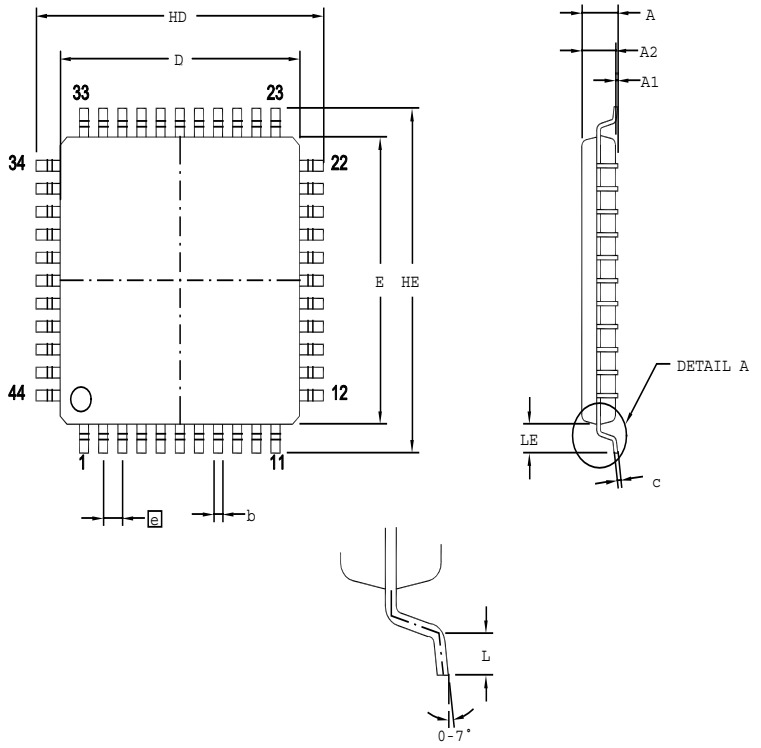
Package Information



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
   INCH

Figure 17. 44-Lead PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
c	0.09	0.20	0.004	0.008
HD	11.75	12.25	0.463	0.482
D	9.90	10.10	0.390	0.398
HE	11.75	12.25	0.463	0.482
E	9.90	10.10	0.390	0.398
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
LE	1.00 REF		0.039 REF	

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : .10mm / 0.004"

Figure 18. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z02201

12.288 MHz

44-Pin PLCC

ROM Code Version 0x48	Z0220112VSCR4078
ROM Code Version 0X31	Z0220112VSCR3470

Refer to the Z02201 Product Update for the software differences between the two ROM codes versions. The Product Update also lists the work-arounds for Ver. 0x31 of the ROM Code.

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.Codes

Speed	12=12.288 MHz
Package	V=Plastic Leaded Chip Carrier
Temperature	S=0°C to +70°C
Environmental	C = Plastic Standard
ROM Code	R4078 = ROM code number 4078 (ROM code Version 0x48) R3470 = ROM code number 3470 (ROM code Version 0x31)

Example

Z02201 12 V S C R 4078 is a Z02201 with ROM code R4078, 12.288 MHz, PLCC, 0 °C to +70 °C, Plastic Standard Flow