Notes:

1. No tracks or vias in the shaded "KEEP OUT" AREA.

2. No other track or signal within 0.020" of any contact pad.

3. Do not allow solder paste on the contact pads. It is essential to eliminate any hole in the solder paste-mask (solder stencil) layer. If this is not possible make the contact pads thru-hole with finished hole size of 0.008" or less.

4. To avoid ordering confusion, please specify DNL in your BOM.

5. The TC2030-CLIP board can attach to the three alignment pins from underneath the PCB to temporarily retain the cable in place.

.2000 "
5.080 mm

.0500 "
1.270 mm

.0500 "
1.270 mm

.0400 " 1.016 mm

.0250 " .635 mm

$\varnothing$.0390 "± .0030
$\varnothing$.991 mm± .076

NON-PLATED
THRU HOLE
ALIGNMENT PIN HOLES

$\varnothing$.0310 "± .0030
$\varnothing$.787 mm± .076

CONDUCTIVE
CONTACT PADS
NO SOLDER PASTE

"KEEP OUT" AREA
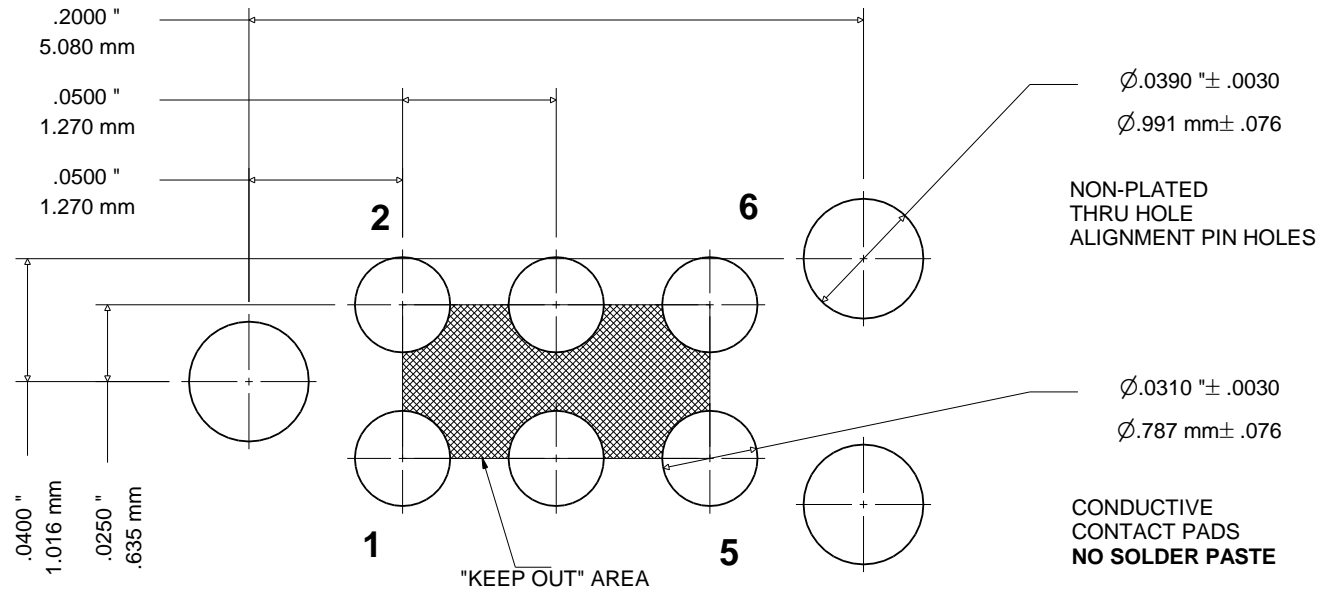
PCB TOP LAYER

Microchip ICD / ICSP signals
Pin 1: MCLR / Vpp
Pin 2: Vdd
Pin 3: GND
Pin 4: PGD (ICSPDAT)
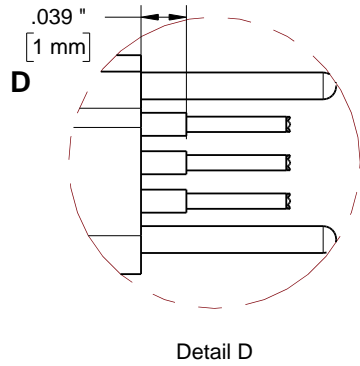**Pin 5: PGC (ICSPCLK)**
Pin 6: Unused / LVP

SIZE	FSCM NO.	DWG NO.	**FOOTPRINT FOR**	REV
A			**TC2030-MCP-NL-FP**	**A**
SCALE 11:1		www.TAG-CONNECT.com	SHEET 1 Of 3

NOTE:
Dimensions subject to change

.125 "
[3.175 mm]

contact pins
compressed

A

1.235 "
[31.369 mm]

.5 "
[12.7 mm]

D

.039 "
[1 mm]

.236 "
[6.000 mm]

.39 "
[9.906 mm]

.285 "
[7.239 mm]

Detail D

.39 "
[9.906 mm]

.150 "
[3.811 mm]

.240 "
[6.096 mm]

| 6 | 2 |
| 5 | 1 |

| 1 | 6 |
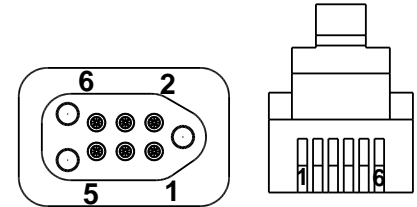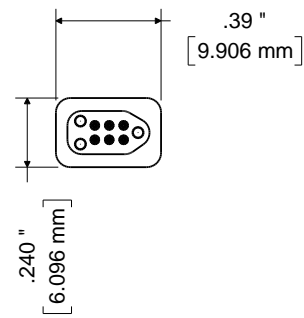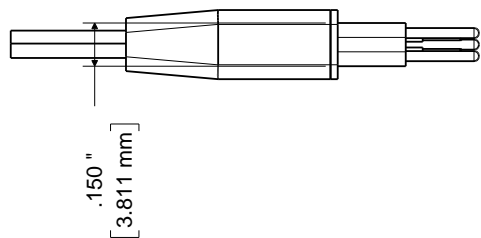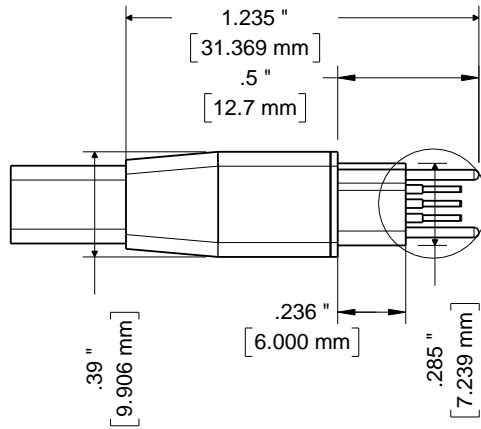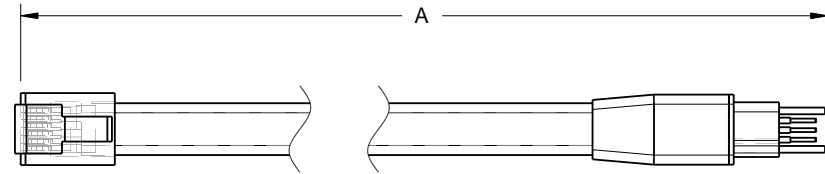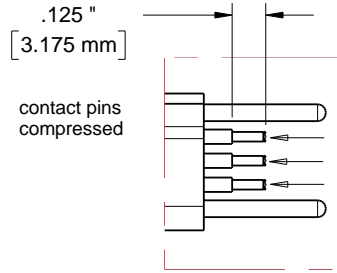
SIGNAL	TAG 6 PIN	RJ12
MCLR / VPP	1	6
VDD	2	5
GND	3	4
PGD(ICSP DAT)	4	3
PGC(ICSP CLK)	5	2
NC / LVP	6	1

| PART NUMBER | A | |
	IN	MM
TC2030-MCP-NL	6	152.4
TC2030-MCP-10-NL	10	254

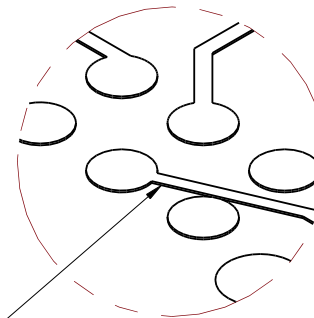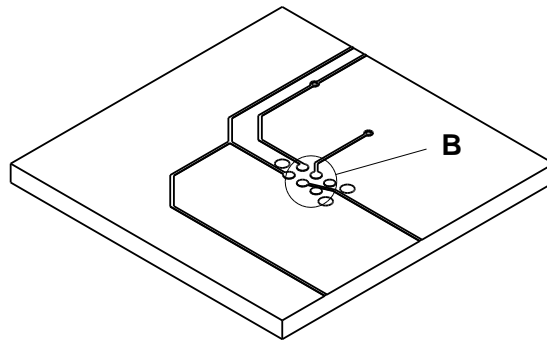| SIZE | FSCM NO. | DWG NO. | | REV |
| A | | **TC2030-MCP-NL** | | **A** |
| SCALE | | www.TAG-CONNECT.com | SHEET 2 Of 3 | |

Layout Problems to Avoid

A
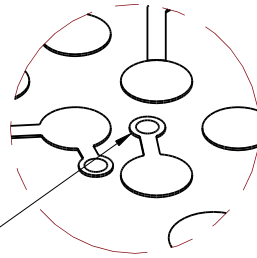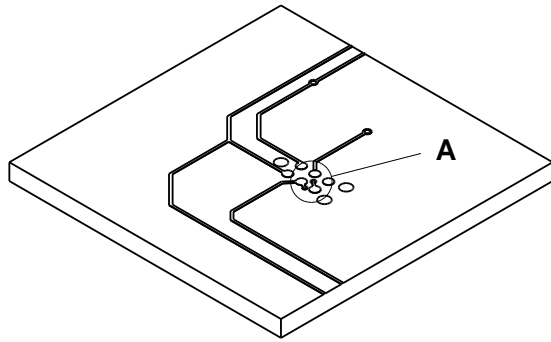
Detail A

Vias between
contact pads

C
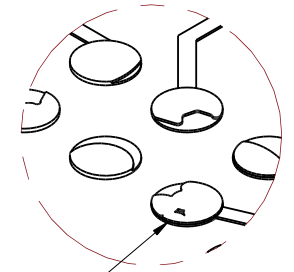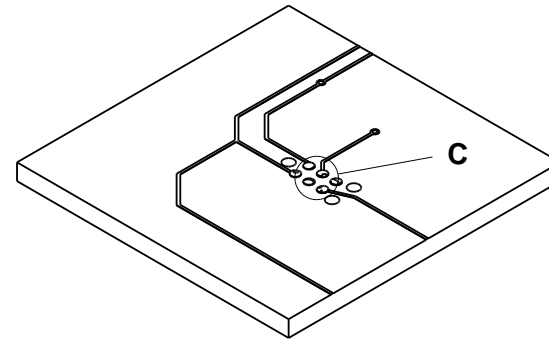
Detail C

Applying solder paste
to contact pads becuase
of holes in solder Paste Mask

B

Detail B

Traces less then .02"
away from contact pad
or in "KEEP OUT" area