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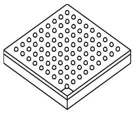
IMX35



Package Information
Plastic Package
Case 5284 17 x 17 mm, 0.8 mm Pitch

i.MX35 Applications Processors for Automotive Products

Ordering Information
See Table 1 on page 3 for ordering information.

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1 Introduction

The i.MX35 Auto Application Processor family is designed for automotive infotainment and navigation applications. These processors are AECQ100 Grade 3 qualified and rated for ambient operating temperatures up to 85 °C.

Based on an ARM11 microprocessor core running at up to 532 MHz, the device offers the following features and optimized system cost for the target applications.

- Audio connectivity and telematics:
  - Compressed audio playback from storage devices (CD, USB, HDD or SD card)
  - PlayFromDevice (1-wire and 2-wire support) for portable media players
  - iPod/iPhone control and playback
  - High-speed CD ripping to USB, SD/MMC or HDD for virtual CD changer
  - Audio processing for hands-free telephony: Bluetooth, AEC/NS, and microphone beam forming
  - Speech recognition

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- A/V connectivity and navigation:
  - Includes audio connectivity and telematics features
  - Map display and route calculation
  - QVGA video decode, WVGA video display
  - Sophisticated graphical user interface

The i.MX35 processor takes advantage of the ARM1136JF-S™ core running at 532 MHz that is boosted by a multilevel cache system, and features peripheral devices such as an autonomous image processing unit, a vector floating point (VFP11) co-processor, and a RISC-based DMA controller.

The i.MX35 supports connections to various types of external memories, such as SDRAM, mobile DDR and DDR2, SLC and MLC NAND Flash, NOR Flash and SRAM. The device can be connected to a variety of external devices such as high-speed USB2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

1.1 Features

The i.MX35 is designed for automotive infotainment video-enabled applications. It provides low-power solutions for applications demanding high-performance multimedia and graphics.

The i.MX35 is based on the ARM1136 platform, which has the following features:

- ARM1136JF-S processor, version r1p3
- 16-Kbyte L1 instruction cache
- 16-Kbyte L1 data cache
- 128-Kbyte L2 cache, version r0p4
- 128 Kbytes of internal SRAM
- Vector floating point unit (VFP11)

To boost multimedia performance, the following hardware accelerators are integrated:

- Image processing unit (IPU)
- OpenVG 1.1 graphics processing unit (GPU) (not available for the MCIMX351)

The MCIMX35 provides the following interfaces to external devices (some of these interfaces are muxed and not available simultaneously):

- 2 controller area network (CAN) interfaces
- 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface (CE-ATA is not available for the MCIMX351)
- 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133 MHz)
- 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
- Enhanced serial audio interface (ESAI)
- 2 synchronous serial interfaces (SSI)
- Ethernet MAC 10/100 Mbps
- 1 USB 2.0 host with ULPI interface or internal full-speed PHY. Up to 480 Mbps if external HS PHY is used.
- 1 USB 2.0 OTG (up to 480 Mbps) controller with internal high-speed OTG PHY

- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I^2C modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Media local bus (MLB) interface
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)
- Parallel ATA (up to 66 Mbytes) (not available for the MCIMX351)
- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for automotive applications.

Table 1. Ordering Information

Description	Part Number	Silicon Revision	Package[1]	Speed	Operating Temperature Range (°C)	Signal Ball Map Locations	Ball Map
i.MX351	MCIMX351AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX351	MCIMX351AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX355	MCIMX355AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX355	MCIMX355AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX356	MCIMX356AVM4B	2.0	5284	400 MHz	–40 to 85	Table 94	Table 96
i.MX356	MCIMX356AVM5B	2.0	5284	532 MHz[2]	–40 to 85	Table 94	Table 96
i.MX351	MCIMX351AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX351	MCIMX351AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX355	MCIMX355AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX355	MCIMX355AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX356	MCIMX356AJQ4C	2.1	5284	400MHz	-40 to 85	Table 95	Table 97
i.MX356	MCIMX356AJQ5C	2.1	5284	532MHz[2]	-40 to 85	Table 95	Table 97
i.MX356	SCIMX356BVMB	2	5284	532MHz	-40 to 85	Table 94	Table 96

[1] Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

[2] 532 MHz rated devices meet all specifications of 400 MHz rated devices. A 532 MHz device can be substituted in place of a 400 MHz device.

The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout. See Section 5, “Package Information and Pinout.”

Table 2 shows the functional differences between the different parts in the i.MX35 family.

Table 2. Functional Differences in the i.MX35 Parts

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
I2C (3)	Yes	Yes	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes	Yes	Yes
ESAI	Yes	Yes	Yes	Yes	Yes
SPDIF I/O	Yes	Yes	Yes	Yes	Yes
USB HS Host	Yes	Yes	Yes	Yes	Yes
USB OTG	Yes	Yes	Yes	Yes	Yes
FlexCAN (2)	Yes	Yes	Yes	Yes	Yes
MLB	Yes	Yes	Yes	Yes	Yes
Ethernet	Yes	Yes	Yes	Yes	Yes
1-Wire	Yes	Yes	Yes	Yes	Yes
KPP	Yes	Yes	Yes	Yes	Yes
SDIO/MMC (2)	Yes	Yes	Yes	Yes	Yes
SDIO/Memory Stick	Yes	Yes	Yes	Yes	Yes
External Memory Controller (EMC)	Yes	Yes	Yes	Yes	Yes
JTAG	Yes	Yes	Yes	Yes	Yes
PATA	—	Yes	Yes	Yes	Yes
CE-ATA	—	Yes	Yes	Yes	Yes
Image Processing Unit (IPU) (inversion and rotation, pre- and post-processing, camera interface, blending, display controller)	—	Yes	Yes	Yes	Yes
Open VG graphics acceleration (GPU)	—	Yes	—	Yes	Yes

1.3 Block Diagram

Figure 1 is the i.MX35 simplified interface block diagram.

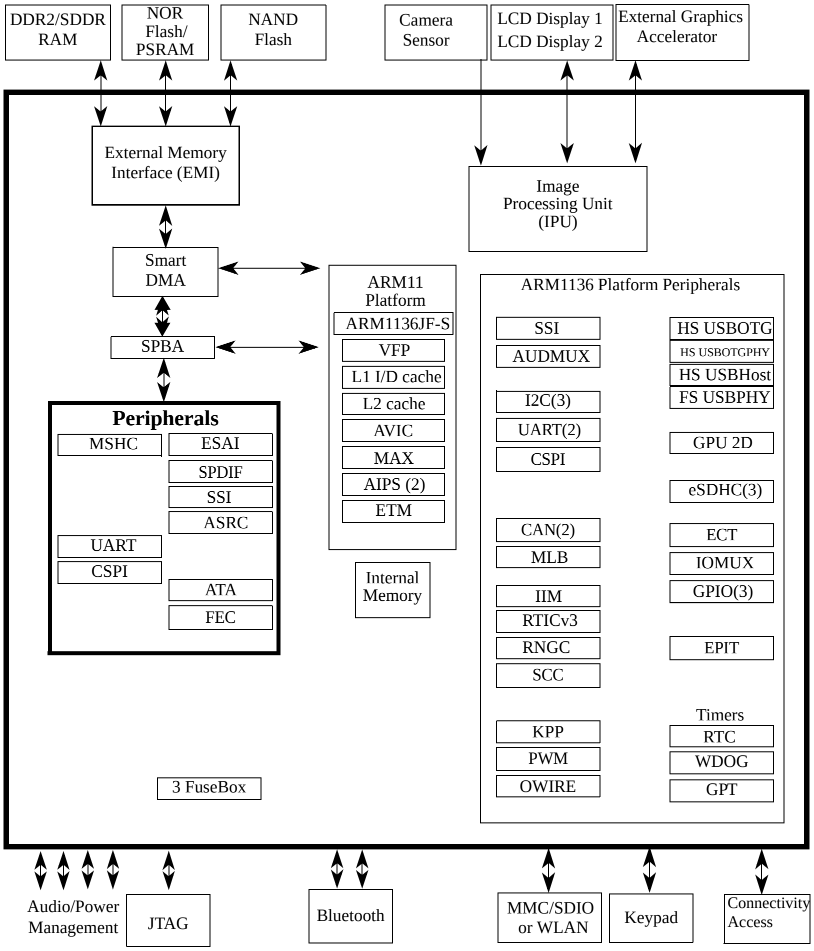

DDR2/SDDR RAM
NOR Flash/ PSRAM
NAND Flash
Camera Sensor
LCD Display 1
LCD Display 2
External Graphics Accelerator
External Memory Interface (EMI)
Image Processing Unit (IPU)
Smart DMA
SPBA
ARM11 Platform
ARM1136JF-S
VFP
L1 I/D cache
L2 cache
AVIC
MAX
AIPS (2)
ETM
Internal Memory
ARM1136 Platform Peripherals
SSI
AUDMUX
I2C(3)
UART(2)
CSPI
CAN(2)
MLB
IIM
RTICv3
RNGC
SCC
KPP
PWM
OWIRE
HS USBOTG
HS USBOTGPHY
HS USBHost
FS USBPHY
GPU 2D
eSDHC(3)
ECT
IOMUX
GPIO(3)
EPIT
Timers
RTC
WDOG
GPT
Peripherals
MSHC
ESAI
SPDIF
SSI
ASRC
UART
CSPI
ATA
FEC
3 FuseBox
Audio/Power Management
JTAG
Bluetooth
MMC/SDIO or WLAN
Keypad
Connectivity Access

Figure 1. i.MX35 Simplified Interface Block Diagram

2 Functional Description and Application Information

The i.MX35 consists of the following major subsystems:

- ARM1136 Platform—AP domain
- SDMA Platform and EMI—Shared domain

2.1 Application Processor Domain Overview

The applications processor (AP) and its domain are responsible for running the operating system and applications software, providing the user interface, and supplying access to integrated and external peripherals. The AP domain is built around an ARM1136JF-S core with 16-Kbyte instruction and data L1 caches, an MMU, a 128-Kbyte L2 cache, a multiported crossbar switch, and advanced debug and trace interfaces.

The i.MX35 core is intended to operate at a maximum frequency of 532 MHz to support the required multimedia use cases. Furthermore, an image processing unit (IPU) is integrated into the AP domain to offload the ARM11 core from performing functions such as color space conversion, image rotation and scaling, graphics overlay, and pre- and post-processing.

The functionality of AP Domain peripherals includes the user interface; the connectivity, display, security, and memory interfaces; and 128 Kbytes of multipurpose SRAM.

2.2 Shared Domain Overview

The shared domain is composed of the shared peripherals, a smart DMA engine (SDMA) and a number of miscellaneous modules. For maximum flexibility, some peripherals are directly accessible by the SDMA engine.

The i.MX35 has a hierarchical memory architecture including L1 caches and a unified L2 cache. This reduces the bandwidth demands for the external bus and external memory. The external memory subsystem supports a flexible external memory system, including support for SDRAM (SDR, DDR2 and mobile DDR) and NAND Flash.

2.3 Advanced Power Management Overview

To address the continuing need to reduce power consumption, the following techniques are incorporated in the i.MX35:

- Clock gating
- Power gating
- Power-optimized synthesis
- Well biasing

The insertion of gating into the clock paths allows unused portions of the chip to be disabled. Because static CMOS logic consumes only leakage power, significant power savings can be realized.

“Well biasing” is applying a voltage that is greater than V_{DD} to the nwells, and one that is lower than V_{SS} to the pwells. The effect of applying this well back bias voltage reduces the subthreshold channel leakage. For the 90-nm digital process, it is estimated that the subthreshold leakage is reduced by a factor of ten over the nominal leakage. Additionally, the supply voltage for internal logic can be reduced from 1.4 V to 1.22 V.

2.4 ARM11 Microprocessor Core

The CPU of the i.MX35 is the ARM1136JF-S core, based on the ARM v6 architecture. This core supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes) and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features are as follows:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline

- Branch prediction with return stack
- Low-interrupt latency
- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with hit-under-miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector floating point co-processor (VFP) for 3D graphics and hardware acceleration of other floating-point applications
- ETM™ and JTAG-based debug support

Table 3 summarizes information about the i.MX35 core.

Table 3. i.MX35 Core

Core Acronym	Core Name	Brief Description	Integrated Memory Features
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 × 5 multi-layer AHB crossbar switch (MAX), and a vector floating processor (VFP). The i.MX35 provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16-Kbyte instruction cache • 16-Kbyte data cache • 128-Kbyte L2 cache • 32-Kbyte ROM • 128-Kbyte RAM

2.5 Module Inventory

Table 4 shows an alphabetical listing of the modules in the MCIMX35. For extended descriptions of the modules, see the MCIMX35 reference manual.

Table 4. Digital and Analog Modules

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
1-WIRE	1-Wire interface	ARM	ARM1136 platform peripherals	1-Wire provides the communication line to a 1-Kbit add-only memory. the interface can send or receive 1 bit at a time.
ASRC	Asynchronous sample rate converter	SDMA	Connectivity peripherals	The ASRC is designed to convert the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. It supports a concurrent sample rate conversion of about –120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ATA	ATA module	SDMA	Connectivity peripherals	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disk drives and ATAPI optical disk drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital audio mux	ARM	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CAN(2)	CAN module	ARM	Connectivity peripherals	The CAN protocol is primarily designed to be used as a vehicle serial data bus running at 1 Mbps.
CCM	Clock control module	ARM	Clocks	This block generates all clocks for the peripherals in the SDMA platform. The CCM also manages ARM1136 platform low-power modes (WAIT, STOP), disabling peripheral clocks appropriately for power conservation, and provides alternate clock sources for the ARM1136 and SDMA platforms.
CSPI(2)	Configurable serial peripheral interface	SDMA, ARM	Connectivity peripherals	This module is a serial interface equipped with data FIFOs; each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts.
ECT	Embedded cross trigger	SDMA, ARM	Debug	ECT (embedded cross trigger) is an IP for real-time debug purposes. It is a programmable matrix allowing several subsystems to interact with each other. ECT receives signals required for debugging purposes (from cores, peripherals, buses, external inputs, and so on) and propagates them (propagation programmed through software) to the different debug resources available within the SoC.
EMI	External memory interface	SDMA	External memory interface	The EMI module provides access to external memory for the ARM and other masters. It is composed of the following main submodules: M3IF—provides arbitration between multiple masters requesting access to the external memory. SDRAM CTRL—interfaces to mDDR, DDR2 (4-bank architecture type), and SDR interfaces. NANDFC—provides an interface to NAND Flash memories. WEIM—interfaces to NOR Flash and PSRAM.
EPIT(2)	Enhanced periodic interrupt timer	ARM	Timer peripherals	Each EPIT is a 32-bit "set-and-forget" timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. **Note:** CE-ATA is not available for the MCIMX351.
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. **Note:** Not available for the MCIMX351.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
$I^2C(3)$	I^2C module	ARM	ARM1136 platform peripherals	Inter-integrated circuit (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance among many devices. The interface operates at up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, with arbitration and collision detection that prevent data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC identification module	ARM	Security modules	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	External signals and pin multiplexing	ARM	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution with the following features: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths held at constant levels for reduced power consumption
IPUv1	Image processing unit	ARM	Multimedia peripherals	The IPU supports video and graphics processing functions. It also provides the interface for image sensors and displays. The IPU performs the following main functions: • Preprocessing of data from the sensor or from the external system memory • Postprocessing of data from the external system memory • Post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 post-filtering algorithms • Displaying video and graphics on a synchronous (dumb or memory-less) display • Displaying video and graphics on an asynchronous (smart) display • Transferring data between IPU sub-modules and to/from the system memory with flexible pixel reformatting
KPP	Keypin port	ARM	Connectivity peripherals	Can be used for either keypin matrix scanning or general purpose I/O.
MLB	Media local bus	ARM	Connectivity peripherals	The MLB is designed to interface to an automotive MOST ring.
OSCAUD	OSC audio reference oscillator	Analog	Clock	The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576-MHz crystal.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
OSC24M	OSC24M 24-MHz reference oscillator	Analog	Clock	The signal from the external 24-MHz crystal is the source of the CLK24M signal fed into USB PHY as the reference clock and to the real time clock (RTC).
MPLL PPLL	Digital phase-locked loops	SDMA	Clocks	DPLLs are used to generate the clocks: MCU PLL (MPLL)—programmable Peripheral PLL (PPLL)—programmable
PWM	Pulse-width modulator	ARM	ARM1136 platform peripherals	The pulse-width modulator (PWM) is optimized to generate sound from stored sample audio images; it can also generate tones.
RTC	Real-time clock	ARM	Clocks	Provides the ARM1136 platform with a clock function (days, hours, minutes, seconds) and includes alarm, sampling timer, and minute stopwatch capabilities.
SDMA	Smart DMA engine	SDMA	System controls	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels and has an interface to connect to the ARM1136 platform subsystem, EMI interface, and the peripherals.
SJC	Secure JTAG controller	ARM	Pins	The secure JTAG controller (SJC) provides debug and test control with maximum security.
SPBA	SDMA peripheral bus arbiter	SDMA	System controls	The SPBA controls access to the SDMA peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
S/PDIF	Serial audio interface	SDMA	Connectivity peripherals	Sony/Philips digital transceiver interface
SSI(2)	Synchronous serial interface	SDMA, ARM(2)	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor connected to it to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the I^2C sound (I^2S) bus standard. The SSIs interface to the AUDMUX for flexible audio routing.
UART(3)	Universal asynchronous receiver/trans mitters	ARM (UART1,2) SDMA (UART3)	Connectivity peripherals	Each UART provides serial communication capability with external devices through an RS-232 cable using the standard RS-232 non-return-to-zero (NRZ) encoding format. Each module transmits and receives characters containing either 7 or 8 bits (program-selectable). Each UART can also provide low-speed IrDA compatibility through the use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission).

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
USBOH	High-speed USB on-the-go	SDMA	Connectivity peripherals	The USB module provides high performance USB on-the-go (OTG) functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 low pin count specification. The module has DMA capabilities handling data transfer between internal buffers and system memory.
WDOG	Watchdog modules	ARM	Timer peripherals	Each module protects against system failures by providing a method of escaping from unexpected events or programming errors. Once activated, the timer must be serviced by software on a periodic basis. If servicing does not take place, the watchdog times out and then either asserts a system reset signal or an interrupt request signal, depending on the software configuration.

[1] ARM = ARM1136 platform, SDMA = SDMA platform

3 Signal Descriptions: Special Function Related Pins

Some special functional requirements are supported in the device. The details about these special functions and the corresponding pin names are listed in Table 5.

Table 5. Special Function Related Pins

Function Name	Pin Name	Mux Mode	Detailed Description
External ARM Clock	EXT_ARMCLK	ALT0	External clock input for ARM clock.
External Peripheral Clock	I2C1_CLK	ALT6	External peripheral clock source.
External 32-kHz Clock	CAPTURE	ALT4	External clock input of 32 kHz, used when the internal 24M Oscillator is powered off, which could be configured either from CAPTURE or CSPI1_SS1.
	CSPI1_SS1	ALT2	
Clock Out	CLKO	ALT0	Clock-out pin from CCM, clock source is controllable and can also be used for debug.
Power Ready	GPIO1_0	ALT1	PMIC power-ready signal, which can be configured either from GPIO1_0 or TX1.
	TX1	ALT1	
Tamper Detect	GPIO1_1	ALT6	Tamper-detect logic is used to issue a security violation. This logic is activated if the tamper-detect input is asserted. Tamper-detect logic is enabled by the bit of IOMUXC_GPRA[2]. After enabling the logic, it is impossible to disable it until the next reset.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 7 on page 13
i.MX35 Operating Ranges	Table 8 on page 14
Interface Frequency	Table 9 on page 15

CAUTION

> Stresses beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 8 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	VDD_{max}[1]	–0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input voltage range	V_{Imax}	–0.5	3.6	V
Storage temperature	$T_{storage}$	–40	125	°C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Charge Device Model (CDM)		—	500[3]	

[1] VDD is also known as QVCC.

[2] HBM ESD classification level according to the AEC-Q100-002 standard

[3] Corner pins max. 750 V

4.1.1 i.MX35 Operating Ranges

Table 8 provides the recommended operating ranges. The term NVCC in this section refers to the associated supply rail of an input or output.

Table 8. i.MX35 Operating Ranges

Parameter	Symbol	Min.	Typical	Max.	Units
Core Operating Voltage $0 < f_{ARM} < 400$ MHz	V_{DD}	1.22	—	1.47	V
Core Operating Voltage $0 < f_{ARM} < 532$ MHz		1.33	—	1.47	V
State Retention Voltage		1	—	—	V
EMI[1]	NVCC_EMI1,2,3	1.7	—	3.6	V
WTDG, Timer, CCM, CSPI1	NVCC_CRM	1.75	—	3.6	V
NANDF	NVCC_NANDF	1.75	—	3.6	V
ATA, USB generic	NVCC_ATA	1.75	—	3.6	V
eSDHC1	NVCC_SDIO	1.75	—	3.6	V
CSI, SDIO2	NVCC_CSI	1.75	—	3.6	V
JTAG	NVCC_JTAG	1.75	—	3.6	V
LCDC, TTM, I2C1	NVCC_LCDC	1.75	—	3.6	V
I2Sx2,ESAI, I2C2, UART2, UART1, FEC	NVCC_MISC	1.75	—	3.6	V
MLB	NVCC_MLB[2]	1.75	—	3.6	V
USB OTG PHY	PHY1_VDDA	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_VDDA_BIAS	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_UPLLVDD	3.17	3.3	3.43	V
USB HOST PHY	PHY2_VDD	3.0	3.3	3.6	V
OSC24M	OSC24M_VDD	3.0	3.3	3.6	V
OSC_AUDIO	OSC_AUDIO_VDD	3.0	3.3	3.6	V
MPLL	MVDD	1.4	—	1.65	V
PPLL	PVDD	1.4	—	1.65	V
Fusebox program supply voltage	FUSE_VDD[3]	3.0	3.6	3.6	V
Operating ambient temperature range	T_A	–40	—	85	°C
Junction temperature range	T_J	–40	—	105	°C

[1] EMI I/O interface power supply should be set up according to external memory. For example, if using SDRAM then NVCC_EMI1,2,3 should all be set at 3.3 V (typ.). If using MDDR or DDR2, NVC_EMI1,2,3 must be set at 1.8 V (typ.).

[2] MLB interface I/O pads can be programmed to function as GPIO by setting NVCC_MLB to 1.8 or 3.3 V, but if used as MLB pads, NVCC_MLB must be set to 2.5 V in order to be compliant with external MOST devices. NVCC_MLB may be left floating.

[3] The Fusebox read supply is connected to supply of the full speed USB PHY. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. FUSE_VDD should be supplied by following the power up sequence given in Section 4.3.1, “Powering Up.”

4.1.2 Interface Frequency Limits

Table 9 provides information on interface frequency limits.

Table 9. Interface Frequency

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz

4.2 Power Modes

Table 10 provides descriptions of the power modes of the i.MX35 processor.

Table 10. i.MX35 Power Modes

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Wait	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is active. L2 cache is kept powered. MCU PLL is on (400 MHz) PER PLL is off (can be configured) (default: 300 MHz) Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured). RNGC internal osc is off.	16 mA	170 mA	7.2 mA	14 mA	1.2 mA	3 mA
Doze	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted. L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is on(400 MHz) PER PLL is off (can be configured). (300 Mhz). Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured) RNGC internal osc is off	12.4 mA	105 mA	7.2 mA	14 mA	1.2 mA	3 mA

Table 10. i.MX35 Power Modes (continued)

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Stop	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24 MHz is on OSC audio is off RNGC internal osc is off	1.1 mA	77 mA	400 μA	2.2 mA	1.2 mA	2.2 mA
Static	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24MHz is on OSC audio is off RNGC internal osc is off	820 μA	72 mA	50 μA	1.7 mA	24 μA	35 μA
Note: Typical column: T_A = 25 °C **Note:** Maximum column: T_A = 85 °C							

4.3 Supply Power-Up/Power-Down Requirements and Restrictions

This section provides power-up and power-down sequence guidelines for the i.MX35 processor.

CAUTION

Any i.MX35 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in irreversible damage to the i.MX35 processor (worst-case scenario).

NOTE

Deviation from these sequences may also result in one or more of the following:

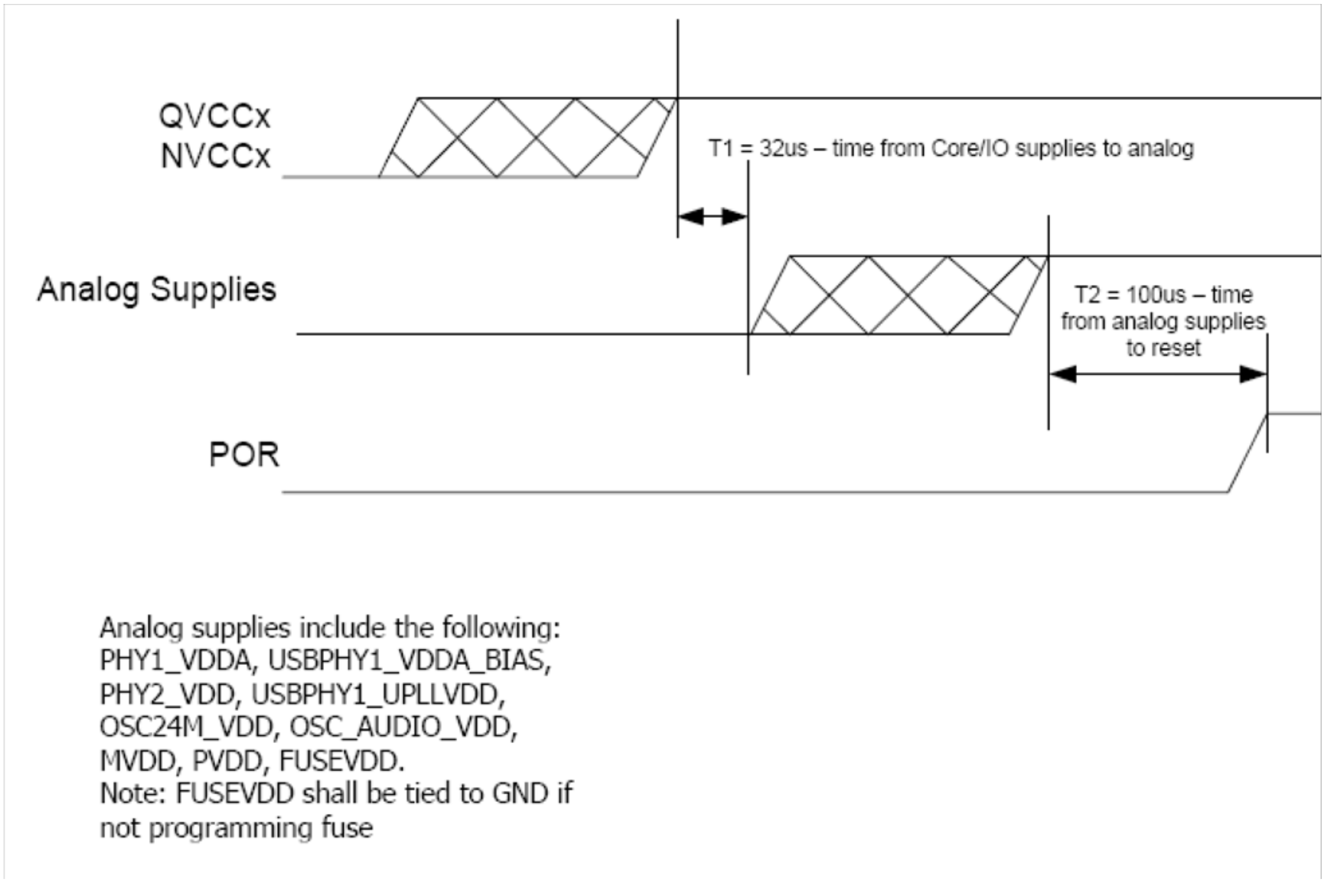
- Excessive current during power-up phase
- Prevent the device from booting
- Programming of unprogrammed fuses

4.3.1 Powering Up

The power-up sequence should be completed as follows:

1. Assert Power on Reset ($\overline{\text{POR}}$).
2. Turn on digital logic domain and IO power supply: VDD*n*, NVCC*x*
3. Wait until VDD*n* and NVCC*x* power supplies are stable + 32 µs.
4. Turn on all other power supplies: PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVDD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, FUSEVDD. (Always FUSE_VDD should be connected to ground, except when eFuses are to be programmed.)
5. Wait until PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVDD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, (FUSEVDD, optional). Power supplies are stable + 100 µs.
6. Deassert the $\overline{\text{POR}}$ signal.

Figure 2 shows the power-up sequence and timing.


QVCCx
NVCCx
T1 = 32us – time from Core/IO supplies to analog
Analog Supplies
T2 = 100us – time from analog supplies to reset
POR

Analog supplies include the following:
PHY1_VDDA, USBPHY1_VDDA_BIAS,
PHY2_VDD, USBPHY1_UPLLVDD,
OSC24M_VDD, OSC_AUDIO_VDD,
MVDD, PVDD, FUSEVDD.
Note: FUSEVDD shall be tied to GND if not programming fuse

Figure 2. i.MX35 Power-Up Sequence and Timing

4.3.2 Powering Down

The power-up sequence in reverse order is recommended for powering down. However, all power supplies can be shut down at the same time.

4.4 Reset Timing

There are two ways of resetting the i.MX35 using external pins:

- Power On Reset (using the POR_B pin)
- System Reset (using the RESET_IN_B pin)

4.4.1 Power On Reset

POR_B is normally connected to a power management integrated circuit (PMIC). The PMIC asserts POR_B while the power supplies are turned on and negates POR_B after the power up sequence is finished. See Figure 2.

Assuming the i.MX35 chip is already fully powered; it is still possible to reset all of the modules to their default reset by asserting POR_B for at least 4 CKIL cycles and later de-asserting POR_B. This method of resetting the i.MX35 can also be supported by tying the POR_B and RESET_IN_B pins together.

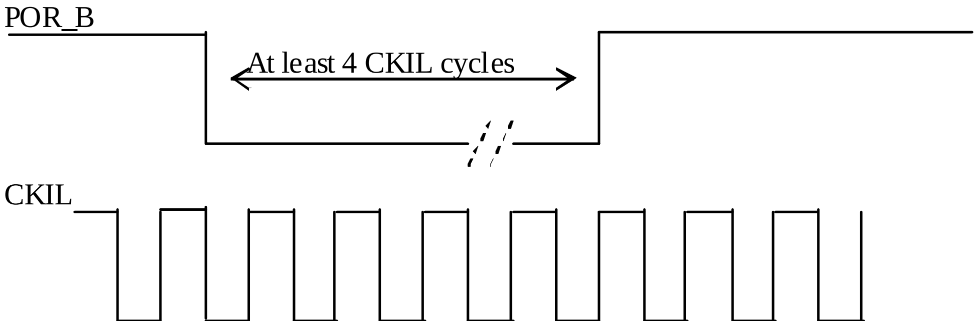


Figure 3. Timing Between POR_B and CKIL for Complete Reset of i.MX35

4.4.2 System Reset

System reset can be achieved by asserting RESET_IN_B for at least 4 CKIL cycles and later negating RESET_IN_B. The following modules are not reset upon system reset: RTC, PLLs, CCM, and IIM. POR_B pin must be deasserted all the time.

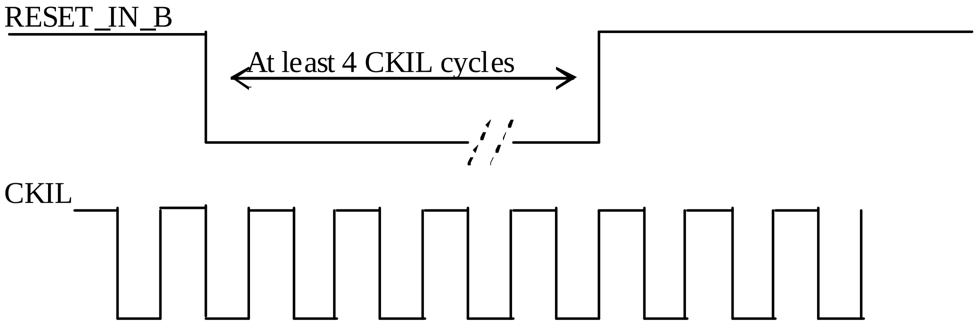


Figure 4. Timing Between RESET_IN_B and CKIL for i.MX35 System Reboot

4.5 Power Characteristics

The table shows values representing maximum current numbers for the i.MX35 under worst case voltage and temperature conditions. These values are derived from the i.MX35 with core clock speeds up to 532 MHz. Common supplies have been bundled according to the i.MX35 power-up sequence requirements. Peak numbers are provided for system designers so that the i.MX35 power supply requirements will be satisfied during startup and transient conditions. Freescale recommends that system current measurements be taken with customer-specific use-cases to reflect normal operating conditions in the end system.

Table 11. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVCC	1.47	400
MVDD, PVDD	1.65	20
NVCC_EMI1, NVCC_EMI2, NVCC_EMI3, NVCC_LCDC, NVCC_NFC	1.9	90
FUSE_VDD[1]	3.6	62
NVCC_MISC, NVCC_CSI, NVCC_SDIO, NVCC_CRM, NVCC_ATA, NVCC_MLB, NVCC_JTAG	3.6	60
OSC24M_VDD, OSC_AUDIO_VDD, PHY1_VDDA, PHY2_VDD, USBPHY1_UPLLVDD, USBPHY1_VDDA_BIAS	3.6	25

[1] This rail is connected to ground; it only needs a voltage if eFuses are to be programmed. FUSE_VDD should be supplied by following the power up sequence given in Section 4.3.1, “Powering Up.”

The method for obtaining max current is as follows:

1. Measure worst case power consumption on individual rails using directed test on i.MX35.
2. Correlate worst case power consumption power measurements with worst case power consumption simulations.
3. Combine common voltage rails based on power supply sequencing requirements
4. Guard band worst case numbers for temperature and process variation. Guard band is based on process data and correlated with actual data measured on i.MX35.
5. The sum of individual rails is greater than real world power consumption, as a real system does not typically maximize power consumption on all peripherals simultaneously.

4.6 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 12. These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.168 mm, Core via plating 0.016 mm.
- Full array map design, but nearly all balls under die are power or ground.
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: k = 0.9 W/m K

Table 12. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	R_{eJA}	53	ºC/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	R_{eJA}	30	ºC/W

Table 12. Thermal Resistance Data (continued)

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] (at 200 ft/min)	Single layer board (1s)	R_{eJMA}	44	ºC/W
Junction to ambient[1] (at 200 ft/min)	Four layer board (2s2p)	R_{eJMA}	27	ºC/W
Junction to boards[2]	—	R_{eJB}	19	ºC/W
Junction to case (top)[3]	—	R_{eJCtop}	10	ºC/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	ºC/W

[1] Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[2] Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

[3] Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[4] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

4.7 I/O Pin DC Electrical Characteristics

I/O pins are of two types: GPIO and DDR. DDR pins can be configured in three different drive strength modes: mobile DDR, SDRAM, and DDR2. The SDRAM and mobile DDR modes can be further customized at three drive strength levels: normal, high, and max.

Table 13 shows currents for the different DDR pin drive strength modes.

Table 13. DDR Pin Drive Strength Mode Current Levels

Drive Mode	Normal	High	Max.
Mobile DDR (1.8 V)	3.6 mA	7.2 mA	10.8 mA
SDRAM (1.8 V)	—	—	6.5 mA
SDRAM (3.3 V)	4 mA	8 mA	12 mA
DDR2 (1.8 V)	—	—	13.4 mA

Table 14 shows the DC electrical characteristics for GPIO, DDR2, mobile DDR, and SDRAM pins. The term NVCC refers to the power supply voltage that feeds the I/O of the module in question. For example, NVCC for the SD/MMC interface refers to NVCC_SDIO.

Table 14. I/O Pin DC Electrical Characteristics

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GPIO	High-level output voltage	Voh	Ioh = –1 mA Ioh = specified drive	NVCC – 0.15 0.8 × NVCC	—	—	V
	Low-level output voltage	Vol	Iol = 1 mA Iol = specified drive	—	—	0.15 0.2 × NVCC	V
	High-level output current for slow mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–2.0 –4.0 –8.0	—	—	mA
	High-level output current for fast mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–4.0 –6.0 –8.0	—	—	mA
	Low-level output current for slow mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	2.0 4.0 8.0	—	—	mA
	Low-level output current for fast mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	4.0 6.0 8.0	—	—	mA
	High-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode)	VIH	—	0.7 × NVCC	—	NVCC	V
	Low-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode	VIL	—	–0.3 V	—	0.3 × NVCC	V
	Input Hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8 V	—	410 330	—	mV
	Schmitt trigger VT+	VT+	—	0.5 × NVCC	—		V
	Schmitt trigger VT–	VT–	—	—	—	0.5 × NVCC	V
	Pull-up resistor (22 kΩ PU)	Rpu	Vi = 0	—	22	—	kΩ
	Pull-up resistor (47 kΩ PU)	Rpu	Vi = 0	—	47	—	kΩ
	Pull-up resistor (100 kΩ PU)	Rpu	Vi = 0	—	100	—	kΩ
	Pull-down resistor (100 kΩ PD)	Rpd	Vi = NVCC	—	100	—	kΩ
	External resistance to pull keeper up when enabled	Rkpu	Ipu > 620 µA @ min Vddio = 3.0 V	—	—	4.8	kΩ
	External resistance to pull keeper down when enabled	Rkpd	Ipu > 510 µA @min Vddio = 3.0 V	—	—	5.9	kΩ

Table 14. I/O Pin DC Electrical Characteristics (continued)

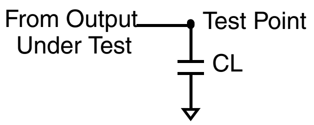
Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DDR2	High-level output voltage	Voh	—	NVCC – 0.28	—	—	V
	Low-level output voltage	Vol	—		—	0.28	V
	Output min. source current	Ioh	—	–13.4	—	—	mA
	Output min. sink current	Iol	—	13.4	—	—	mA
	DC input logic high	VIH(dc)	—	NVCC ÷ 2 + 0.125	—	NVCC + 0.3	V
	DC input logic low	VIL(dc)	—	–0.3 V	—	NVCC ÷ 2 – 0.125	V
	DC input signal voltage (for differential signal)	Vin(dc)	—	–0.3	—	NVCC + 0.3	V
	DC differential input voltage	Vid(dc)	—	0.25	—	NVCC + 0.6	V
	Termination voltage	Vtt	—	NVCC ÷ 2 – 0.04	NVCC ÷ 2	NVCC ÷ 2 + 0.04	V
	Input current (no pull-up/down)	IIN	—	—	—	±1	µA
	Tri-state I/O supply current	Icc – NVCC	—	—	—	±1	µA
Mobile DDR	High-level output voltage	—	I_{OH} = –1mA I_{OH} = specified drive	NVCC – 0.08 0.8 × NVCC	—	—	V
	Low-level output voltage	—	I_{OL} = 1mA I_{OL} = specified drive	—	—	0.08 0.2 × NVCC	V
	High-level output current (Voh = 0.8 × NVCCV)	—	Standard drive High drive Max. drive	–3.6 –7.2 –10.8	—	—	mA
	Low-level output current (Vol = 0.2 × NVCCV)	—	Standard Drive High Drive Max. Drive	3.6 7.2 10.8	—	—	mA
	High-Level DC CMOS input voltage	VIH	—	0.7 × NVCC	—	NVCC + 0.3	V
	Low-Level DC CMOS input voltage	VIL	—	–0.3	—	0.2 × NVCC	V
	Differential receiver VTH+	VTH+	—	—	—	100	mV
	Differential receiver VTH–	VTH–	—	–100	—		mV
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	µA
	Tri-state I/O supply current	Icc – NVCC	VI = NVCC or 0	—	—	±1	µA

Table 14. I/O Pin DC Electrical Characteristics (continued)

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SDR (1.8 V)	High-level output voltage	Voh	Ioh = 5.7 mA	OVDD – 0.28	—	—	V
	Low-level output voltage	Vol	Ioh = 5.7 mA	—	—	0.4	V
	High-level output current	Ioh	Max. drive	5.7	—	—	mA
	Low-level output current	Iol	Max. drive	7.3	—	—	mA
	High-level DC Input Voltage	VIH	—	1.4	—	1.98	V
	Low-level DC Input Voltage	VIL	—	–0.3	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI=NVCC	—	—	150 80	μA
	Tri-state I/O supply current	Icc (NVCC)	VI = OVDD or 0	—	—	1180	μA
	Tri-state core supply current	Icc (NVCC)	VI = VDD or 0	—	—	1220	μA
SDR (3.3 V)	High-level output voltage	Voh	Ioh=specified drive (Ioh = –4, –8, –12, –16 mA)	2.4	—	—	V
	Low-level output voltage	Vol	Ioh=specified drive (Ioh = 4, 8, 12, 16 mA)	—	—	0.4	V
	High-level output current	Ioh	Standard drive High drive Max. drive	–4.0 –8.0 –12.0	—	—	mA
	Low-level output current	Iol	Standard drive High drive Max. drive	4.0 8.0 12.0	—	—	mA
	High-level DC Input Voltage	VIH	—	2.0	—	3.6	V
	Low-level DC Input Voltage	VIL	—	–0.3V	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	μA
	Tri-state I/O supply current	Icc (NVCC)	VI = NVCC or 0	—	—	±1	μA

4.8 I/O Pin AC Electrical Characteristics

Figure 5 shows the load circuit for output pins.



CL includes package, probe and jig capacitance

Figure 5. Load Circuit for Output Pin

Figure 6 shows the output pin transition time waveform.

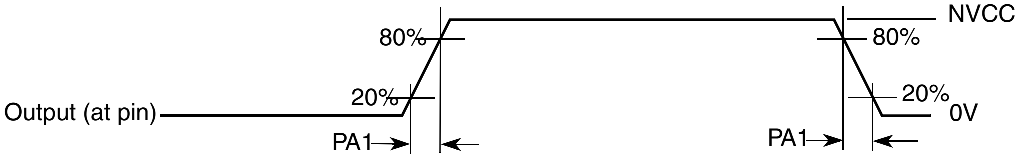


Figure 6. Output Pin Transition Time Waveform

4.8.1 AC Electrical Test Parameter Definitions

AC electrical characteristics in Table 16 through Table 21 are not applicable for the output open drain pull-down driver.

The dI/dt parameters are measured with the following methodology:

- The zero voltage source is connected between pin and load capacitance.
- The current (through this source) derivative is calculated during output transitions.

Table 15. AC Requirements of I/O Pins

Parameter	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V

Table 16. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.79/1.12 0.49/0.73	1.30/1.77 0.84/1.23	2.02/2.58 1.19/1.58	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.48/0.72 0.27/0.42	0.76/1.10 0.41/0.62	1.17/1.56 0.63/0.86	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.25/0.40 0.14/0.21	0.40/0.59 0.21/0.32	0.60/0.83 0.32/0.44	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	15 16	36 38	76 80	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	8 9	20 21	45 47	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	4 4	10 10	22 23	mA/ns

Table 17. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.30/0.42 0.20/0.29	0.54/0.73 0.35/0.50	0.91/1.20 0.60/0.80	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.19/0.28 0.12/0.18	0.34/0.49 0.34/0.49	0.58/0/79 0.36/0.49	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.12/0.18 0.07/0.11	0.20/0.30 0.11/0.17	0.34/0.47 0.20/0.27	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	21 22	56 58	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	5 5	14 15	38 40	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	2 2	7 7	18 19	mA/ns

Table 18. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode for [NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. rise/fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	22 23	52 55	116 121	mA/ns

Table 19. AC Electrical Characteristics, GPIO Pins in Fast Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns

Table 20. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.63/0.85 0.52/0.67 0.41/0.59	1.10/1.40 0.90/1.10 0.73/0.99	1.86/2.20 1.53/1.73 1.20/1.50	V/ns
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.40/0.58 0.33/0.43 0.25/0.37	0.71/0.98 0.56/0.70 0.43/0.60	1.16/1.40 0.93/1.07 0.68/0.90	V/ns
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.19/0.25 0.13/0.21	0.41/0.59 0.32/0.35 0.23/0.33	0.66/0.87 0.51/0.59 0.36/0.48	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	22 23	62 65	148 151	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	15 16	42 44	102 107	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	7 8	21 22	52 54	mA/ns

Table 21. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pin di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.8.2 AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)

Table 22. AC Electrical Characteristics of DDR Type IO Pins in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pin di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 23. AC Requirements of DDR2 Pins

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V
AC differential cross point voltage for output[2]	Vox(ac)	NVCC ÷ 2 – 0.125	NVCC ÷ 2 + 0.125	V

[1] The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

[2] The typical value of Vox(ac) is expected to be about 0.5 × NVCC and Vox(ac) is expected to track variation in NVCC. Vox(ac) indicates the voltage at which the differential output signal must cross. Cload = 25 pF.

Table 24. AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns

Table 25. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Min. Clock Frequency	Max. Rise/Fall	Units
Clock frequency	f	—	—	125	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns

Table 26. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Clock frequency	f	—	125	—	—	MHz
Output pin slew rate (max. drive)[1]	tps	25 pF 50 pF	2.83/2.68 1.59/1.49	1.84/1.85 1.03/1.05	1.21/1.40 0.70/0.75	V/ns
Output pin di/dt (max. drive)[2]	didt	25 pF 50 pF	89 95	202 213	435 456	mA/ns
Input pin transition times[3]	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns
Input pin propagation delay, 50%–50%	tpi	1.0 pF	0.35/1.17	0.63/1.53	1.16/2.04	ns
Input pin propagation delay, 40%–60%	tpi	1.0 pF	1.18/1.99	1.45/2.35	1.97/2.85	ns

[1] Min. condition for tps: wcs model, 1.1 V, IO 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

[2] Max. condition for tdit: bcs model, 1.3 V, IO 1.95 V, and –40 °C.

[3] Max. condition for tpi and trfi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Min. condition for tpi and trfi: bcs model, 1.3 V, IO 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

4.9 Module-Level AC Electrical Specifications

This section contains the AC electrical information (including timing specifications) for the modules of the i.MX35. The modules are listed in alphabetical order.

4.9.1 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. See the electrical specification for SSI.

4.9.2 CSPI AC Electrical Specifications

The i.MX35 provides two CSPI modules. CSPI ports are multiplexed in the i.MX35 with other pins. See the “External Signals and Multiplexing” chapter of the reference manual for more details.

Figure 7 and Figure 8 depict the master mode and slave mode timings of the CSPI, and Table 27 lists the timing parameters.

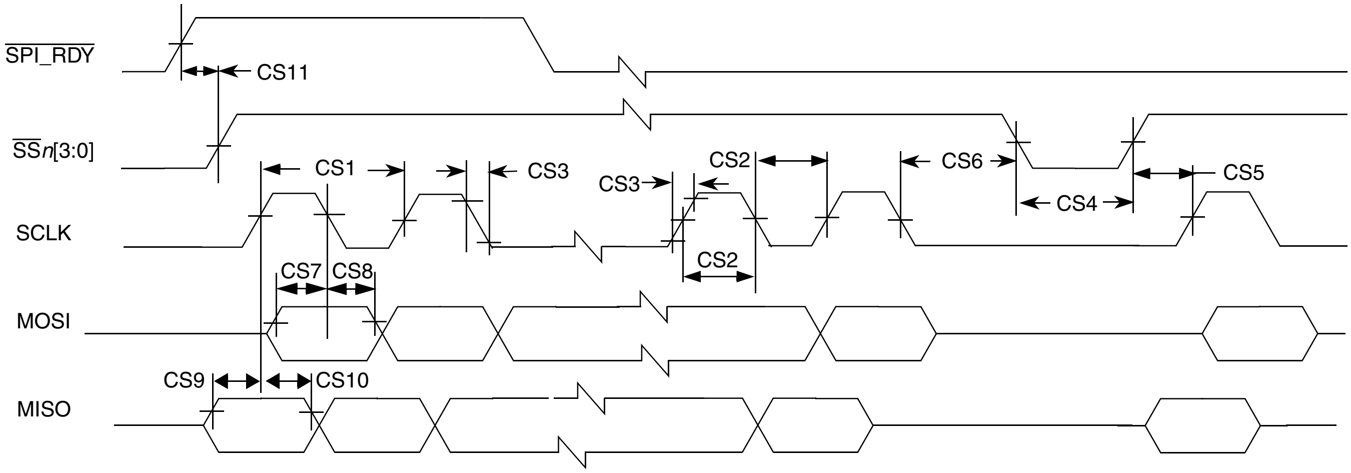

SPI_RDY
CS11
SSn[3:0]
CS1
CS3
CS3
CS2
CS6
CS5
CS4
SCLK
CS7
CS8
CS2
MOSI
CS9
CS10
MISO

Figure 7. CSPI Master Mode Timing Diagram

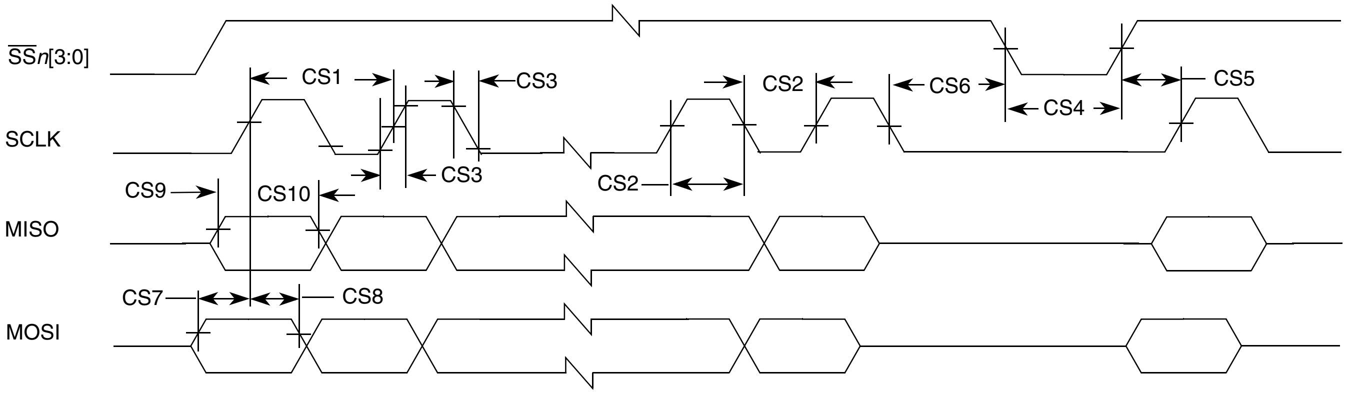

SSn[3:0]
CS1
CS3
CS2
CS6
CS5
CS4
SCLK
CS3
CS9
CS10
CS2
MISO
CS7
CS8
MOSI

Figure 8. CSPI Slave Mode Timing Diagram

Table 27. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
CS1	SCLK cycle time	t_{clk}	60	—	ns
CS2	SCLK high or low time	t_{SW}	30	—	ns
CS3	SCLK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{\text{SS}}$*n*[3:0] pulse width	t_{CSLH}	30	—	ns
CS5	$\overline{\text{SS}}$*n*[3:0] lead time (CS setup time)	t_{SCS}	30	—	ns
CS6	$\overline{\text{SS}}$*n*[3:0] lag time (CS hold time)	t_{HCS}	30	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns

Table 27. CSPI Interface Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
CS10	MISO hold time	t_{Hmiso}	5	—	ns
CS11	$\overline{\text{SPI\_RDY}}$ setup time	t_{SDRY}	5	—	ns

4.9.3 DPLL Electrical Specifications

There are three PLLs inside the i.MX35, all based on the same PLL design. The reference clock for these PLLs is normally generated from an external 24-MHz crystal connected to an internal oscillator via EXTAL24M and XTAL24 pins. It is also possible to connect an external 24-MHz clock directly to EXTAL24M, bypassing the internal oscillator.

DPLL specifications are listed in Table 28.

Table 28. DPLL Specifications

Parameter	Min.	Typ.	Max.	Unit	Comments
Reference clock frequency	10	24	100	MHz	
Max. allowed reference clock phase noise	—	—	0.03 0.01 0.15	2 Tdck[1]	Fmodulation < 50 kHz 50 kHz < Fmodulation 300 Hz Fmodulation > 300 KHz
Frequency lock time (FOL mode or non-integer MF)	—	—	80	µs	—
Phase lock time	—	—	100	µs	—
Max. allowed PL voltage ripple	—	—	150 100 150	mV	Fmodulation < 50 kHz 50 kHz < Fmodulation 300 Hz Fmodulation > 300 KHz

[1] There are two PLL are used in the i.MX35, MPLL and PPLL. Both are based on same DPLL design.

If crystals are used instead of external oscillators, they should meed the following specifications:

Table 29. Clock Input Tolerance

Parameters	OSC24M	OSC_AUDIO
Normal Frequency	24 MHz	25.576 MHz
Frequency Tolerance	30 ppm	20 ppm (high quality)
ESR	<80 Ω	<80 Ω
Load Capacitance	8 pF-12 pF	8 pF-12 pF
Shunt capacitance	<7 pF	<7 pF
Level of drive	>150 µW	>150 µW

4.9.4 Embedded Trace Macrocell (ETM) Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a test point access (TPA) that supports TRACECLK frequencies up to 133 MHz.

Figure 9 depicts the TRACECLK timings of ETM, and Table 30 lists the timing parameters.

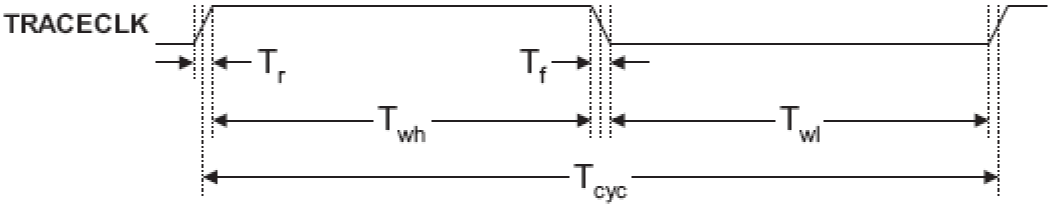


Figure 9. ETM TRACECLK Timing Diagram

Table 30. ETM TRACECLK Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 10 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 31 lists the timing parameters.

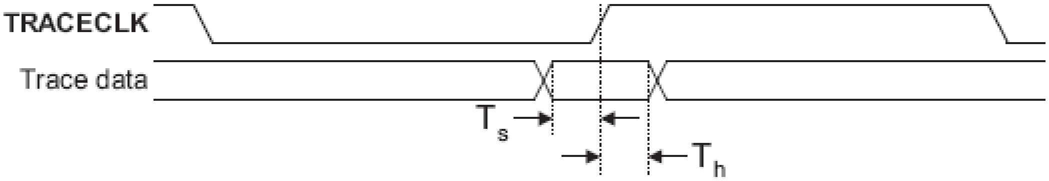


Figure 10. Trace Data Timing Diagram

Table 31. ETM Trace Data Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.9.4.1 Half-Rate Clocking Mode

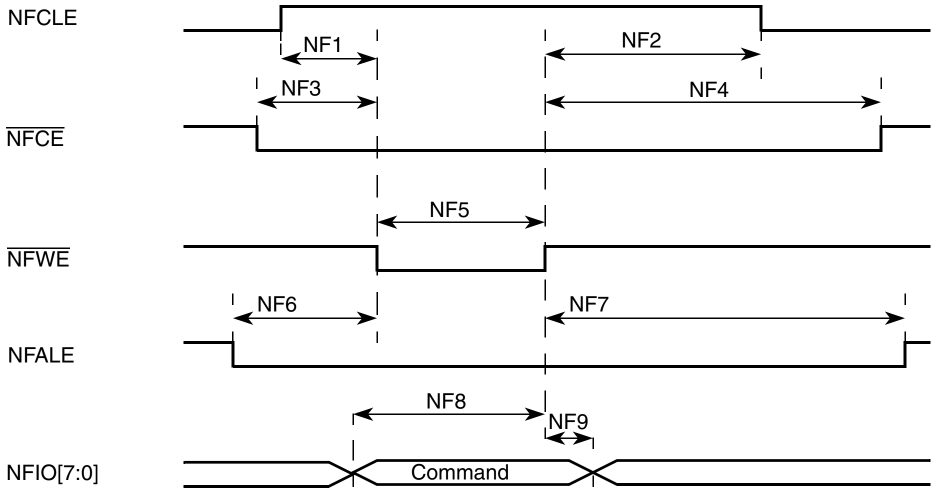
When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 10. The same T_s and T_h parameters from Table 31 still apply with respect to the falling edge of the TRACECLK signal.

4.9.5 EMI Electrical Specifications

This section provides electrical parametrics and timing for the EMI module.

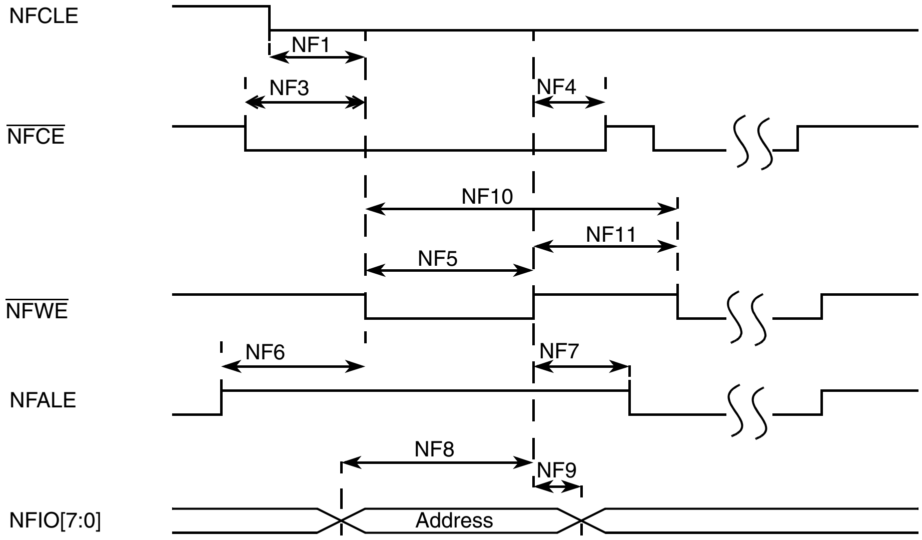
4.9.5.1 NAND Flash Controller Interface (NFC)

The i.MX35 NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{\text{RE}}$ and $\overline{\text{WE}}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 11, Figure 12, Figure 13, and Figure 14 depict the relative timing requirements among different signals of the NFC at module level for normal mode. Table 32 lists the timing parameters.



NFCLE
NF1
NF2
NF3
NF4
NFCE
NF5
NFWE
NF6
NF7
NFALE
NF8
NF9
NFIO[7:0]
Command

Figure 11. Command Latch Cycle Timing DIagram



NFCLE
NF1
NF3
NF4
NFCE
NF10
NF11
NF5
NFWE
NF6
NF7
NFALE
NF8
NF9
NFIO[7:0]
Address

Figure 12. Address Latch Cycle Timing DIagram

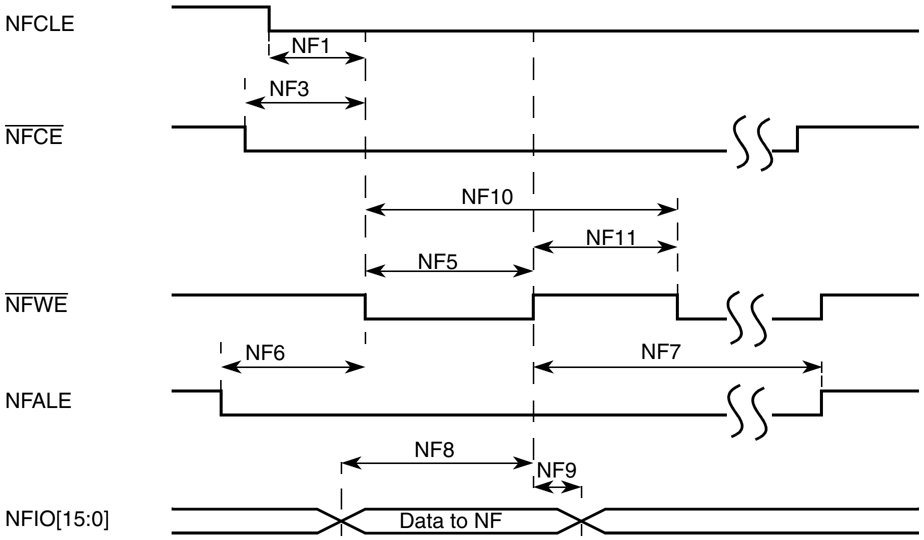

NFCLE
NF1
NF3
NFCE
NF10
NF11
NF5
NFWE
NF6
NF7
NFALE
NF8
NF9
NFIO[15:0]
Data to NF

Figure 13. Write Data Latch Cycle Timing Dlagram

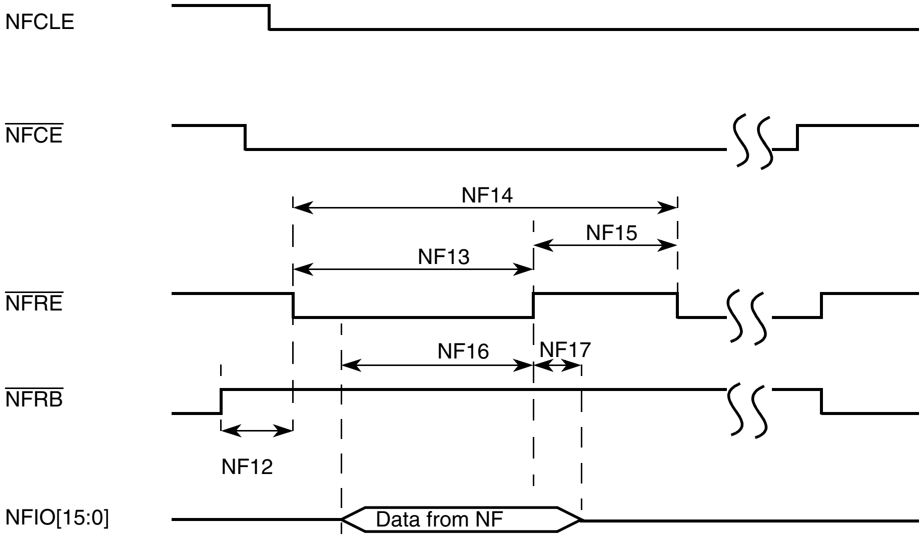

NFCLE
NFCE
NF14
NF15
NF13
NFRE
NF16
NF17
NFRB
NF12
NFIO[15:0]
Data from NF

Figure 14. Read Data Latch Cycle Timing Dlagram

Table 32. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T – 4.0 ns	—	26	—	ns
NF2	NFCLE hold time	tCLH	T – 5.0 ns	—	25	—	ns
NF3	$\overline{\text{NFCE}}$ setup time	tCS	T – 2.0 ns	—	28	—	ns
NF4	$\overline{\text{NFCE}}$ hold time	tCH	T – 1.0 ns	—	29	—	ns

Table 32. NFC Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{\text{NF\_WP}}$ pulse width	tWP	T – 1.0 ns		29		ns
NF6	NFALE setup time	tALS	T – 4.0 ns	—	26	—	ns
NF7	NFALE hold time	tALH	T – 4.5 ns	—	25.5	—	ns
NF8	Data setup time	tDS	T – 2.0 ns	—	28	—	ns
NF9	Data hold time	tDH	T – 5.0 ns	—	25	—	ns
NF10	Write cycle time	tWC	2T – 3.0 ns		57		ns
NF11	$\overline{\text{NFWE}}$ hold time	tWH	T – 5.0 ns		25		ns
NF12	Ready to $\overline{\text{NFRE}}$ low	tRR	6T	—	180	—	ns
NF13	$\overline{\text{NFRE}}$ pulse width	tRP	1.5T – 1.0 ns	—	44	—	ns
NF14	READ cycle time	tRC	2T – 5.5 ns	—	54.5	—	ns
NF15	$\overline{\text{NFRE}}$ high hold time	tREH	0.5T – 4.0 ns		11	—	ns
NF16	Data setup on READ	tDSR	N/A		9	—	ns
NF17	Data hold on READ	tDHR	N/A		0	—	ns

[1] The flash clock maximum frequency is 50 MHz.

[2] Subject to DPLL jitter specification listed in Table 28, "DPLL Specifications," on page 32.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.9.5.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clocks related to the BCLK rising edge or falling edge according to the corresponding assertion or negation control fields. The address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration.

Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 15 depicts the timing of the WEIM module, and Table 33 lists the timing parameters.

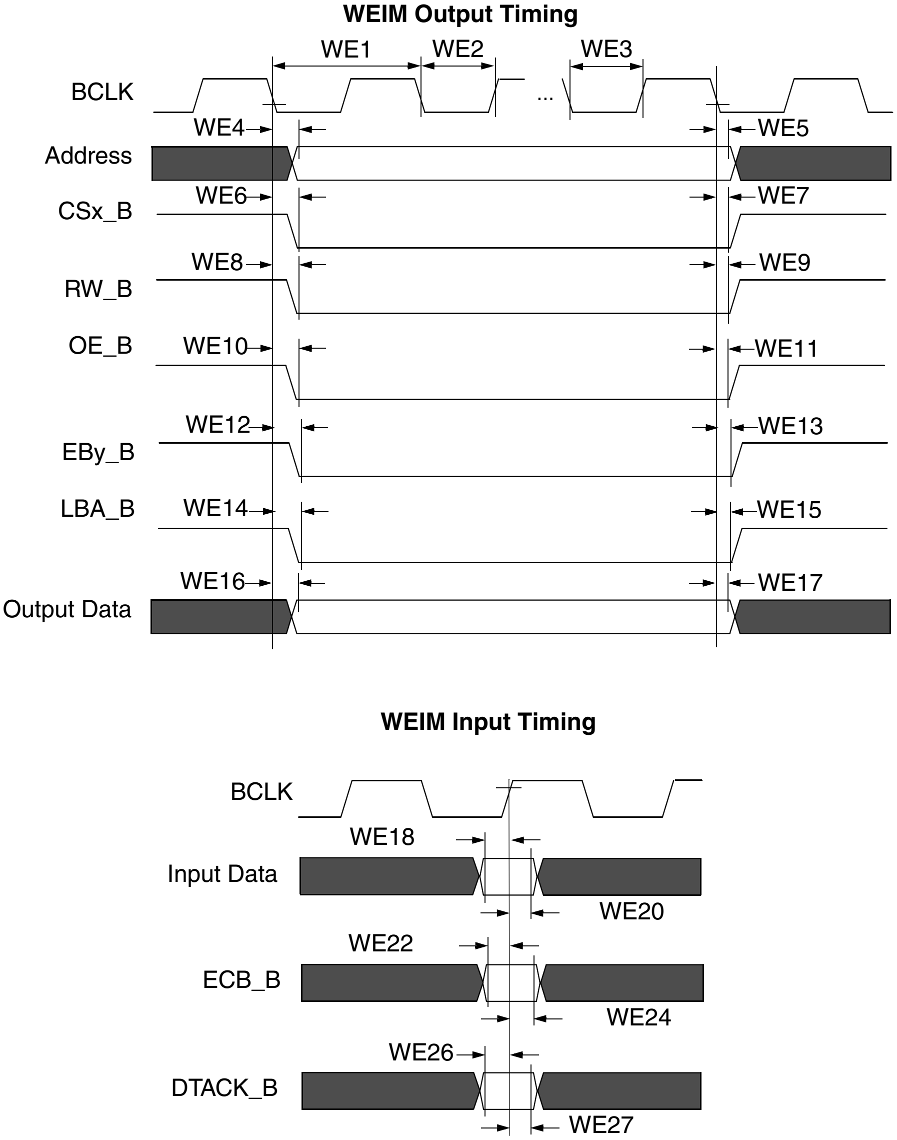

WEIM Output Timing
WE1
WE2
WE3
BCLK
...
WE4
WE5
Address
WE6
WE7
CSx_B
WE8
WE9
RW_B
OE_B
WE10
WE11
WE12
WE13
EBy_B
LBA_B
WE14
WE15
WE16
WE17
Output Data
WEIM Input Timing
BCLK
WE18
Input Data
WE20
WE22
ECB_B
WE24
WE26
DTACK_B
WE27

Figure 15. WEIM Bus Timing Diagram

Table 33. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Address valid to Clock rise/fall	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to CSx_B valid	15	19	ns
WE7	Clock rise/fall to CSx_B invalid	3.6	5	ns
WE8	Clock rise/fall to RW_B valid	8	12	ns
WE9	Clock rise/fall to RW_B invalid	3	8	ns
WE10	Clock rise/fall to OE_B valid	7	12	ns
WE11	Clock rise/fall to OE_B invalid	3.8	5.5	ns
WE12	Clock rise/fall to EBy_B valid	6	11.5	ns
WE13	Clock rise/fall to EBy_B invalid	6	10	ns
WE14	Clock rise/fall to LBA_B valid	17.5	20	ns
WE15	Clock rise/fall to LBA_B invalid	0	1	ns
WE16	Clock rise/fall to Output Data valid	5	10	ns
WE17	Clock rise to Output Data invalid	0	2.5	ns
WE18	Input Data Valid to Clock rise[3]	1	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is ECB_B asserted during access)	(BCLK/2) + 3.01	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is NO ECB_B asserted during access)	6.9	—	ns
WE20	Clock rise to Input Data invalid[3]	1	—	ns
WE22	ECB_B setup time[3]	5	—	ns
WE24	ECB_B hold time[3]	0	—	ns
WE26	DTACK_B setup time	5.4	—	ns
WE27	DTACK_B hold time	–3.2	—	ns

[1] “High” is defined as 80% of signal value, and “low” is defined as 20% of signal value.

[2] BCLK parameters are measured from the 50% point. For example, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

[3] Parameters W18, W20, W22, and W24 are tested when FCE=1. i.MX35 does not support FCE=0.

NOTE

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is set to maximum drive.

Recommended drive strength for all controls, address and BCLK is set to maximum drive.

Figure 16 through Figure 21 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

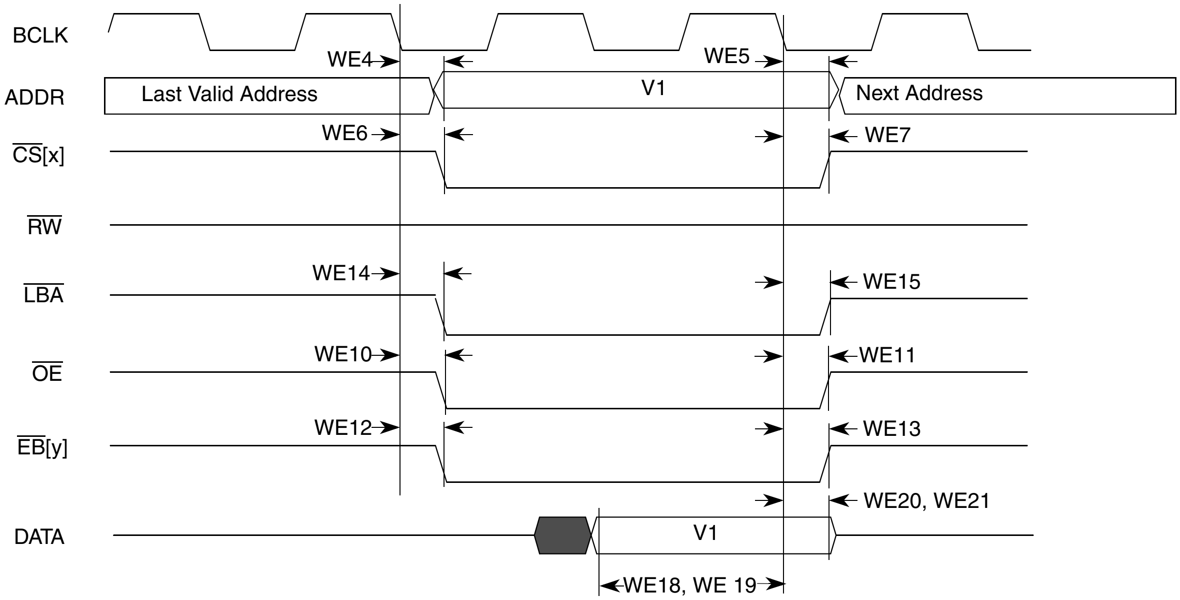

BCLK
ADDR
CS[x]
RW
LBA
OE
EB[y]
DATA
WE4
WE5
Last Valid Address
V1
Next Address
WE6
WE7
WE14
WE15
WE10
WE11
WE12
WE13
WE20, WE21
V1
WE18, WE 19

Figure 16. Synchronous Memory Timing Diagram for Read Access—WSC = 1

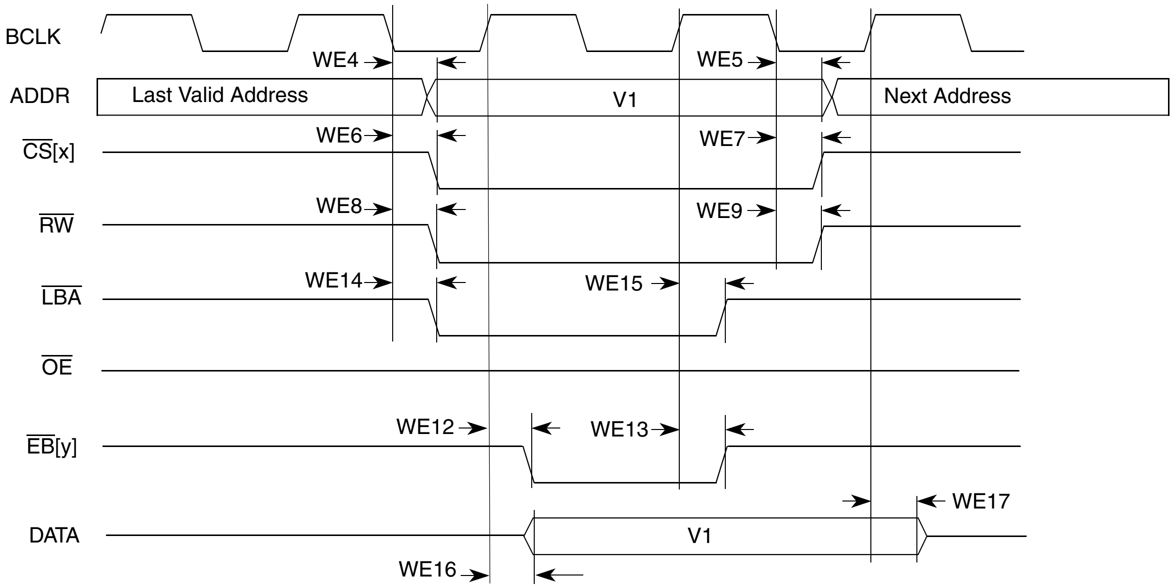

BCLK
ADDR
CS[x]
RW
LBA
OE
EB[y]
DATA
WE4
WE5
Last Valid Address
V1
Next Address
WE6
WE7
WE8
WE9
WE14
WE15
WE12
WE13
WE17
V1
WE16

Figure 17. Synchronous Memory Timing Diagram for Write Access—WSC = 1, EBWA = 1, EBWN = 1, LBN = 1

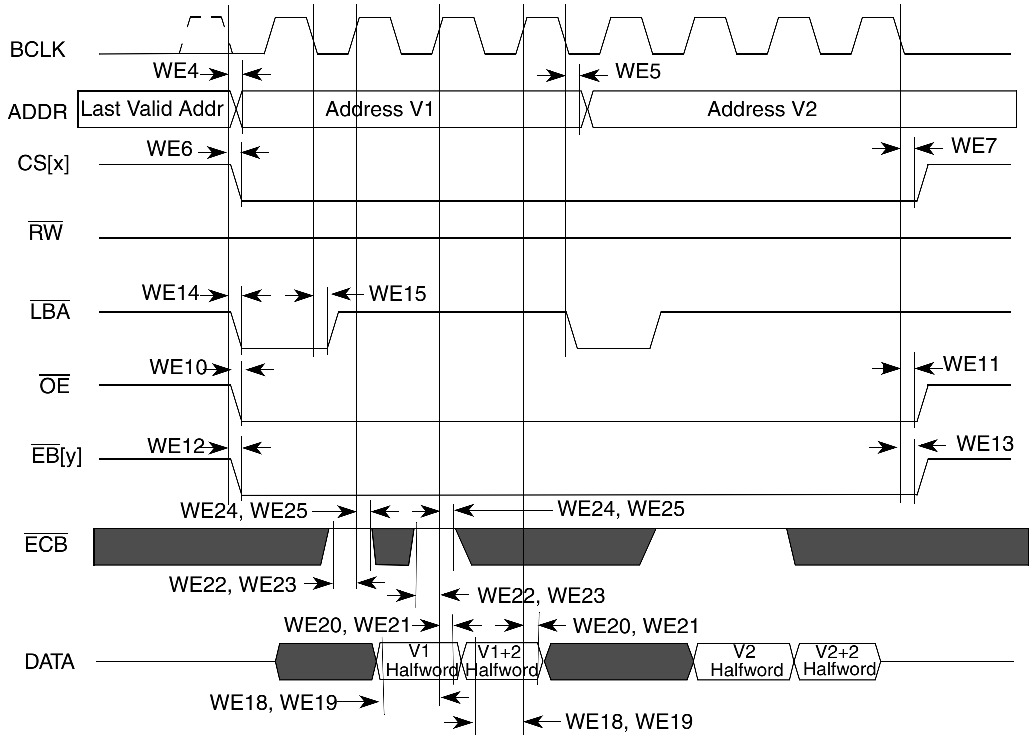

BCLK
ADDR
CS[x]
RW
LBA
OE
EB[y]
ECB
DATA
WE4
WE5
Last Valid Addr
Address V1
Address V2
WE6
WE7
WE14
WE15
WE10
WE11
WE12
WE13
WE24, WE25
WE24, WE25
WE22, WE23
WE22, WE23
WE20, WE21
WE20, WE21
V1 Halfword
V1+2 Halfword
V2 Halfword
V2+2 Halfword
WE18, WE19
WE18, WE19

Figure 18. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses— WSC = 2, SYNC = 1, DOL = 0

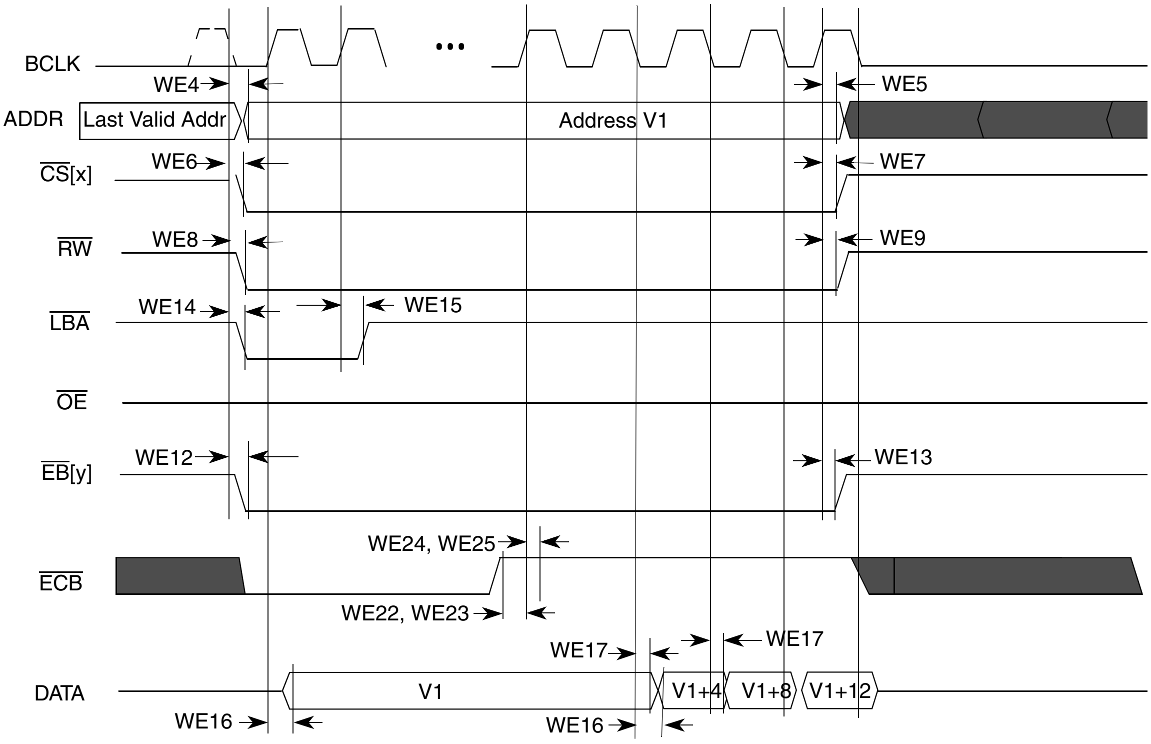

BCLK
ADDR
CS[x]
RW
LBA
OE
EB[y]
ECB
DATA
WE4
WE5
Last Valid Addr
Address V1
WE6
WE7
WE8
WE9
WE14
WE15
WE12
WE13
WE24, WE25
WE22, WE23
WE17
WE17
V1
V1+4
V1+8
V1+12
WE16
WE16

Figure 19. Synchronous Memory TIming Diagram for Burst Write Access— BCS = 1, WSC = 4, SYNC = 1, DOL = 0, PSR = 1

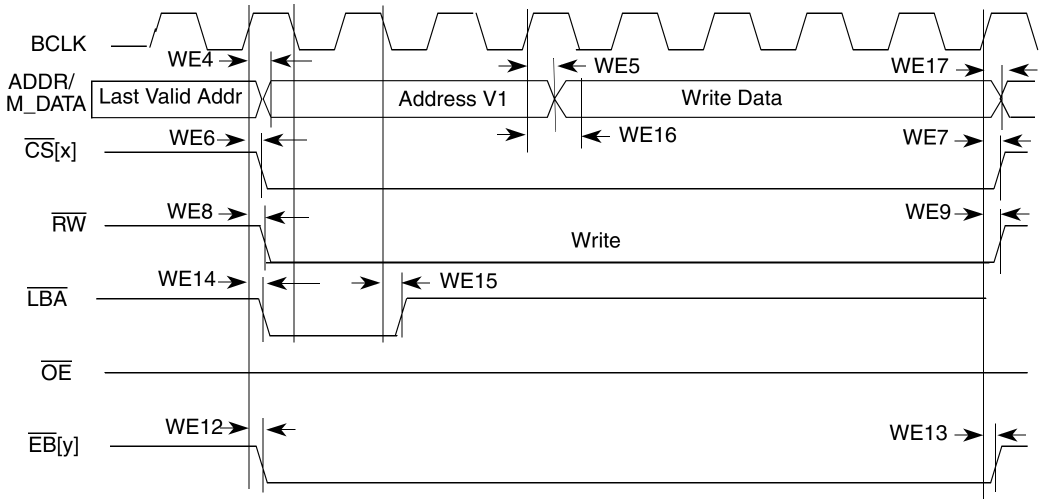

BCLK
ADDR/
M_DATA
Last Valid Addr
Address V1
Write Data
CS[x]
RW
Write
LBA
OE
EB[y]
WE4
WE5
WE17
WE6
WE16
WE7
WE8
WE9
WE14
WE15
WE12
WE13

Figure 20. Muxed A/D Mode Timing Diagram for Synchronous Write Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1

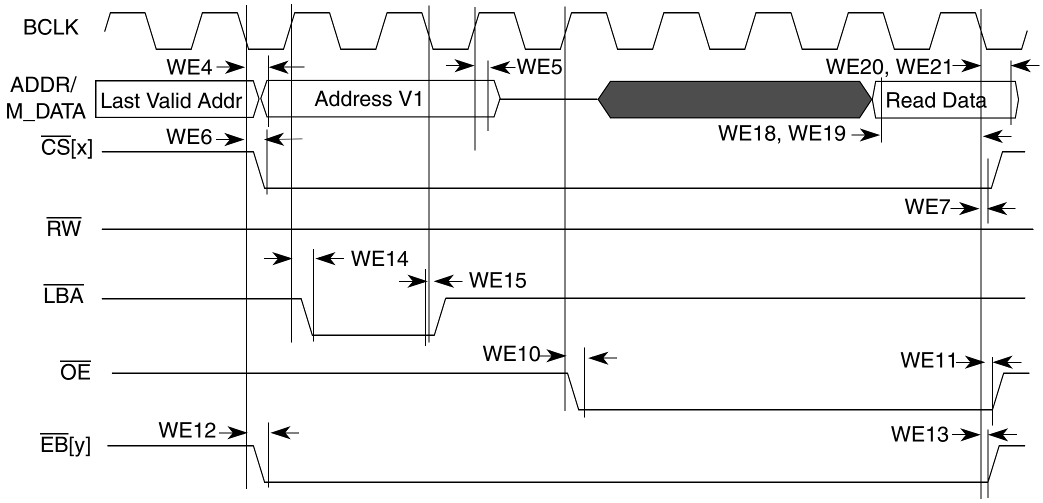
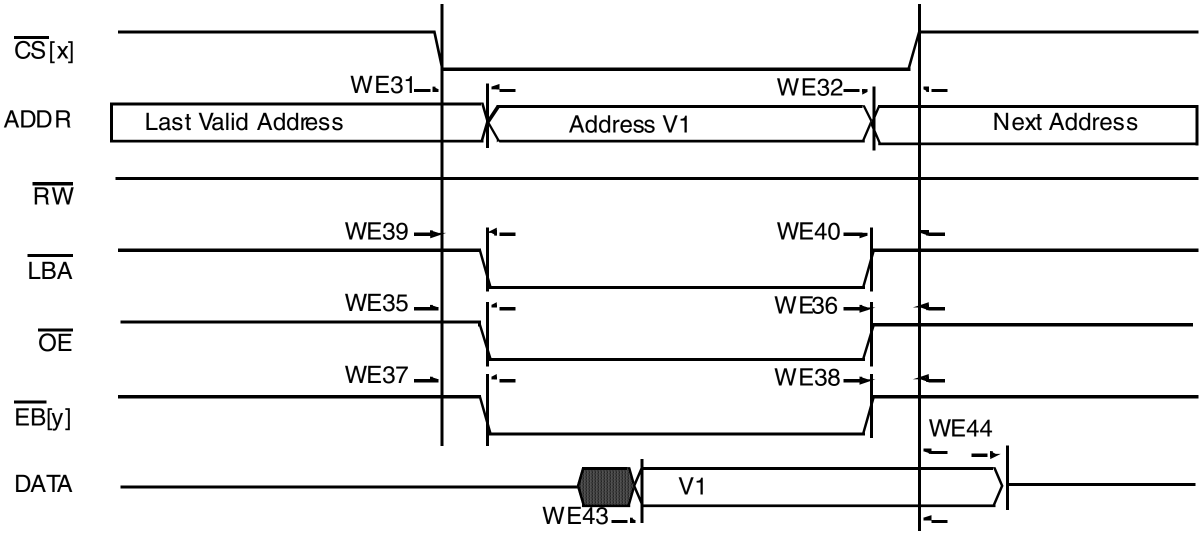

BCLK
ADDR/
M_DATA
Last Valid Addr
Address V1
Read Data
CS[x]
RW
LBA
OE
EB[y]
WE4
WE5
WE20, WE21
WE6
WE18, WE19
WE7
WE14
WE15
WE10
WE11
WE12
WE13

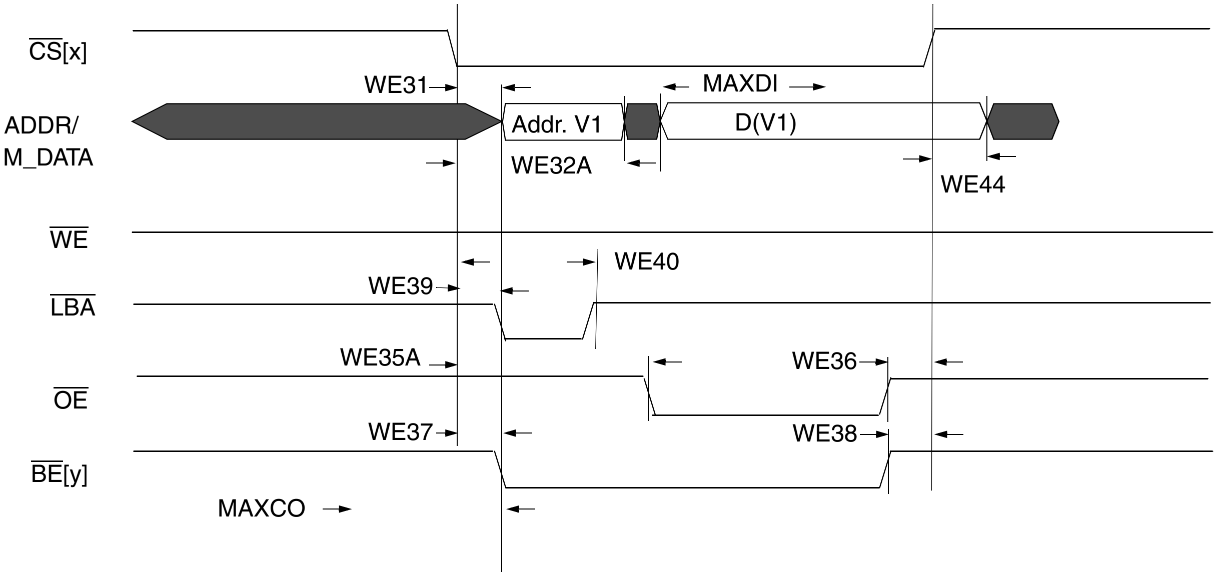
Figure 21. Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7

Figure 22 through Figure 26, and Table 34 help to determine timing parameters relative chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.



CS[x]
ADDR
RW
LBA
OE
EB[y]
DATA
WE31
WE32
Last Valid Address
Address V1
Next Address
WE39
WE40
WE35
WE36
WE37
WE38
WE44
V1
WE43

Figure 22. Asynchronous Memory Read Access



CS[x]
ADDR/
M_DATA
WE
LBA
OE
BE[y]
WE31
MAXDI
Addr. V1
D(V1)
WE32A
WE44
WE40
WE39
WE35A
WE36
WE37
WE38
MAXCO

Figure 23. Asynchronous A/D muxed Read Access (RWSC = 5)

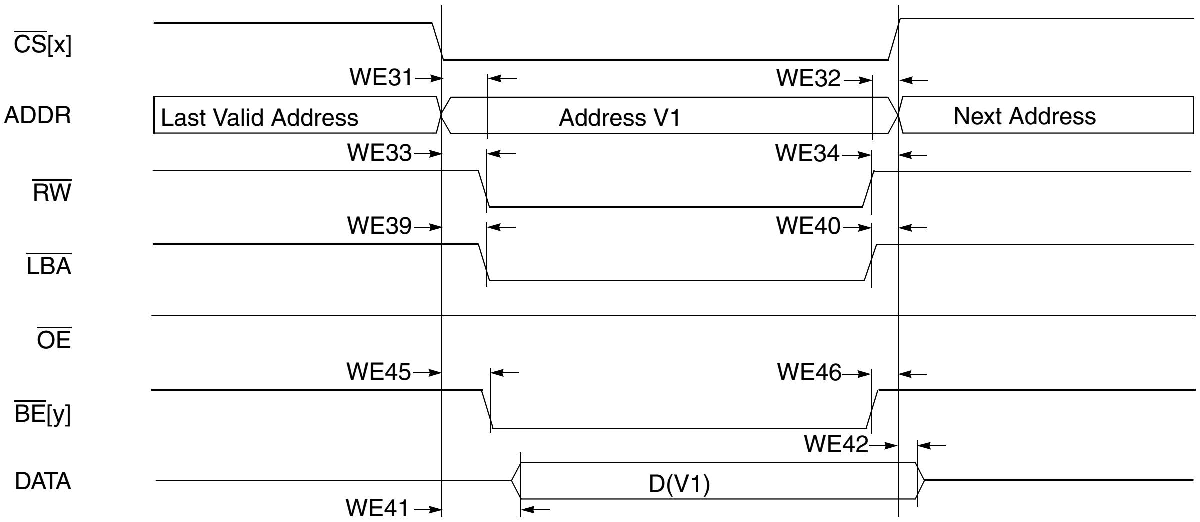

CS[x]
ADDR
RW
LBA
OE
BE[y]
DATA
WE31
WE32
Last Valid Address
Address V1
Next Address
WE33
WE34
WE39
WE40
WE45
WE46
WE42
D(V1)
WE41

Figure 24. Asynchronous Memory Write Access

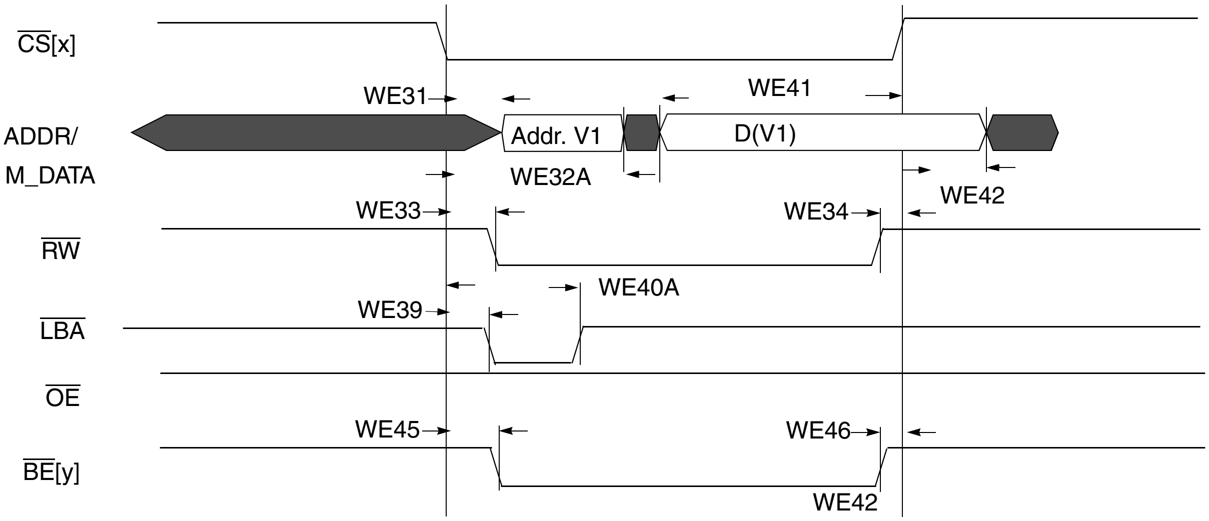
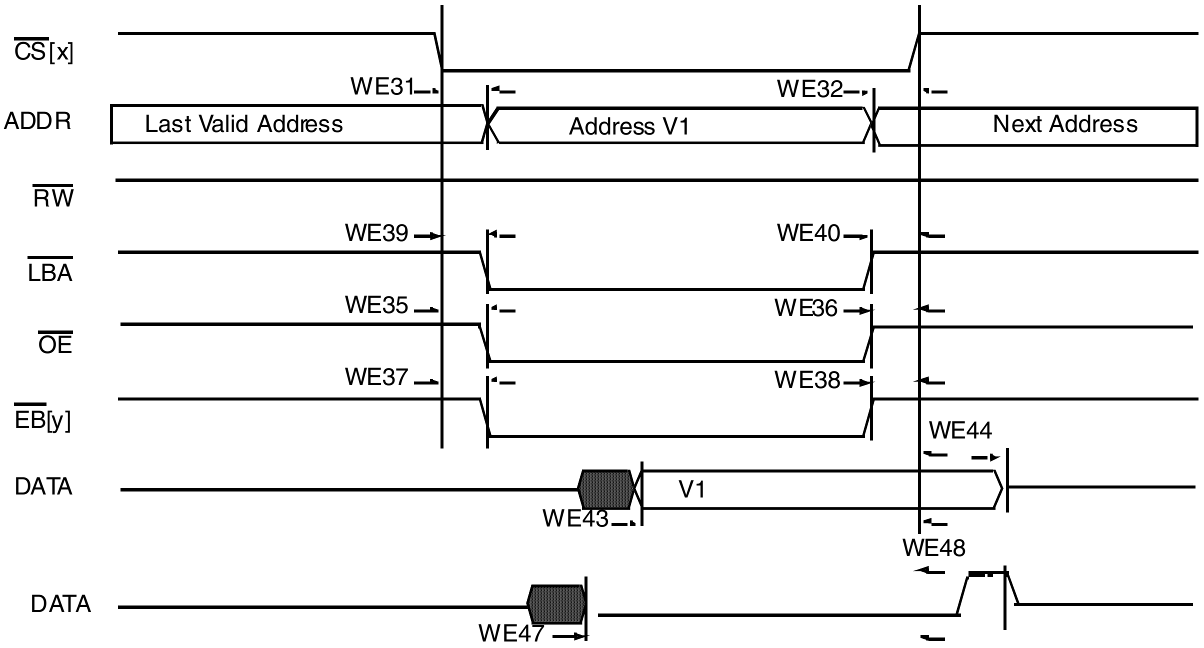

CS[x]
WE31
WE41
ADDR/
M_DATA
Addr. V1
D(V1)
WE32A
WE42
WE33
WE34
RW
WE40A
WE39
LBA
OE
WE45
WE46
BE[y]
WE42

Figure 25. Asynchronous A/D Mux Write Access



$\overline{CS}$[x]
ADDR
$\overline{RW}$
$\overline{LBA}$
$\overline{OE}$
$\overline{EB}$[y]
DATA
DATA
WE31
WE32
Last Valid Address
Address V1
Next Address
WE39
WE40
WE35
WE36
WE37
WE38
WE44
V1
WE43
WE48
WE47

Figure 26. DTACK Read Access

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}$[x] valid to Address valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address invalid to $\overline{CS}$[x] invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns
WE32A(muxed A/D	$\overline{CS}$[x] valid to address invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] valid to $\overline{WE}$ valid	WE8 – WE6 + (WEA – CSA)	—	3 + (WEA – CSA)	ns
WE34	$\overline{WE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	–3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	ns
WE36	$\overline{OE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] valid to $\overline{BE}$[y] valid (read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	$\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	$\overline{CS}$[x] valid to $\overline{LBA}$ valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE15 – CSN	—	3 – CSN	ns

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE40A (muxed A/D)	$\overline{\text{CS}}$[x] valid to $\overline{\text{LBA}}$ invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{\text{CS}}$[x] valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE41A (muxed A/D)	$\overline{\text{CS}}$[x] valid to Output Data valid	WE16 – WE6 + (WLBN + WLBA + ADH + 1 – WCSA)	—	3 + (WLBN + WLBA + ADH + 1 – WCSA)	ns
WE42	Output Data invalid to $\overline{\text{CS}}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to $\overline{\text{CS}}$[x] invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{\text{CS}}$[x] invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{\text{CS}}$[x] valid to $\overline{\text{BE}}$[y] valid (write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	$\overline{\text{BE}}$[y] invalid to $\overline{\text{CS}}$[x] invalid (write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	$\overline{\text{DTACK}}$ valid to $\overline{\text{CS}}$[x] invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{\text{CS}}$[x] Invalid to $\overline{\text{DTACK}}$ invalid	0	0	—	ns

[1] For the value of parameters WE4–WE21, see column BCD = 0 in Table 33.

[2] $\overline{\text{CS}}$ Assertion. This bit field determines when the $\overline{\text{CS}}$ signal is asserted during read/write cycles.

[3] $\overline{\text{CS}}$ Negation. This bit field determines when the $\overline{\text{CS}}$ signal is negated during read/write cycles.

[4] $\overline{\text{BE}}$ Assertion. This bit field determines when the $\overline{\text{BE}}$ signal is asserted during read cycles.

[5] $\overline{\text{BE}}$ Negation. This bit field determines when the $\overline{\text{BE}}$ signal is negated during read cycles.

[6] Output maximum delay from internal driving ADDR/control FFs to chip outputs.

[7] Output maximum delay from $\overline{\text{CS}}$[x] internal driving FFs to $\overline{\text{CS}}$[x] out.

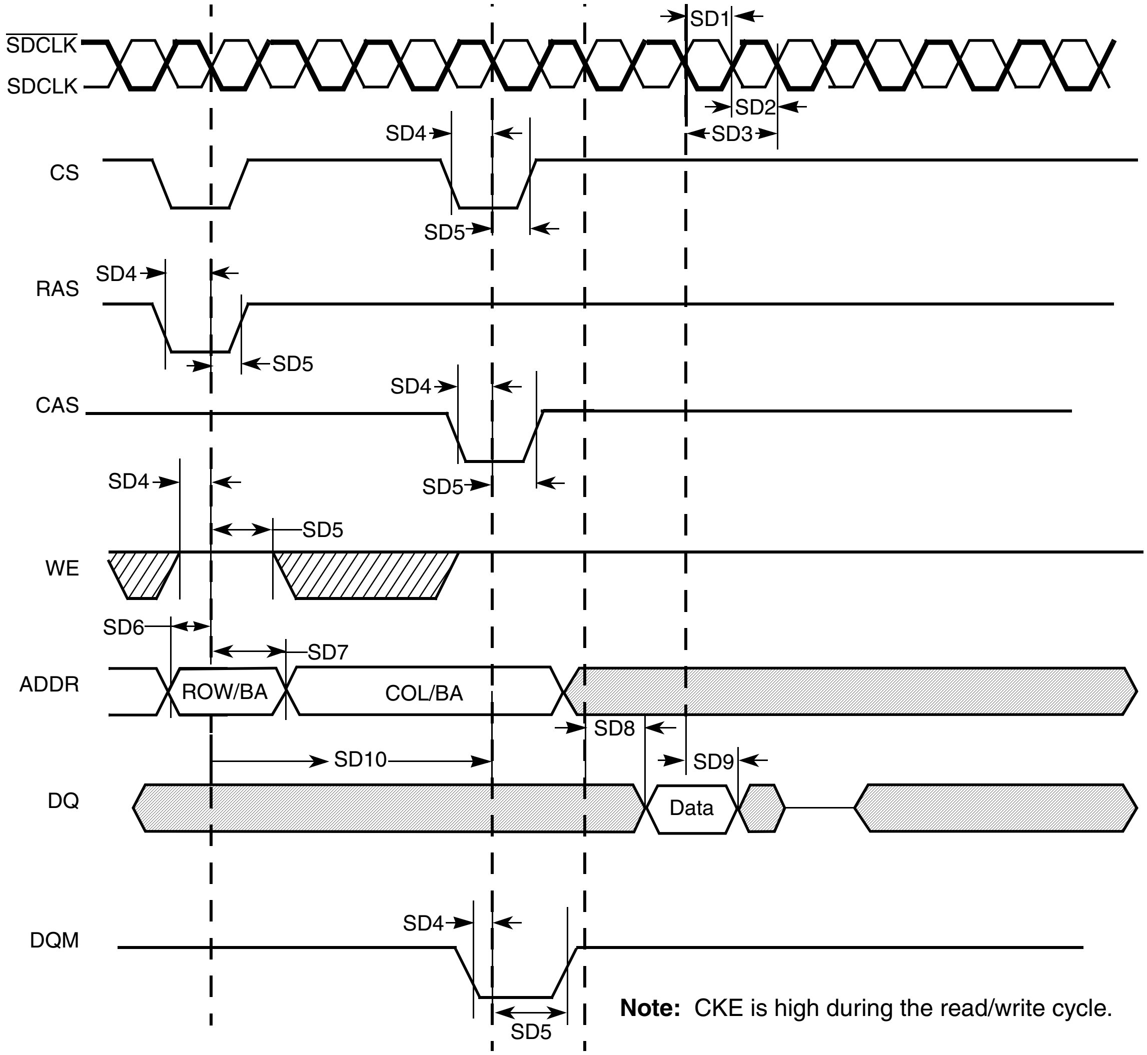
[8] DATA maximum delay from chip input data to its internal FF.

[9] DTACK maximum delay from chip dtack input to its internal FF.

Note: All configuration parameters (CSA, CSN, WBEA, WBEN, LBA, LBN, OEN, OEA, RBEA, and RBEN) are in cycle units.

4.9.5.3 ESDCTL Electrical Specifications

Figure 27 through Figure 35 depict the timings pertaining to the ESDCTL module, which interfaces with mobile DDR or SDR SDRAM. Table 35 through Table 45 list the timing parameters.


SD1
SDCLK
SDCLK
SD2
SD3
SD4
CS
SD5
SD4
RAS
SD5
SD4
CAS
SD4
SD5
SD5
WE
SD6
SD7
ADDR
ROW/BA
COL/BA
SD8
SD9
SD10
DQ
Data
DQM
SD4
SD5

Note: CKE is high during the read/write cycle.

Figure 27. SDRAM Read Cycle Timing Diagram

Table 35. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.0	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns

Table 35. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns
SD9	Data out hold time[1]	tOH	1.2	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 44 and Table 45.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

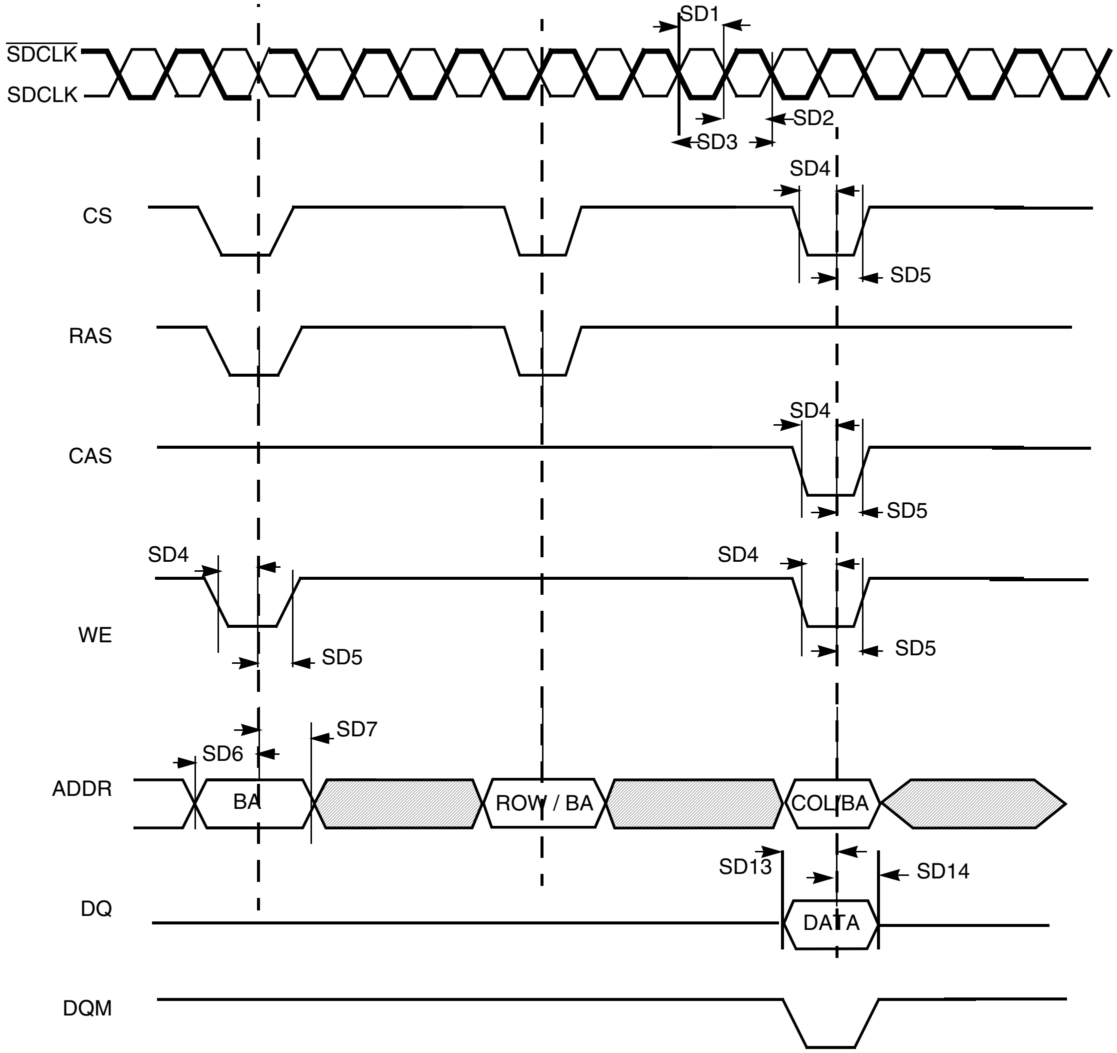

SD1
SDCLK
SDCLK
SD2
SD3
SD4
CS
SD5
RAS
SD4
CAS
SD5
SD4
SD4
WE
SD5
SD5
SD7
SD6
ADDR
BA
ROW / BA
COL/BA
SD13
SD14
DQ
DATA
DQM

Figure 28. SDR SDRAM Write Cycle Timing Diagram

Table 36. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	0.45	0.55	ns
SD2	$\overline{\text{SDRAM}}$ clock low-level width	tCL	0.45	0.55	ns
SD3	SDRAM clock cycle time	tCK	7.0	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.4	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.4	—	ns
SD6	Address setup time	tAS	2.4	—	ns
SD7	Address hold time	tAH	1.4	—	ns
SD13	Data setup time	tDS	2.4	—	ns
SD14	Data hold time	tDH	1.4	—	ns

NOTE

Test conditions are: pin voltage 1.7 V–1.95 V, capacitance 15 pF for all pins (both DDR and non-DDR pins), drive strength is high (7.2 mA). “High” is defined as 80% of signal value and “low” is defined as 20% of signal value.

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value. tCH + tCL will not exceed 7.5 ns for 133 MHz. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

The timing parameters are similar to the ones used in SDRAM data sheets. Table 36 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

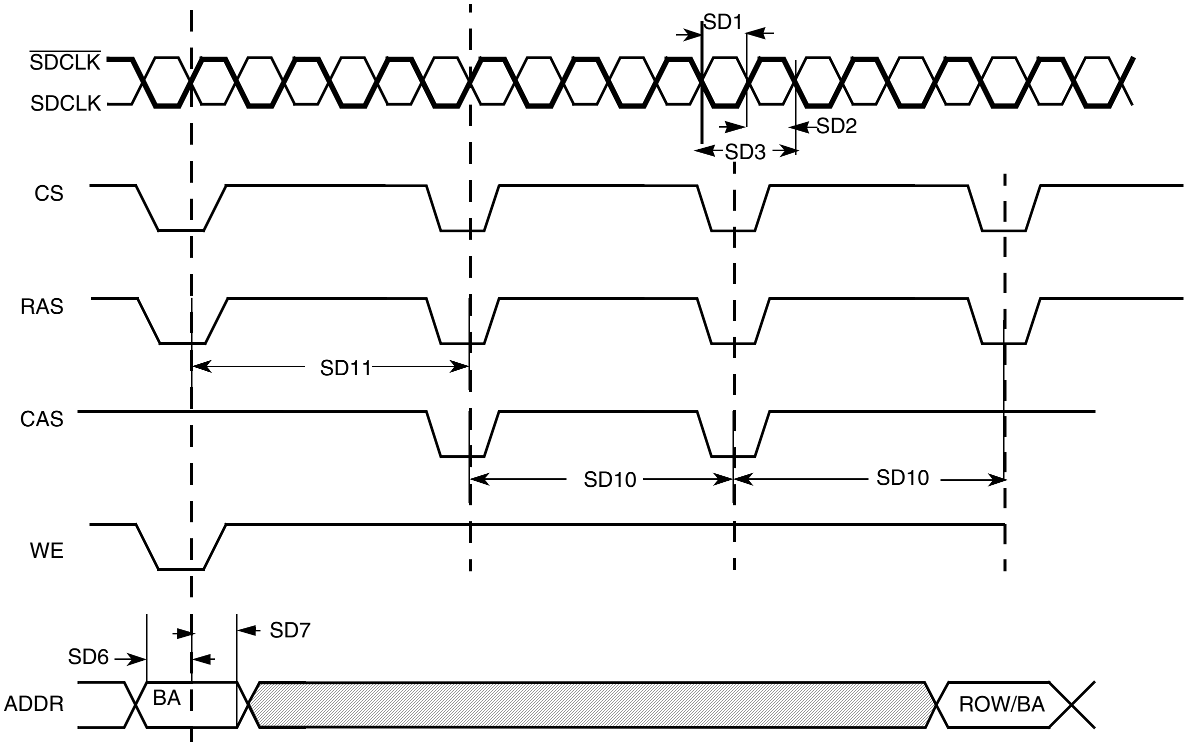


Figure 29. SDRAM Refresh Timing Diagram

Table 37. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns

Table 37. SDRAM Refresh Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

[1] SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 37 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

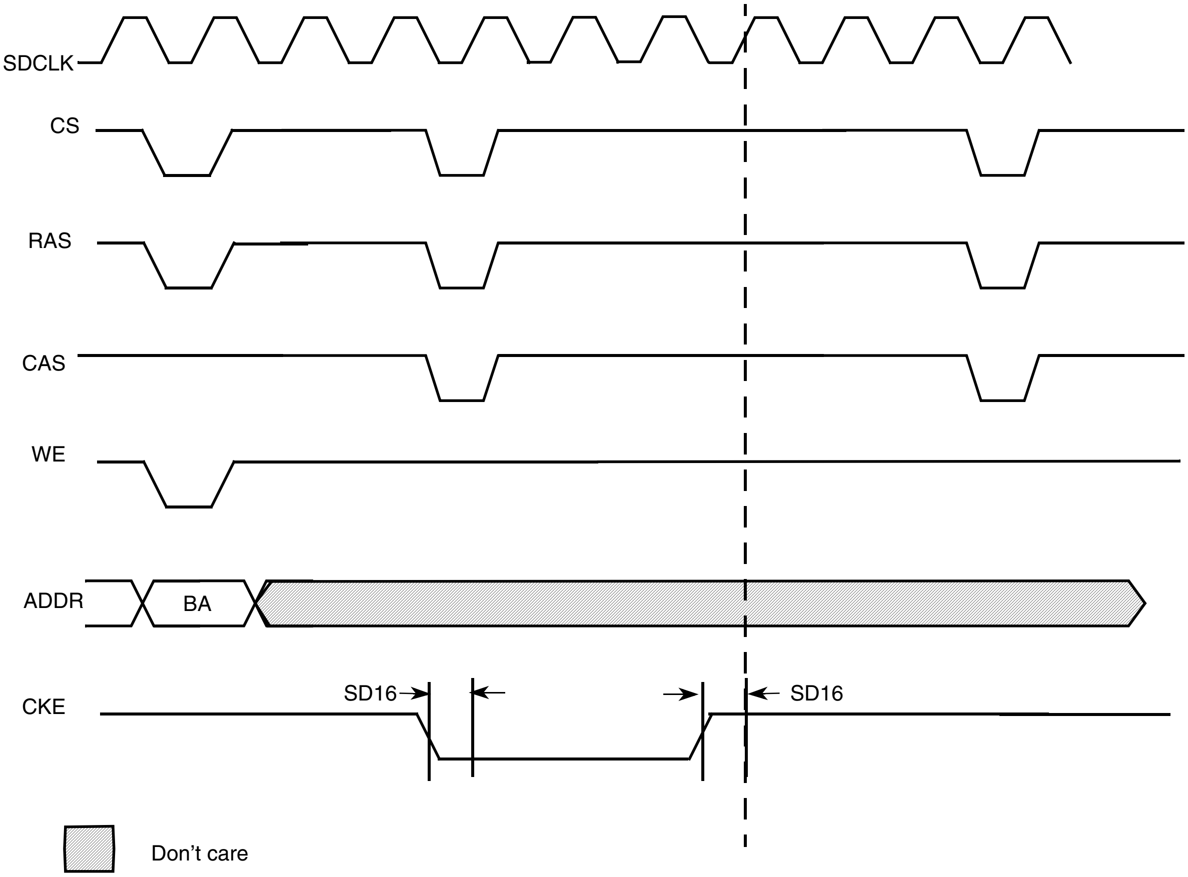


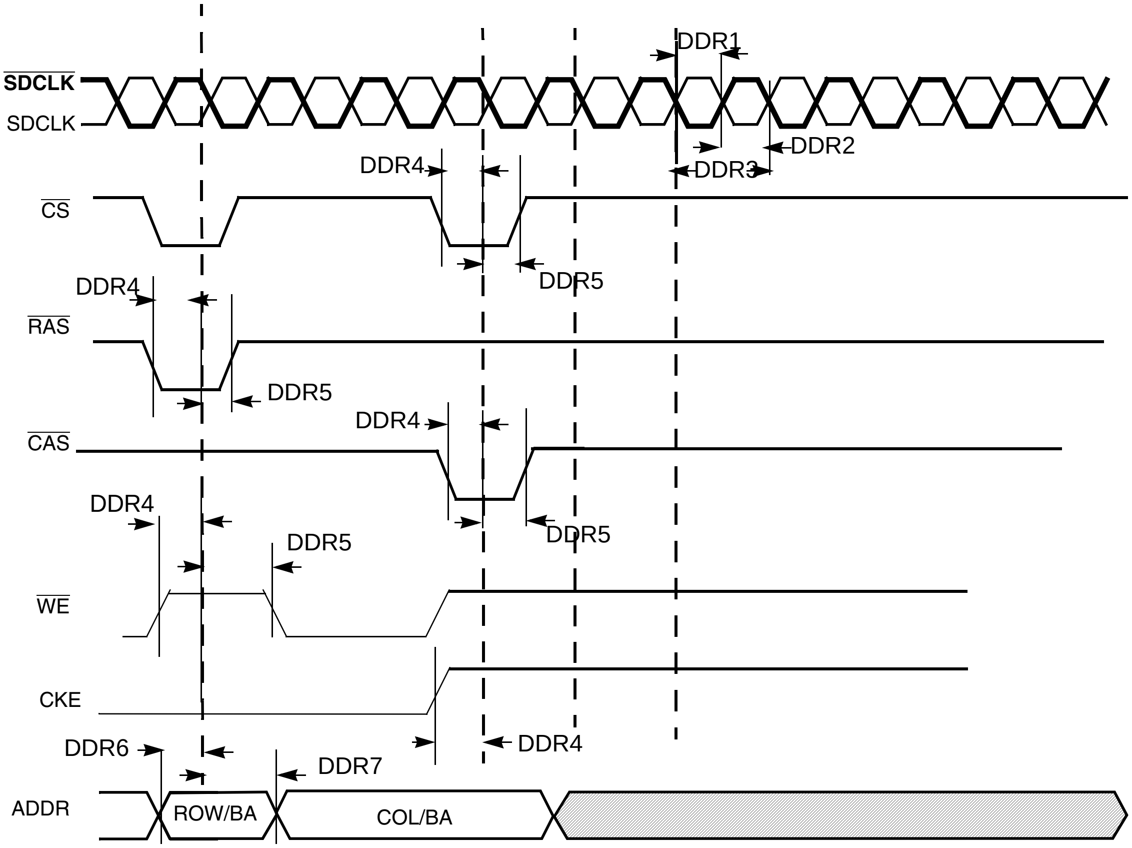
Figure 30. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 38. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns



SDCLK
SDCLK
DDR1
DDR2
DDR3
DDR4
DDR5
CS
RAS
CAS
WE
CKE
ADDR
DDR6
DDR7
ROW/BA
COL/BA

Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	tCH	0.45	0.55	tCK
DDR2	SDRAM clock low-level width	tCL	0.45	0.55	tCK
DDR3	SDRAM clock cycle time	tCK	7.0	8.0	ns
DDR4	CS, RAS, CAS, CKE, WE setup time	tIS[1]	1.5	—	ns

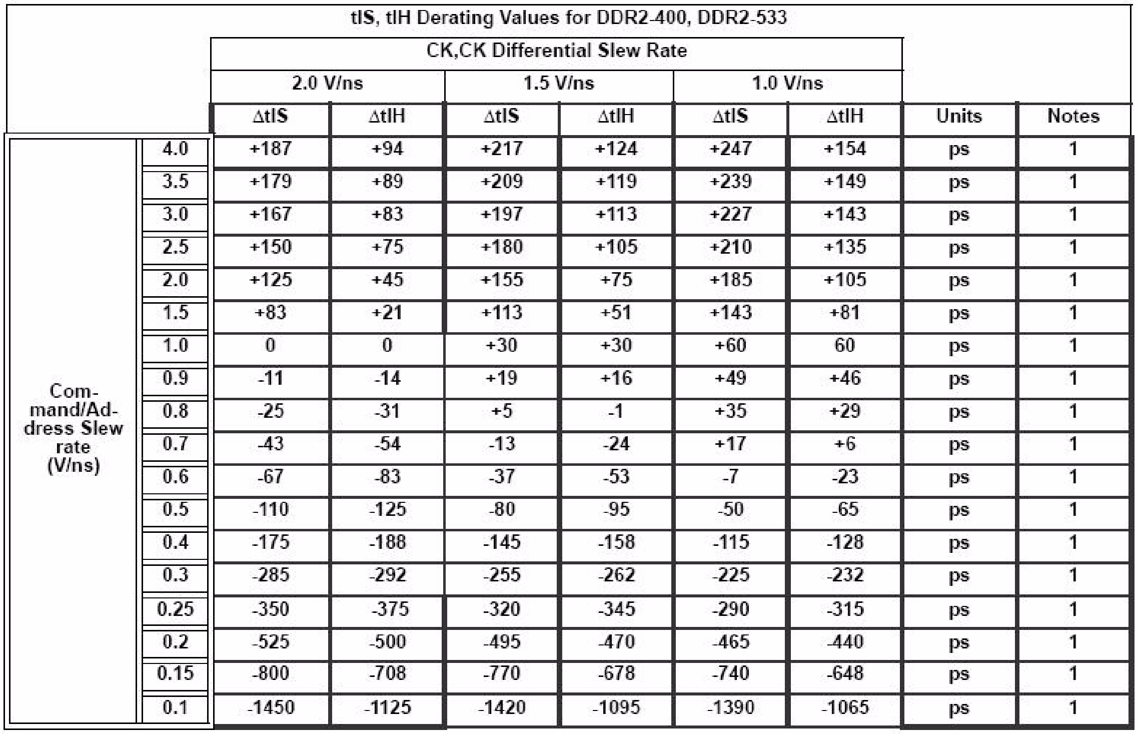
Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR5	CS, RAS, CAS, CKE, WE hold time	tIH[1]	1.25	—	ns
DDR6	Address output setup time	tIS[1]	1.5	—	ns
DDR7	Address output hold time	tIH[1]	1.5	—	ns

NOTE

These values are for command/address slew rate of 1 V/ns and SDCLK, SDCLK_B differential slew rate of 2 V/ns. For different values, use the derating table.

Table 40. Derating Values for DDR2–400, DDR2–533



tIS, tIH Derating Values for DDR2-400, DDR2-533									
		CK,CK Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Com-mand/Ad-dress Slew rate (V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps	1
	3.5	+179	+89	+209	+119	+239	+149	ps	1
	3.0	+167	+83	+197	+113	+227	+143	ps	1
	2.5	+150	+75	+180	+105	+210	+135	ps	1
	2.0	+125	+45	+155	+75	+185	+105	ps	1
	1.5	+83	+21	+113	+51	+143	+81	ps	1
	1.0	0	0	+30	+30	+60	60	ps	1
	0.9	-11	-14	+19	+16	+49	+46	ps	1
	0.8	-25	-31	+5	-1	+35	+29	ps	1
	0.7	-43	-54	-13	-24	+17	+6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1

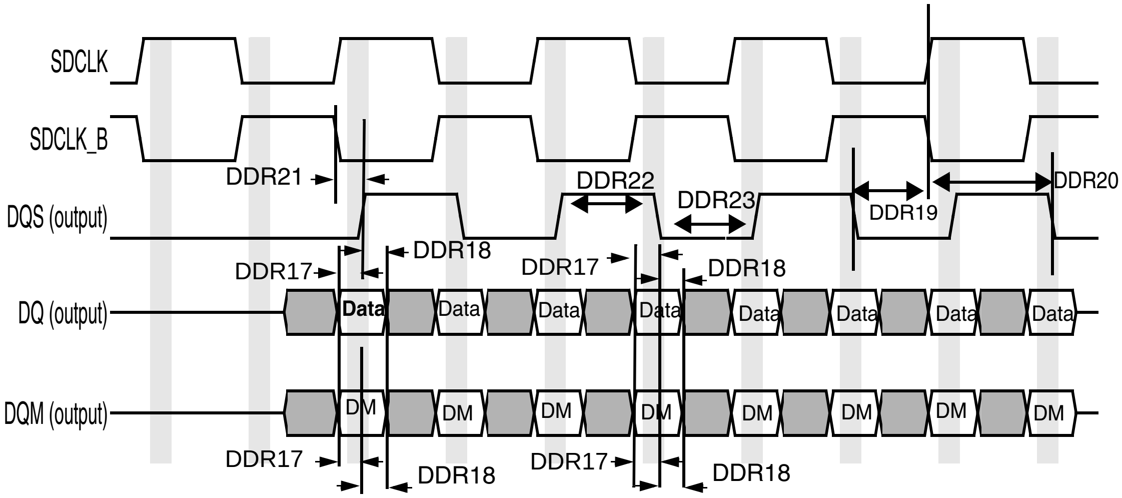

SDCLK
SDCLK_B
DQS (output)
DQ (output)
DQM (output)
DDR21
DDR22
DDR23
DDR19
DDR20
DDR17
DDR18
Data
DM

Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 41. DDR2 SDRAM Write Cycle Parameters

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (single-ended strobe)	tDS1(base)	0.5	—	ns
DDR18	DQ and DQM hold time to DQS (single-ended strobe)	tDH1(base)	0.5	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time.	tDSS	0.2	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	0.2	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	–0.25	0.25	tCK
DDR22	DQS high level width	tDQSH	0.35	—	tCK
DDR23	DQS low level width	tDQSL	0.35	—	tCK

NOTE

These values are for DQ/DM slew rate of 1 V/ns and DQS slew rate of 1 V/ns. For different values use the derating table.

Table 42. DDR Single-ended Slew Rate

ΔtDS1, ΔtDH1 derating values for DDR2-400, DDR2-533 (All units in ‘ps’; the note applies to the entire table)																			
		DQS Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1	ΔtD S1	ΔtD H1
DQ Slew rate V/ns	2.0	188	188	167	146	125	63	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-132	-181	-183	-246
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

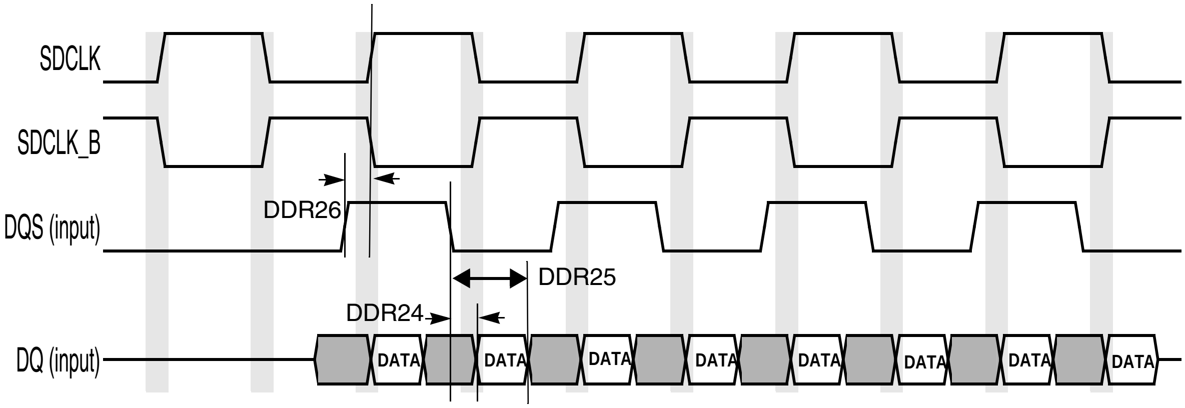


Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 43. DDR2 SDRAM Read Cycle Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR24	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS[1]	tQH	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	tDQSCK	–0.5	0.5	ns

[1] The value was calculated for an SDCLK frequency of 133 MHz by the formula tQH = tHP – tQHS = min (tCL,tCH) – tQHS = 0.45 × tCK – tQHS = 0.45 × 7.5 – 0.45 = 2.925 ns.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

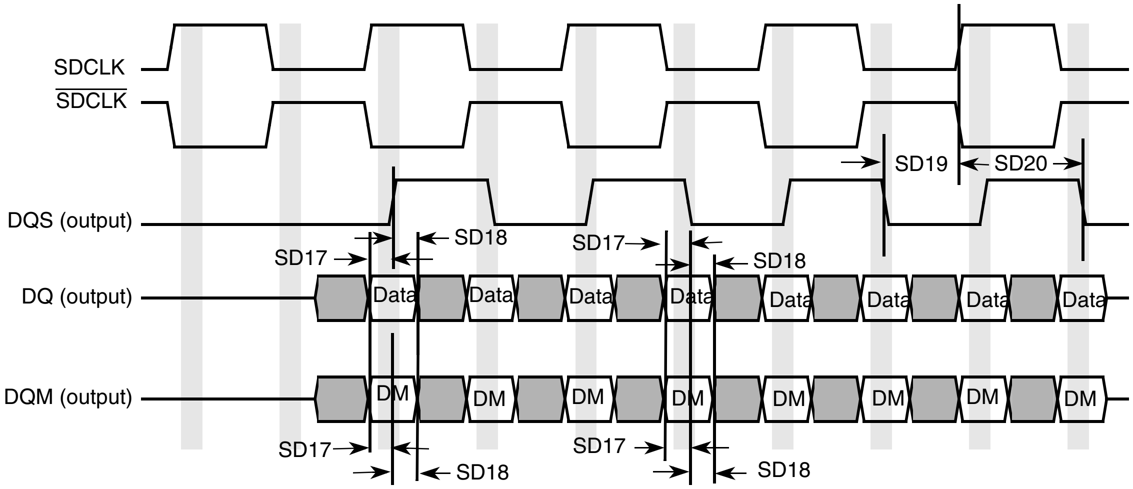


Figure 34. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 44 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

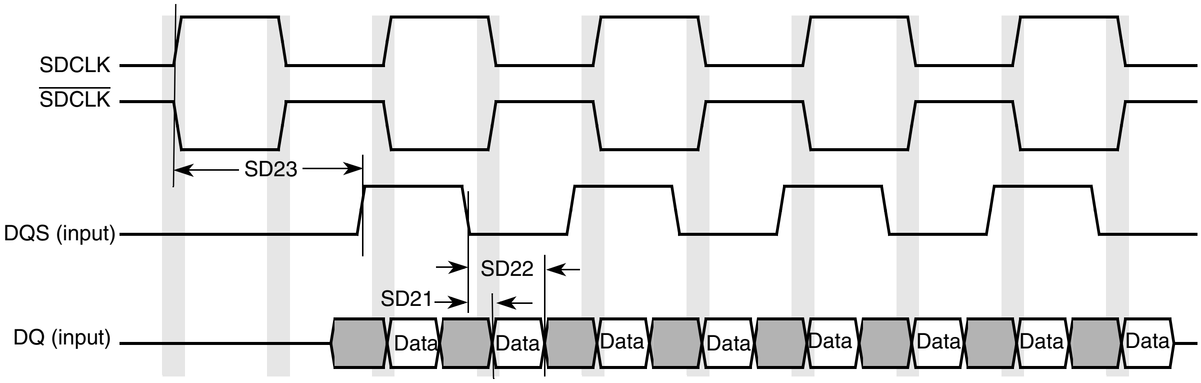


Figure 35. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 45. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value, and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 45 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

4.9.6 Enhanced Serial Audio Interface (ESAI) Timing Specifications

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 46 shows the interface timing values. The number field in the table refers to timing signals found in Figure 36 and Figure 37.

Table 46. Enhanced Serial Audio Interface Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
64	Clock low period • For internal clock • For external clock	 — —	 $2 \times T_C - 9.0$ $2 \times T_C$	 6 15	 — —	 — —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 46. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
80	SCKT rising edge to FST out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns

---

[1] i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

[2] bl = bit length
wl = word length
wr = word length relative

[3] SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

[4] For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

[5] The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

[6] Periodically sampled and not 100% tested.

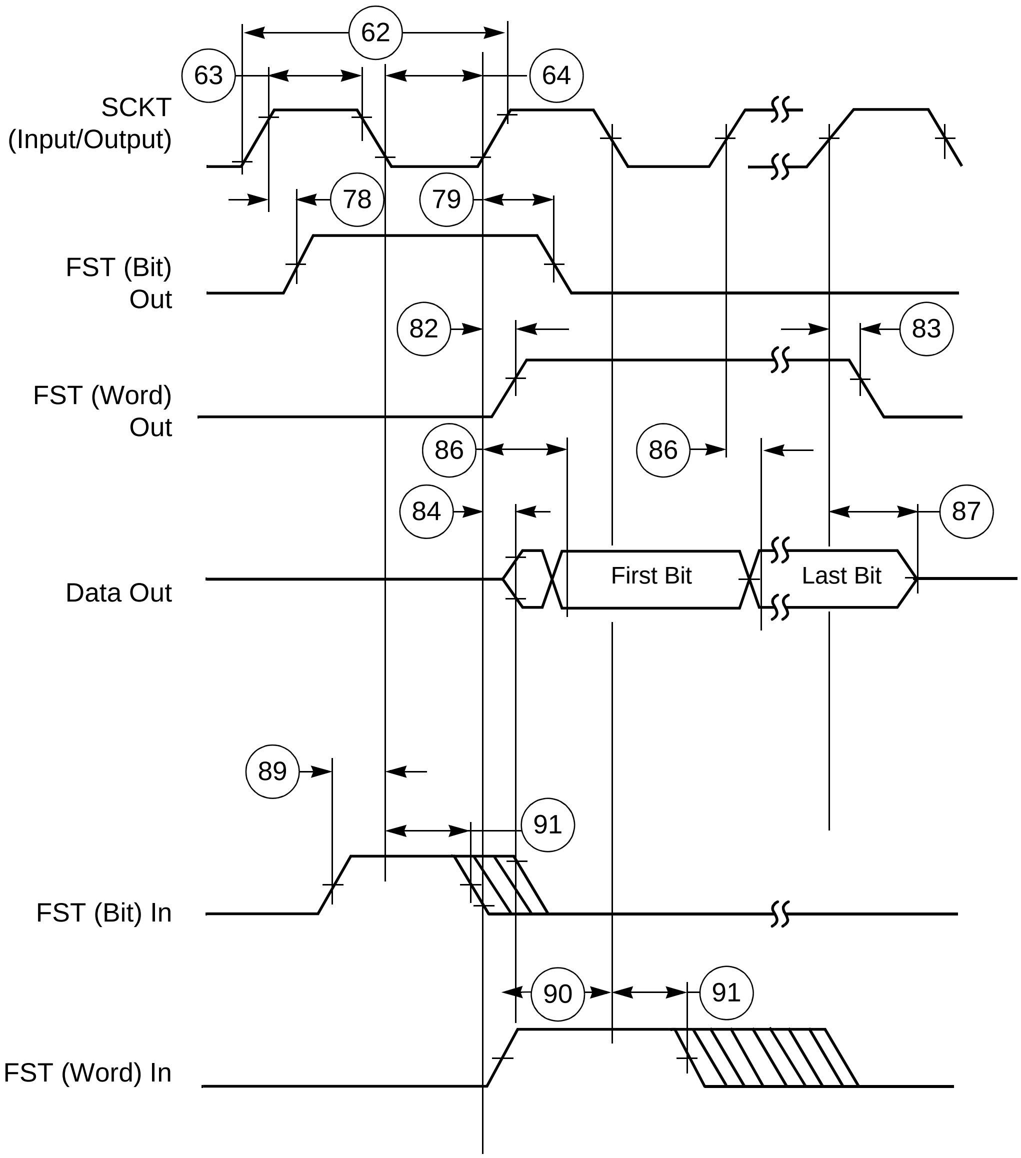

62
63
64
SCKT
(Input/Output)
78
79
FST (Bit)
Out
82
83
FST (Word)
Out
86
86
84
87
Data Out
First Bit
Last Bit
89
91
FST (Bit) In
90
91
FST (Word) In

Figure 36. ESAI Transmitter Timing

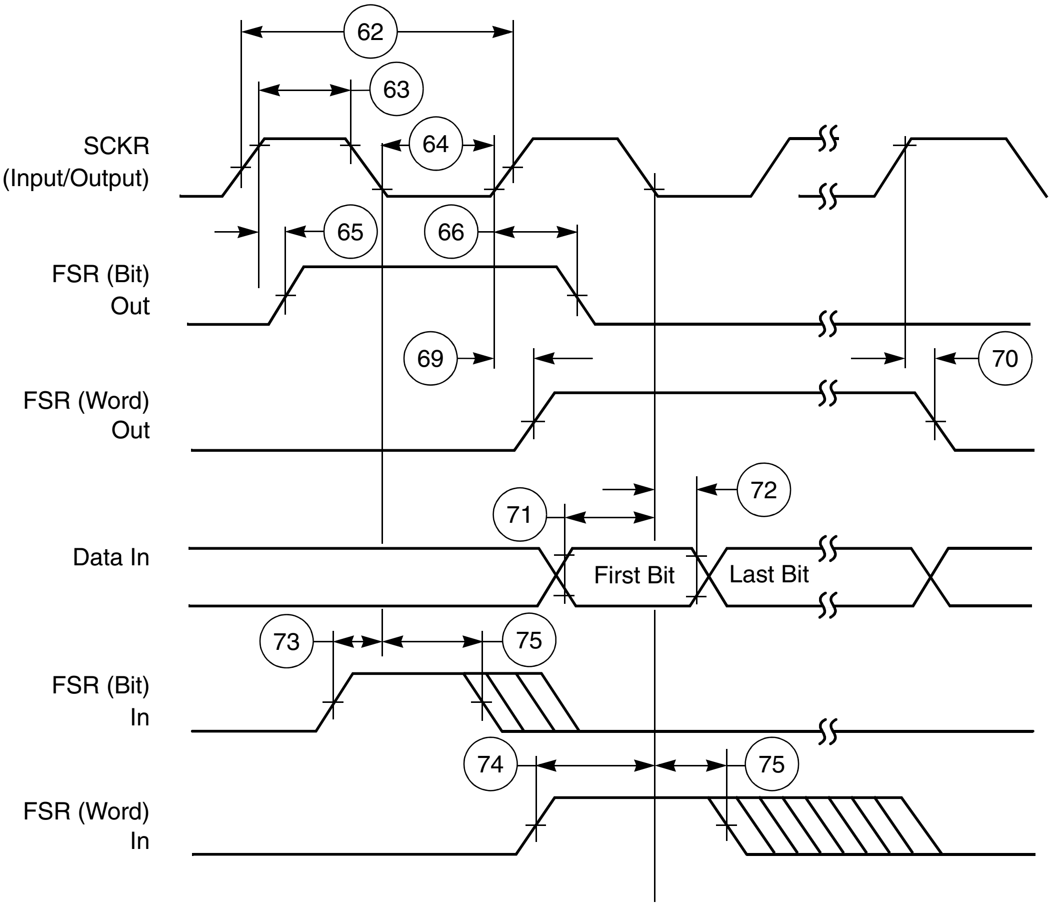

62
63
64
SCKR (Input/Output)
65
66
FSR (Bit) Out
69
70
FSR (Word) Out
71
72
Data In
First Bit
Last Bit
73
75
FSR (Bit) In
74
75
FSR (Word) In

Figure 37. ESAI Receiver Timing

4.9.7 eSDHCv2 AC Electrical Specifications

Figure 38 depicts the timing of eSDHCv2, and Table 47 lists the eSDHCv2 timing characteristics. The following definitions apply to values and signals described in Table 47:

- LS: low-speed mode. Low-speed card can tolerate a clock up to 400 kHz.
- FS: full-speed mode. For a full-speed MMC card, the card clock can reach 20 MHz; a full-speed SD/SDIO card can reach 25 MHz.
- HS: high-speed mode. For a high-speed MMC card, the card clock can reach 52 MHz; SD/SDIO can reach 50 MHz.

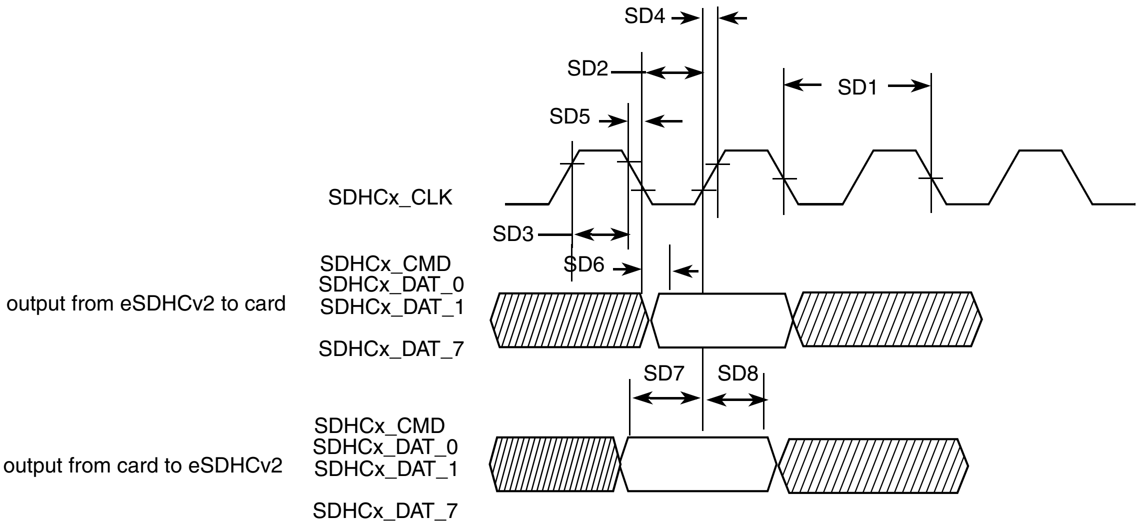

SD4
SD2
SD1
SD5
SDHCx_CLK
SD3
SD6
output from eSDHCv2 to card
SDHCx_CMD
SDHCx_DAT_0
SDHCx_DAT_1
SDHCx_DAT_7
SD7
SD8
output from card to eSDHCv2
SDHCx_CMD
SDHCx_DAT_0
SDHCx_DAT_1
SDHCx_DAT_7

Figure 38. eSDHCv2 Timing

Table 47. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

[1] In low-speed mode, the card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

[2] In normal-speed mode for the SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

[3] In normal-speed mode for MMC card, clock frequency can be any value between 0 and 20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

[4] To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.8 Fast Ethernet Controller (FEC) AC Electrical Specifications

This section describes the electrical information of the FEC module. The FEC is designed to support both 10- and 100-Mbps Ethernet networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps Media Independent Interface (MII) using a total of 18 pins. The 10-Mbps 7-wire interface that is restricted to a 10-Mbps data rate uses seven of the MII pins for connection to an external Ethernet transceiver.

4.9.8.1 FEC AC Timing

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.9.8.2 MII Receive Signal Timing

The MII receive timing signals consist of FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 48 lists MII receive channel timings.

Table 48. MII Receive Signal Timing

Num.	Characteristic[1]	Min.	Max.	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

[1] FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 39 shows the MII receive signal timings listed in Table 48.

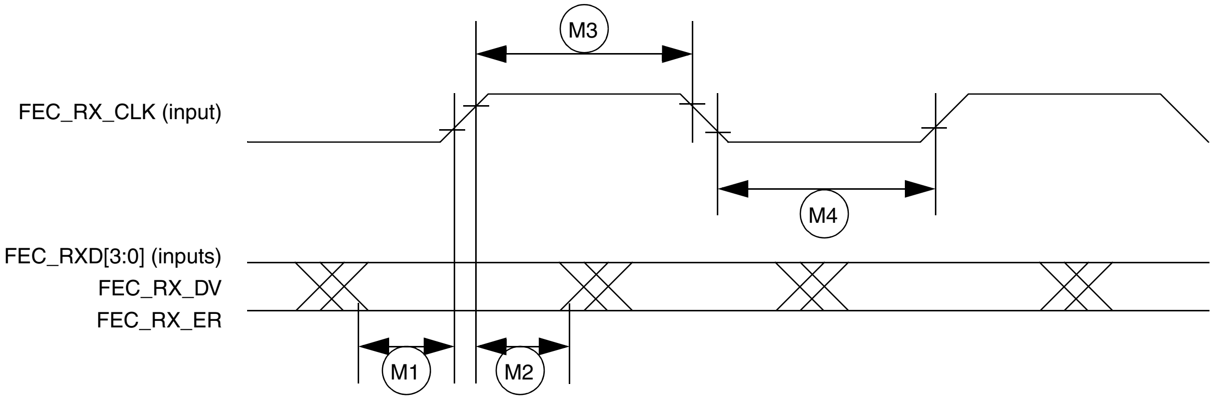


Figure 39. MII Receive Signal Timing Diagram

4.9.8.3 MII Transmit Signal Timing

The transmitter timing signals consist of FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency. Table 49 lists MII transmit channel timings.

Table 49. MII Transmit Signal Timing

Num	Characteristic[1]	Min.	Max.	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

[1] FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 40 shows the MII transmit signal timings listed in Table 49.

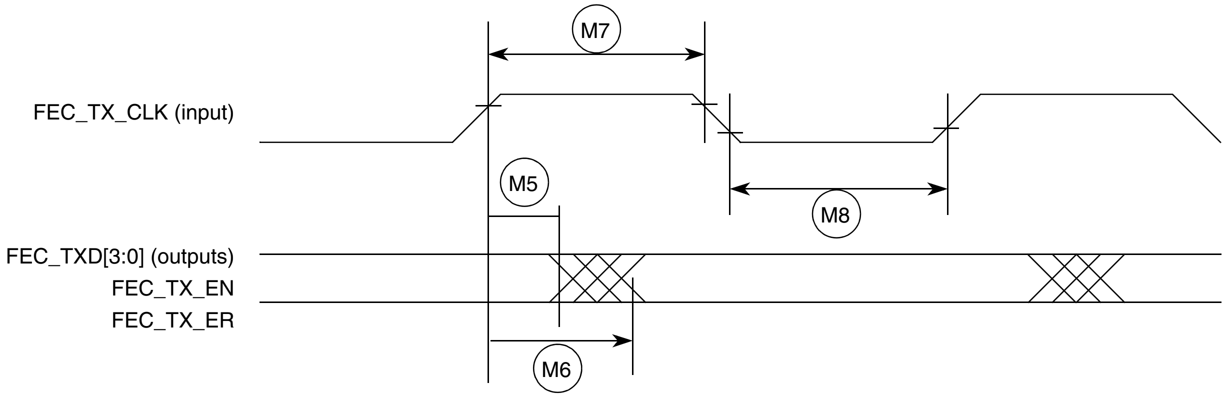


Figure 40. MII Transmit Signal Timing Diagram

4.9.8.4 MII Asynchronous Inputs Signal Timing

The MII asynchronous timing signals are FEC_CRS and FEC_COL. Table 50 lists MII asynchronous inputs signal timing.

Table 50. MII Asynch Inputs Signal Timing

Num	Characteristic	Min.	Max.	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

Figure 41 shows MII asynchronous input timings listed in Table 50.

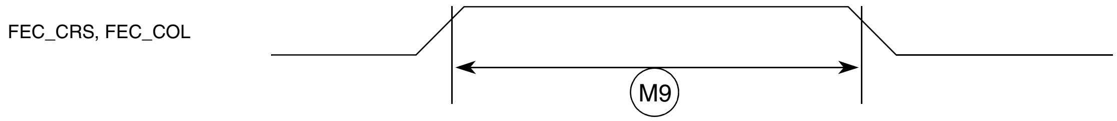


Figure 41. MII Asynch Inputs Timing Diagram

4.9.8.5 MII Serial Management Channel Timing

Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 51 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 51. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 42 shows MII serial management channel timings listed in Table 51.

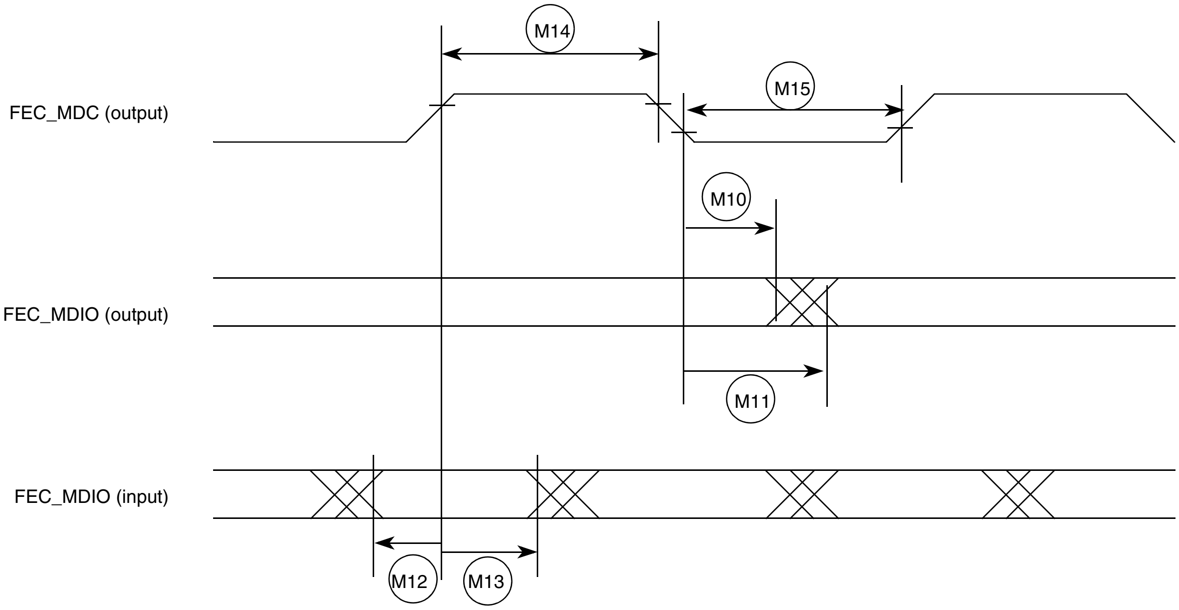


Figure 42. MII Serial Management Channel Timing Diagram

4.9.9 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) defined by IrDA® (Infrared Data Association). Refer to the IrDA® website for details on FIR and MIR protocols.

4.9.10 FlexCAN Module AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver outside the chip. The i.MX35 has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. Refer to the IOMUX chapter of the *MCIMX35 Multimedia Applications Processor Reference Manual* to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.9.11 I^{2}C AC Electrical Specifications

This section describes the electrical characteristics of the I^{2}C module.

4.9.11.1 I^{2}C Module Timing

Figure 43 depicts the timing of the I^{2}C module. Table 52 lists the I^{2}C module timing parameters.

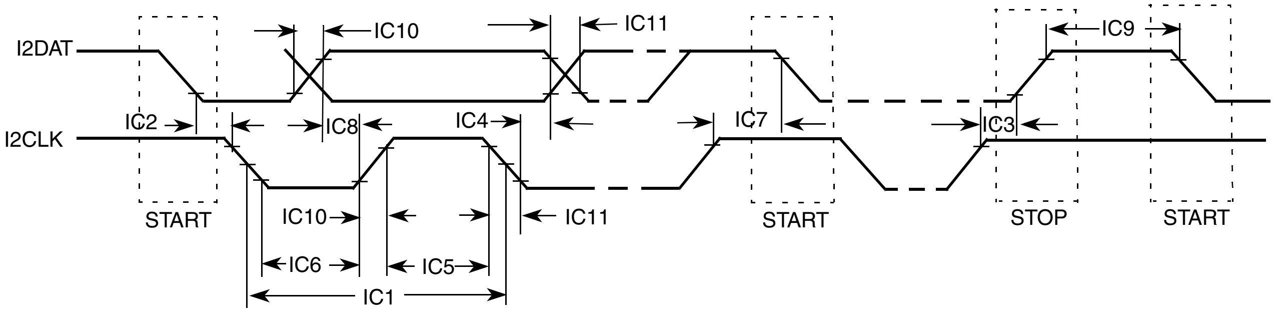


Figure 43. I^{2}C Bus Timing Diagram

Table 52. I^{2}C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	—	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	—	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

[1] A device must internally provide a hold time of at least 300 ns for the I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

[2] The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

[3] A fast-mode I^{2}C-bus device can be used in a standard-mode I^{2}C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the I2CLK line is released.

4.9.12 IPU—Sensor Interfaces

This section contains a list of supported camera sensors, a functional description, and the electrical characteristics.

4.9.12.1 Supported Camera Sensors

Table 53 lists the known supported camera sensors at the time of publication.

Table 53. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI-SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630, OV2640
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

[1] Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

[2] These sensors have not been validated at the time of publication.

4.9.12.2 Functional Description

There are three timing modes supported by the IPU.

4.9.12.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which typically include image processing capability, support video mode transfer operations. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of the ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with an EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

4.9.12.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 44.

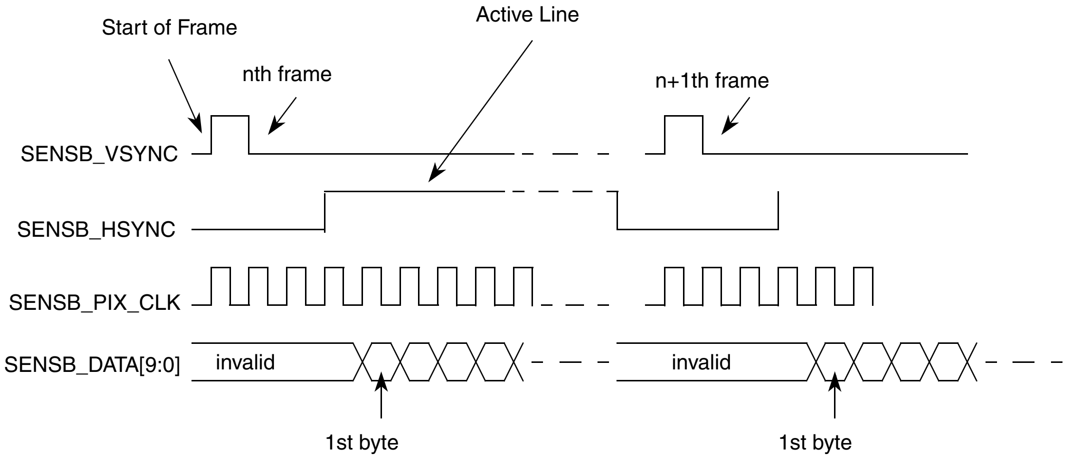

Start of Frame
Active Line
nth frame
n+1th frame
SENSB_VSYNC
SENSB_HSYNC
SENSB_PIX_CLK
SENSB_DATA[9:0]
invalid
invalid
1st byte
1st byte

Figure 44. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timing corresponds to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. The pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of the line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the SENSB_HSYNC timing repeats. For the next frame, the SENSB_VSYNC timing repeats.

4.9.12.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.9.12.2.2, “Gated Clock Mode”), except for the SENSB_HSYNC signal, which is not used. See Figure 45. All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

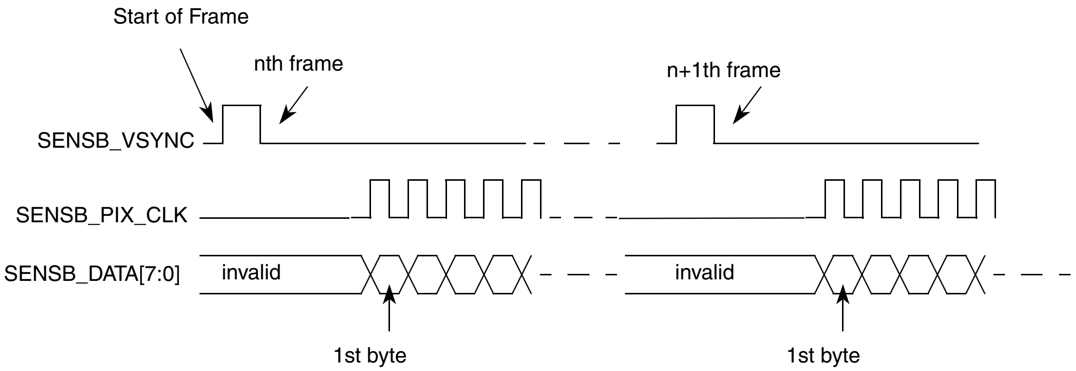

Start of Frame
nth frame
n+1th frame
SENSB_VSYNC
SENSB_PIX_CLK
SENSB_DATA[7:0]
invalid
invalid
1st byte
1st byte

Figure 45. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 45 is that of a Motorola sensor. Some other sensors may have slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.9.12.3 Electrical Characteristics

Figure 46 depicts the sensor interface timing, and Table 54 lists the timing parameters.

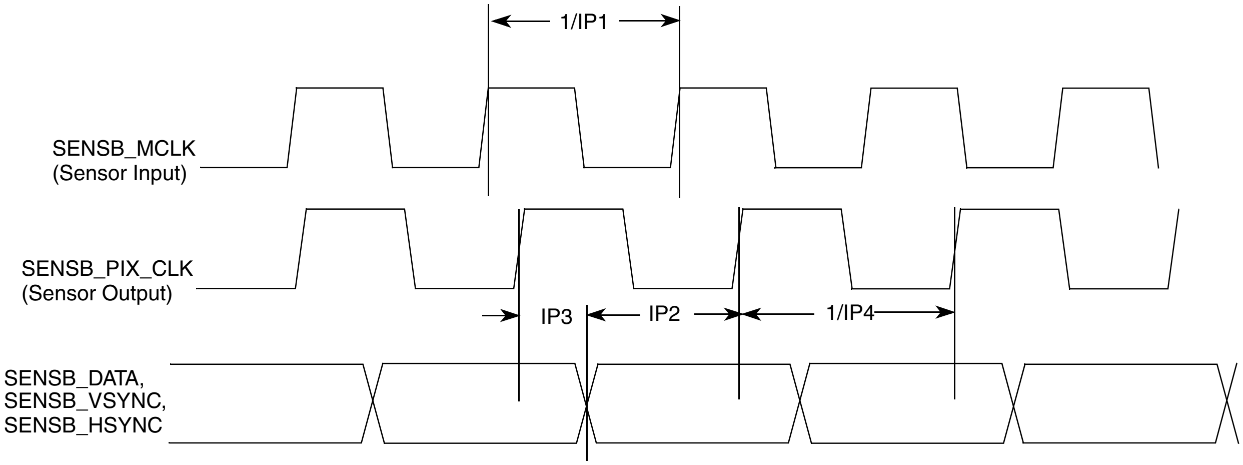


Figure 46. Sensor Interface Timing Diagram

Table 54. Sensor Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

4.9.13 IPU—Display Interfaces

This section describes the following types of display interfaces:

- Section 4.9.13.1, “Synchronous Interfaces”
- Section 4.9.13.2, “Interface to Sharp HR-TFT Panels”
- Section 4.9.13.3, “Synchronous Interface to Dual-Port Smart Displays”
- Section 4.9.13.4, “Asynchronous Interfaces”
- Section 4.9.13.5, “Serial Interfaces, Functional Description”

4.9.13.1 Synchronous Interfaces

This section discusses the interfaces to active matrix TFT LCD panels, Sharp HR-TFT, and dual-port smart displays.

4.9.13.1.4 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 47 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is as follows:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted to the display. When disabled, the data is invalid and the trace is off.

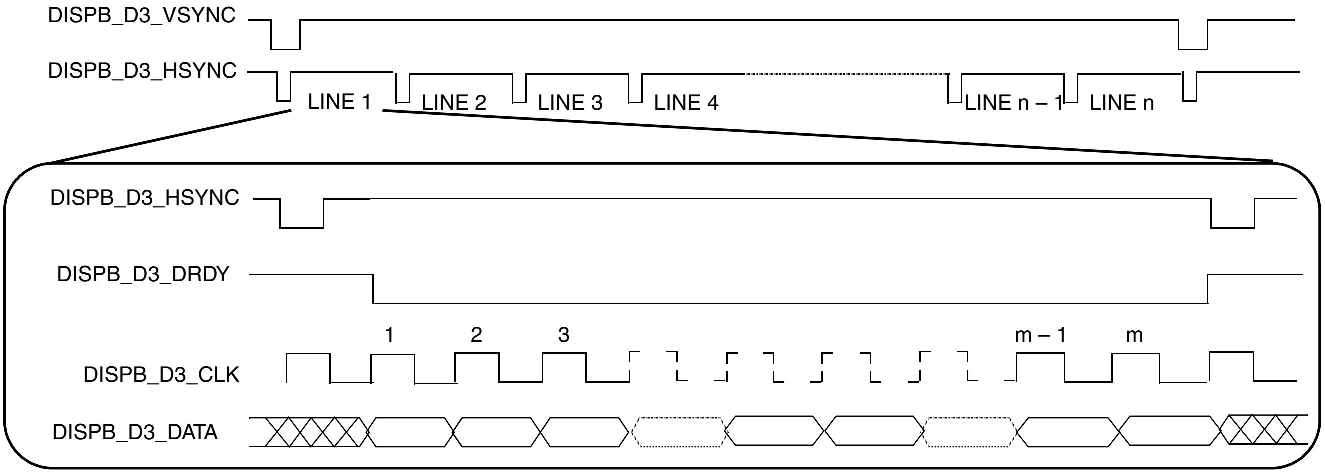


Figure 47. Interface Timing Diagram for TFT (Active Matrix) Panels

4.9.13.1.5 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 48 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

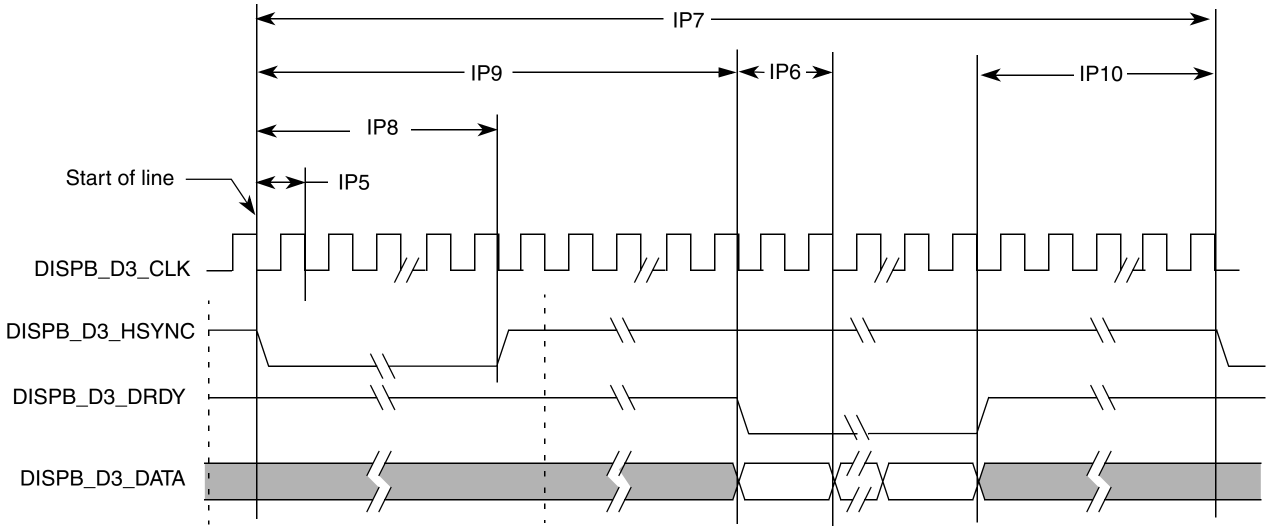

IP7
IP9
IP6
IP10
IP8
Start of line
IP5
DISPB_D3_CLK
DISPB_D3_HSYNC
DISPB_D3_DRDY
DISPB_D3_DATA

Figure 48. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 49 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

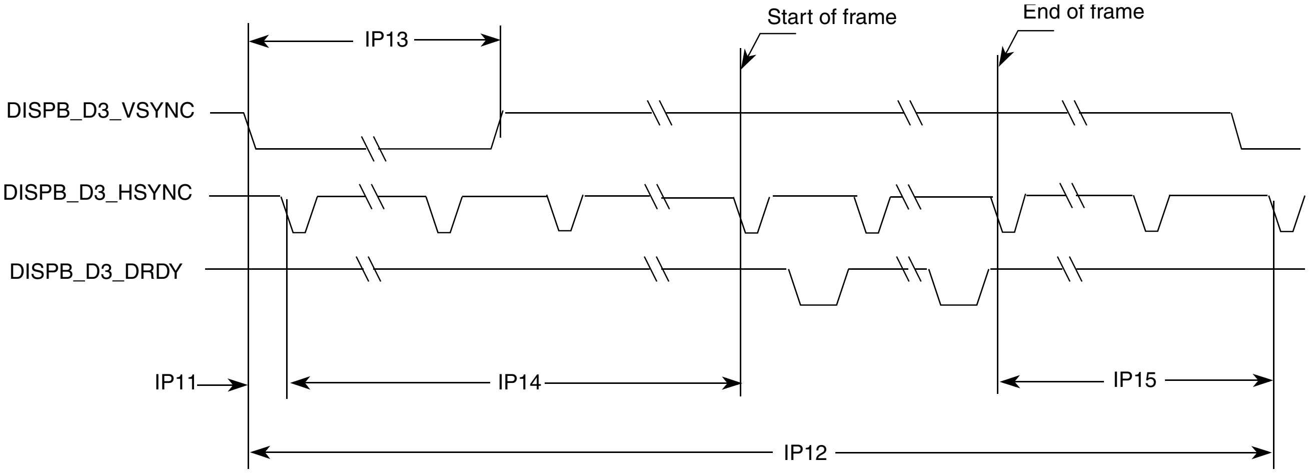

IP13
Start of frame
End of frame
DISPB_D3_VSYNC
DISPB_D3_HSYNC
DISPB_D3_DRDY
IP11
IP14
IP15
IP12

Figure 49. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 55 shows timing parameters of signals presented in Figure 48 and Figure 49.

Table 55. Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP5	Display interface clock period	Tdicp	Tdicp[1]	ns
IP6	Display pixel clock period	Tdpcp	(DISP3_IF_CLK_CNT_D + 1) × Tdicp	ns
IP7	Screen width	Tsw	(SCREEN_WIDTH + 1) × Tdpcp	ns
IP8	HSYNC width	Thsw	(H_SYNC_WIDTH + 1) × Tdpcp	ns

Table 55. Synchronous Display Interface Timing Parameters—Pixel Level (continued)

ID	Parameter	Symbol	Value	Units
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdpcp	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdpcp	ns
IP11	HSYNC delay	Thsd	H_SYNC_DELAY × Tdpcp	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT + 1) × Tsw	ns
IP13	VSYNC width	Tvsw	if V_SYNC_WIDTH_L = 0 than (V_SYNC_WIDTH + 1) × Tdpcp else (V_SYNC_WIDTH + 1) × Tsw	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	ns

[1] Display interface clock period immediate value

Display interface clock period average value.

$$\bar{T}dicp = T_{HSP\_CLK} \cdot \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}$$

Figure 50 depicts the synchronous display interface timing for access level, and Table 56 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

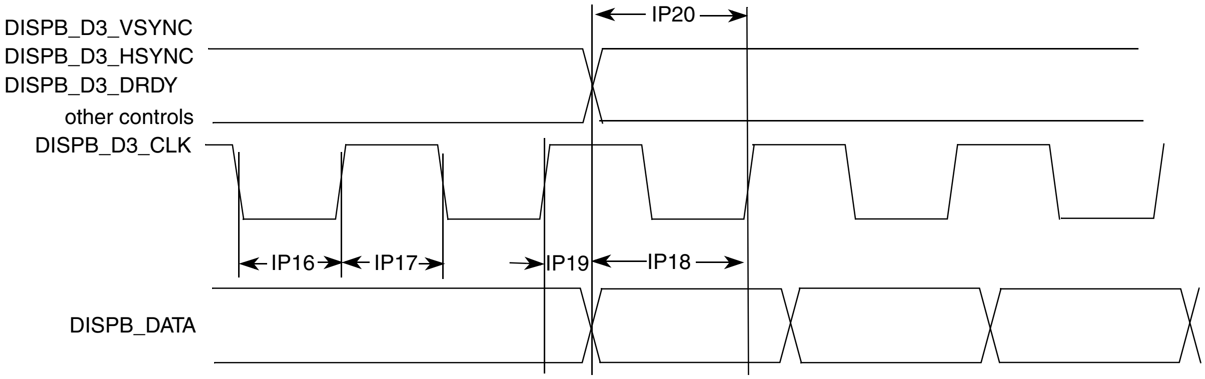


Figure 50. Synchronous Display Interface Timing Diagram—Access Level

Table 56. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP16	Display interface clock low time	Tckl	Tdicd – Tdicu – 1.5	Tdicd[2] – Tdicu[3]	Tdicd – Tdicu + 1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp – Tdicd + Tdicu – 1.5	Tdicp – Tdicd + Tdicu	Tdicp – Tdicd + Tdicu + 1.5	ns
IP18	Data setup time	Tdsu	Tdicd – 3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp – Tdicd – 3.5	Tdicp – Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd – 3.5	Tdicu	—	ns

[1] The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

[2] Display interface clock down time

$$\text{Tdicd} = \frac{1}{2}\text{T}_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{2 \cdot \text{DISP3\_IF\_CLK\_DOWN\_WR}}{\text{HSP\_CLK\_PERIOD}}\right]$$

[3] Display interface clock up time

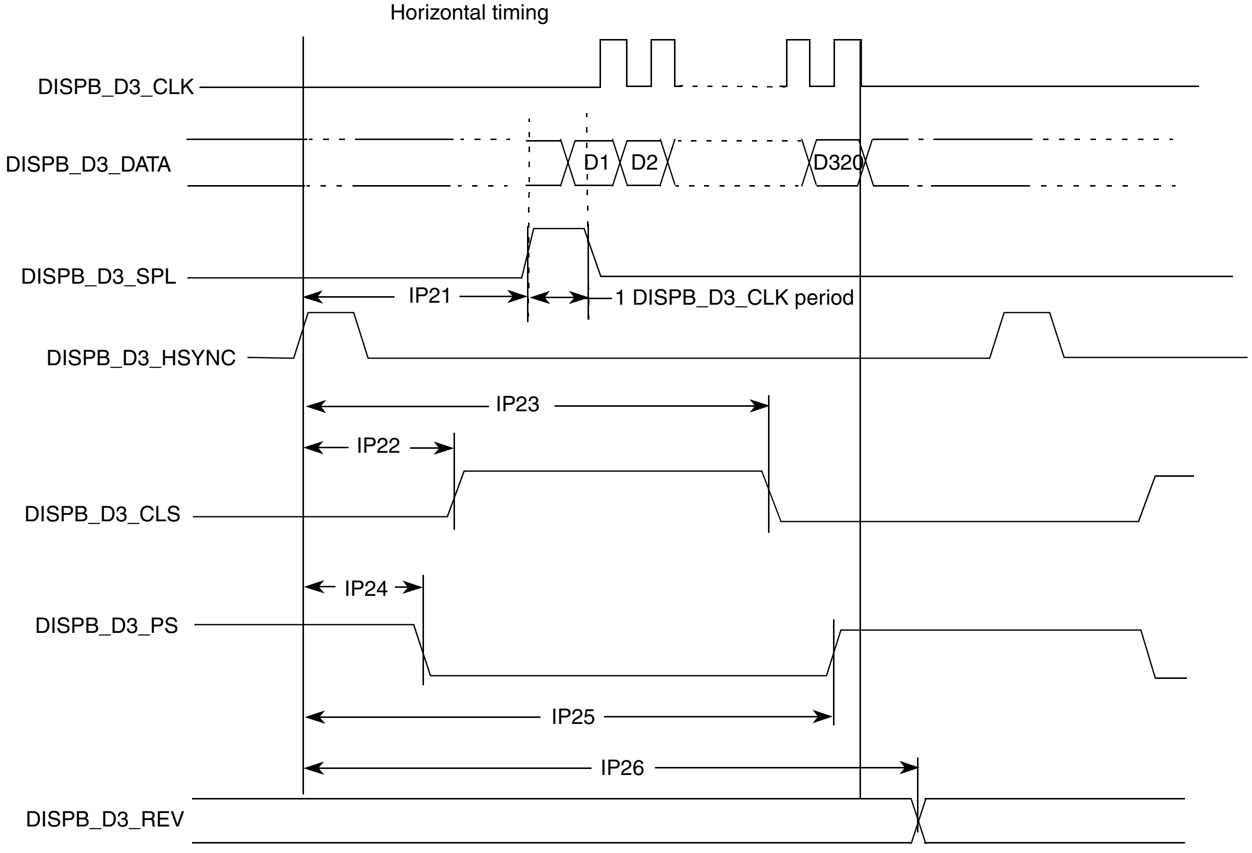
$$\text{Tdicu} = \frac{1}{2}\text{T}_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{2 \cdot \text{DISP3\_IF\_CLK\_UP\_WR}}{\text{HSP\_CLK\_PERIOD}}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

4.9.13.2 Interface to Sharp HR-TFT Panels

Figure 51 depicts the Sharp HR-TFT panel interface timing, and Table 57 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to

Section 4.9.13.1.5, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics." The timing images correspond to straight polarity of the Sharp signals.



Horizontal timing
DISPB_D3_CLK
DISPB_D3_DATA
D1
D2
D320
DISPB_D3_SPL
IP21
1 DISPB_D3_CLK period
DISPB_D3_HSYNC
IP23
IP22
DISPB_D3_CLS
IP24
DISPB_D3_PS
IP25
IP26
DISPB_D3_REV

Example is drawn with FW + 1 = 320 pixel/line, FH + 1 = 240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

Figure 51. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

Table 57. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	(BGXP – 1) × Tdpcp	ns
IP22	CLS rise time	Tclsr	CLS_RISE_DELAY × Tdpcp	ns
IP23	CLS fall time	Tclsf	CLS_FALL_DELAY × Tdpcp	ns
IP24	CLS rise and PS fall time	Tpsf	PS_FALL_DELAY × Tdpcp	ns
IP25	PS rise time	Tpsr	PS_RISE_DELAY × Tdpcp	ns
IP26	REV toggle time	Trev	REV_TOGGLE_DELAY × Tdpcp	ns

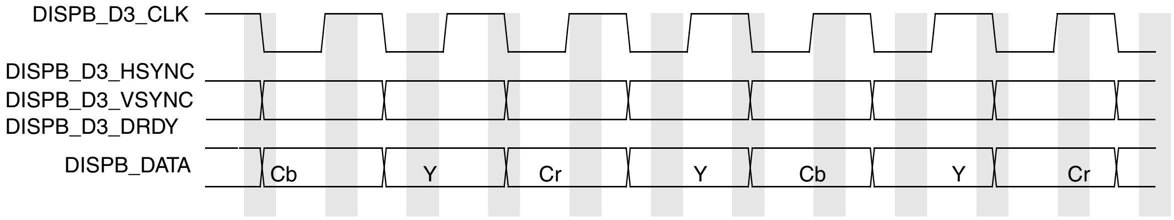
4.9.13.3 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

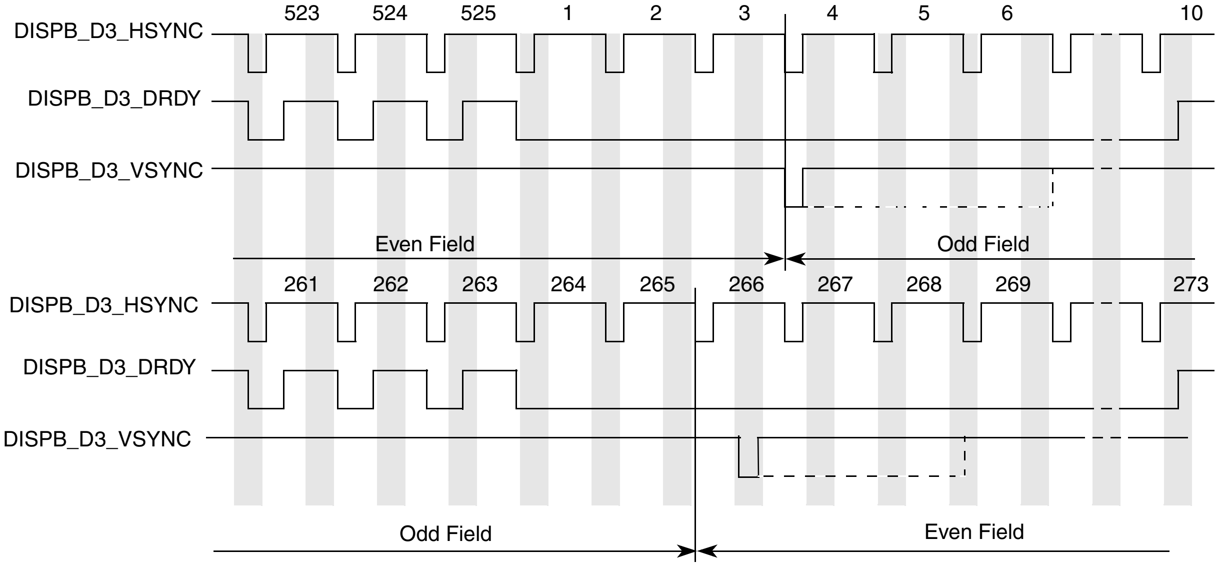
4.9.13.3.6 Interface to a TV Encoder—Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. Figure 52 depicts the interface timing.

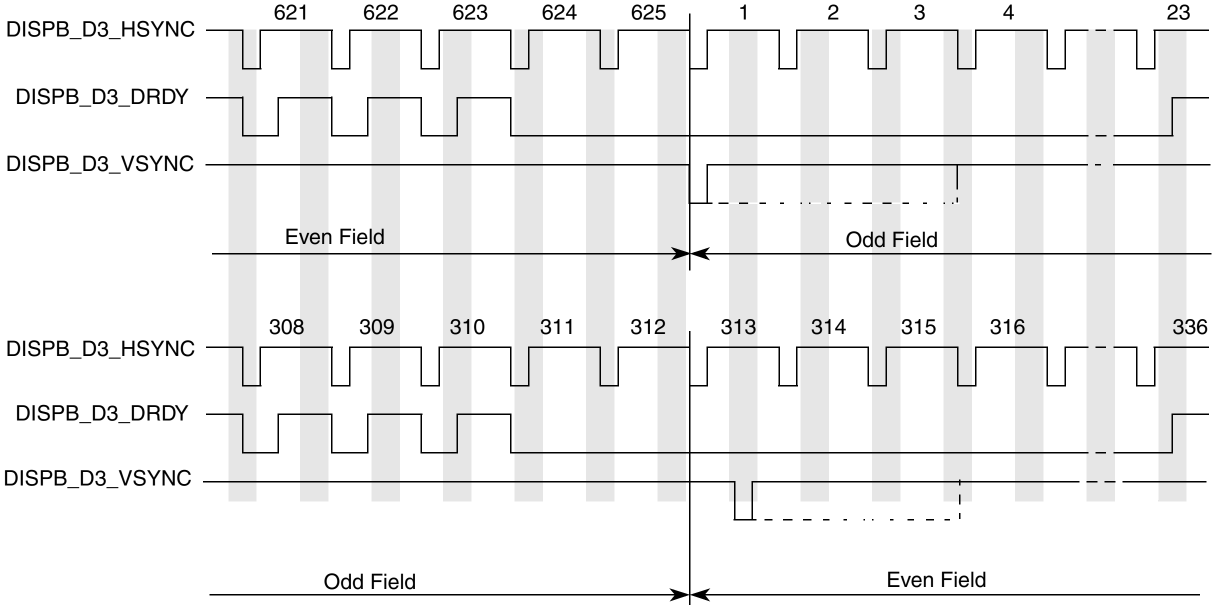
- The frequency of the clock DISPB_D3_CLK is 27 MHz.
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
    - At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
    - At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.


DISPB_D3_CLK
DISPB_D3_HSYNC
DISPB_D3_VSYNC
DISPB_D3_DRDY
DISPB_DATA
Cb
Y
Cr
Y
Cb
Y
Cr

Pixel Data Timing


DISPB_D3_HSYNC
523
524
525
1
2
3
4
5
6
10
DISPB_D3_DRDY
DISPB_D3_VSYNC
Even Field
Odd Field
DISPB_D3_HSYNC
261
262
263
264
265
266
267
268
269
273
DISPB_D3_DRDY
DISPB_D3_VSYNC
Odd Field
Even Field

Line and Field Timing - NTSC


DISPB_D3_HSYNC
621
622
623
624
625
1
2
3
4
23
DISPB_D3_DRDY
DISPB_D3_VSYNC
Even Field
Odd Field
DISPB_D3_HSYNC
308
309
310
311
312
313
314
315
316
336
DISPB_D3_DRDY
DISPB_D3_VSYNC
Odd Field
Even Field

Line and Field Timing - PAL

Figure 52. TV Encoder Interface Timing Diagram

4.9.13.3.7 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

4.9.13.4 Asynchronous Interfaces

This section discusses the asynchronous parallel and serial interfaces.

4.9.13.4.8 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

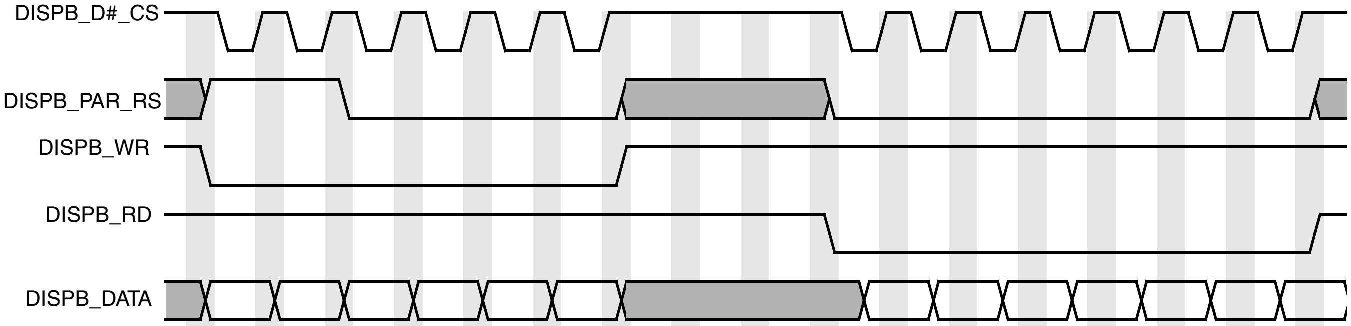
- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

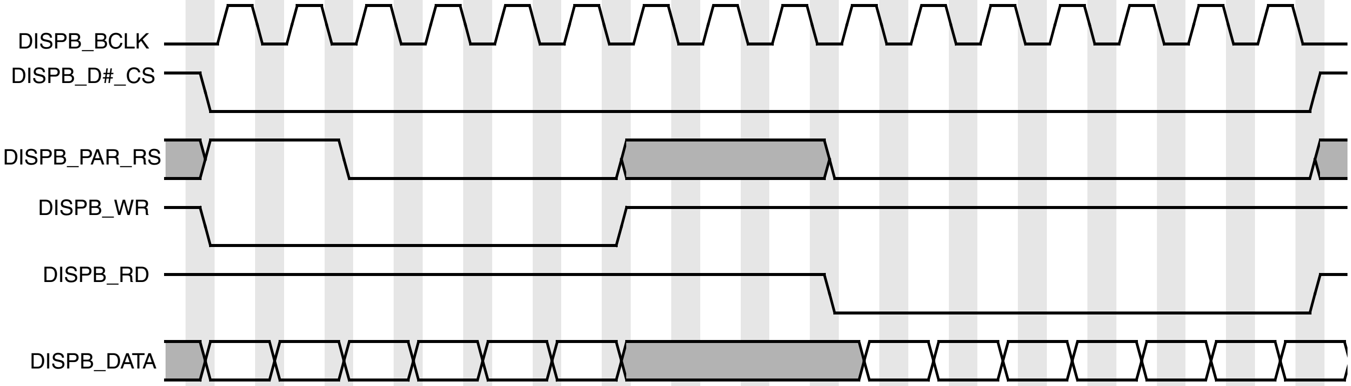
1. Burst mode without a separate clock—The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) or by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals change only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k), and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK—In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode—In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according to the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 53, Figure 54, Figure 55, and Figure 56. These timing images correspond to active-low DISPB_D*n*_CS, DISPB_D*n*_WR and DISPB_D*n*_RD signals.

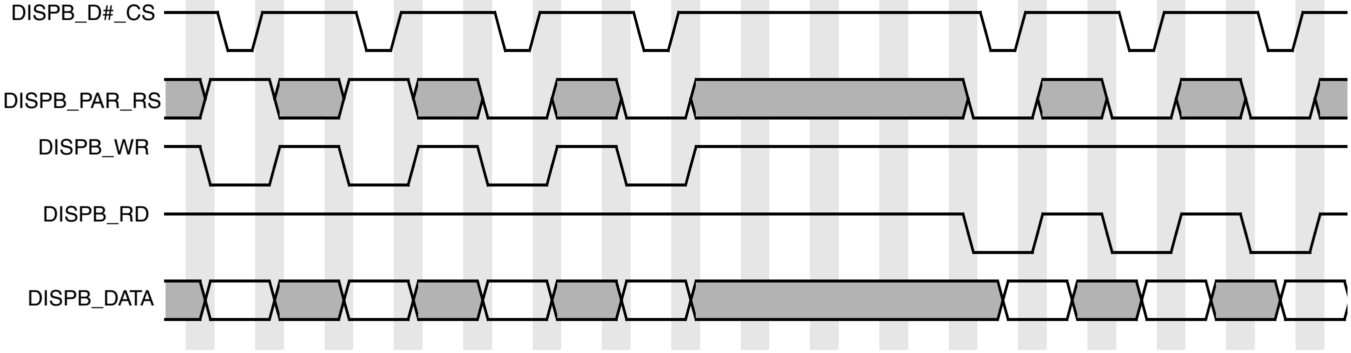
Additionally, the IPU allows a programmable pause between two bursts. The pause is defined in the HSP_CLK cycles. It allows the prevention of timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.


DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
DISPB_RD
DISPB_DATA

Burst access mode with sampling by CS signal

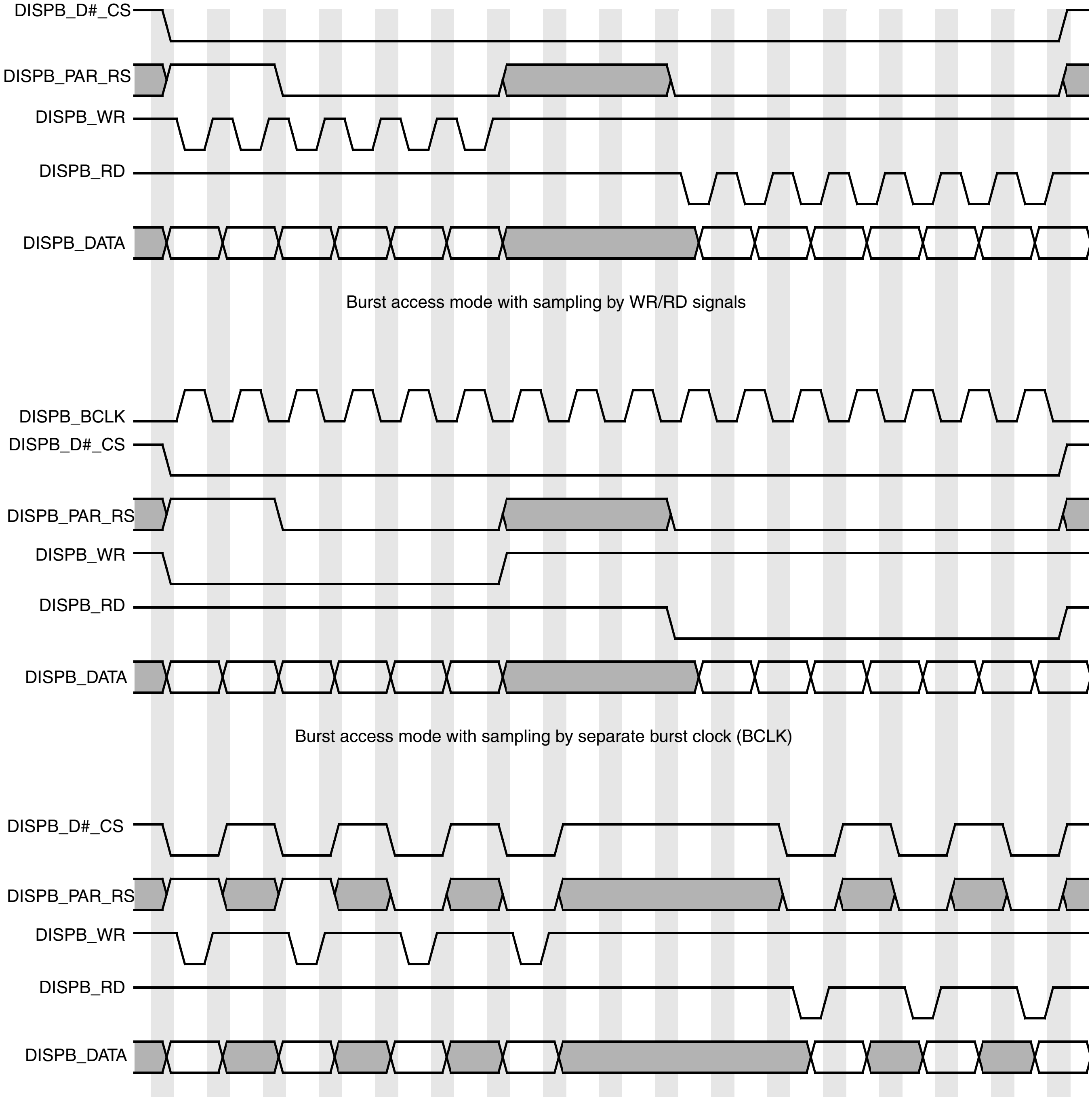

DISPB_BCLK
DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
DISPB_RD
DISPB_DATA

Burst access mode with sampling by separate burst clock (BCLK)


DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
DISPB_RD
DISPB_DATA

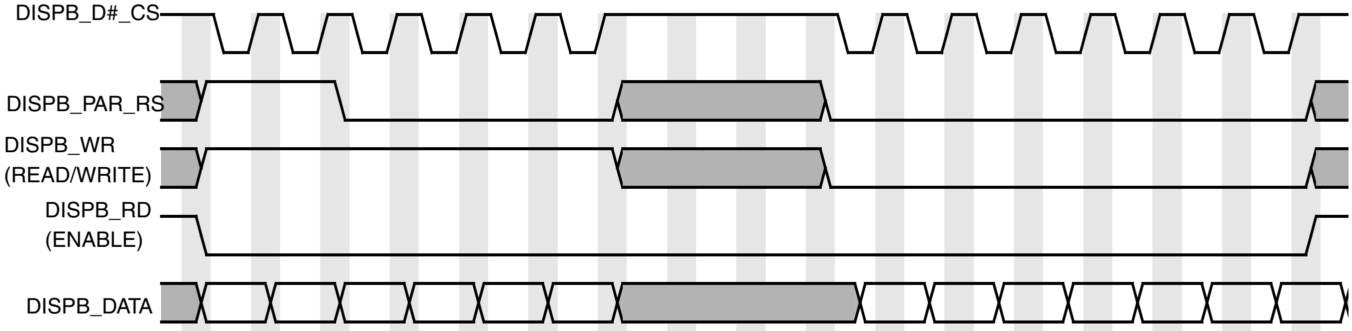
Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 53. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram

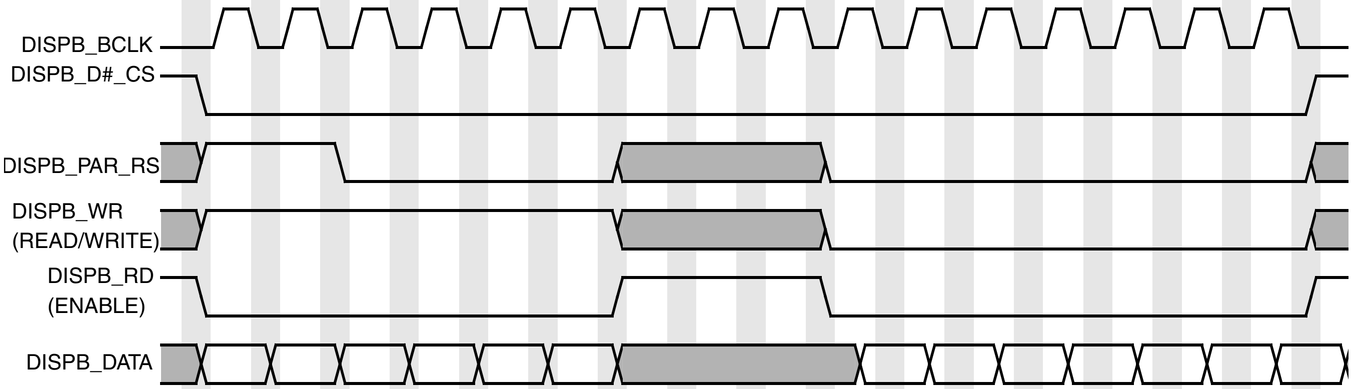

DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
DISPB_RD
DISPB_DATA
Burst access mode with sampling by WR/RD signals
DISPB_BCLK
DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
DISPB_RD
DISPB_DATA
Burst access mode with sampling by separate burst clock (BCLK)
DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
DISPB_RD
DISPB_DATA

Single access mode (all control signals are not active for one display interface clock after each display access)

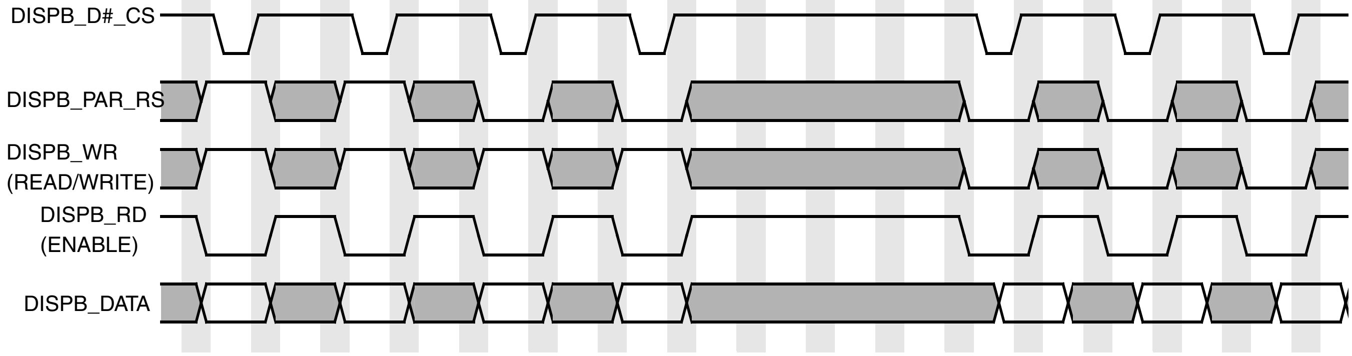
Figure 54. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram


DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
(READ/WRITE)
DISPB_RD
(ENABLE)
DISPB_DATA

Burst access mode with sampling by CS signal

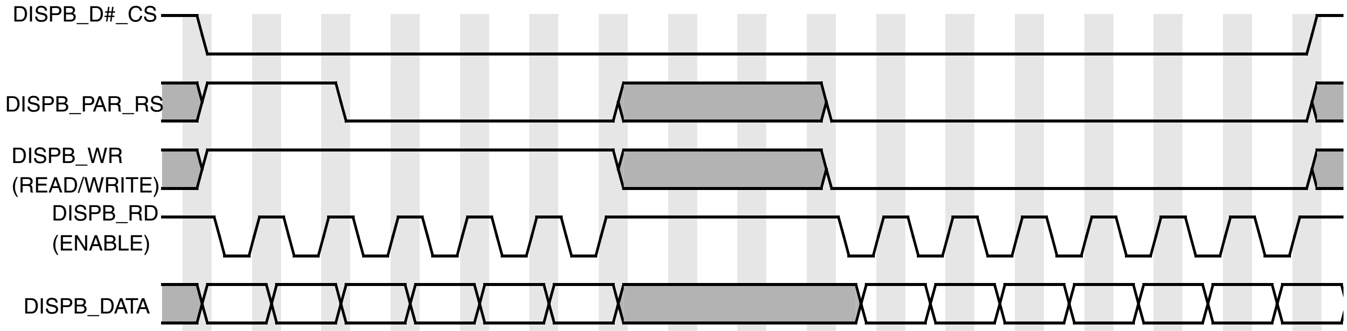

DISPB_BCLK
DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
(READ/WRITE)
DISPB_RD
(ENABLE)
DISPB_DATA

Burst access mode with sampling by separate burst clock (BCLK)

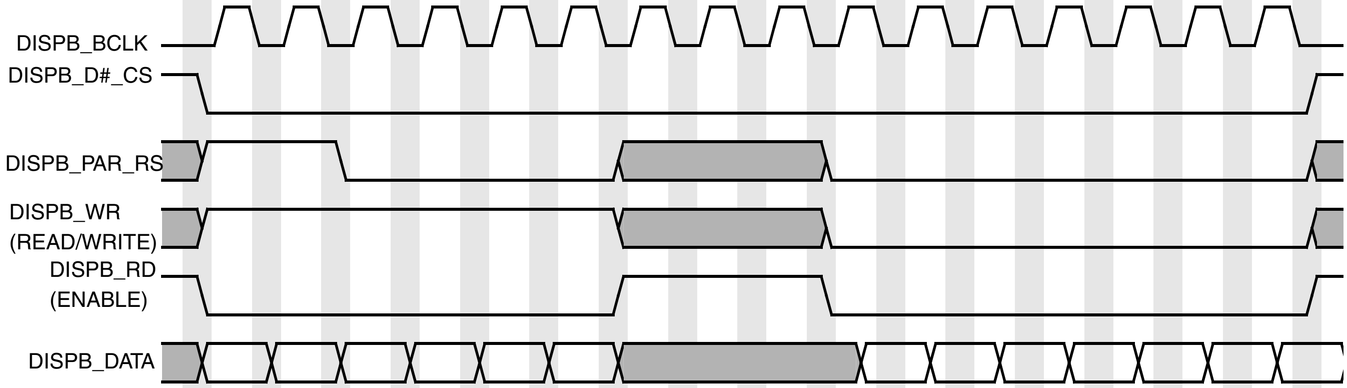

DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
(READ/WRITE)
DISPB_RD
(ENABLE)
DISPB_DATA

Single access mode (all control signals are not active for one display interface clock after each display access)

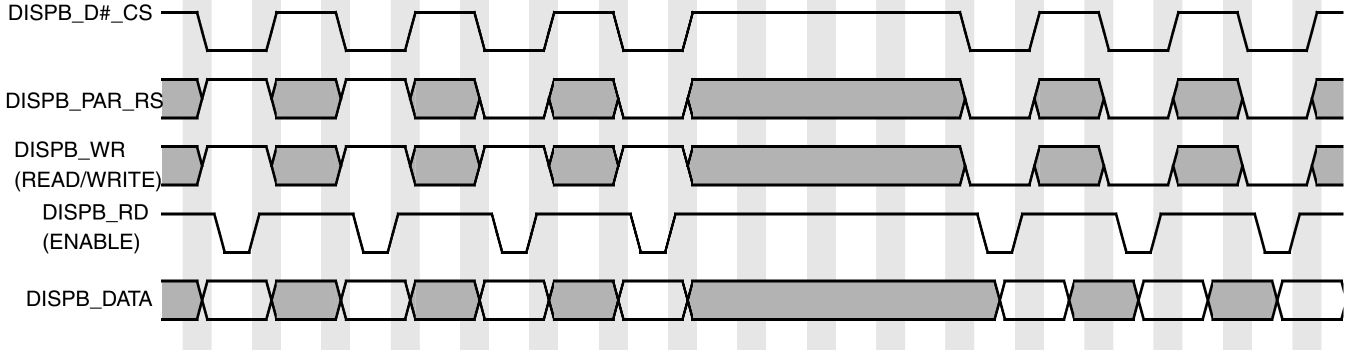
Figure 55. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram


DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
(READ/WRITE)
DISPB_RD
(ENABLE)
DISPB_DATA

Burst access mode with sampling by ENABLE signal


DISPB_BCLK
DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
(READ/WRITE)
DISPB_RD
(ENABLE)
DISPB_DATA

Burst access mode with sampling by separate burst clock (BCLK)


DISPB_D#_CS
DISPB_PAR_RS
DISPB_WR
(READ/WRITE)
DISPB_RD
(ENABLE)
DISPB_DATA

Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 56. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the

DI_DISP*n*_TIME_CONF_3 registers ($n = 0,1,2$). Figure 57 shows the timing of the parallel interface with read wait states.

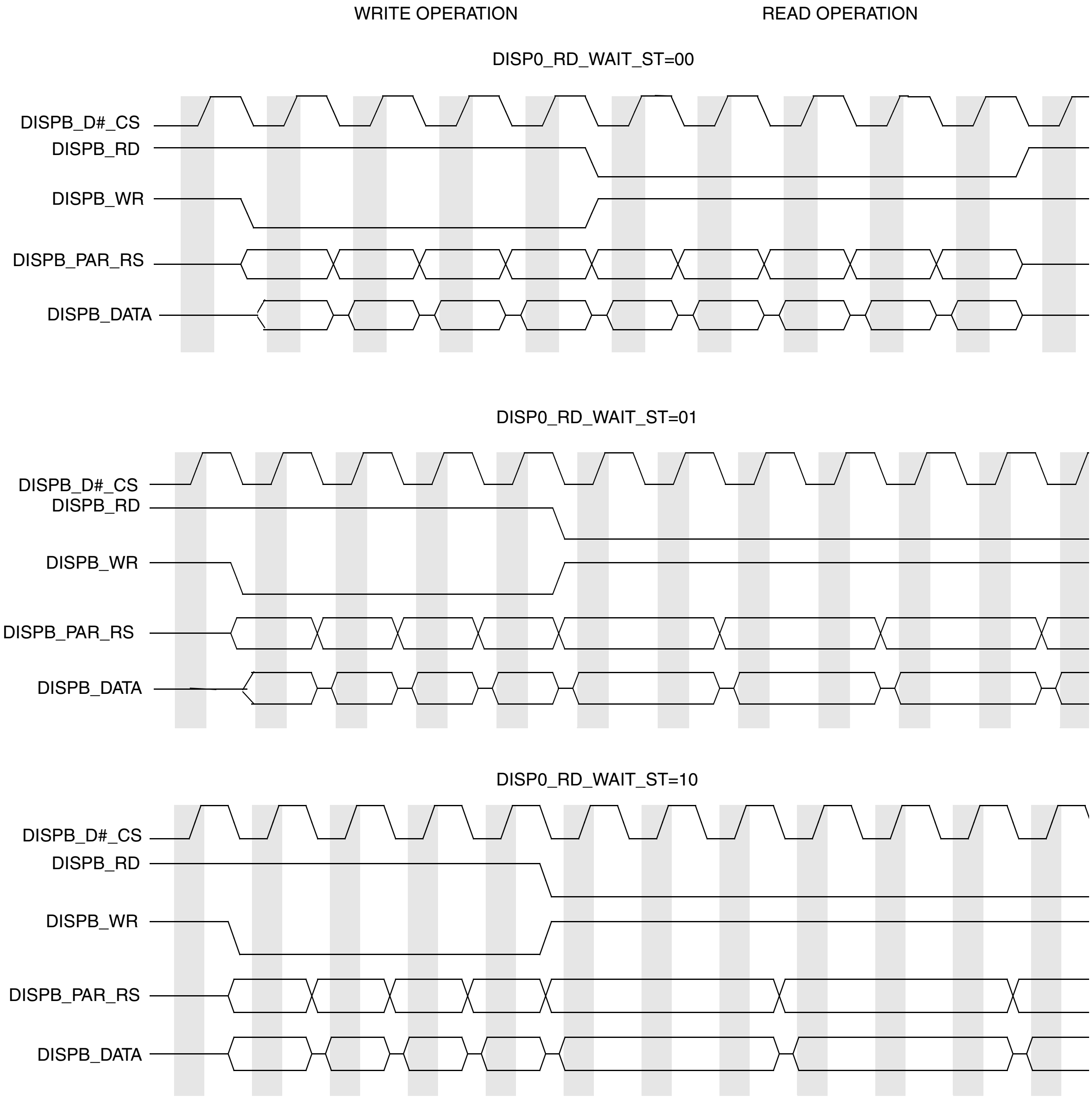

WRITE OPERATION
READ OPERATION
DISP0_RD_WAIT_ST=00
DISPB_D#_CS
DISPB_RD
DISPB_WR
DISPB_PAR_RS
DISPB_DATA
DISP0_RD_WAIT_ST=01
DISPB_D#_CS
DISPB_RD
DISPB_WR
DISPB_PAR_RS
DISPB_DATA
DISP0_RD_WAIT_ST=10
DISPB_D#_CS
DISPB_RD
DISPB_WR
DISPB_PAR_RS
DISPB_DATA

Figure 57. Parallel Interface Timing Diagram—Read Wait States

4.9.13.4.9 Parallel Interfaces, Electrical Characteristics

Figure 58, Figure 60, Figure 59, and Figure 61 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 58 lists the timing parameters at display access level. All timing images are based on active low control signals (signal polarity is controlled via the DI_DISP_SIG_POL register).

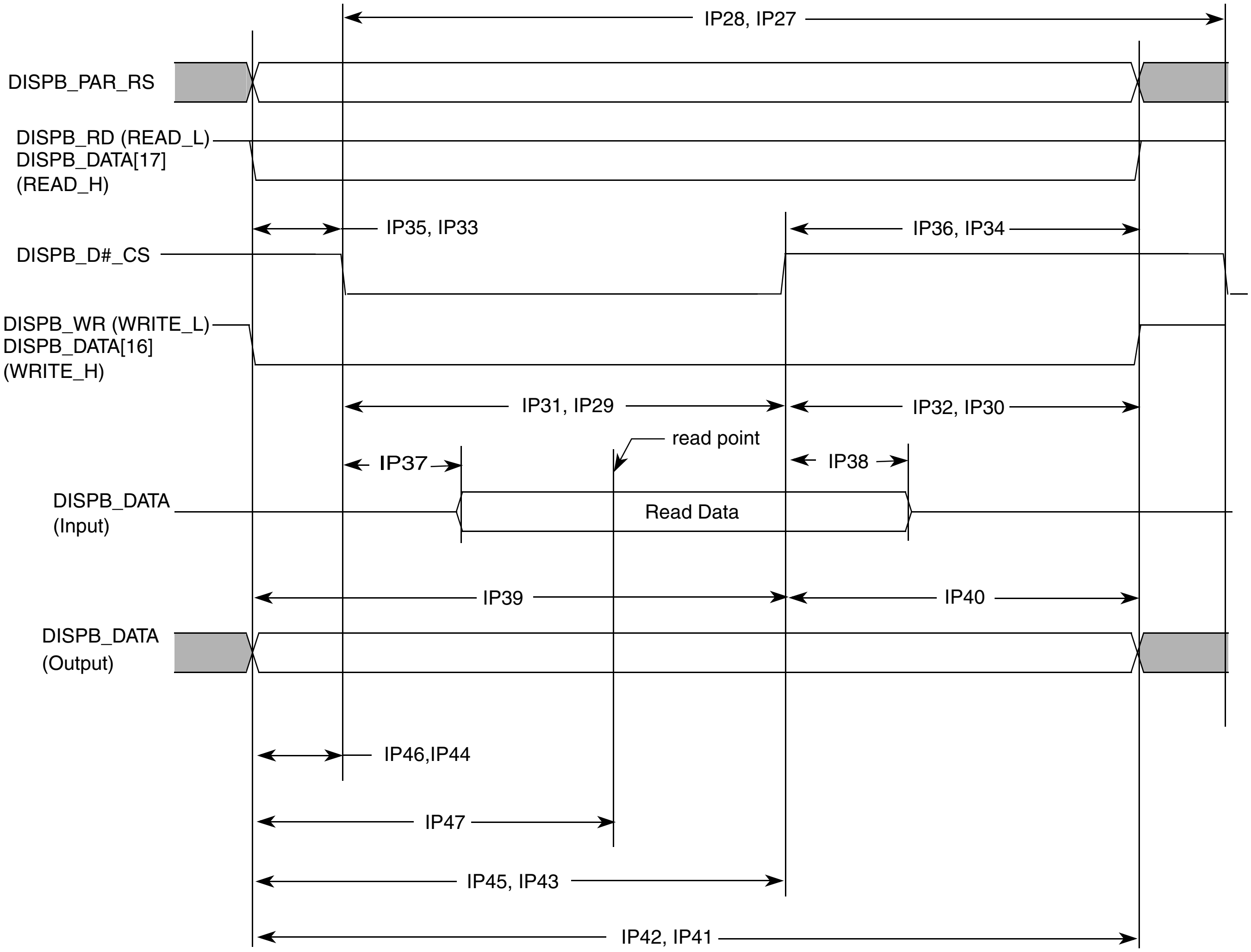

IP28, IP27
DISPB_PAR_RS
DISPB_RD (READ_L)
DISPB_DATA[17]
(READ_H)
IP35, IP33
IP36, IP34
DISPB_D#_CS
DISPB_WR (WRITE_L)
DISPB_DATA[16]
(WRITE_H)
IP31, IP29
IP32, IP30
read point
IP37
IP38
DISPB_DATA
(Input)
Read Data
IP39
IP40
DISPB_DATA
(Output)
IP46,IP44
IP47
IP45, IP43
IP42, IP41

Figure 58. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

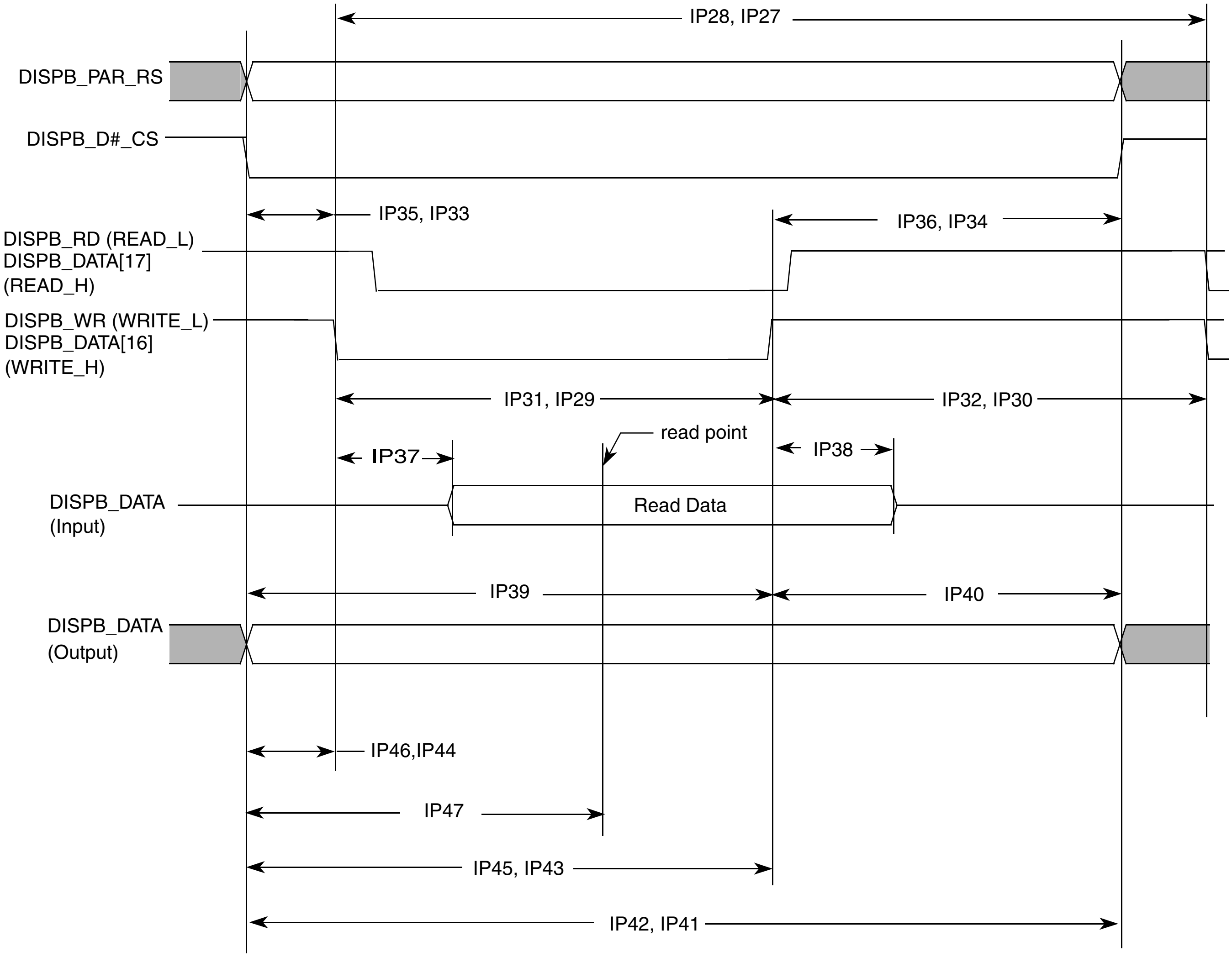

IP28, IP27
DISPB_PAR_RS
DISPB_D#_CS
IP35, IP33
IP36, IP34
DISPB_RD (READ_L)
DISPB_DATA[17]
(READ_H)
DISPB_WR (WRITE_L)
DISPB_DATA[16]
(WRITE_H)
IP31, IP29
IP32, IP30
read point
IP37
IP38
DISPB_DATA
(Input)
Read Data
IP39
IP40
DISPB_DATA
(Output)
IP46,IP44
IP47
IP45, IP43
IP42, IP41

Figure 59. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

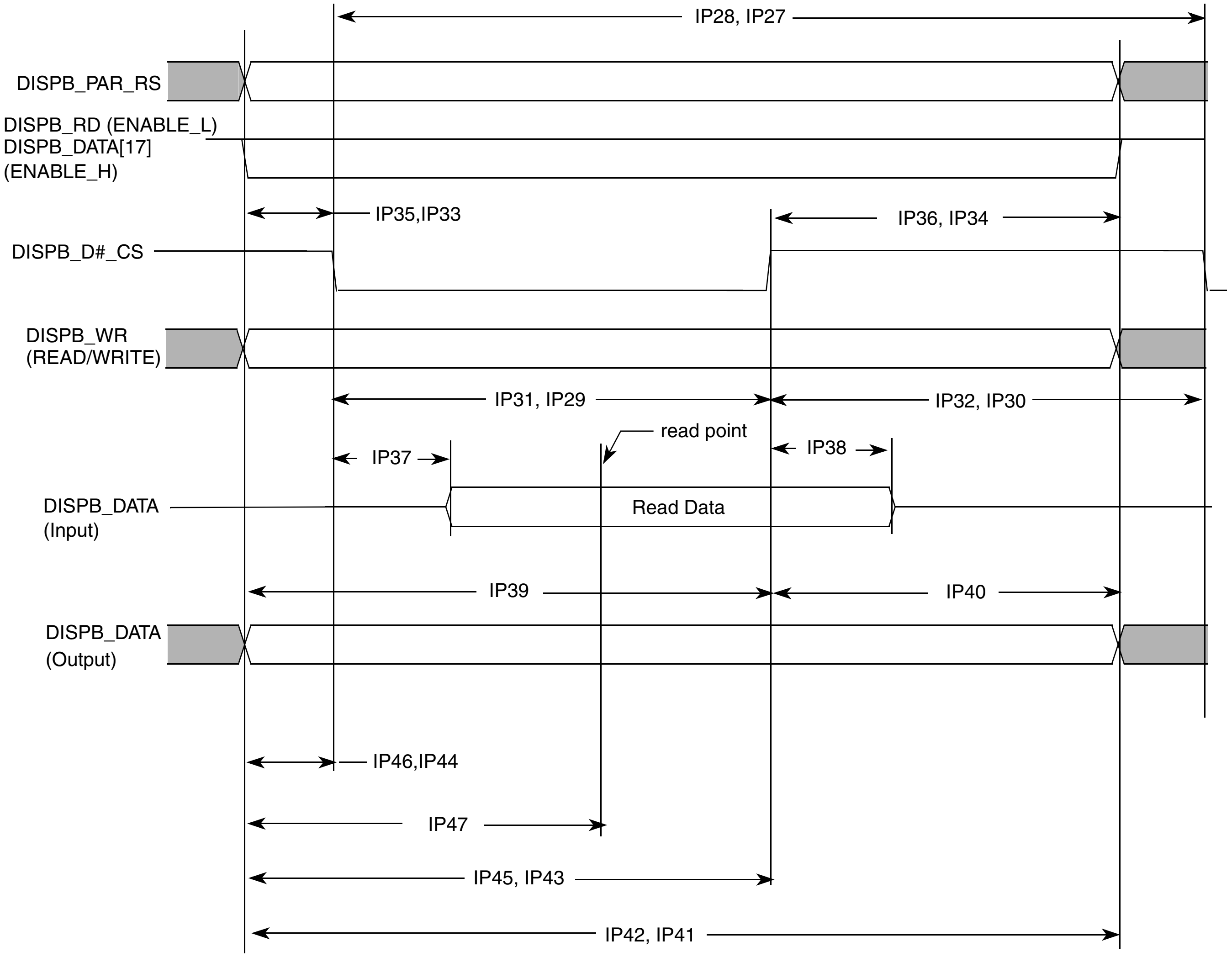
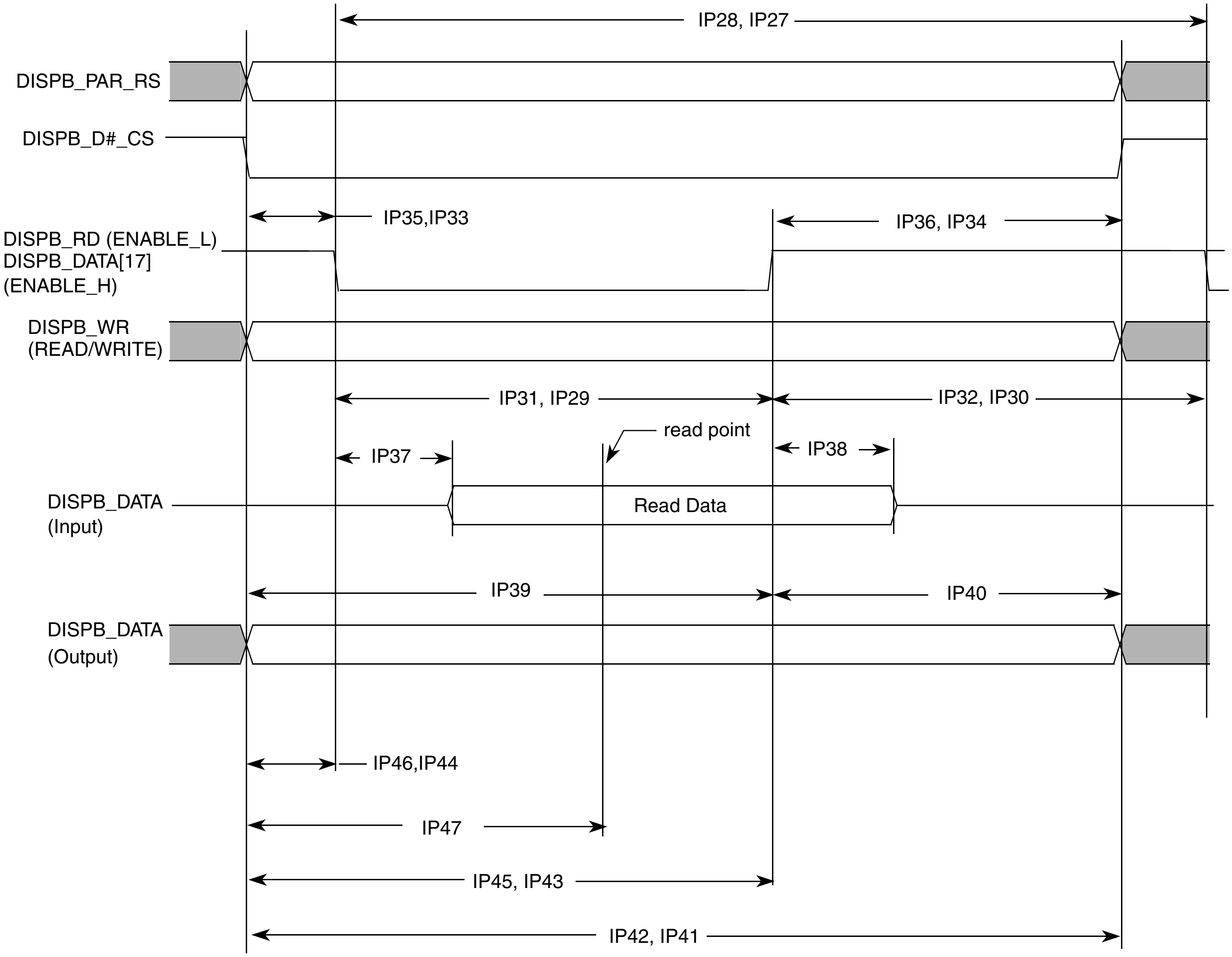

IP28, IP27
DISPB_PAR_RS
DISPB_RD (ENABLE_L)
DISPB_DATA[17]
(ENABLE_H)
IP35,IP33
IP36, IP34
DISPB_D#_CS
DISPB_WR
(READ/WRITE)
IP31, IP29
IP32, IP30
read point
IP37
IP38
DISPB_DATA
(Input)
Read Data
IP39
IP40
DISPB_DATA
(Output)
IP46,IP44
IP47
IP45, IP43
IP42, IP41

Figure 60. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram



IP28, IP27
DISPB_PAR_RS
DISPB_D#_CS
IP35,IP33
IP36, IP34
DISPB_RD (ENABLE_L)
DISPB_DATA[17]
(ENABLE_H)
DISPB_WR
(READ/WRITE)
IP31, IP29
IP32, IP30
read point
IP37
IP38
DISPB_DATA
(Input)
Read Data
IP39
IP40
DISPB_DATA
(Output)
IP46,IP44
IP47
IP45, IP43
IP42, IP41

Figure 61. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Table 58. Asynchronous Parallel Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP29	Read low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP30	Read high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP31	Write low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP32	Write high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns
IP34	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns

Table 58. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP35	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP36	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP37	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP39	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP40	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP41	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP42	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP43	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP44	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP45	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP46	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP47	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

[1] The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device-specific.

[2] Display interface clock period value for read:

$$\mathrm{Tdicpr} = T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{\mathrm{DISP\#\_IF\_CLK\_PER\_RD}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[3] Display interface clock period value for write:

$$\mathrm{Tdicpw} = T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{\mathrm{DISP\#\_IF\_CLK\_PER\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[4] Display interface clock down time for read:

$$\mathrm{Tdicdr} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_DOWN\_RD}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[5] Display interface clock up time for read:

$$\mathrm{Tdicur} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_UP\_RD}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[6] Display interface clock down time for write:

$$\mathrm{Tdicdw} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_DOWN\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[7] Display interface clock up time for write:

$$\mathrm{Tdicuw} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_UP\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

[9] Data read point

$$\text{Tdrp} = T_{\text{HSP\_CLK}} \cdot \text{ceil}\left[\frac{\text{DISP\#\_READ\_EN}}{\text{HSP\_CLK\_PERIOD}}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device – level output delay, board delays, a device – level input delay, an IPU input delay. This value is device specific.

The following parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2, and DI_HSP_CLK_PER registers:

- DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD
- HSP_CLK_PERIOD
- DISP#_IF_CLK_DOWN_WR
- DISP#_IF_CLK_UP_WR
- DISP#_IF_CLK_DOWN_RD
- DISP#_IF_CLK_UP_RD
- DISP#_READ_EN

4.9.13.5 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 62 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux connects the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP*n*_CONF registers ($n = 1, 2$).

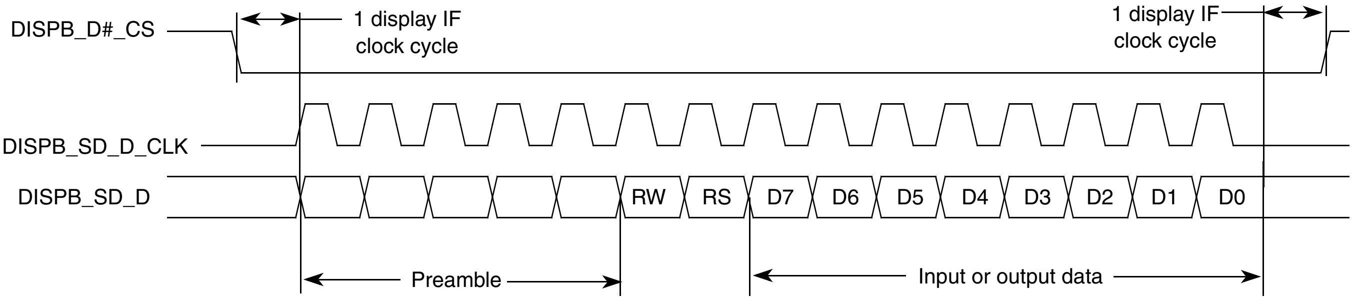

DISPB_D#_CS
1 display IF clock cycle
1 display IF clock cycle
DISPB_SD_D_CLK
DISPB_SD_D
RW
RS
D7
D6
D5
D4
D3
D2
D1
D0
Preamble
Input or output data

Figure 62. 3-Wire Serial Interface Timing Diagram

Figure 63 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

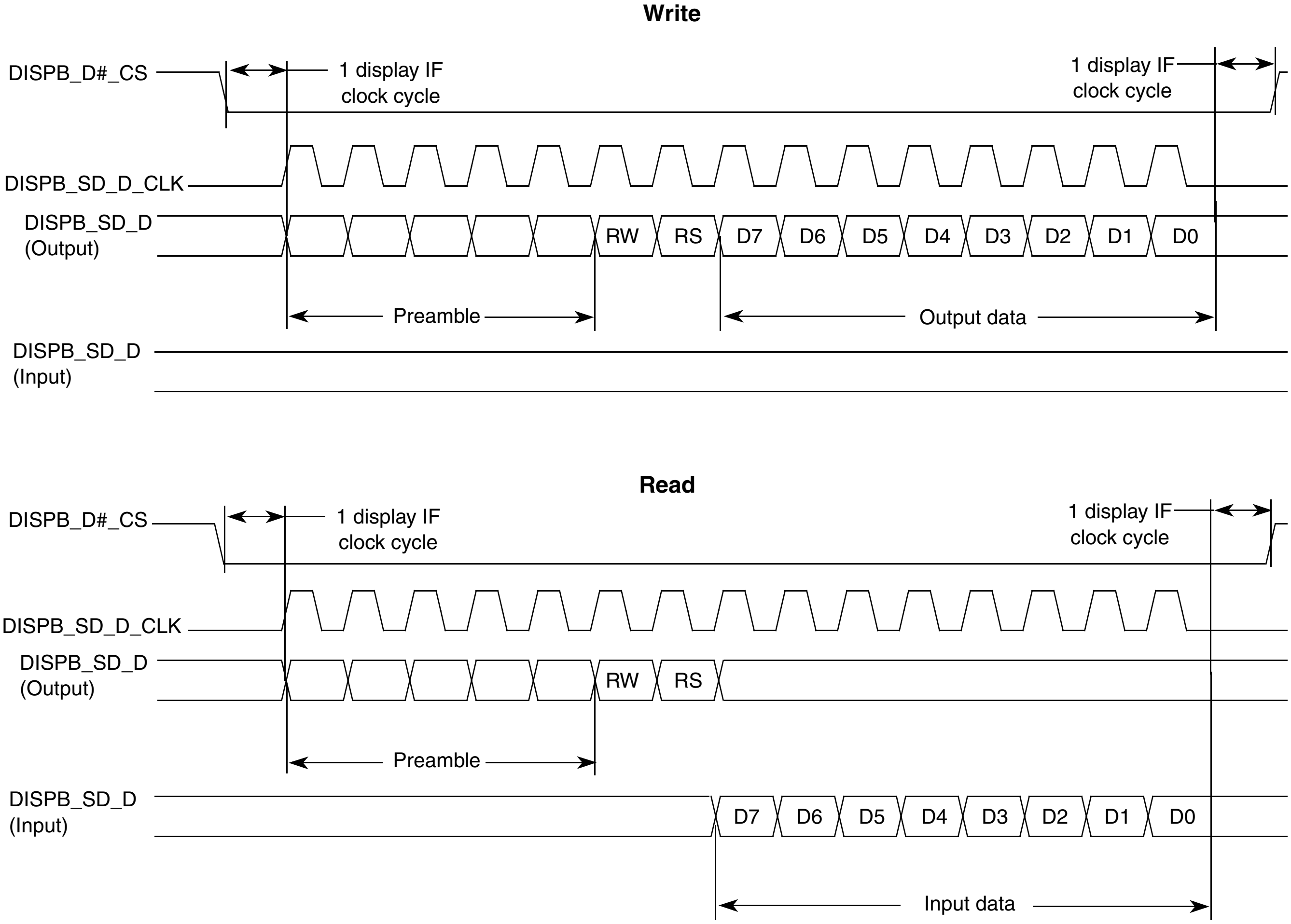

Write
DISPB_D#_CS
1 display IF clock cycle
1 display IF clock cycle
DISPB_SD_D_CLK
DISPB_SD_D (Output)
RW
RS
D7
D6
D5
D4
D3
D2
D1
D0
Preamble
Output data
DISPB_SD_D (Input)
Read
DISPB_D#_CS
1 display IF clock cycle
1 display IF clock cycle
DISPB_SD_D_CLK
DISPB_SD_D (Output)
RW
RS
Preamble
DISPB_SD_D (Input)
D7
D6
D5
D4
D3
D2
D1
D0
Input data

Figure 63. 4-Wire Serial Interface Timing Diagram

Figure 64 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

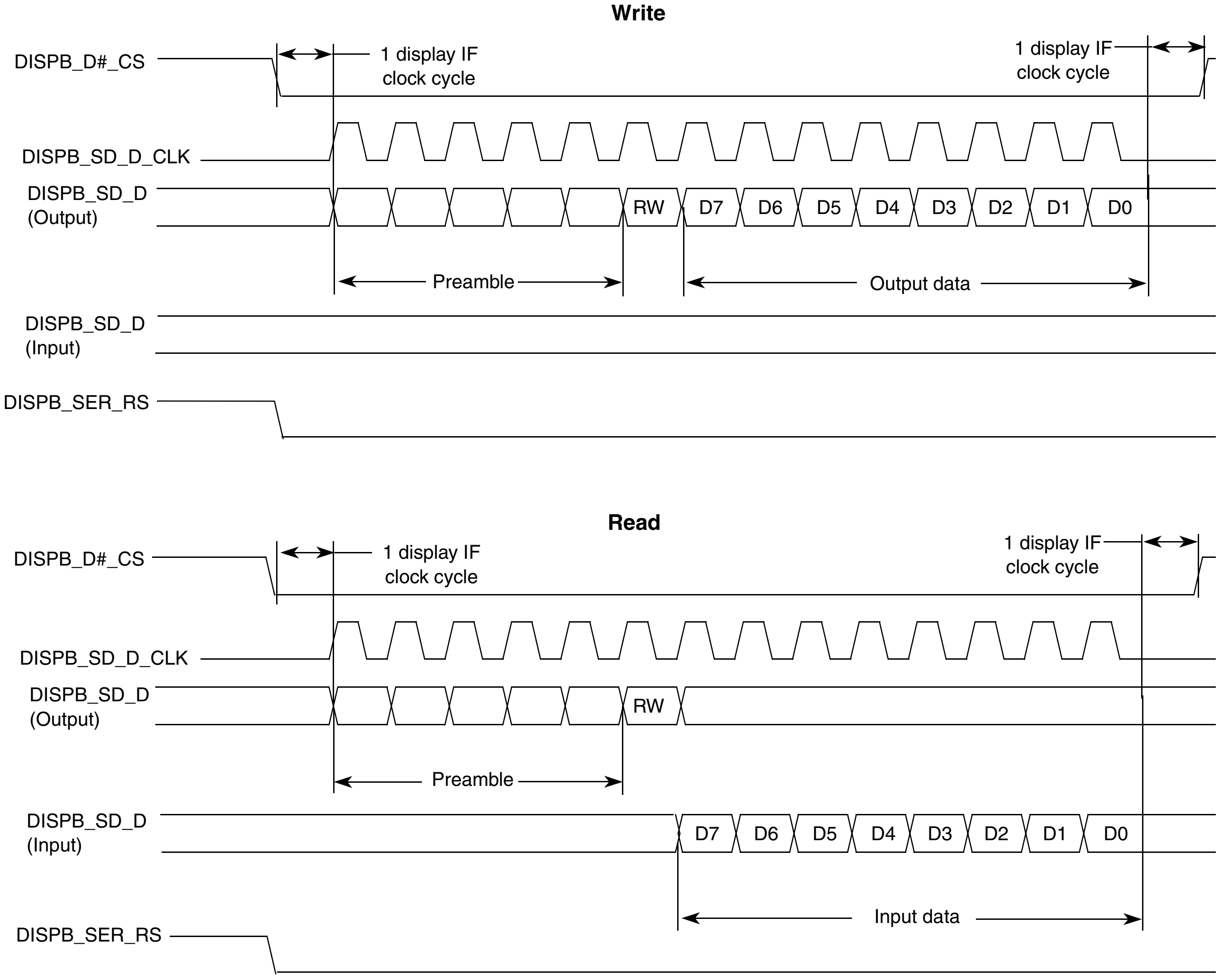

Write
DISPB_D#_CS
1 display IF clock cycle
1 display IF clock cycle
DISPB_SD_D_CLK
DISPB_SD_D (Output)
RW
D7
D6
D5
D4
D3
D2
D1
D0
Preamble
Output data
DISPB_SD_D (Input)
DISPB_SER_RS
Read
DISPB_D#_CS
1 display IF clock cycle
1 display IF clock cycle
DISPB_SD_D_CLK
DISPB_SD_D (Output)
RW
Preamble
DISPB_SD_D (Input)
D7
D6
D5
D4
D3
D2
D1
D0
Input data
DISPB_SER_RS

Figure 64. 5-Wire Serial Interface (Type 1) Timing Diagram

Figure 65 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

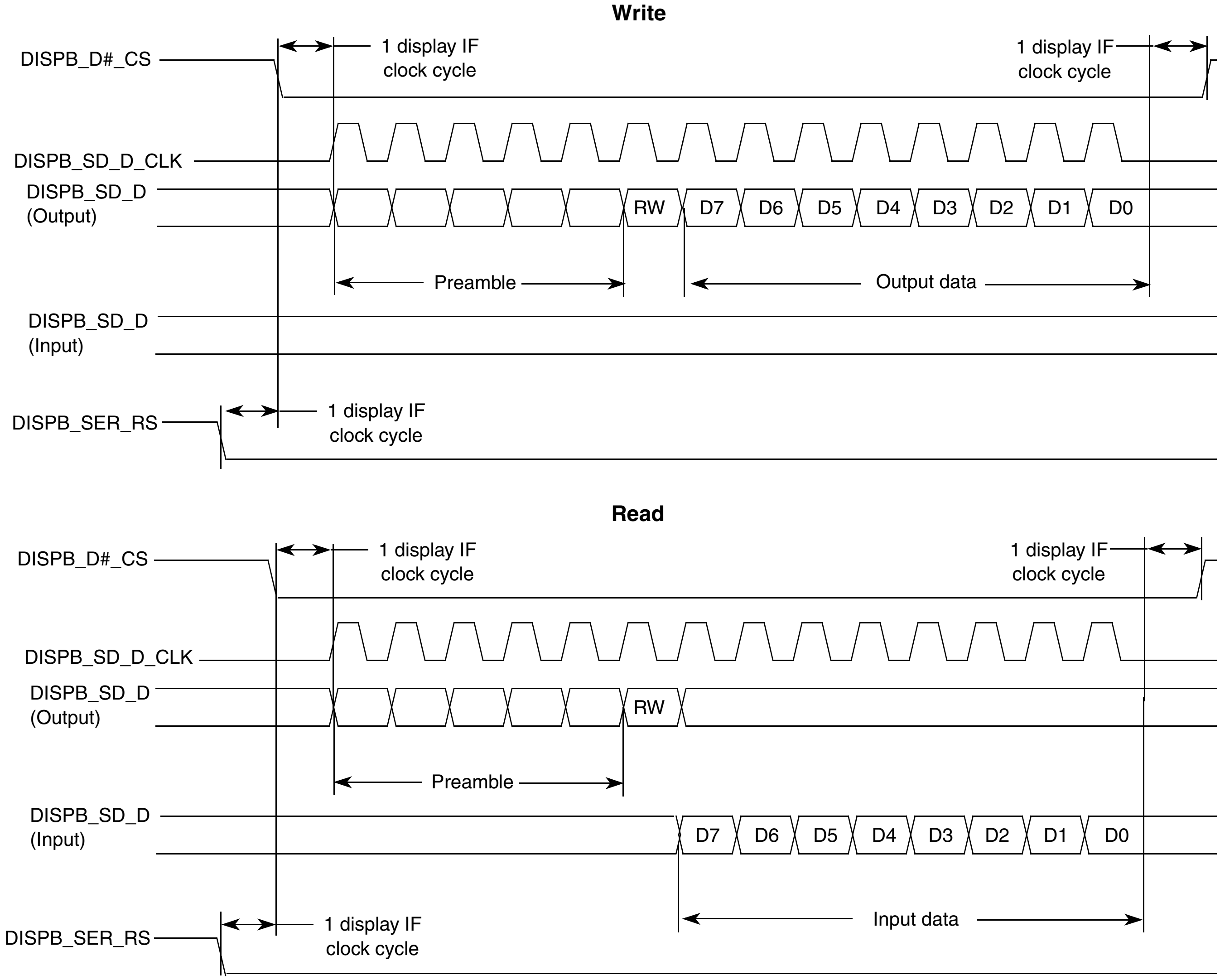

Write
DISPB_D#_CS
1 display IF clock cycle
1 display IF clock cycle
DISPB_SD_D_CLK
DISPB_SD_D (Output)
RW
D7
D6
D5
D4
D3
D2
D1
D0
Preamble
Output data
DISPB_SD_D (Input)
DISPB_SER_RS
1 display IF clock cycle
Read
DISPB_D#_CS
1 display IF clock cycle
1 display IF clock cycle
DISPB_SD_D_CLK
DISPB_SD_D (Output)
RW
Preamble
DISPB_SD_D (Input)
D7
D6
D5
D4
D3
D2
D1
D0
DISPB_SER_RS
1 display IF clock cycle
Input data

Figure 65. 5-Wire Serial Interface (Type 2) Timing Diagram

4.9.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 66 depicts timing of the serial interface. Table 59 lists the timing parameters at display access level.

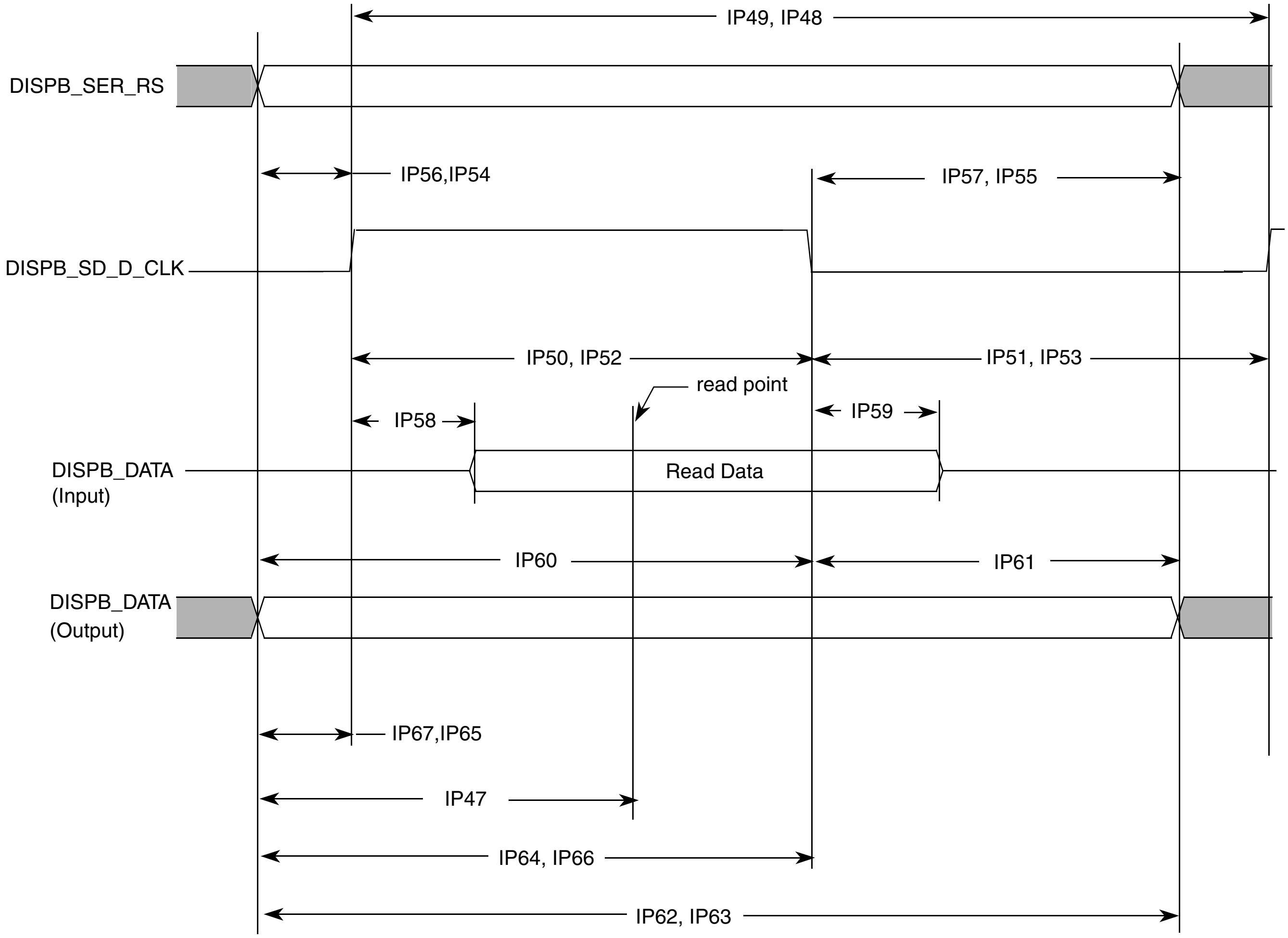

IP49, IP48
DISPB_SER_RS
IP56,IP54
IP57, IP55
DISPB_SD_D_CLK
IP50, IP52
IP51, IP53
read point
IP58
IP59
DISPB_DATA
(Input)
Read Data
IP60
IP61
DISPB_DATA
(Output)
IP67,IP65
IP47
IP64, IP66
IP62, IP63

Figure 66. Asynchronous Serial Interface Timing Diagram

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

[1] The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

[2] Display interface clock period value for read:

$$\mathrm{Tdicpr} = T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{\mathrm{DISP\#\_IF\_CLK\_PER\_RD}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[3] Display interface clock period value for write:

$$\mathrm{Tdicpw} = T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{\mathrm{DISP\#\_IF\_CLK\_PER\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[4] Display interface clock down time for read:

$$\mathrm{Tdicdr} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_DOWN\_RD}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[5] Display interface clock up time for read:

$$\mathrm{Tdicur} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_UP\_RD}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[6] Display interface clock down time for write:

$$\mathrm{Tdicdw} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_DOWN\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[7] Display interface clock up time for write:

$$\mathrm{Tdicuw} = \frac{1}{2}T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{2 \cdot \mathrm{DISP\#\_IF\_CLK\_UP\_WR}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[8] This parameter is a requirement to the display connected to the IPU.

[9] Data read point:

$$\mathrm{Tdrp} = T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{\mathrm{DISP\#\_READ\_EN}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, and an IPU input delay. This value is device specific.

The following parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2, and DI_HSP_CLK_PER registers:

- DISP#_IF_CLK_PER_WR
- DISP#_IF_CLK_PER_RD
- HSP_CLK_PERIOD
- DISP#_IF_CLK_DOWN_WR
- DISP#_IF_CLK_UP_WR
- DISP#_IF_CLK_DOWN_RD
- DISP#_IF_CLK_UP_RD
- DISP#_READ_EN

4.9.14 Memory Stick Host Controller (MSHC)

Figure 67, Figure 68, and Figure 69 depict the MSHC timings, and Table 60 and Table 61 list the timing parameters.

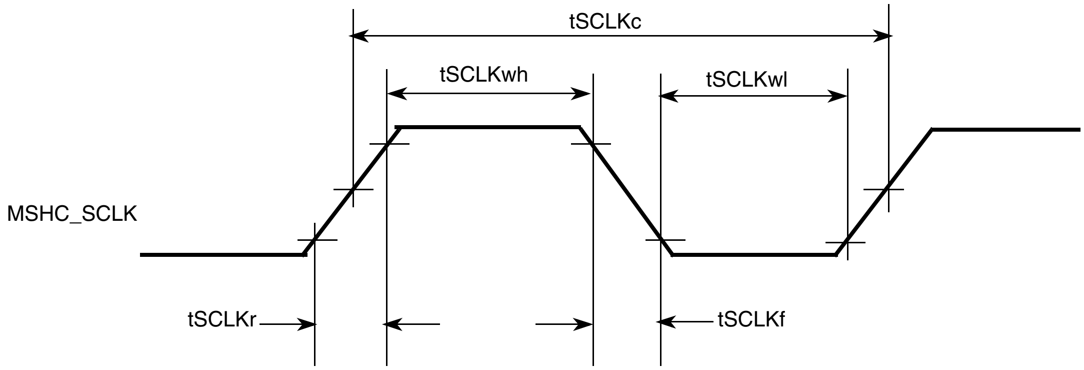


Figure 67. MSHC_CLK Timing Diagram

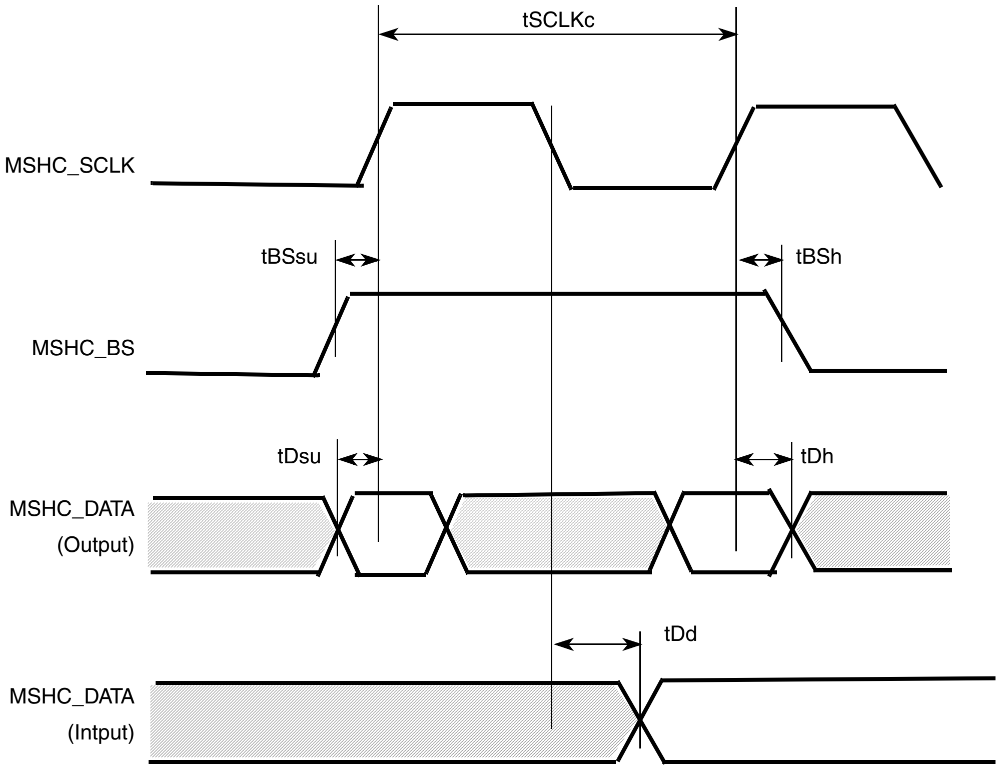

tSCLKc
MSHC_SCLK
tBSsu
tBSh
MSHC_BS
tDsu
tDh
MSHC_DATA
(Output)
tDd
MSHC_DATA
(Intput)

Figure 68. Transfer Operation Timing Diagram (Serial)

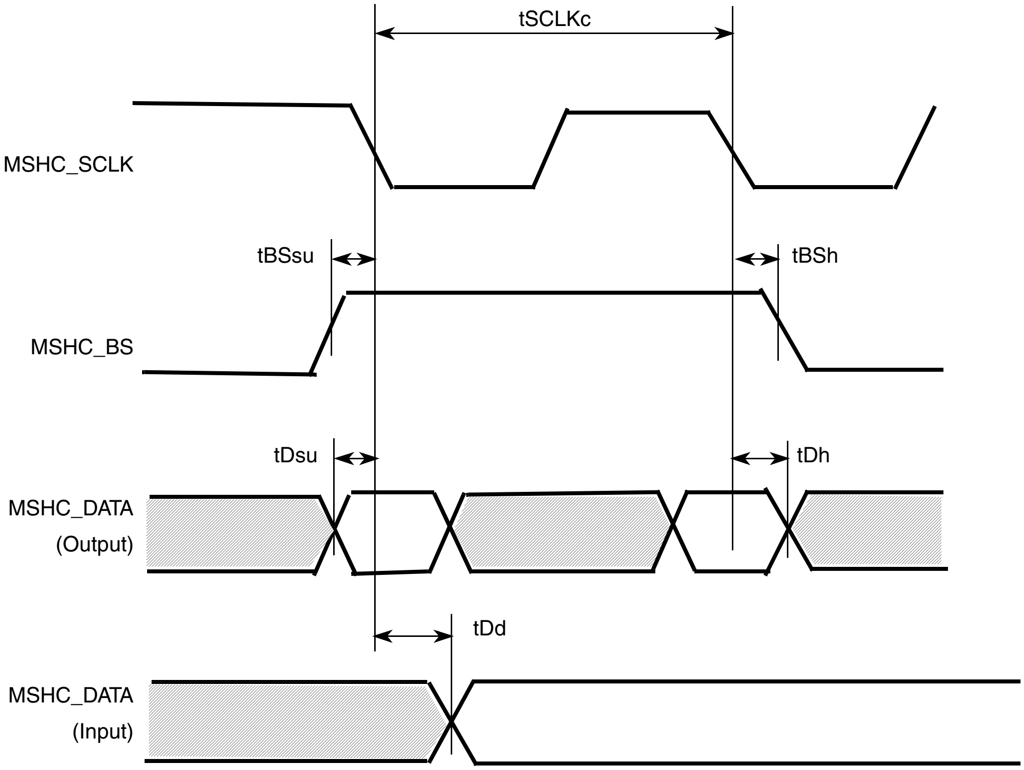

tSCLKc
MSHC_SCLK
tBSsu
tBSh
MSHC_BS
tDsu
tDh
MSHC_DATA
(Output)
tDd
MSHC_DATA
(Input)

Figure 69. Transfer Operation Timing Diagram (Parallel)

NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

Table 60. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns

Table 60. Serial Interface Timing Parameters[1] (continued)

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

[1] Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 61.

Table 61. Parallel Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

[1] Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See the NVCC restrictions described in Table 8.

4.9.15 MediaLB Controller Electrical Specifications

This section describes the electrical information of the MediaLB Controller module.

Table 62. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256 × Fs at 44.0 kHz Typ: 256 × Fs at 48.0 kHz Typ: 512 × Fs at 48.0 kHz Max: 512 × Fs at 48.1 kHz Max: 512 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} TO V_{IH}

Table 62. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLB fall time	t_{mckf}	—	—	3	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	— —	81 40	— —	ns	256 × Fs 512 × Fs
MLBCLK low time	t_{mckl}	31.5 30	37 35.5	— —	ns	256 × Fs 256 × Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512 × Fs 512 × Fs PLL unlocked
MLBCLK high time	t_{mckh}	31.5 30	38 36.5	— —	ns	256 × Fs 256 × Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512 × Fs 512 × Fs PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	2	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	4	—	—	ns	Note[3]

[1] The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

[2] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

[3] The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below unless otherwise noted.

Table 63. MLB Device 1024Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	49.152	49.2544 51.200	MHz	Min: 1024 × Fs at 44.0 kHz Typ: 1024 × Fs at 48.0 kHz Max: 1024 × Fs at 48.1 kHz Max: 1024 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	1	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}	—	—	1	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	—	20.3	—	ns	—
MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3	—	ns	PLL unlocked

Table 63. MLB Device 1024Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2	— —	ns	PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	0.7	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	2	—	—	ns	Note[3]

[1] The MLB Controller can shut off MLBCLK to place MediaLB in a low-power state.

[2] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

[3] The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

4.9.16 1-Wire Timing Specifications

Figure 70 depicts the RPP timing, and Table 64 lists the RPP timing parameters.

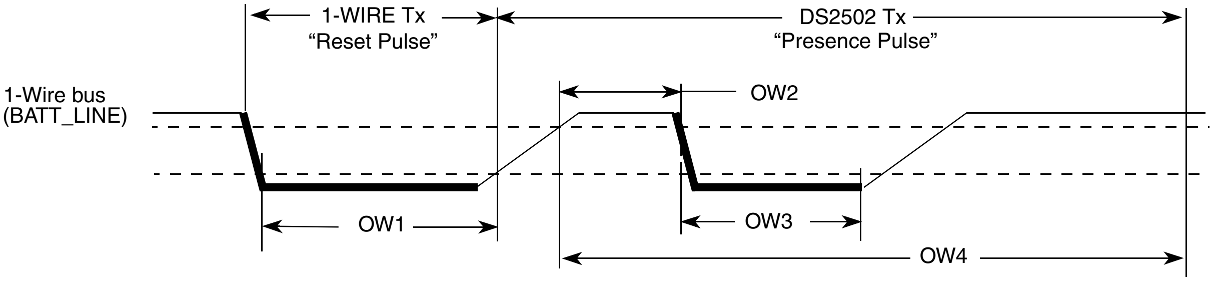


Figure 70. Reset and Presence Pulses (RPP) Timing Diagram

Table 64. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset time low	t_{RSTL}	480	511	—	µs
OW2	Presence detect high	t_{PDH}	15	—	60	µs
OW3	Presence detect low	t_{PDL}	60	—	240	µs
OW4	Reset time high	t_{RSTH}	480	512	—	µs

Figure 71 depicts write 0 sequence timing, and Table 65 lists the timing parameters.

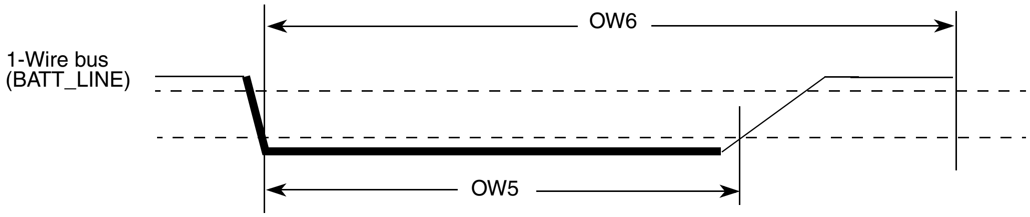


Figure 71. Write 0 Sequence Timing Diagram

Table 65. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	µs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	µs

Figure 72 shows write 1 sequence timing, and Figure 73 depicts the read sequence timing. Table 66 lists the timing parameters.

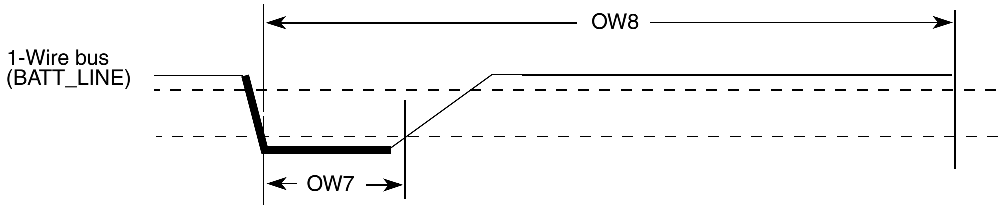


Figure 72. Write 1 Sequence Timing Diagram

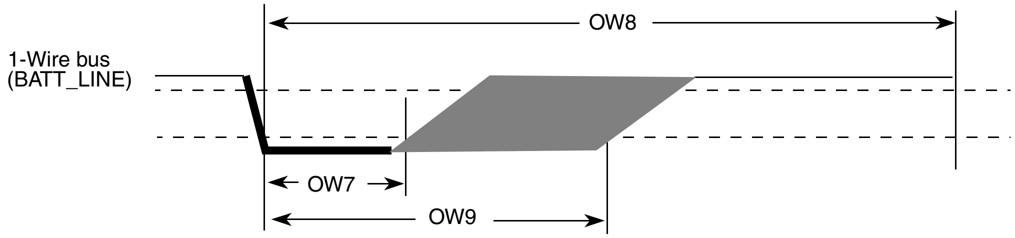


Figure 73. Read Sequence Timing Diagram

Table 66. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1/read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

4.9.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes (not available for the MCIMX351). Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.9.17.1 General Timing Requirements

Table 67 and Figure 74 define the AC characteristics of the interface signals on all data transfer modes.

Table 67. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface[1]	S_{rise}[1]	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface[1]	S_{fall}[1]	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

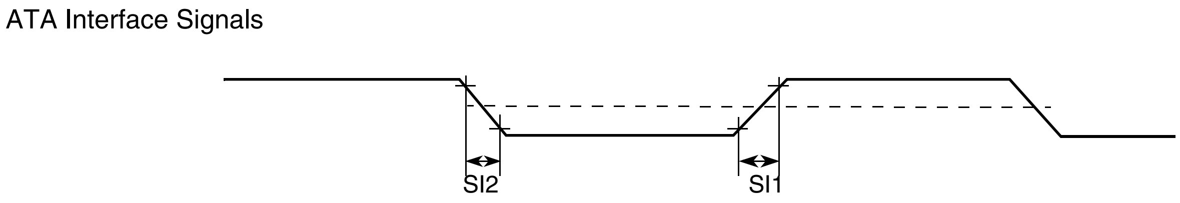


Figure 74. ATA Interface Signals Timing Diagram

4.9.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When ata_buffer_en is negated, the bus drives from device to host. Steering of the signal is such that contention on the host and device tri-state buses is always avoided.

4.9.17.3 Timing Parameters

Table 68 shows the parameters used in the timing equations. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay, and the cable skew.

Table 68. ATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (ipg_clk_ata)	Peripheral clock frequency
ti_ds	Set-up time **ata_data** to **ata_iordy** edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time **ata_iordy** edge to **ata_data** (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en**	12.0 ns
tsu	Set-up time **ata_data** to bus clock L-to-H	8.5 ns
tsui	Set-up time **ata_iordy** to bus clock H-to-L	8.5 ns
thi	Hold time **ata_iordy** to bus clock H to L	2.5 ns
tskew1	Maximum difference in propagation delay bus clock L-to-H to any of following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en**	7 ns
tskew2	Maximum difference in buffer propagation delay for any of following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en**	Transceiver
tskew3	Maximum difference in buffer propagation delay for any of following signals **ata_iordy, ata_data (read)**	Transceiver
tbuf	Maximum buffer propagation delay	Transceiver
tcable1	Cable propagation delay for **ata_data**	Cable
tcable2	Cable propagation delay for control signals **ata_dior, ata_diow, ata_iordy, ata_dmack**	Cable
tskew4	Maximum difference in cable propagation delay between **ata_iordy** and **ata_data (read)**	Cable
tskew5	Maximum difference in cable propagation delay between (**ata_dior, ata_diow, ata_dmack)** and **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)**	Cable
tskew6	Maximum difference in cable propagation delay without accounting for ground bounce	Cable

[1] Values provided where applicable.

4.9.17.4 PIO Mode Timing

Figure 75 shows timing for PIO read, and Table 69 lists the timing parameters for PIO read.

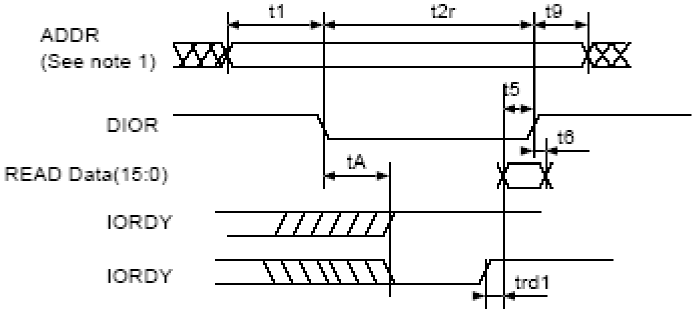


Figure 75. PIO Read Timing Diagram

Table 69. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 75	Value	Controlling Variable
t1	t1	t1 (min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min.) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min.) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
trd	trd1	trd1 (max.) = (–trd) + (tskew3 + tskew4) trd1 (min.) = (time_pio_rdx – 0.5) × T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

Figure 76 shows timing for PIO write, and Table 70 lists the timing parameters for PIO write.

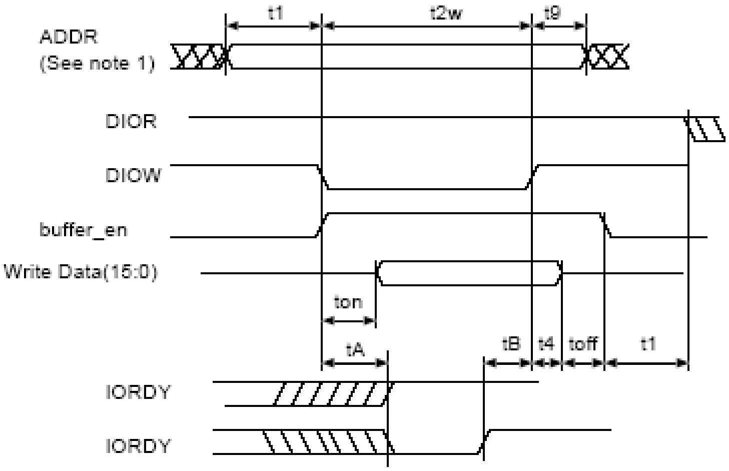


Figure 76. PIO Write Timing Diagram

Table 70. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 76	Value	Controlling Variable
t1	t1	t1 (min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min.) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min.) = (time_2w – time_on) × T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min.) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 77 shows timing for MDMA read, and Figure 78 shows timing for MDMA write. Table 71 lists the timing parameters for MDMA read and write.

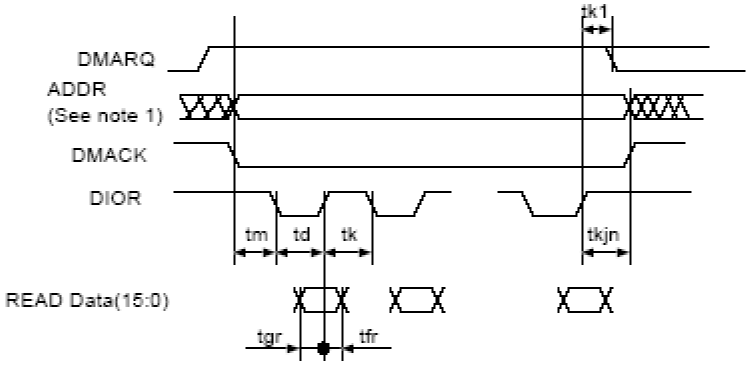

tk1
DMARQ
ADDR
(See note 1)
DMACK
DIOR
tm
td
tk
tkjn
READ Data(15:0)
tgr
tfr

Figure 77. MDMA Read Timing Diagram

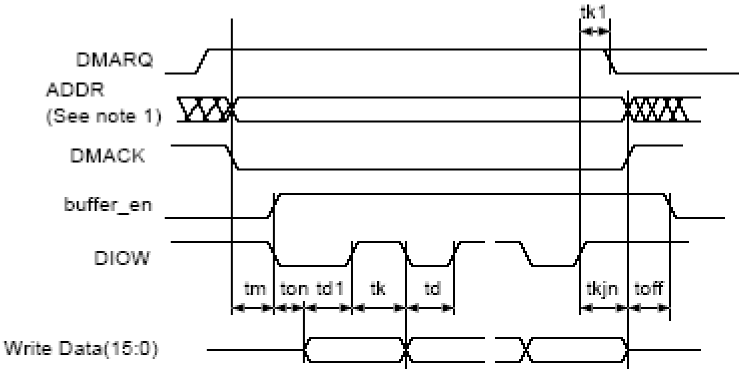

tk1
DMARQ
ADDR
(See note 1)
DMACK
buffer_en
DIOW
tm
ton
td1
tk
td
tkjn
toff
Write Data(15:0)

Figure 78. MDMA Write Timing Diagram

Table 71. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 77, Figure 78	Value	Controlling Variable
tm, ti	tm	tm (min.) = ti (min.) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min.) = td (min.) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min.) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min.) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr (min. – read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min. – drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min. – drive) = 0	—
tg(write)	—	tg (min. – write) = time_d × T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min. – write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max.) = (time_d + time_k–2) × T – (tsu + tco + 2 × tbuf + 2 × tcable2)	time_d, time_k

Table 71. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 77, Figure 78	Value	Controlling Variable
tn, tj	tkjn	tn = tj = tkjn = (max.(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.9.17.5 UDMA-In Timing

Figure 79 shows timing when the UDMA-in transfer starts, Figure 80 shows timing when the UDMA-in host terminates transfer, Figure 81 shows timing when the UDMA-in device terminates transfer, and Table 72 lists the timing parameters for the UDMA-in burst.

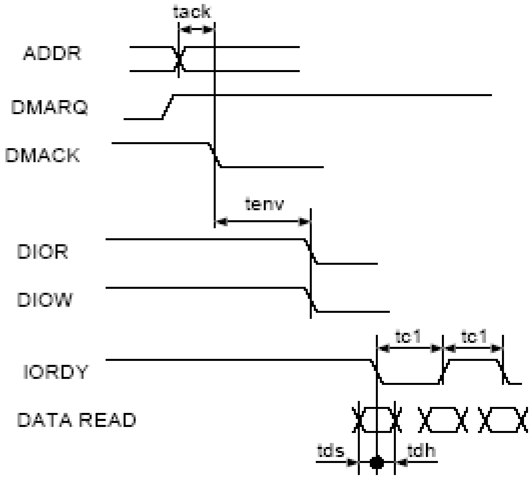

tack
ADDR
DMARQ
DMACK
tenv
DIOR
DIOW
tc1
tc1
IORDY
DATA READ
tds
tdh

Figure 79. UDMA-In Transfer Starts Timing Diagram

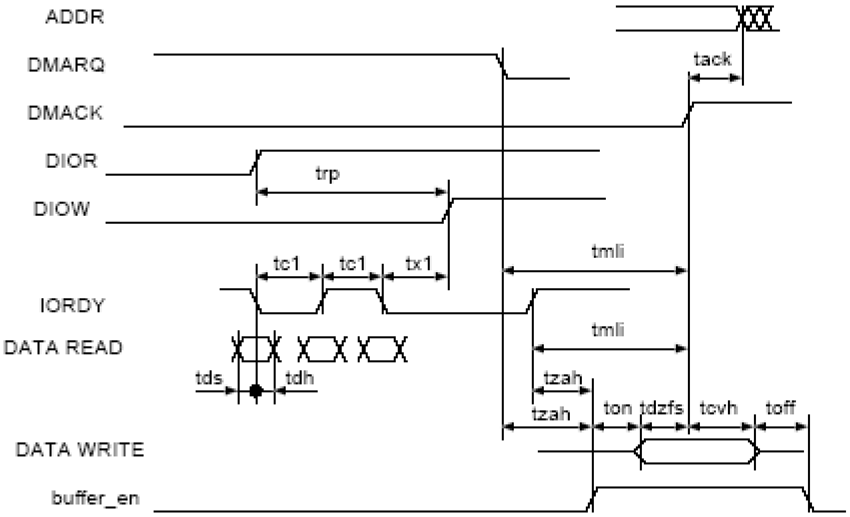

ADDR
DMARQ
tack
DMACK
DIOR
trp
DIOW
tc1
tc1
tx1
tmli
IORDY
DATA READ
tmli
tds
tdh
tzah
tzah
ton
tdzfs
tcvh
toff
DATA WRITE
buffer_en

Figure 80. UDMA-In Host Terminates Transfer Timing Diagram

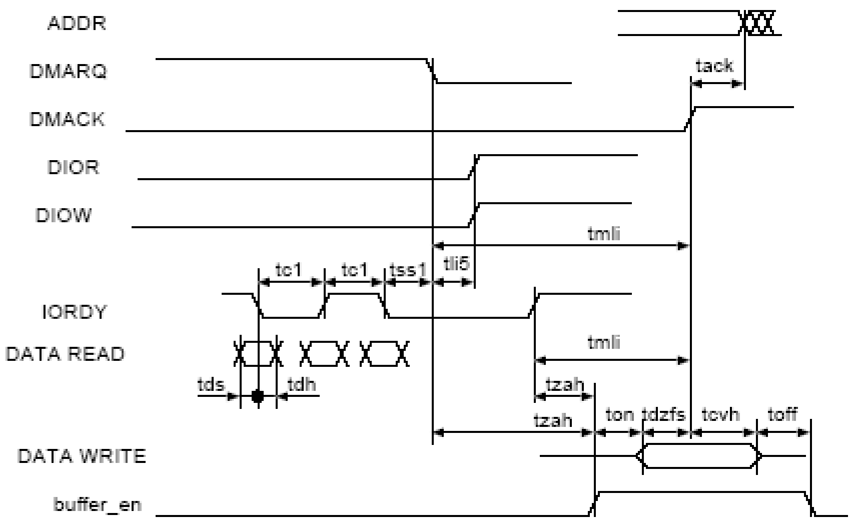

ADDR
DMARQ
DMACK
DIOR
DIOW
IORDY
DATA READ
DATA WRITE
buffer_en
tack
tmli
tc1
tc1
tss1
tli5
tmli
tds
tdh
tzah
tzah
ton
tdzfs
tcvh
toff

Figure 81. UDMA-In Device Terminates Transfer Timing Diagram

Table 72. UDMA-In Burst Timing Parameters

ATA Parameter	Parameters from Figure 79, Figure 80, Figure 81	Description	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew > T	T big enough
trp	trp	trp (min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff large enough to avoid bus contention.

4.9.17.6 UDMA-Out Timing

Figure 82 shows timing when the UDMA-out transfer starts, Figure 83 shows timing when the UDMA-out host terminates transfer, Figure 84 shows timing when the UDMA-out device terminates transfer, and Table 73 lists the timing parameters for the UDMA-out burst.

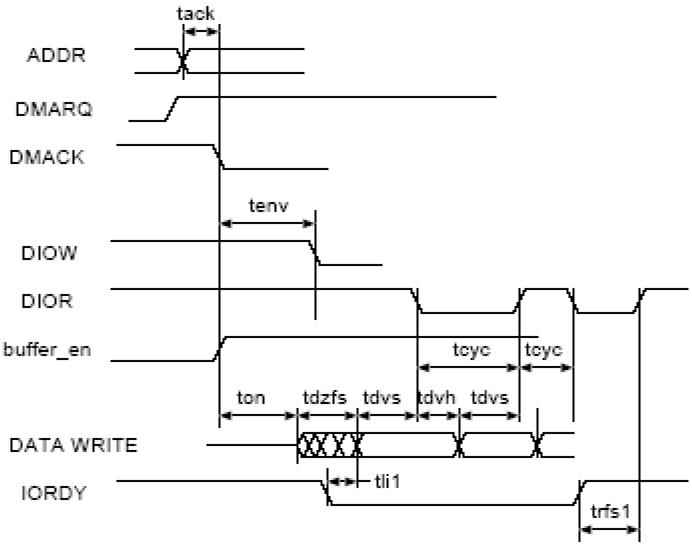

tack
ADDR
DMARQ
DMACK
tenv
DIOW
DIOR
buffer_en
tcyc
tcyc
ton
tdzfs
tdvs
tdvh
tdvs
DATA WRITE
tli1
IORDY
trfs1

Figure 82. UDMA-Out Transfer Starts Timing Diagram

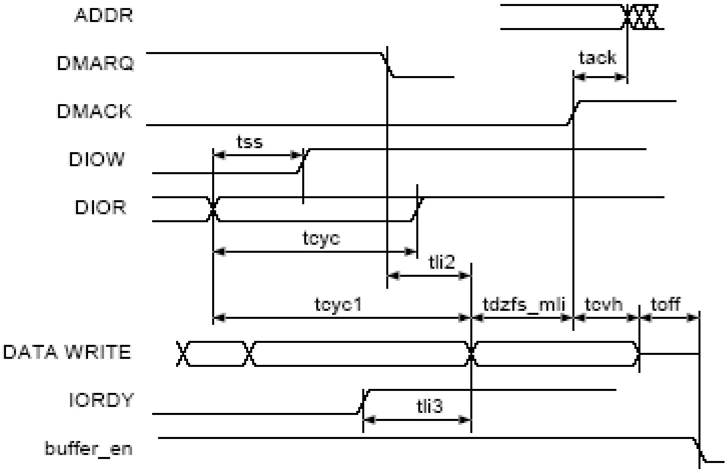

ADDR
DMARQ
tack
DMACK
tss
DIOW
DIOR
tcyc
tli2
tcyc1
tdzfs_mli
tcvh
toff
DATA WRITE
IORDY
tli3
buffer_en

Figure 83. UDMA-Out Host Terminates Transfer Timing Diagram

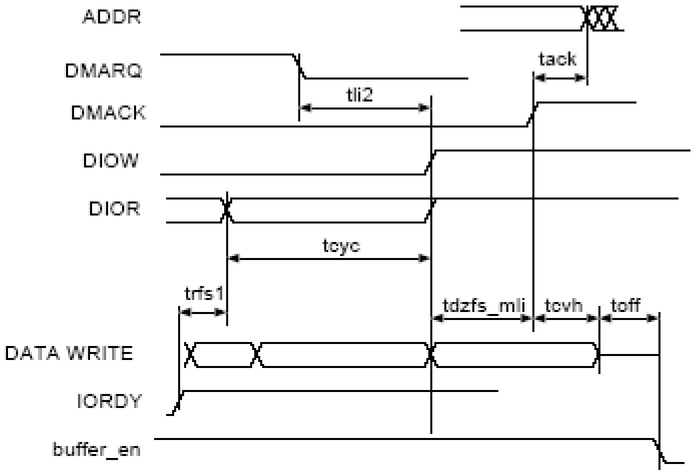


Figure 84. UDMA-Out Device Terminates Transfer Timing Diagram

Table 73. UDMA-Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 82, Figure 83, Figure 84	Value	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs ×T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli = max. (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.9.18 Parallel Interface (ULPI) Timing

Electrical and timing specifications of the parallel interface are presented in the subsequent sections.

Table 74. Signal Definitions—Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to the clock.
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

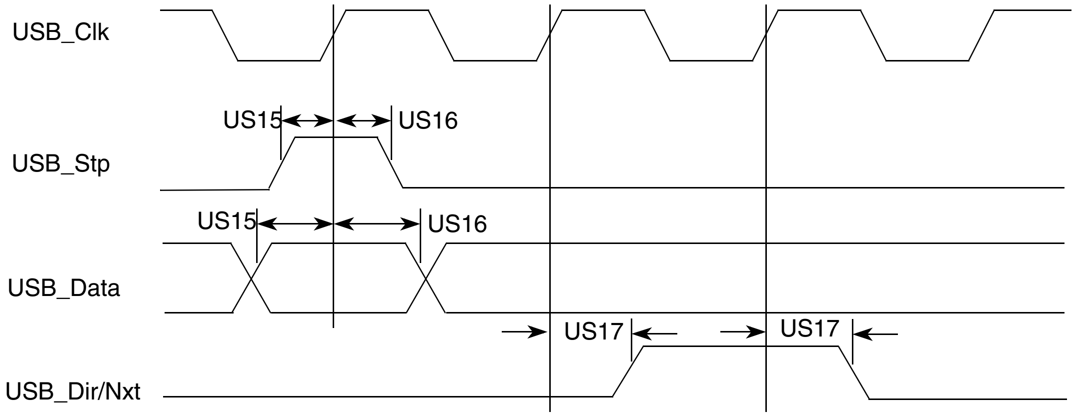


Figure 85. USB Transmit/Receive Waveform in Parallel Mode

Table 75. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Min.	Max.	Unit	Conditions / Reference Signal
US15	USB_TXOE_B	—	6.0	ns	10 pF
US16	USB_DAT_VP	—	0.0	ns	10 pF
US17	USB_SE0_VM	—	9.0	ns	10 pF

4.9.19 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. The modulated signal of the module is observed at this pin. It can be viewed as a clock signal whose period and duty cycle can be varied with different settings of the PWM. The smallest period is two ipg_clk periods with duty cycle of 50 percent.

4.9.20 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 86 depicts the SJC test clock input timing. Figure 87 depicts the SJC boundary scan timing, Figure 88 depicts the SJC test access port, Figure 89 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 76 lists the SJC timing parameters.

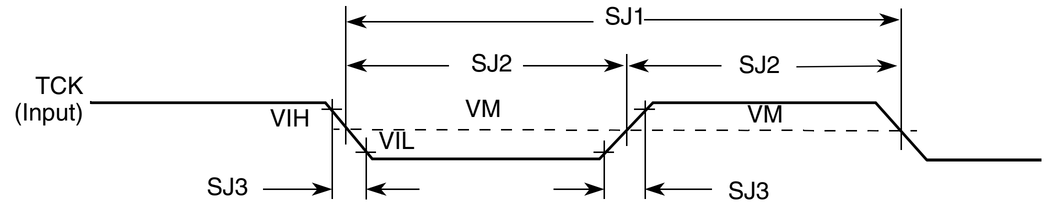

SJ1
SJ2
SJ2
TCK
(Input)
VIH
VM
VM
VIL
SJ3
SJ3

Figure 86. Test Clock Input Timing Diagram

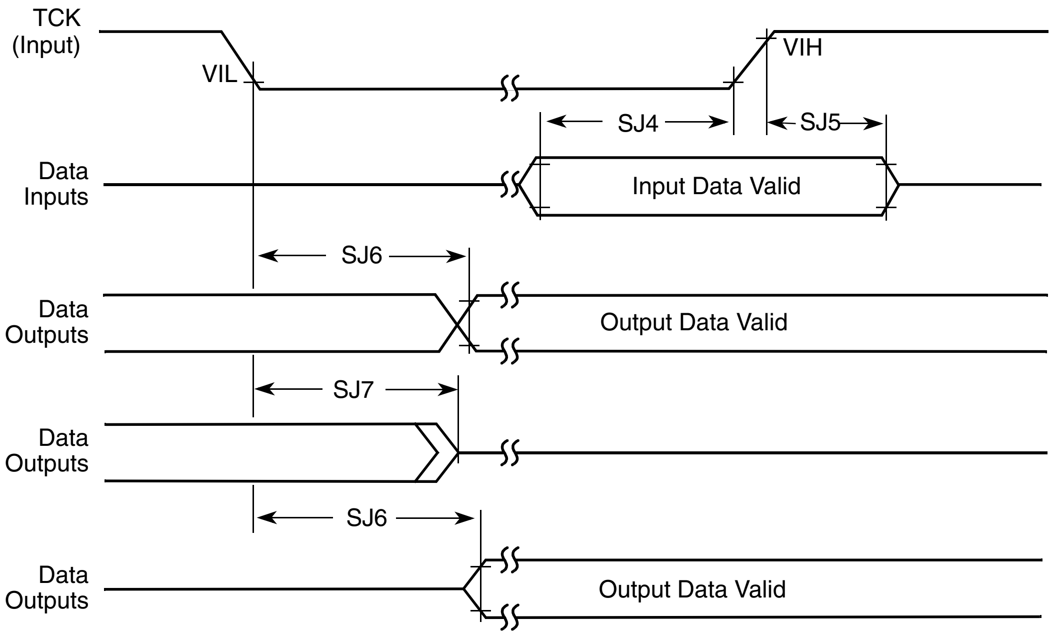

TCK
(Input)
VIL
VIH
SJ4
SJ5
Data
Inputs
Input Data Valid
SJ6
Data
Outputs
Output Data Valid
SJ7
Data
Outputs
SJ6
Data
Outputs
Output Data Valid

Figure 87. Boundary Scan (JTAG) Timing Diagram

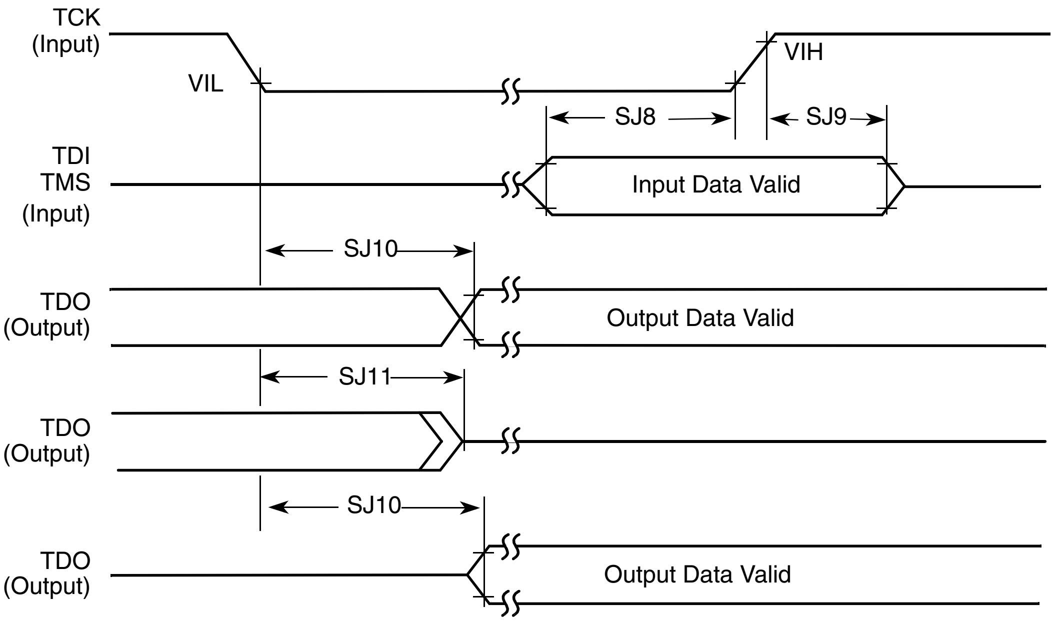

TCK
(Input)
VIL
VIH
SJ8
SJ9
TDI
TMS
(Input)
Input Data Valid
SJ10
TDO
(Output)
Output Data Valid
SJ11
TDO
(Output)
SJ10
TDO
(Output)
Output Data Valid

Figure 88. Test Access Port Timing Diagram

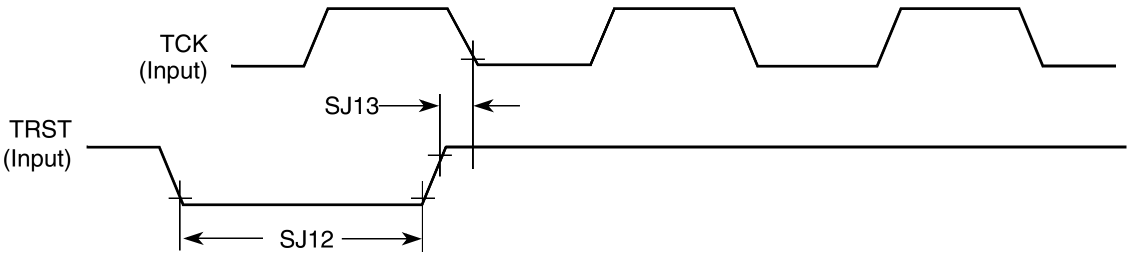

TCK
(Input)
SJ13
TRST
(Input)
SJ12

Figure 89. $\overline{\text{TRST}}$ Timing Diagram

Table 76. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

Table 76. SJC Timing Parameters (continued)

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

[1] On cases where SDMA TAP is put in the chain, the max. TCK frequency is limited by max. ratio of 1:8 of SDMA core frequency to TCK limitation. This implies max. frequency of 8.25 MHz (or 121.2 ns) for 66 MHz IPG clock.

[2] V_M = mid point voltage

4.9.21 SPDIF Timing

SPDIF data is sent using bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Figure 90 shows SPDIF timing parameters, including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK). for SPDIF in Tx mode.

Table 77. SPDIF Timing Parameters

Parameters	Symbol	Timing Parameter Range		Units
		Min.	Max.	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	— — —	— — —	1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30 pf) • Skew • Transition rising • Transition falling	— — —	— — —	1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

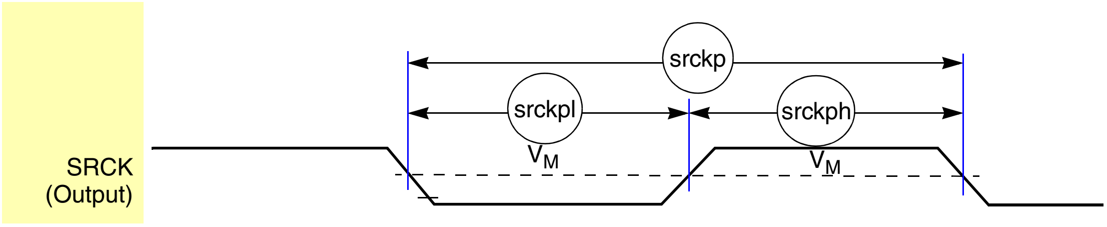


Figure 90. SRCK Timing

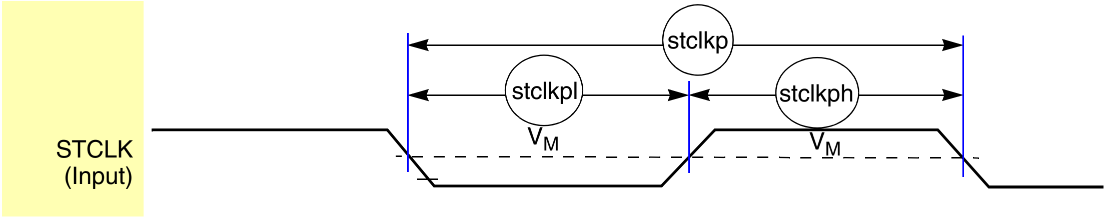


Figure 91. STCLK Timing

4.9.22 SSI Electrical Specifications

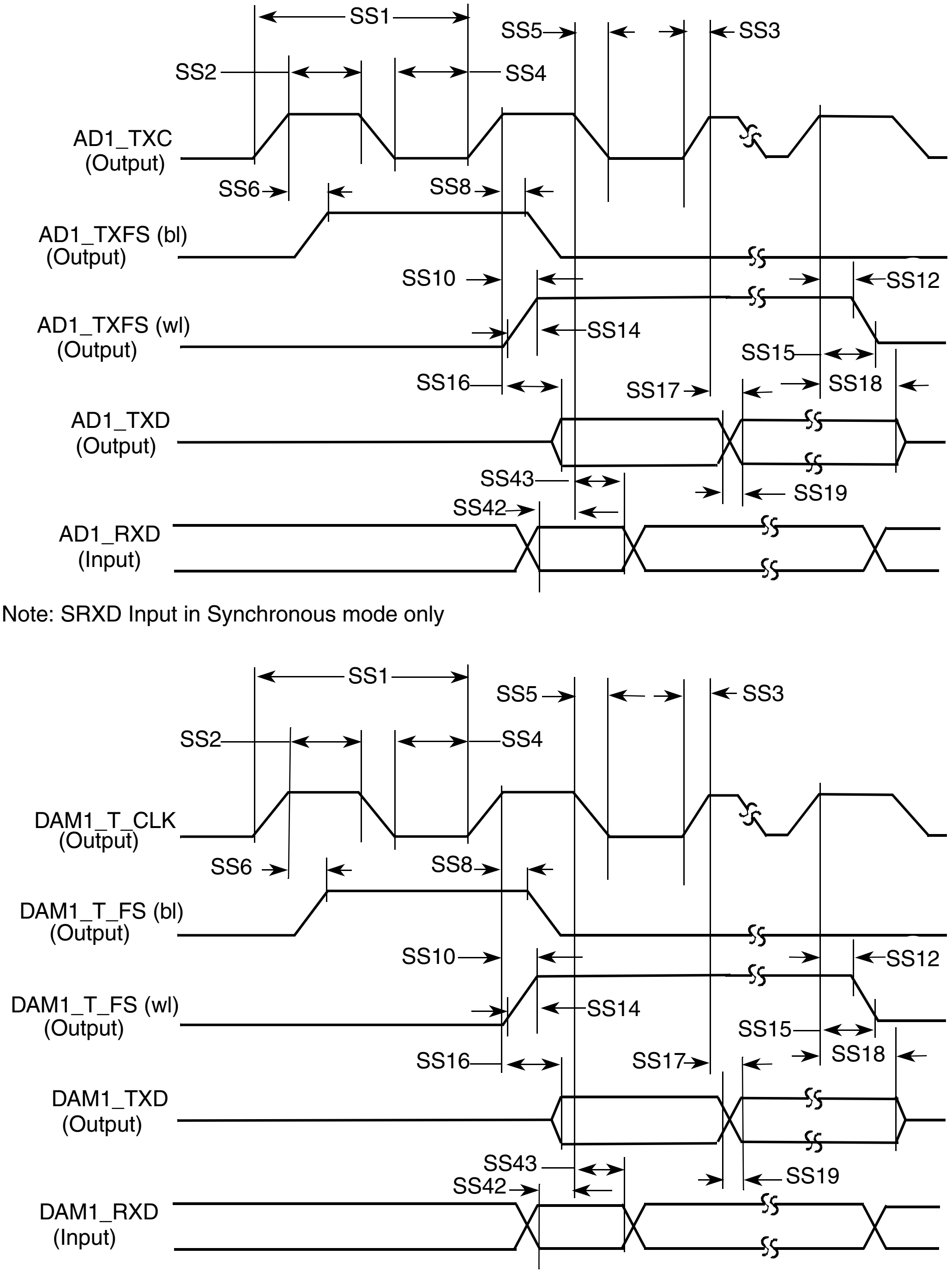
This section describes electrical characteristics of the SSI.

NOTE

- All of the timing for the SSI is given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timing is on AUDMUX signals when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the transmit and receive sections of the SSI, respectively.
- For internal frame sync operations using the external clock, the FS timing will be the same as that of Tx Data (for example, during AC97 mode of operation).

4.9.22.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter timing with internal clock, and Table 78 lists the timing parameters.


SS1
SS5
SS3
SS2
SS4
AD1_TXC
(Output)
SS6
SS8
AD1_TXFS (bl)
(Output)
SS10
SS12
AD1_TXFS (wl)
(Output)
SS14
SS15
SS16
SS17
SS18
AD1_TXD
(Output)
SS43
SS42
SS19
AD1_RXD
(Input)
SS1
SS5
SS3
SS2
SS4
DAM1_T_CLK
(Output)
SS6
SS8
DAM1_T_FS (bl)
(Output)
SS10
SS12
DAM1_T_FS (wl)
(Output)
SS14
SS15
SS16
SS17
SS18
DAM1_TXD
(Output)
SS43
SS42
SS19
DAM1_RXD
(Input)

Note: SRXD Input in Synchronous mode only

Note: SRXD Input in Synchronous mode only

Figure 92. SSI Transmitter with Internal Clock Timing Diagram

Table 78. SSI Transmitter with Internal Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6	ns
SS15	(Tx/Rx) Internal FS fall time	—	6	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0	—	ns
SS52	Loading	—	25	pF

4.9.22.2 SSI Receiver Timing with Internal Clock

Figure 93 depicts the SSI receiver timing with internal clock. Table 79 lists the timing parameters shown in Figure 93.

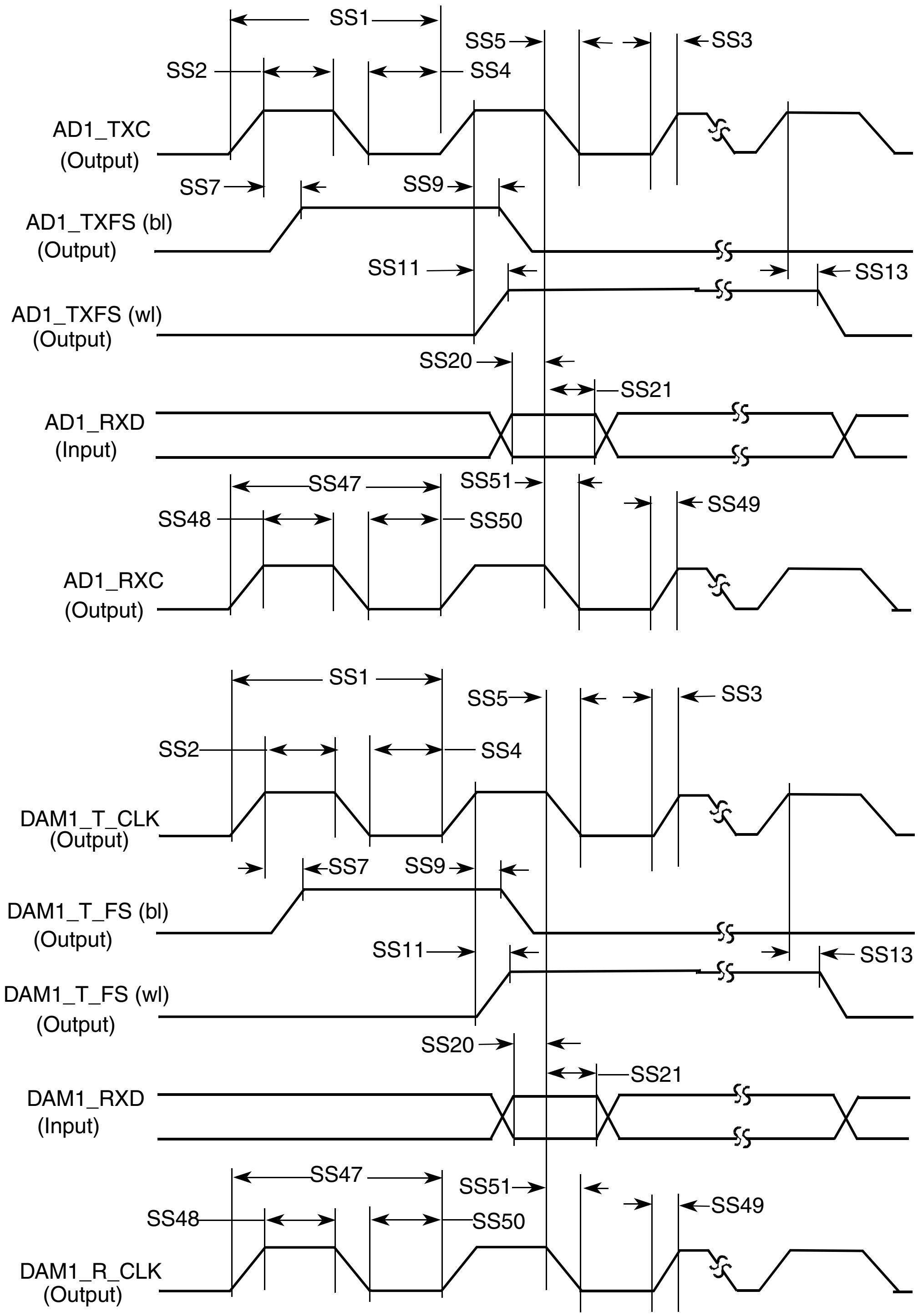

SS1
SS5
SS3
SS2
SS4
AD1_TXC
(Output)
SS7
SS9
AD1_TXFS (bl)
(Output)
SS11
SS13
AD1_TXFS (wl)
(Output)
SS20
SS21
AD1_RXD
(Input)
SS47
SS51
SS48
SS50
SS49
AD1_RXC
(Output)
SS1
SS5
SS3
SS2
SS4
DAM1_T_CLK
(Output)
SS7
SS9
DAM1_T_FS (bl)
(Output)
SS11
SS13
DAM1_T_FS (wl)
(Output)
SS20
SS21
DAM1_RXD
(Input)
SS47
SS51
SS49
SS48
SS50
DAM1_R_CLK
(Output)

Figure 93. SSI Receiver with Internal Clock Timing Diagram

Table 79. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

4.9.22.3 SSI Transmitter Timing with External Clock

Figure 94 depicts the SSI transmitter timing with external clock, and Table 80 lists the timing parameters.

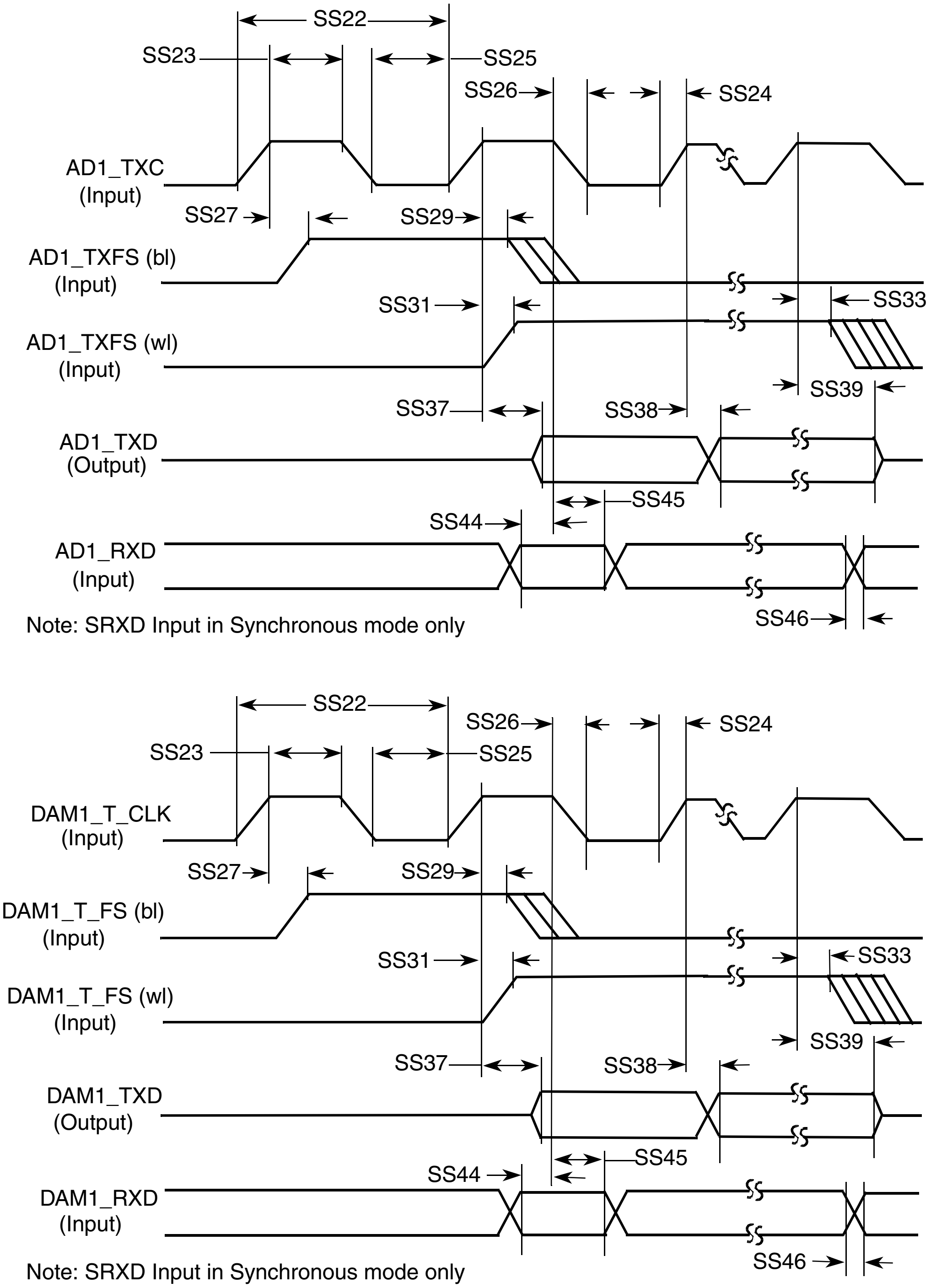

SS22
SS23
SS25
SS26
SS24
AD1_TXC
(Input)
SS27
SS29
AD1_TXFS (bl)
(Input)
SS31
SS33
AD1_TXFS (wl)
(Input)
SS39
SS37
SS38
AD1_TXD
(Output)
SS45
SS44
AD1_RXD
(Input)
Note: SRXD Input in Synchronous mode only
SS46
SS22
SS26
SS24
SS23
SS25
DAM1_T_CLK
(Input)
SS27
SS29
DAM1_T_FS (bl)
(Input)
SS31
SS33
DAM1_T_FS (wl)
(Input)
SS39
SS37
SS38
DAM1_TXD
(Output)
SS45
SS44
DAM1_RXD
(Input)
Note: SRXD Input in Synchronous mode only
SS46

Figure 94. SSI Transmitter with External Clock Timing Diagram

Table 80. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

4.9.22.4 SSI Receiver Timing with External Clock

Figure 95 depicts the SSI receiver timing with external clock, and Table 81 lists the timing parameters.

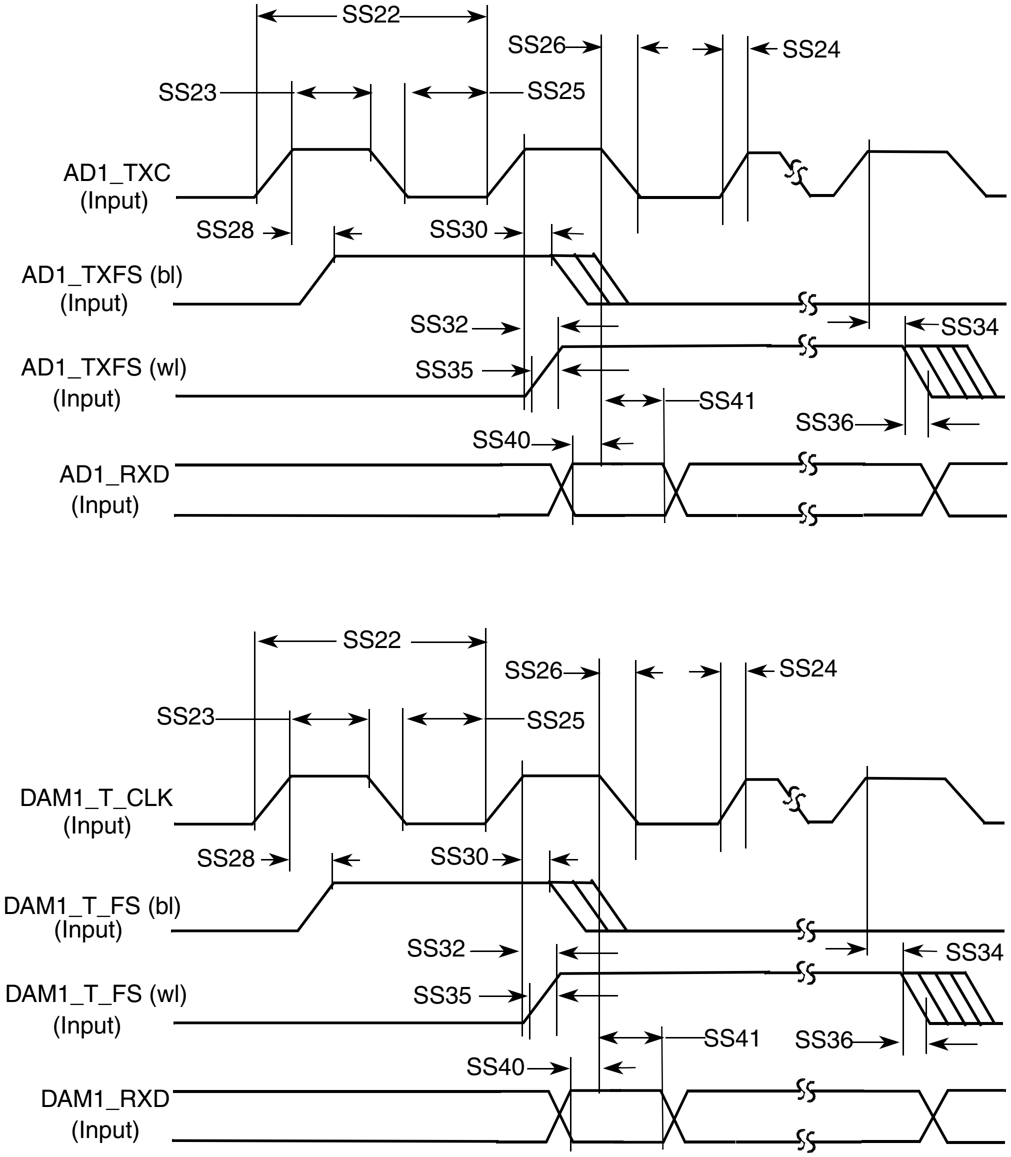

SS22
SS26
SS24
SS23
SS25
AD1_TXC
(Input)
SS28
SS30
AD1_TXFS (bl)
(Input)
SS32
SS34
AD1_TXFS (wl)
(Input)
SS35
SS41
SS36
SS40
AD1_RXD
(Input)
SS22
SS26
SS24
SS23
SS25
DAM1_T_CLK
(Input)
SS28
SS30
DAM1_T_FS (bl)
(Input)
SS32
SS34
DAM1_T_FS (wl)
(Input)
SS35
SS41
SS36
SS40
DAM1_RXD
(Input)

Figure 95. SSI Receiver with External Clock Timing Diagram

Table 81. SSI Receiver with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns

Table 81. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min.	Max.	Unit
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.9.23 UART Electrical

This section describes the electrical information of the UART module.

4.9.23.1 UART RS-232 Serial Mode Timing

The following subsections give the UART transmit and receive timings in RS-232 serial mode.

4.9.23.1.11 UART Transmitter

Figure 96 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 82 lists the UART RS-232 serial mode transmit timing characteristics.

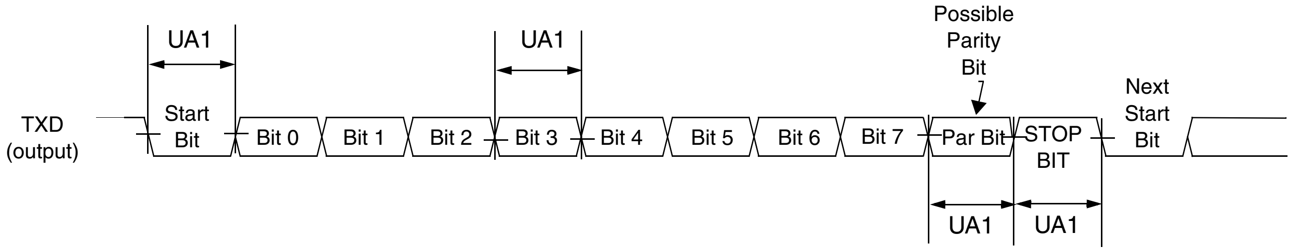

UA1
UA1
Possible Parity Bit
Next Start Bit
TXD (output)
Start Bit
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
Par Bit
STOP BIT
UA1
UA1

Figure 96. UART RS-232 Serial Mode Transmit Timing Diagram

Table 82. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate}$ + T_{ref_clk}	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.23.1.12 UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 83 lists serial mode receive timing characteristics.

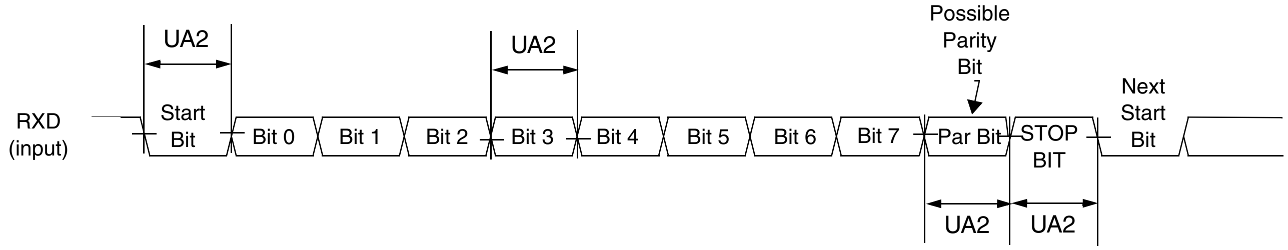

Possible Parity Bit
Next Start Bit
UA2
UA2
RXD (input)
Start Bit
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
Par Bit
STOP BIT
UA2
UA2

Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 83. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate}$ + $1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency) ÷ 16.

4.9.23.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.9.23.2.13 UART IrDA Mode Transmitter

Figure 98 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 84 lists the transmit timing characteristics.

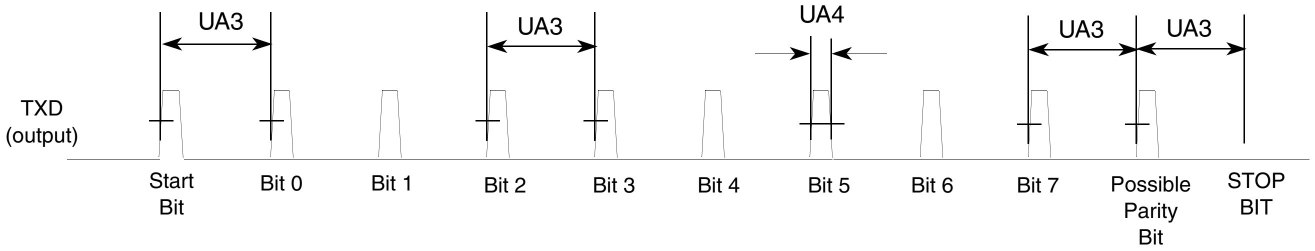

UA3
UA3
UA4
UA3
UA3
TXD (output)
Start Bit
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
Possible Parity Bit
STOP BIT

Figure 98. UART IrDA Mode Transmit Timing Diagram

Table 84. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.23.2.14 UART IrDA Mode Receiver

Figure 99 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 85 lists the receive timing characteristics.

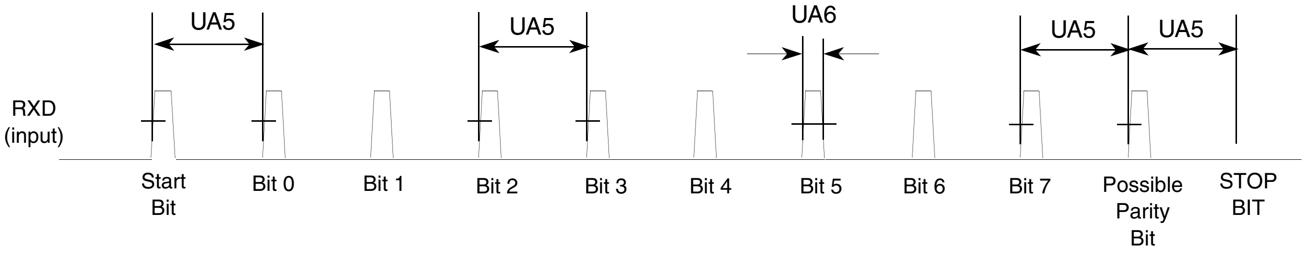


Figure 99. UART IrDA Mode Receive Timing Diagram

Table 85. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 us	$(5/16) \times (1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency) ÷ 16.

4.9.24 USB Electrical Specifications

In order to support four different serial interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

4.9.24.1 DAT_SE0 Bidirectional Mode

Table 86 defines the signals for DAT_SE0 bidirectional mode. Figure 100 and Figure 101 show the transmit and receive waveforms respectively.

Table 86. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

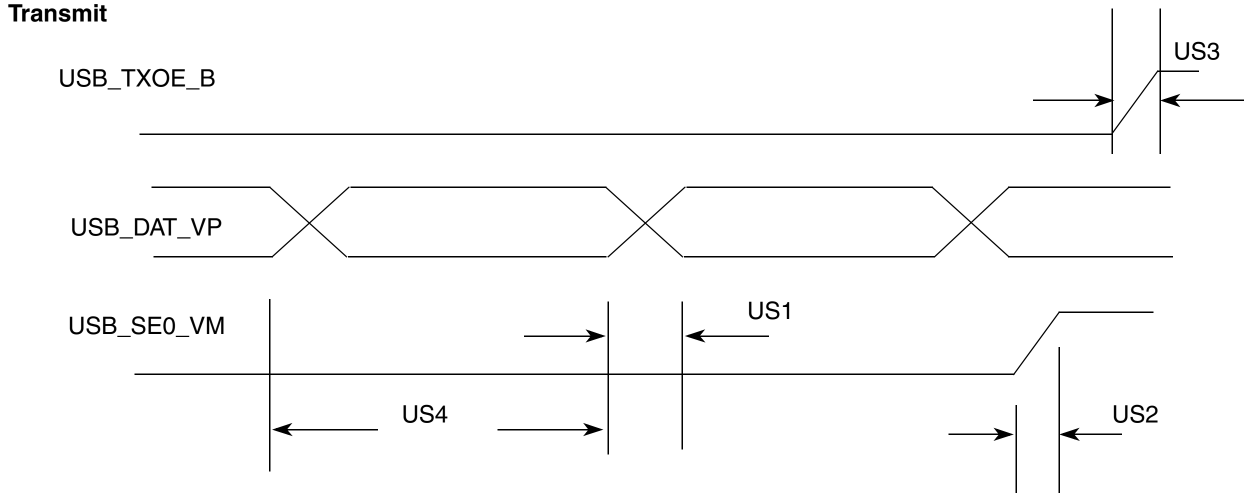

Transmit
USB_TXOE_B
US3
USB_DAT_VP
USB_SE0_VM
US1
US4
US2

Figure 100. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

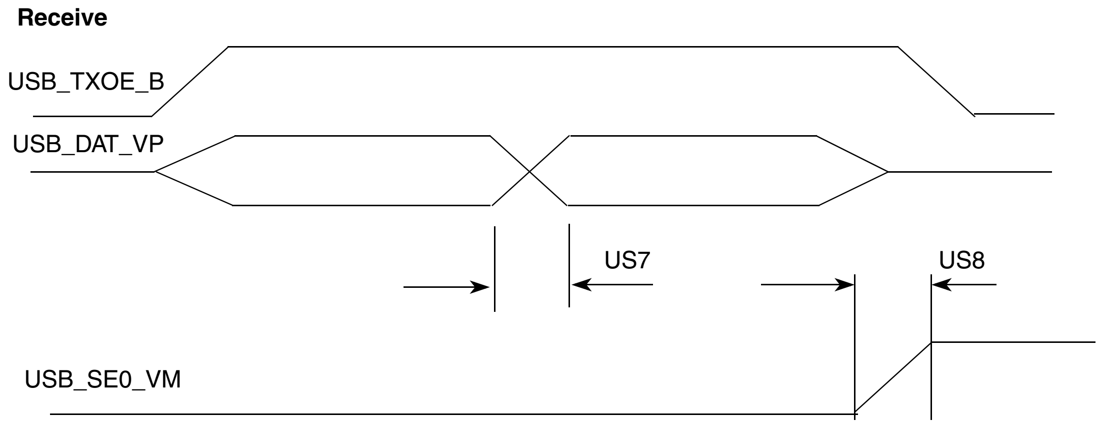

Receive
USB_TXOE_B
USB_DAT_VP
US7
US8
USB_SE0_VM

Figure 101. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 87 describes the port timing specification in DAT_SE0 bidirectional mode.

Table 87. Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.9.24.2 DAT_SE0 Unidirectional Mode

Table 88 defines the signals for DAT_SE0 unidirectional mode. Figure 102 and Figure 103 show the transmit and receive waveforms respectively.

Table 88. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

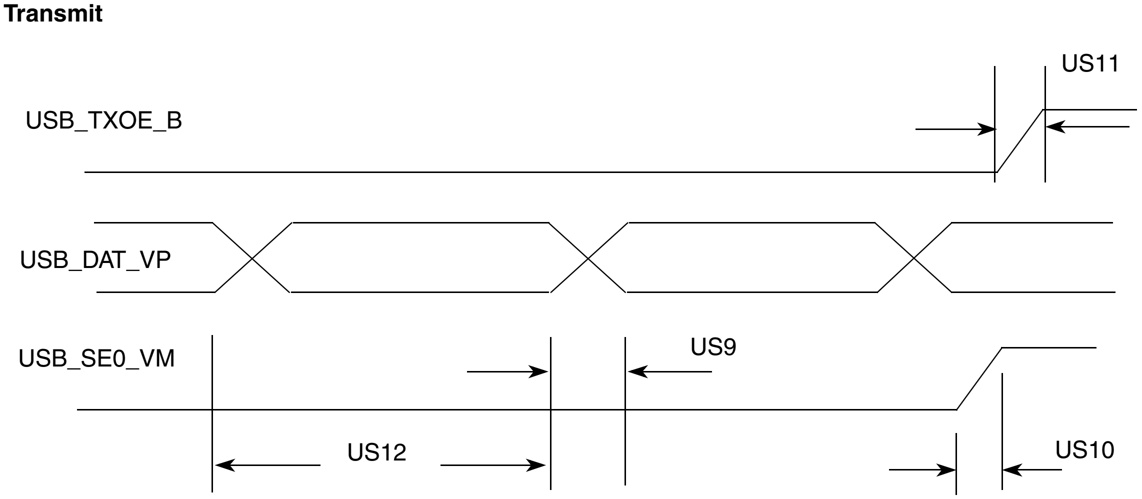


Figure 102. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

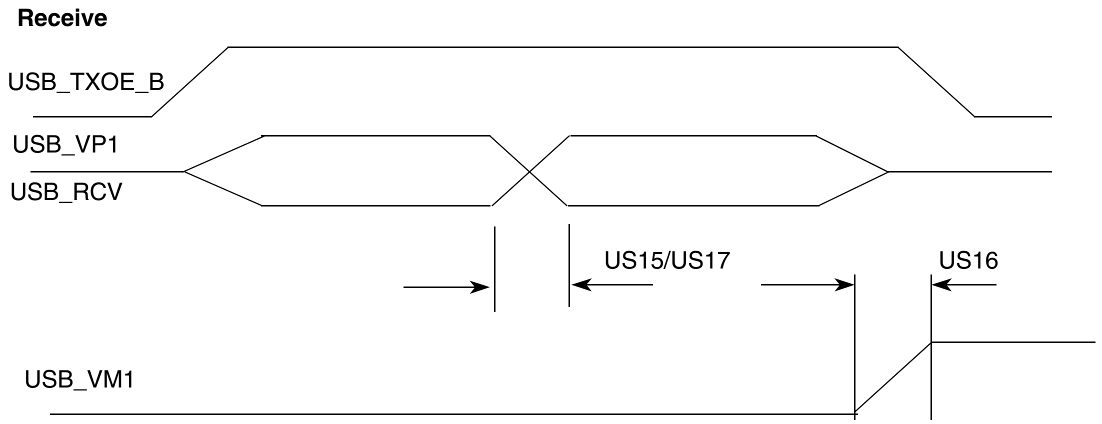


Figure 103. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 89 describes the port timing specification in DAT_SE0 unidirectional mode.

Table 89. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min.	Max.	Unit	Condition/ Reference Signal
US9	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US16	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US17	Rx rise/fall time	USB_RCV	In	—	3.0	ns	35 pF

4.9.24.3 VP_VM Bidirectional Mode

Table 90 defines the signals for VP_VM bidirectional mode. Figure 104 and Figure 105 show the transmit and receive waveforms respectively.

Table 90. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	Tx VP data when USB_TXOE_B is low Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	Tx VM data when USB_TXOE_B low Rx VM data when USB_TXOE_B high
USB_RCV	In	Differential Rx data

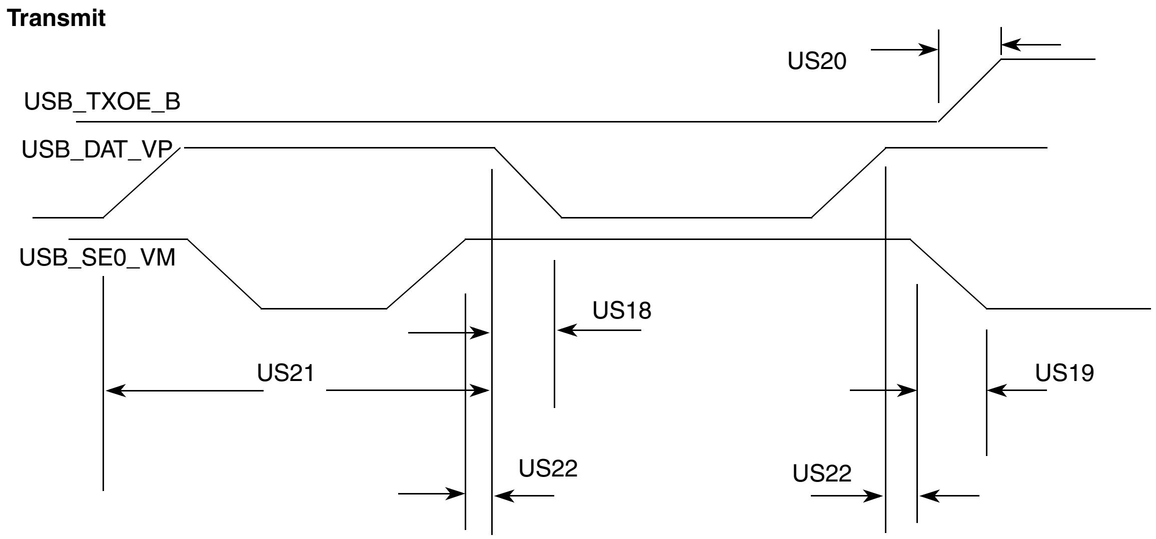

Transmit
USB_TXOE_B
USB_DAT_VP
USB_SE0_VM
US20
US18
US21
US19
US22
US22

Figure 104. USB Transmit Waveform in VP_VM Bidirectional Mode

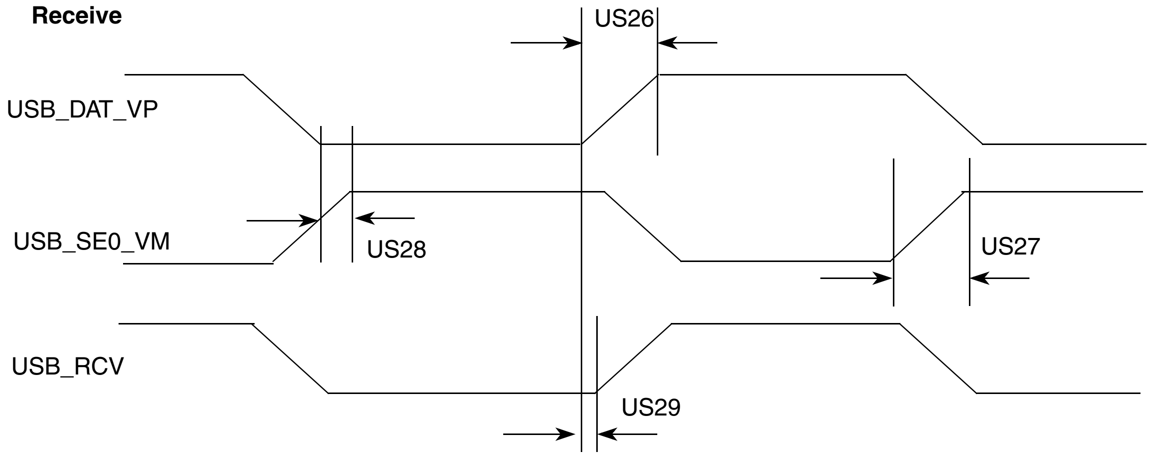

Receive
USB_DAT_VP
USB_SE0_VM
USB_RCV
US26
US28
US27
US29

Figure 105. USB Receive Waveform in VP_VM Bidirectional Mode

Table 91 describes the port timing specification in VP_VM bidirectional mode.

Table 91. USB Port Timing Specification in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US18	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	Tx overlap	USB_SE0_VM	Out	–3.0	+3.0	ns	USB_DAT_VP
US26	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

Table 91. USB Port Timing Specification in VP_VM Bidirectional Mode (continued)

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US28	Rx skew	USB_DAT_VP	In	–4.0	+4.0	ns	USB_SE0_VM
US29	Rx skew	USB_RCV	In	–6.0	+2.0	ns	USB_DAT_VP

4.9.24.4 VP_VM Unidirectional Mode

Table 92 defines the signals for VP_VM unidirectional mode. Figure 106 and Figure 107 show the transmit and receive waveforms respectively.

Table 92. Signal Definitions—VP_VM Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx VP data when USB_TXOE_B is low
USB_SE0_VM	Out	Tx VM data when USB_TXOE_B is low
USB_VP1	In	Rx VP data when USB_TXOE_B is high
USB_VM1	In	Rx VM data when USB_TXOE_B is high
USB_RCV	In	Differential Rx data

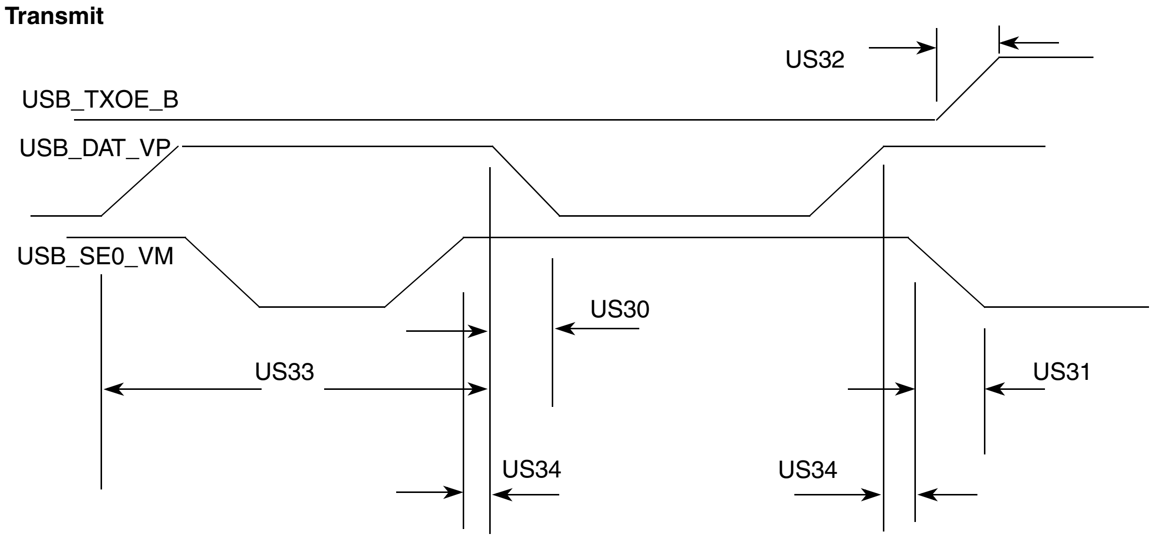


Figure 106. USB Transmit Waveform in VP_VM Unidirectional Mode

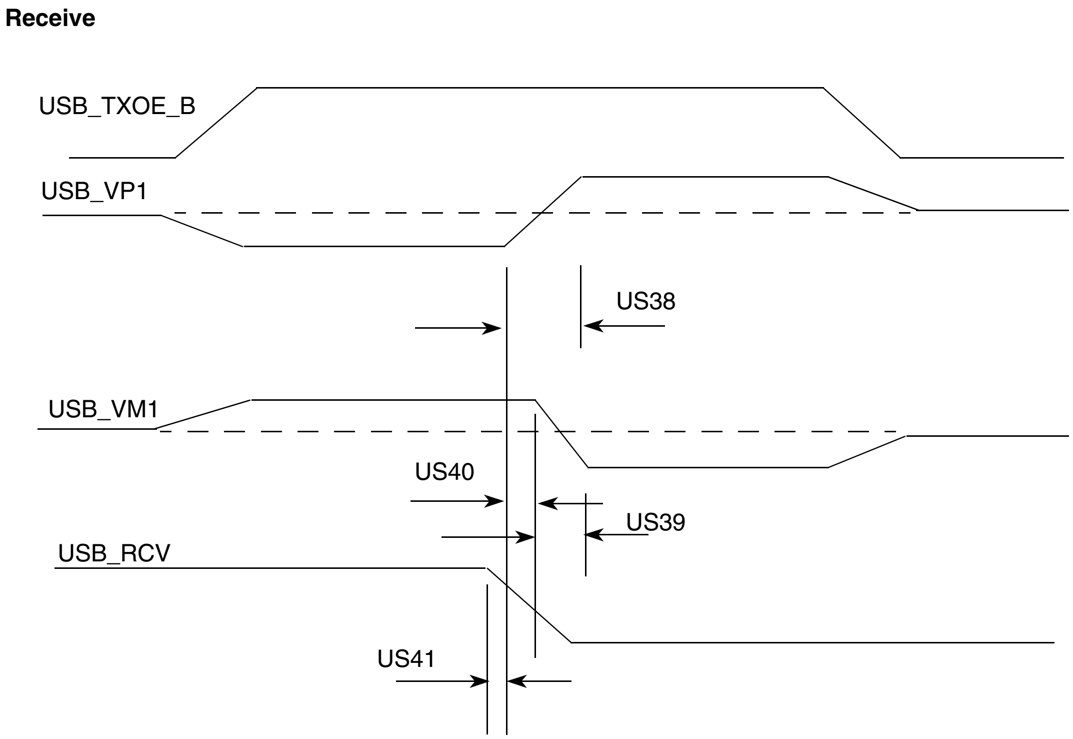


Figure 107. USB Receive Waveform in VP_VM Unidirectional Mode

Table 93 describes the port timing specification in VP_VM unidirectional mode.

Table 93. USB Timing Specification in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx overlap	USB_SE0_VM	Out	–3.0	+3.0	ns	USB_DAT_VP
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	In	–4.0	+4.0	ns	USB_VM1
US41	Rx skew	USB_RCV	In	–6.0	+2.0	ns	USB_VP1

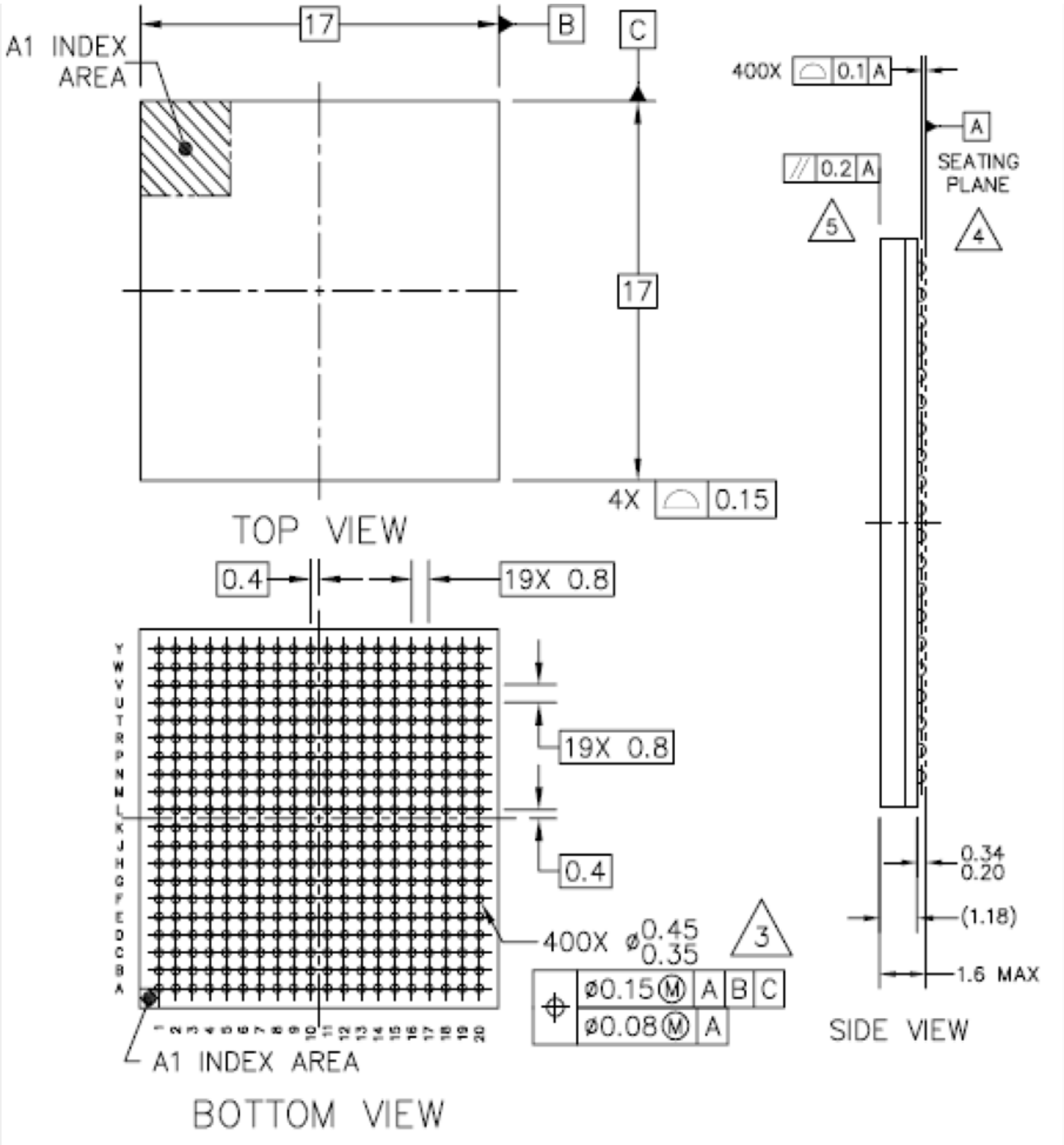
5 Package Information and Pinout

This section includes the following:

- Mechanical package drawing
- Pin/contact assignment information

5.1 MAPBGA Production Package 1568-01, 17 × 17 mm, 0.8 Pitch

See Figure 108 for the package drawing and dimensions of the production package.


A1 INDEX AREA
17
B
C
400X ⌓ 0.1 A
A
SEATING PLANE
4
// 0.2 A
5
17
4X ⌓ 0.15
TOP VIEW
0.4
19X 0.8
Y W V U T R P N M L K J H G F E D C B A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
19X 0.8
0.4
400X ø0.45 0.35
3
⌖ ø0.15 Ⓜ A B C
ø0.08 Ⓜ A
0.34 0.20
(1.18)
1.6 MAX
SIDE VIEW
A1 INDEX AREA
BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.

3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 108. Production Package: Mechanical Drawing

5.2 MAPBGA Signal Assignments

Table 94 and Table 95 list MAPBGA signals, alphabetized by signal name, for silicon revisions 2.0 and 2.1, respectively. Table 96 and Table 97 show the signal assignment on the i.MX35 ball map for silicon revisions 2.0 and 2.1, respectively. The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout.

Table 94. Silicon Revision 2.0 Signal Ball Map Locations

Signal ID	Ball Location
A0	A5
A1	D7
A10	F15
A11	D5
A12	F6
A13	B3
A14	D14
A15	D15
A16	D13
A17	D12
A18	E11
A19	D11
A2	E7
A20	D10
A21	E10
A22	D9
A23	E9
A24	D8
A25	E8
A3	C6
A4	D6
A5	B5
A6	C5
A7	A4
A8	B4
A9	A3
ATA_BUFF_EN[1]	T5
ATA_CS0[1]	V7
ATA_CS1[1]	T7
ATA_DA0[1]	R4
ATA_DA1[1]	V1
ATA_DA2[1]	R5
ATA_DATA0[1]	Y5
ATA_DATA1[1]	W5
ATA_DATA10[1]	V3
ATA_DATA11[1]	Y2
ATA_DATA12[1]	U3
ATA_DATA7[1]	Y3
ATA_DATA8[1]	U4
ATA_DATA9[1]	W3
ATA_DIOR[1]	Y6
ATA_DIOW[1]	W6
ATA_DMACK[1]	V6
ATA_DMARQ[1]	T3
ATA_INTRQ[1]	V2
ATA_IORDY[1]	U6
ATA_RESET_B[1]	T6
BCLK	E14
BOOT_MODE0	W10
BOOT_MODE1	U9
CAPTURE	V12
CAS	E16
CLK_MODE0	Y10
CLK_MODE1	T10
CLKO	V10
COMPARE	T12
CONTRAST[1]	L16
CS0	F17
CS1	E19
CS2	B20
CS3	C19
CS4	E18
CS5	F19
CSI_D10[1]	V16
CSI_D11[1]	T15
CSI_D12[1]	W16
CSI_D13[1]	V15
CSI_D14[1]	U14
CSI_D15[1]	Y16
CSI_D8[1]	U15
CSI_D9[1]	W17
CSI_HSYNC[1]	V14
CSI_MCLK[1]	W15
CSI_PIXCLK[1]	Y15

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
ATA_DATA13[1]	W2
ATA_DATA14[1]	W1
ATA_DATA15[1]	T4
ATA_DATA2[1]	V5
ATA_DATA3	U5
ATA_DATA4	Y4
ATA_DATA5	W4
ATA_DATA6	V4
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS[1]	L17
D3_DRDY[1]	L20
D3_FPSHIFT[1]	L15
D3_HSYNC[1]	L18
D3_REV[1]	M17
D3_SPL[1]	M18
D3_VSYNC[1]	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
DQM1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1
CSI_VSYNC[1]	T14
CSPI1_MISO	V9
CSPI1_MOSI	W9
CSPI1_SCLK	W8
CSPI1_SPI_RDY	T8
CSPI1_SS0	Y8
CSPI1_SS1	U8
CTS1	R3
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0[1]	F20
LD1[1]	G18
LD10[1]	H20
LD11[1]	J18
LD12[1]	J16
LD13[1]	J19
LD14[1]	J17
LD15[1]	J20
LD16[1]	K14
LD17[1]	K19
LD18[1]	K18
LD19[1]	K20
LD2[1]	G17
LD20[1]	K16
LD21[1]	K17
LD22[1]	K15

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3
MA10	C4
MGND	N11
MLB_CLK	W13
MLB_DAT	Y13
MLB_SIG	W12
MVDD	P11
NF_CE0	G3
NFALE	F2
NFCLE	E1
NFRB	F3
NFRE_B	F1
NFWE_B	G2
NFWP_B	F4
NGND_ATA	M9
NGND_ATA	P9
NGND_ATA	L10
NGND_CRM	L11
NGND_CSI	N10
NGND_EMI1	H8
NGND_EMI1	H10
NGND_EMI1	J10
NGND_EMI2	J11
NGND_EMI3	J12
NGND_EMI3	K12
NGND_JTAG	M13
NGND_LCDC	K11
NGND_LCDC	L12
NGND_MISC	M7
NGND_MISC	K8
NGND_MLB	M10
NGND_NFC	K9
NGND_SDIO	N12
NVCC_ATA	N6
NVCC_ATA	P6
NVCC_ATA	P7
NVCC_ATA	P8
NVCC_CRM	R9
NVCC_CSI	R11
LD23[1]	L19
LD3[1]	G16
LD4[1]	G19
LD5[1]	H16
LD6[1]	H18
LD7[1]	G20
LD8[1]	H17
LD9[1]	H19
NVCC_EMI2	G12
NVCC_EMI2	F13
NVCC_EMI2	F14
NVCC_EMI3	G14
NVCC_JTAG	P16
NVCC_LCDC	H14
NVCC_LCDC	J14
NVCC_LCDC	L14
NVCC_LCDC	M14
NVCC_MISC	K6
NVCC_MISC	K7
NVCC_MISC	L8
NVCC_MLB	R10
NVCC_NFC	G6
NVCC_NFC	H6
NVCC_NFC	H7
NVCC_SDIO	P14
OE	E20
OSC_AUDIO_VDD	V20
OSC_AUDIO_VSS	U19
OSC24M_VDD	T19
OSC24M_VSS	T18
PGND	M12
PHY1_VDDA	M15
PHY1_VDDA	N20
PHY1_VSSA	N16
PHY1_VSSA	P20
PHY2_VDD	R13
PHY2_VSS	P12
POR_B	W11
POWER_FAIL	Y9
PVDD	N13
RAS	E15
RESET_IN_B	U10
RTCK	U18
RTS1	U1
RTS2	G1
RW	C20

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
NVCC_EMI1	G7	RXD1	U2
NVCC_EMI1	G8	RXD2	H3
NVCC_EMI1	G9	SCK4	L4
NVCC_EMI1	H9	SCK5	L5
NVCC_EMI1	F10	SCKR	K3
NVCC_EMI1	G10	SCKT	J4
NVCC_EMI1	F11	SD0	C17
NVCC_EMI1	G11	SD1	A19
SD1_CLK	V18	SDCLK	E12
SD1_CMD	Y19	SDCLK_B	E13
SD1_DATA0	R14	SDQS0	B17
SD1_DATA1	U16	SDQS1	A13
SD1_DATA2	W18	SDQS2	A10
SD1_DATA3	V17	SDQS3	C7
SD10	A15	SDWE	G15
SD11	B15	SJC_MOD	U17
SD12	C13	SRXD4	L1
SD13	B14	SRXD5	K4
SD14	A14	STXD4	M2
SD15	B13	STXD5	K1
SD16	C12	STXFS4	L2
SD17	C11	STXFS5	J6
SD18	A12	TCK	R17
SD19	B12	TDI	P15
SD2	B18	TDO	R15
SD2_CLK	W14	TEST_MODE	Y7
SD2_CMD	U13	TMS	R16
SD2_DATA0	V13	TRSTB	T16
SD2_DATA1	T13	TTM_PIN	M16
SD2_DATA2	Y14	TX0	G4
SD2_DATA3	U12	TX1	H1
SD20	B11	TX2_RX3	H5
SD21	A11	TX3_RX2	J2
SD22	C10	TX4_RX1	H4
SD23	B10	TX5_RX0	J3
SD24	A9	TXD1	R6
SD25	C9	TXD2	H2
SD26	B9	USBOTG_OC	U7
SD27	A8	USBOTG_PWR	W7
SD28	B8	USBPHY1_DM	N19
SD29	C8	USBPHY1_DP	P19
SD3	C16	USBPHY1_RREF	R19
SD30	A7	USBPHY1_UID	N18
SD31	B7	USBPHY1_UPLLGND	N14
SD4	A18	USBPHY1_UPLLVDD	N15
SD5	C15	USBPHY1_UPLLVDD	P17

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
SD6	A17
SD7	B16
SD8	C14
SD9	A16
SDBA0	A6
SDBA1	B6
SDCKE0	D18
SDCKE1	E17
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9
USBPHY1_VBUS	P18
USBPHY1_VDDA_BIAS	R20
USBPHY1_VSSA_BIAS	R18
USBPHY2_DM	Y17
USBPHY2_DP	Y18
VDD	M6
VDD	F7
VDD	J7
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
VSS	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

[1] Not available for the MCIMX351.

Table 95. Silicon Revision 2.1 Signal Ball Map Locations

Signal ID	Ball Location
A0	A5
A1	D7
A10	F15
A11	D5
A12	F6
A13	B3
A14	D14
A15	D15
A16	D13
A18	D12
SDQS1	E11
A19	D11
A2	E7
A21	D10
SDQS2	E10
A22	D9
SDQS3	E9
A24	D8
A25	E8
A3	C6
A4	D6
A5	B5
A6	C5
A7	A4
A8	B4
A9	A3
ATA_BUFF_EN[1]	T5
ATA_CS0	V7
ATA_CS1	T7
ATA_DA0	R4
ATA_DA1	V1
ATA_DA2	R5
ATA_DATA0	Y5
ATA_DATA1	W5
ATA_DATA10	V3
ATA_DATA11	Y2
ATA_DATA12	U3
ATA_DATA13	W2
ATA_DATA14	W1
ATA_DATA15	T4
ATA_DATA2	V5
ATA_DATA3	U5
ATA_DATA4	Y4
ATA_DATA5	W4
ATA_DATA6	V4

Signal ID	Ball Location
ATA_DATA7	Y3
ATA_DATA8	U4
ATA_DATA9	W3
ATA_DIOR	Y6
ATA_DIOW	W6
ATA_DMACK	V6
ATA_DMARQ	T3
ATA_INTRQ	V2
ATA_IORDY	U6
ATA_RESET_B	T6
SDQS0	E14
BOOT_MODE0	W10
BOOT_MODE1	U9
CAPTURE	V12
RAS	E16
CLK_MODE0	Y10
CLK_MODE1	T10
CLKO	V10
COMPARE	T12
CONTRAST	L16
CS0	F17
CS1	E19
CS2	B20
CS3	C19
CS4	E18
CS5	F19
CSI_D10	V16
CSI_D11	T15
CSI_D12	W16
CSI_D13	V15
CSI_D14	U14
CSI_D15	Y16
CSI_D8	U15
CSI_D9	W17
CSI_HSYNC	V14
CSI_MCLK	W15
CSI_PIXCLK	Y15
CSI_VSYNC	T14
CSPI1_MISO	V9
CSPI1_MOSI	W9
CSPI1_SCLK	W8
CSPI1_SPI_RDY	T8
CSPI1_SS0	Y8
CSPI1_SS1	U8
CTS1	R3

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS	L17
D3_DRDY	L20
D3_FPSHIFT	L15
D3_HSYNC	L18
D3_REV	M17
D3_SPL	M18
D3_VSYNC	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
SDCKE1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0	F20
LD1	G18
LD10	H20
LD11	J18
LD12	J16
LD13	J19
LD14	J17
LD15	J20
LD16	K14
LD17	K19
LD18	K18
LD19	K20
LD2	G17
LD20	K16
LD21	K17
LD22	K15
LD23	L19
LD3	G16
LD4	G19
LD5	H16
LD6	H18
LD7	G20
LD8	H17
LD9	H19

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
MA10	C4	NVCC_EMI2	G12
MGND	N11	NVCC_EMI2	F13
MLB_CLK	W13	VSS	F14
MLB_DAT	Y13	NVCC_EMI3	G14
MLB_SIG	W12	NVCC_JTAG	P16
MVDD	P11	NVCC_LCDC	H14
NF_CE0	G3	NVCC_LCDC	J14
NFALE	F2	NVCC_LCDC	L14
NFCLE	E1	NVCC_LCDC	M14
NFRB	F3	NVCC_MISC	K6
NFRE_B	F1	NVCC_MISC	K7
NFWE_B	G2	NVCC_MISC	L8
NFWP_B	F4	NVCC_MLB	R10
NGND_ATA	M9	NVCC_NFC	G6
NGND_ATA	P9	NVCC_NFC	H6
NGND_ATA	L10	NVCC_NFC	H7
NGND_CRM	L11	NVCC_SDIO	P14
NGND_CSI	N10	OE	E20
NGND_EMI1	H8	OSC_AUDIO_VDD	V20
NVCC_EMI1	H10	OSC_AUDIO_VSS	U19
NGND_EMI1	J10	OSC24M_VDD	T19
NGND_EMI2	J11	OSC24M_VSS	T18
NGND_EMI3	J12	PGND	M12
NGND_EMI3	K12	PHY1_VDDA	M15
NGND_JTAG	M13	PHY1_VDDA	N20
NGND_LCDC	K11	PHY1_VSSA	N16
NGND_LCDC	L12	PHY1_VSSA	P20
NGND_MISC	M7	PHY2_VDD	R13
NGND_MISC	K8	PHY2_VSS	P12
NGND_MLB	M10	POR_B	W11
NGND_NFC	K9	POWER_FAIL	Y9
NGND_SDIO	N12	PVDD	N13
NVCC_ATA	N6	BCLK	E15
NVCC_ATA	P6	RESET_IN_B	U10
NVCC_ATA	P7	RTCK	U18
NVCC_ATA	P8	RTS1	U1
NVCC_CRM	R9	RTS2	G1
NVCC_CSI	R11	RW	C20
NVCC_EMI1	G7	RXD1	U2
NVCC_EMI1	G8	RXD2	H3
NVCC_EMI1	G9	SCK4	L4
NVCC_EMI1	H9	SCK5	L5
NGND_EMI1	F10	SCKR	K3
NVCC_EMI1	G10	SCKT	J4
NVCC_EMI1	F11	DQM1	C17
NVCC_EMI1	G11	SD1	A19

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
SD1_CLK	V18	SDCLK	E12
SD1_CMD	Y19	SDCLK_B	E13
SD1_DATA0	R14	SD0	B17
SD1_DATA1	U16	SD15	A13
SD1_DATA2	W18	SD23	A10
SD1_DATA3	V17	A23	C7
SD10	A15	SDWE	G15
SD11	B15	SJC_MOD	U17
A17	C13	SRXD4	L1
SD13	B14	SRXD5	K4
SD14	A14	STXD4	M2
SD12	B13	STXD5	K1
SD16	C12	STXFS4	L2
SD17	C11	STXFS5	J6
SD18	A12	TCK	R17
SD19	B12	TDI	P15
SD2	B18	TDO	R15
SD2_CLK	W14	TEST_MODE	Y7
SD2_CMD	U13	TMS	R16
SD2_DATA0	V13	TRSTB	T16
SD2_DATA1	T13	TTM_PIN	M16
SD2_DATA2	Y14	TX0	G4
SD2_DATA3	U12	TX1	H1
SD20	B11	TX2_RX3	H5
SD21	A11	TX3_RX2	J2
A20	C10	TX4_RX1	H4
SD22	B10	TX5_RX0	J3
SD24	A9	TXD1	R6
SD25	C9	TXD2	H2
SD26	B9	USBOTG_OC	U7
SD27	A8	USBOTG_PWR	W7
SD28	B8	USBPHY1_DM	N19
SD29	C8	USBPHY1_DP	P19
SD3	C16	USBPHY1_RREF	R19
SD30	A7	USBPHY1_UID	N18
SD31	B7	USBPHY1_UPLLGND	N14
SD4	A18	USBPHY1_UPLLVDD	N15
SD5	C15	USBPHY1_UPLLVDD	P17
SD6	A17	USBPHY1_VBUS	P18
SD7	B16	USBPHY1_VDDA_BIAS	R20
SD8	C14	USBPHY1_VSSA_BIAS	R18
SD9	A16	USBPHY2_DM	Y17
SDBA0	A6	USBPHY2_DP	Y18
SDBA1	B6	VDD	M6
SDCKE0	D18	VDD	F7
CAS	E17	VDD	J7

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
VDD	L7	VSS	L9
VDD	N7	VSS	N9
VDD	R7	VSS	K10
VDD	F8	VSS	P10
VDD	R8	VSS	H11
VDD	F9	VSS	H12
VDD	F12	NVCC_EMI2	H13
VDD	R12	VSS	J13
VDD	G13	VSS	K13
VDD	H15	VSS	L13
VDD	J15	VSS	T17
VSS	A1	VSS	A20
VSS	Y1	VSS	Y20
VSS	J8	VSTBY	T9
VSS	M8	WDOG_RST	Y12
VSS	N8	XTAL_AUDIO	V19
VSS	J9	XTAL24M	U20

[1] Not available for the MCIMX351.

Table 96. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	D0	A9	A7	A0	SDBA0	SD30	SD27	SD24	SDQS2	SD21	SD18	SDQS1	SD14	SD10	SD9	SD6	SD4	SD1	VSS	A
B	D5	D2	A13	A8	A5	SDBA1	SD31	SD28	SD26	SD23	SD20	SD19	SD15	SD13	SD11	SD7	SDQS0	SD2	DQM0	CS2	B
C	D8	D7	D4	MA10	A6	A3	SDQS3	SD29	SD25	SD22	SD17	SD16	SD12	SD8	SD5	SD3	SD0	DQM3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A20	A19	A17	A16	A14	A15	DQM2	DQM1	SDCKE0	ECB	LBA	D
E	NFCLE	D15	D12	D9	D3	D11	A2	A25	A23	A21	A18	SDCLK	SDCLK_B	BCLK	RAS	CAS	SDCKE1	CS4	CS1	OE	E
F	NFRE_B	NFALE	NFRB	NFWP_B	D13	A12	VDD	VDD	VDD	NVCC_EMI1	NVCC_EMI1	VDD	NVCC_EMI2	NVCC_EMI2	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFWE_B	NF_CE0	TX0	CTS2	NVCC_NFC	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD	NVCC_EMI3	SDWE	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_RX1	TX2_RX3	NVCC_NFC	NVCC_NFC	NGND_EMI1	NVCC_EMI1	NGND_EMI1	VSS	VSS	VSS	NVCC_LCDC	VDD	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCKT	HCKT	STXFS5	VDD	VSS	VSS	NGND_EMI1	NGND_EMI2	NGND_EMI3	VSS	NVCC_LCDC	VDD	LD12	LD14	LD11	LD13	LD15	J
K	STXD5	HCKR	SCKR	SRXD5	FSR	NVCC_MISC	NVCC_MISC	NGND_MISC	NGND_NFC	VSS	NGND_LCDC	NGND_EMI3	VSS	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD4	STXFS4	I2C2_CLK	SCK4	SCK5	FEC_TDATA3	VDD	NVCC_MISC	VSS	NGND_ATA	NGND_CRM	NGND_LCDC	VSS	NVCC_LCDC	D3_FPSHIFT	CONTRAST	D3_CLS	D3_HSYNC	LD23	D3_DRDY	L
M	I2C2_DAT	STXD4	FEC_RDATA2	FEC_TDATA1	FEC_TDATA2	VDD	NGND_MISC	VSS	NGND_ATA	NGND_MLB	FUSE_VSS	PGND	NGND_JTAG	NVCC_LCDC	PHY1_VDDA	TTM_PIN	D3_REV	D3_SPL	D3_VSYNC	I2C1_CLK	M
N	FEC_RDATA3	FEC_RDATA1	FEC_RX_ERR	FEC_TX_ERR	FEC_CRS	NVCC_ATA	VDD	VSS	VSS	NGND_CSI	MGND	NGND_SDIO	PVDD	USBPHY1_UPLLGND	USBPHY1_UPLLVDD	PHY1_VSSA	I2C1_DAT	USBPHY1_UID	USBPHY1_DM	PHY1_VDDA	N
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	NGND_ATA	VSS	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD	VDD	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_RREF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	VSS	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U

Table 96. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch[1] (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	VSS	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	VSS	Y

[1] See Table 95 for pins unavailable in the MCIMX351 SoC.

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	D0	A9	A7	A0	SDBA0	SD30	SD27	SD24	SD23	SD21	SD18	SD15	SD14	SD10	SD9	SD6	SD4	SD1	GND	A
B	D5	D2	A13	A8	A5	SDBA1	SD31	SD28	SD26	SD22	SD20	SD19	SD12	SD13	SD11	SD7	SD0	SD2	DQM0	CS2	B
C	D8	D7	D4	MA10	A6	A3	A23	SD29	SD25	A20	SD17	SD16	A17	SD8	SD5	SD3	DQM1	DQM3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A21	A19	A18	A16	A14	A15	DQM2	SDCKE1	SDCKE0	ECB	LBA	D
E	NFCLE	D15	D12	D9	D3	D11	A2	A25	SDQS3	SDQS2	SDQS1	SDCLK	SDCLK_B	SDQS0	BCLK	RAS	CAS	CS4	CS1	OE	E
F	NFRE_B	NFALE	NFRB	NFWP_B	D13	A12	VDD7	VDD7	VDD7	GND	NVCC_EMI1	VDD7	NVCC_EMI2	GND	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFWE_B	NF_CE0	TX0	CTS2	NVCC_NFC	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD6	NVCC_EMI3	SDWE	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_RX1	TX2_RX3	NVCC_NFC	NVCC_NFC	GND	NVCC_EMI1	NVCC_EMI1	GND	GND	NVCC_EMI2	NVCC_LCDC	VDD5	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCKT	HCKT	STXFS5	VDD1	GND	GND	GND	GND	GND	GND	NVCC_LCDC	VDD5	LD12	LD14	LD11	LD13	LD15	J
K	STXD5	HCKR	SCKR	SRXD5	FSR	NVCC_MISC	NVCC_MISC	GND	GND	GND	GND	GND	GND	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD4	STXFS4	I2C2_CLK	SCK4	SCK5	FEC_TDATA3	VDD2	NVCC_MISC	GND	GND	GND	GND	GND	NVCC_LCDC	D3_FPSHIFT	CONTRAST	D3_CLS	D3_HSYNC	LD23	D3_DRDY	L
M	I2C2_DAT	STXD4	FEC_RDATA2	FEC_TDATA1	FEC_TDATA2	VDD2	GND	GND	GND	GND	FUSE_VSS	PGND	GND	NVCC_LCDC	PHY1_VDDA	TTM_PAD	D3_REV	D3_SPL	D3_VSYNC	I2C1_CLK	M
N	FEC_RDATA3	FEC_RDATA1	FEC_RX_ERR	FEC_TX_ERR	FEC_CRS	NVCC_ATA	VDD3	GND	GND	GND	MGND	GND	PVDD	USBPHY1_UPLLGND	USBPHY1_UPLLVDD	PHY1_VSSA	I2C1_DAT	USBPHY1_UID	USBPHY1_DM	PHY1_VDDA	N

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	GND	GND	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD3	VDD3	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD4	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_RREF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	GND	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	GND	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

6 Product Documentation

All related product documentation for the i.MX35 processor is located at http://www.freescale.com/imx.

7 Revision History

Table 98 shows the revision history of this document. Note: There were no revisions of this document between revision 1 and revision 4 or between revision 6 and revision 7.

Table 98. i.MX35 Data Sheet Revision History

Revision Number	Date	Substantive Change(s)
10	06/2012	• In Table 2, "Functional Differences in the i.MX35 Parts," on page 4, added two columns for part numbers MCIMX353 and MCIMX357. • Added Table 29, "Clock Input Tolerance," on page 32 in Section 4.9.3, “DPLL Electrical Specifications.” • Updated Table 39, "DDR2 SDRAM Timing Parameter Table," on page 51 for DDR2-400 values. • Updated Table 41, "DDR2 SDRAM Write Cycle Parameters," on page 53 for DDR2-400 values. • Added Table 15, "AC Requirements of I/O Pins," on page 25. • Updated WE4 parameter in Table 33, "WEIM Bus Timing Parameters," on page 38.
9	08/2010	• Updated Table 32, “NFC Timing Parameters.” • Updated Table 33, “WEIM Bus Timing Parameters.”
8	04/2010	• Updated Table 1, “Ordering Information.” • Updated Table 14, “I/O Pin DC Electrical Characteristics.”
6	10/21/2009	• Added information for silicon rev. 2.1 • Updated Table 1, “Ordering Information.” • Added Table 95, “Silicon Revision 2.1 Signal Ball Map Locations.” • Added Table 97, “Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch.”
5	08/06/2009	• Filled in TBDs in Table 14. • Revised Figure 15 and Table 33 by removing FCE = 0 and FCE = 1. Added footnote 3 to the table. • Added Table 26, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V).”
4	04/30/2009	Note: There were no revisions of this document between revision 1 and revision 4. • In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6. • Updated values in Table 10, “i.MX35 Power Modes.” • Added Section 4.4, “Reset Timing.” • In Section 4.8.2, “AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes),” removed Slow Slew rate tables, relabeled Table 24, “AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode,” and Table 25, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode,” to exclude mention of slew rate. • In Section 4.9.5.2, “Wireless External Interface Module (WEIM),” modified Figure 16, “Synchronous Memory Timing Diagram for Read Access—WSC = 1,” through Figure 21, “Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7.” • In Section 4.9.6, “Enhanced Serial Audio Interface (ESAI) Timing Specifications,” modified Figure 36, “ESAI Transmitter Timing,” and Figure 37, “ESAI Receiver Timing,” to remove extraneous signals. Removed a note from Figure 36, “ESAI Transmitter Timing.”
1	12/2008	• Updated Section 4.3.1, “Powering Up.” • Section 4.7, “Module-Level AC Electrical Specifications”: Updated NFC, SDRAM and mDDR SDRAM timing. Inserted DDR2 SDRAM timing.
0	10/2008	Initial public release

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