TELEDYNE LECROY
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QualiPHY™
Compliance Test Software

QPHY-DDR2
DDR2 Serial Data
Operator's Manual

Revision A – December, 2014

Relating to the Following Release Versions:

- **Software Option Rev. 5.9**
- **DDR2 Script Rev. 1.0**
- **Style Sheet Rev. 1.2**

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INTRODUCTION TO QPHY-DDR2

QPHY-DDR2 is an automated test package performing all of the real time oscilloscope tests for Double Data Rate in accordance with JEDEC Standard No. 79-2E. The software can be run on the LeCroy SDA/DDA/WavePro 740Zi and 760Zi and all SDA/DDA/WaveMaster 8Zi oscilloscopes.

Required equipment

- SDA/DDA/WavePro 740/760Zi or SDA/DDA/WaveMaster 8Zi oscilloscope
- Four D620 Probes with WL-Plink Prolink probe body
- Alternatively, D610 probes may be used if the voltage swing of the signal is within +/- 2.5Vp-p.
- TF-DSQ Probe Deskew and Calibration Fixture (not needed if using a Zi oscilloscope)

SIGNALS MEASURED

The compliance test requires probing the following signals (# is the negative polarity of the differential signal):

CK, CK# Input

Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output (read) data is referenced to the crossings of CK and CK# (both directions of crossing).

DQ Input/Output

Data Input/Output: Bi-directional data bus.

DQS, DQS# Input/Output

Data Strobe: output with read data, input with write data. This signal is in phase with read data and 90 degrees out of phase with write data. The data strobes DQS may be used in single ended mode or paired with optional complementary signal DQS# to provide differential pair signaling to the system during both reads and writes.

ADD/CTRL

In addition to the Clock, Data and Strobe signals, address and control signals can also be measured. Bank Address (BA0 – BA2), Chip Select (CS), Command Inputs (RAS, CAS and WE), Clock Enable (CKE) and On Die Termination (ODT) can all be specified as the signal under test.

BASIC FUNCTIONALITY

The functionality is extracted from JEDEC Standard No. 79-2E section 3.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command.

Prior to normal operation, the DDR2 SDRAM must be initialized.

Burst Read

The Burst Read command is initiated by having CS# and CAS# LOW while holding RAS# and WE# HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner.

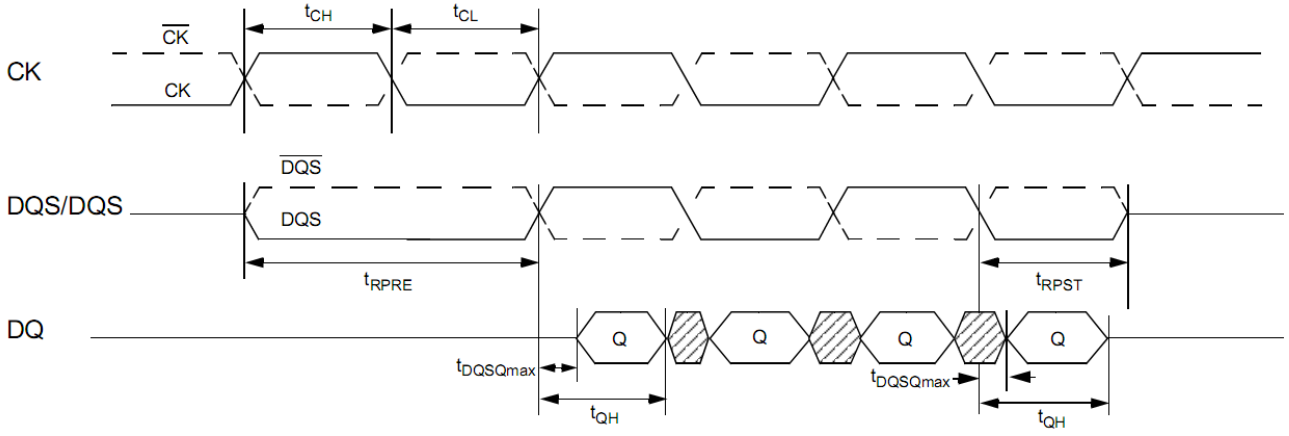


Figure 1. Data output (read) timing [JESD79-2E figure 32]

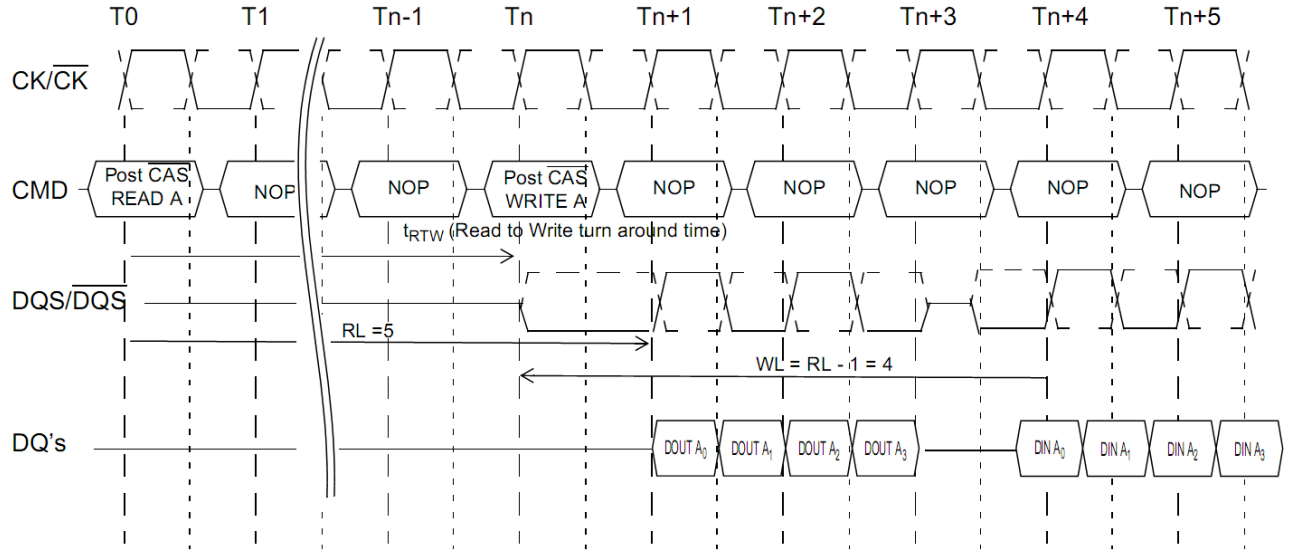


Figure 2. Burst read followed by burst write [JESD79-2E figure 35]

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation.

Burst Write

The Burst Write command is initiated by having CS#, CAS# and WE# LOW while holding RAS# HIGH at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) nominally half clock prior to the [first rising edge]. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst.

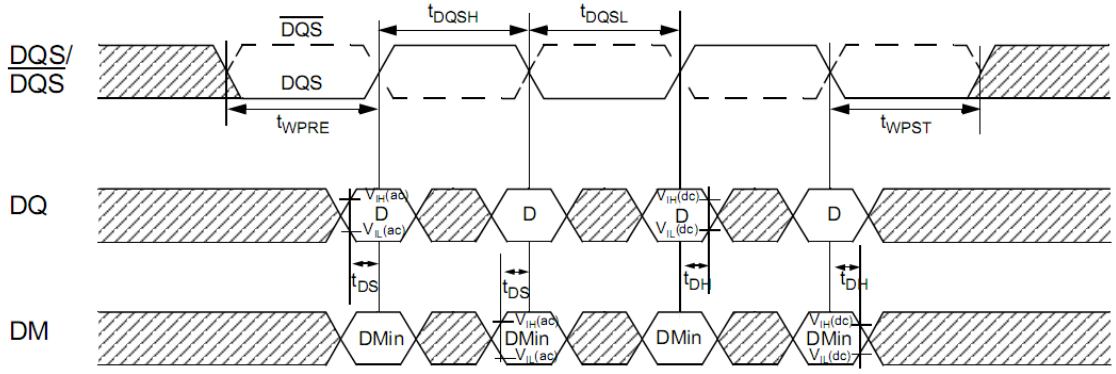


Figure 3. Data input (write) timing [JESD79-2E figure 38]

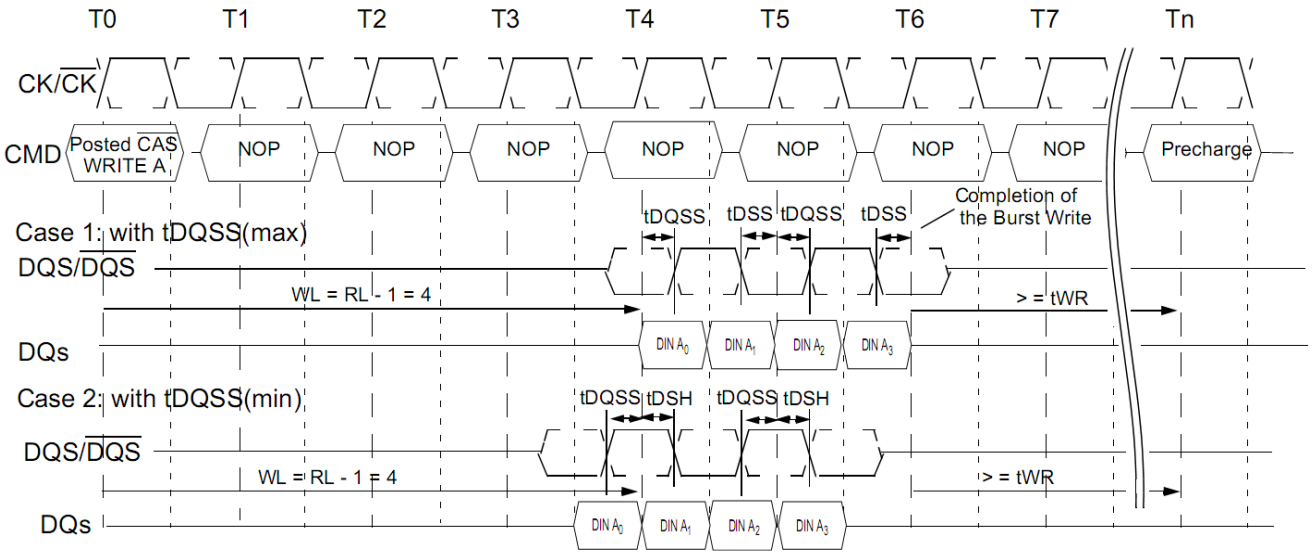
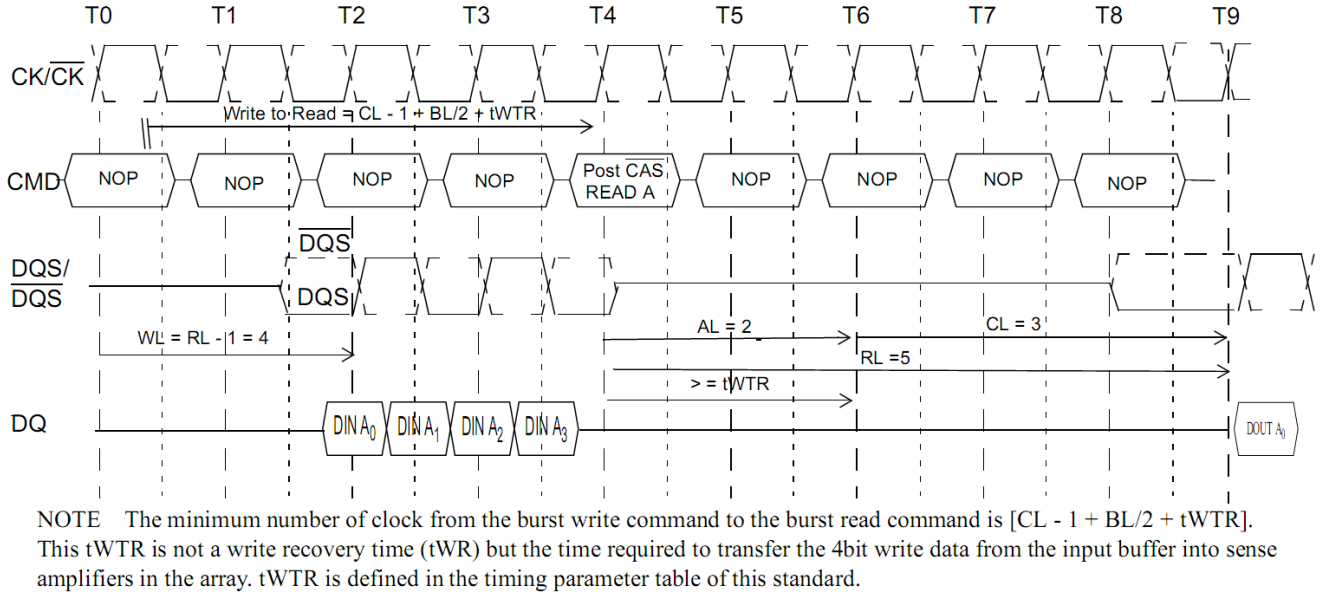


Figure 4. Burst write operation [JESD79-2E figure 39]



NOTE The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in the timing parameter table of this standard.

Figure 5. Burst write followed by burst read [JESD79-2E figure 41]

USING QUALIPHY DDR2

QualiPHY DDR2 guides the user, step-by-step, through each of the source tests described in JEDEC Standard No. 79-2E. To do this, the user must setup a test session.

Users choose test configurations to run. There are several pre-loaded test configurations including:

- **1) Clock tests DDR2-667 (1 Probe)**
- **2) CKdiff-DQse-DQSdiff 667 Write Burst (3 probes)**
- **3) CKdiff-DQse-DQSdiff 667 Read Burst (3 probes)**
- **4) Eye Diagram (3 Probes Debug)**
- **5) All tests that require 4 Probes**
- **D1) Demo of All Clock tests**
- **D2) Demo of Eye Diagram (Debug)**
- **D3) Demo of All tests**
- **D4) Demo of All Ck-diff-DQSdiff-DQse tests**

The pre-loaded configurations provide quick and easy ways to begin compliance testing. You can create your own custom configurations (see the **Customizing QualiPHY** topic for details).

The variables are pre-loaded with the standard settings for compliance testing; however, the user may choose to create their own configuration with the variables set as desired.

QUALIPHY COMPLIANCE TEST PLATFORM

QualiPHY is Teledyne LeCroy's compliance test framework which leads the user through the compliance tests. QualiPHY displays connection diagrams to ensure tests run properly, automates the oscilloscope setup, and generates complete, detailed reports.

The QualiPHY software application automates the test and report generation.

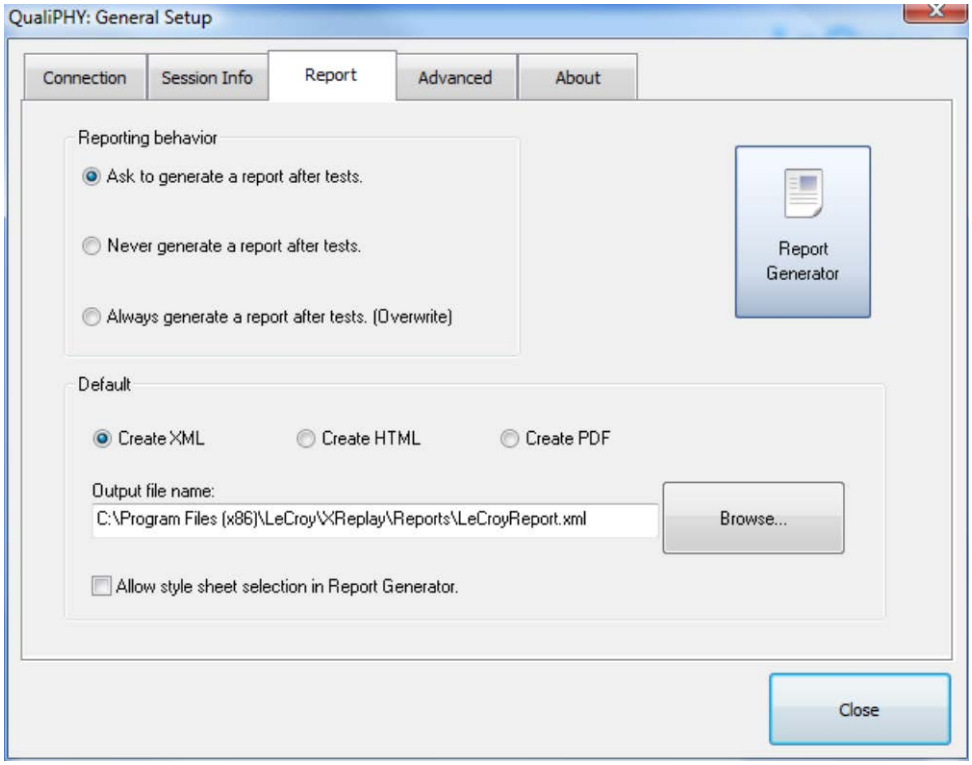


Figure 6. Report menu in QualiPHY General Setup

LeCroy

QualiPHY

DDR2 Test Report

Overall result: Pass

DUT:	Demo
Comment:	Example
Time of test:	02/28/2009 02:58:51
Operator:	LeCroy
Temperature	25° C
Configuration in use:	Demo of All tests
Limits in use:	DDR2-667
Standard in use:	DDR2
Oscilloscope Name:	geneva-nb201 Model: WP760ZI
Oscilloscope Serial #:	GENEVA-NB201
Computer:	GENEVA-NB201
Oscilloscope firmware version:	0.5.9.0 (Build 122911)
QualiPHY core version:	0.5.8.0 (Build 122474)
QualiPHY script version:	0.1.3.235
Stylesheet version:	1.2.0.2

Summary Table

[Hide Table]

Pass	Test	Measurement	Current Value	Test Criteria
✔	Timing	tAC.Min	29 ps	>= -450 ps
✔	Timing	tDS(base).min	567 ps	>= 100 ps
✔	Clock	Clock Speed Grade	668.868 MHz	Informational Only
✔	Timing	tDS1(base).min	486 ps	>= -25 ps

Details

PROBE SETUP: CKdiff-DQse-DQSdiff

Clock Tests

[Up]

Measurement:	***Clock Speed Grade***
Limit Name:	InfoOnlyMHz
Current Value:	668.863 MHz
Test Criteria:	Informational Only
Timestamp:	02/28/2009 02:59:04
Description:	Check that Clock has the expected frequency

Clock Frequency
Timestamp: 02/28/2009 02:59:05

[Up]

Pass

Measurement:	***tJIT(per)rise, min***
Limit Name:	tJIT(per)_limit
Current Value:	-57 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:11
Description:	Clock Period Jitter, rising edge, min

[Up]

Pass

Measurement:	***tJIT(per)rise, max***
Limit Name:	tJIT(per)_limit
Current Value:	41 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:11
Description:	Clock Period Jitter, rising edge, max

Test Timing - tDS(base) min: DQ10 VIH/VIL(ac) to DQS1 VREF
Timestamp: 02/28/2009 03:02:35

[Up]

Pass

Measurement:	***tJIT(per)fall, min***
Limit Name:	tJIT(per)_limit
Current Value:	-59 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:11
Description:	Clock Period Jitter, falling edge, min

[Up]

Pass

Measurement:	***tJIT(per)fall, max***
Limit Name:	tJIT(per)_limit
Current Value:	50 ps
Test Criteria:	-125 ps <= n <= 125 ps
Timestamp:	02/28/2009 02:59:12
Description:	Clock Period Jitter, falling edge, max

[Up]

Pass

Measurement:	***tJIT(cc)rise***
Limit Name:	tJIT(cc)_limit_abs
Current Value:	94 ps
Test Criteria:	<= 250 ps
Timestamp:	02/28/2009 02:59:12
Description:	Cycle to Cycle Period Jitter, rising edge

[Up]

Pass

Measurement:	***tJIT(cc)fall***
Limit Name:	tJIT(cc)_limit_abs
Current Value:	102 ps
Test Criteria:	<= 250 ps
Timestamp:	02/28/2009 02:59:12
Description:	Cycle to Cycle Period Jitter, falling edge

[Up]

Measurement:	***Number of Clock Cycles***
Limit Name:	InfoOnly
Current Value:	200
Test Criteria:	Informational Only
Timestamp:	02/28/2009 02:59:12
Description:	200 clock cycles are required for compliance test

[Up]

Pass

Measurement:	***tDS1(base) min***
Limit Name:	tDS1(base)_min
Current Value:	486 ps
Test Criteria:	>= -25 ps
Timestamp:	02/28/2009 03:02:54
Description:	DQ and DM Input Setup Time

Test Timing - tDS1(base) min: DQ10 VIH/VIL(ac) to DQS1p VIH/VIL(dc) and DQS1n VIH/VIL(dc)
Timestamp: 02/28/2009 03:02:55

Figure 7. The Test Report includes a summary table with links to the detailed test results

Oscilloscope Option Key Installation

An option key must be purchased to enable the QPHY-DDR2 option. Call Teledyne LeCroy Customer Support to place an order and receive the code.

Enter the key and enable the purchased option as follows:

1. From the oscilloscope menu select **Utilities → Utilities Setup**
2. Select the **Options** tab and click the **Add Key** button.
3. Enter the **Key Code** using the on-screen keyboard.
4. Restart the oscilloscope to activate the option after installation.

Typical (Recommended) Configuration

QualiPHY software can be executed from the oscilloscope or a host computer. The first step is to install QualiPHY.

Teledyne LeCroy recommends running QualiPHY on an oscilloscope equipped with Dual Monitor Display capability (Option DMD-1 for oscilloscopes where this is not standard). This allows the waveform and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

By default, the oscilloscope appears as a local host when QualiPHY is executed in the oscilloscope. Follow the steps under **Oscilloscope Selection** (as follows) and check that the IP address is 127.0.0.1.

Remote (Network) Configuration

It is also possible to install and run QualiPHY on a host computer, controlling the oscilloscope with a Network/LAN Connection.

The oscilloscope must already be configured, and an IP address (fixed or network-assigned) must already be established.

Oscilloscope Selection

Set up the oscilloscope using QualiPHY over a LAN (Local Area Network) by doing the following:

1. Make sure the host computer is connected to the same LAN as the oscilloscope. If unsure, contact your system administrator.
2. From the oscilloscope menu, select **Utilities → Utilities Setup**
3. Select the **Remote** tab.
4. Verify the oscilloscope has an IP address and the control is set to TCP/IP.
5. Run QualiPHY in the host computer and click the **General Setup** button.
6. Select the **Connection** tab.
7. Enter the IP address from step 4 (previous).
8. Click the **Close** button.

QualiPHY is now ready to control the oscilloscope.

QualiPHY tests the oscilloscope connection after clicking the **Start** button. The system prompts you if there is a connection problem. QualiPHY's **Scope Selector** function can also be used to verify the connection.

Accessing the QPHY-DDR2 Software using QualiPHY

This topic provides a basic overview of QualiPHY's capabilities.

Access the QPHY-DDR2 software using the following steps:

1. Wait for the oscilloscope to start and have its main application running.
2. Launch QualiPHY from the **Analysis** menu if installed on the oscilloscope or from the desktop icon if installed on a host computer.
3. From the QualiPHY main window (as follows), select **Standard**, then **DDR2** from the pop-up menu (if not already selected). If you check the **Pause on Failure** box (circled) QualiPHY prompts to retry the test in the case of a failure.

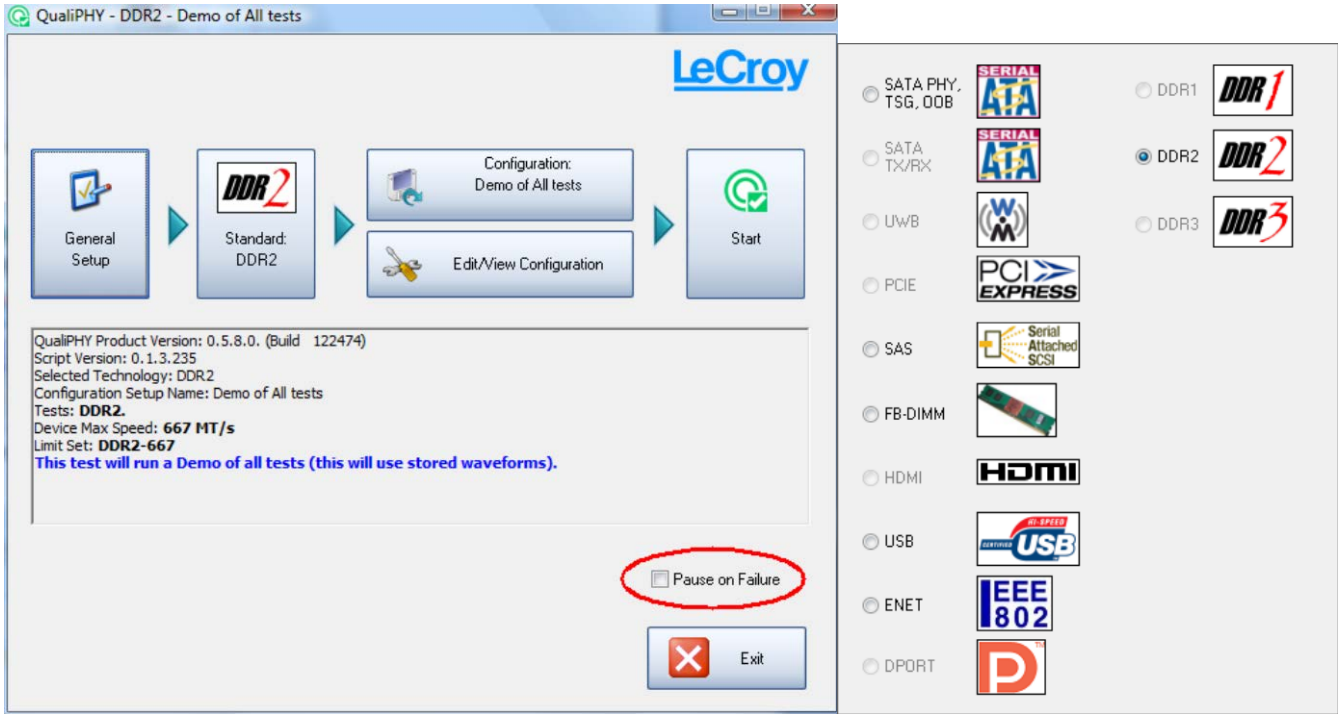


Figure 8. QualiPHY main menu and compliance test Standard selection menu

4. Click the **Configuration** button in the QualiPHY main menu:

5. Select a configuration from the pop-up menu:

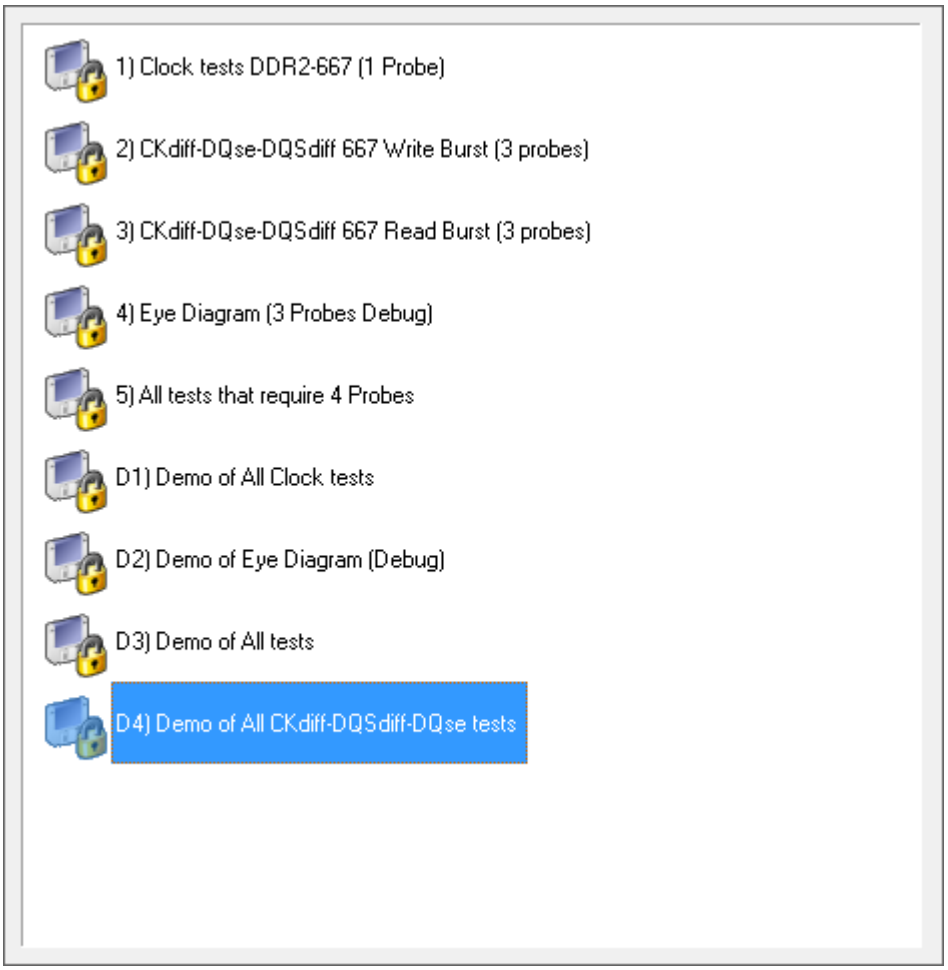


Figure 9. QualiPHY configuration selection menu

6. Click **Start**.

7. Follow the pop-up window prompts.

Customizing QualiPHY

The predefined configurations in the **Configuration** screen cannot be modified. However, you can create your own test configurations by copying one of the standard test configurations and making modifications. A description of the test is also shown in the description field when selected.

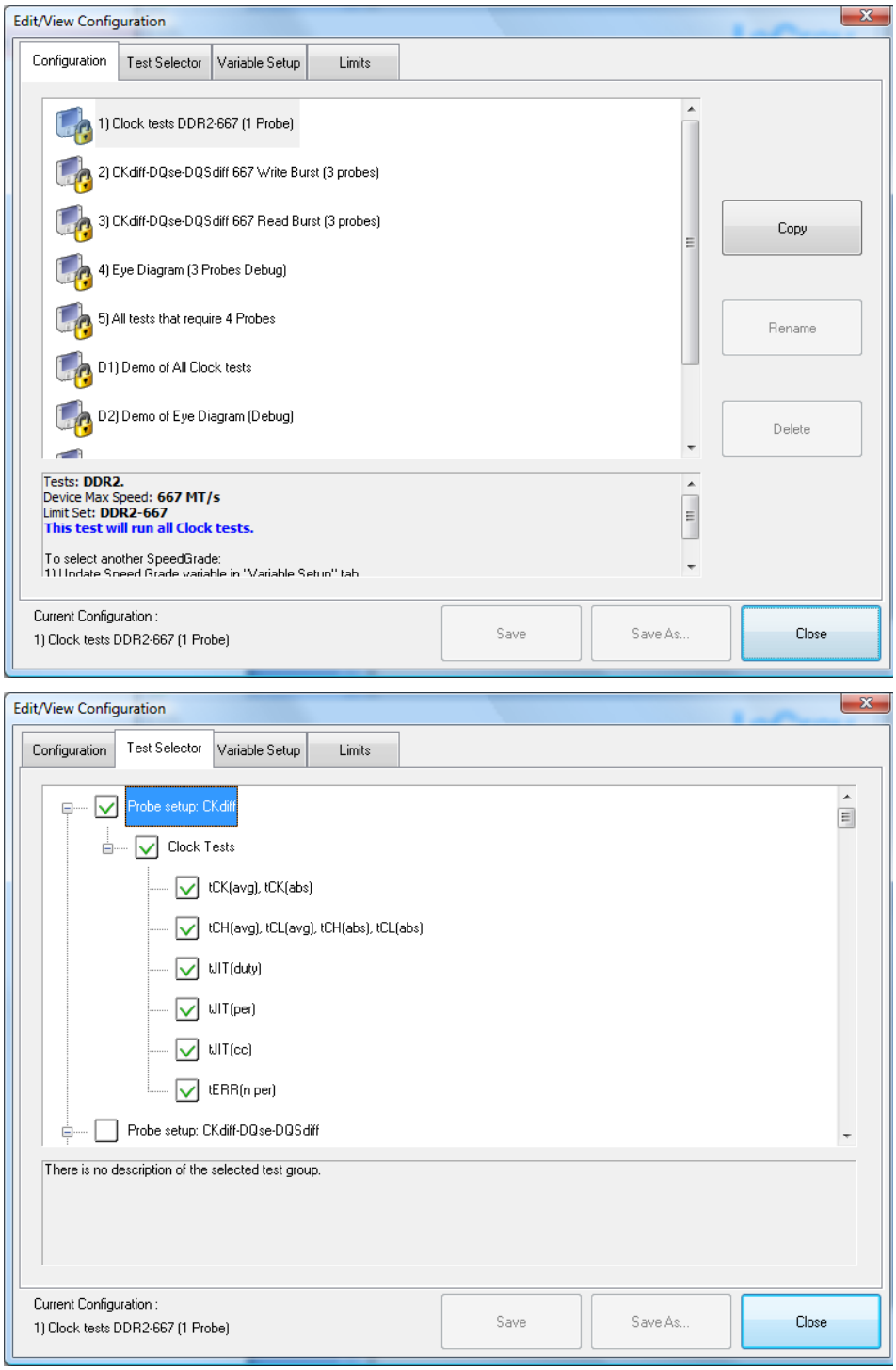


Figure 10. QualiPHY test item selection menu

Once a custom configuration is defined, script variables and the test limits can be changed by using the **Variable Setup** and **Limits Manager** from the **Edit/View Configuration** window.

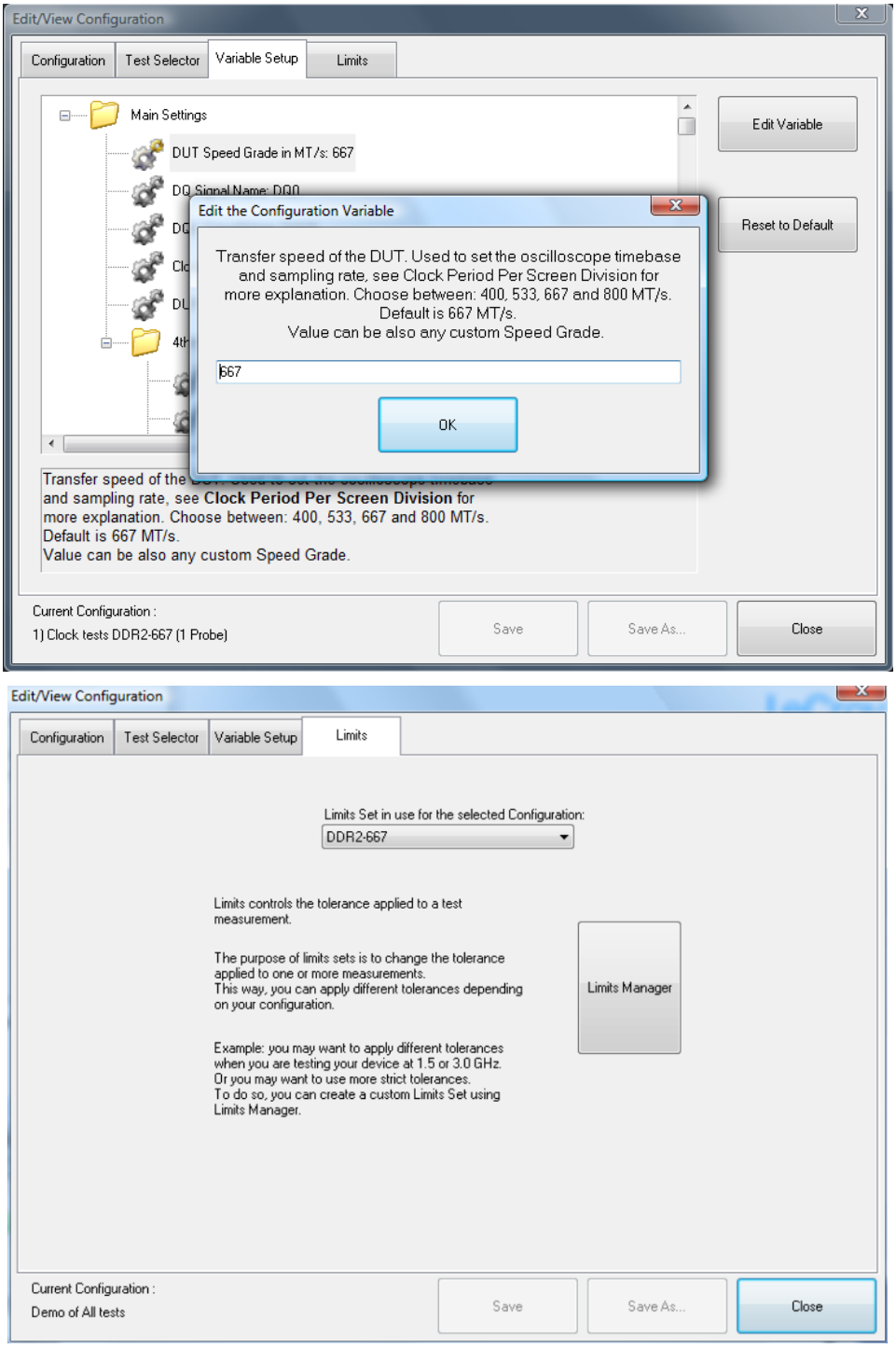


Figure 11. Variable Setup and Limits Manager windows

QPHY-DDR2 Operation

After pressing **Start** in the QualiPHY menu, the software instructs how to set up the test using pop-up connection diagrams and dialog boxes.

Figure 12. Start button

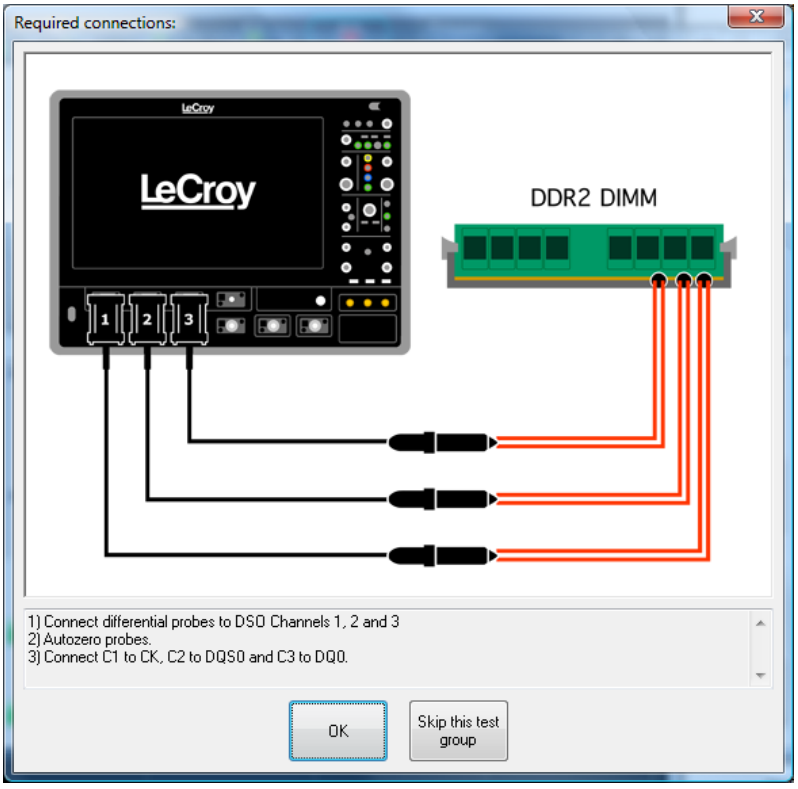


Figure 13. Example of pop-up connection diagram and dialog box

DDR2 MEASUREMENT PREPARATION

Before starting any test or data acquisition, the oscilloscope must be warmed for at least 20 minutes. Calibration is automatic under software control and no manual calibration is required. The procedure should be run again if the temperature of the oscilloscope changes by more than a few degrees.

Differential Probe Deskew Procedure using TF-DSQ

Note: Another procedure can be used for Zi oscilloscopes, refer to the next section for details.

Follow the procedure described in the TF-DSQ Probe Deskew and Calibration Fixture manual. Deskew all four channels with their respective probe, using external trigger (AUX IN) as reference signal.

You can get more information on TF-DSQ using the oscilloscope Help menu and searching for Probe Calibration. There is also a section on Deskew Theory of Operation.

Differential Probe Deskew Procedure on Zi oscilloscopes using PCF200

Use the PCF200 Characterization Fixture provided as standard accessory with WaveLink series probes. The fixture determines the effect of probe input loading on the circuit under test and the probe response to the signal being measured, using the AT, ST, Dx10, and Dx20 modules with SI, or SP, or QC (QC for WL-Plink only) interconnect leads.

Probe calibration is accomplished with the PCF200 fixture by following the basic steps in the following flowchart. It is recommended that you read the instructions presented here in their entirety to familiarize yourself with the advanced features of the PCF200 fixture.

Connecting probes to the circuit under test can be a difficult procedure. With this in mind, Teledyne LeCroy's system is designed in a manner that allows you to set up the probe calibration fixture, calibrate each individual probe once, connect your probes to the circuit, and disconnects the fixture. Once your probes are in the circuit, there is no need to revisit the fixture until the next calibration interval.

You should familiarize yourself with the following topics:

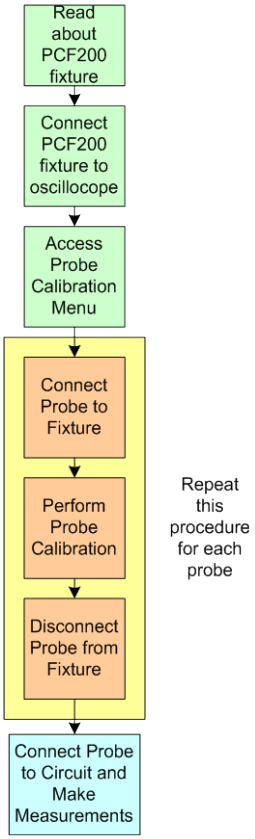
-

PCF200 Fixture Overview

- **Probe Connection to PCF200**
- **Probe Calibration Menu**
- **D620 Probe Calibration**

Advanced mode is available:

- **Advanced Mode Probe Calibration Menu**
- **Advanced Probe Calibration**



Connecting probes to the circuit under test can be a difficult procedure. With this in mind, Teledyne LeCroy's system is designed in a manner that allows you to set up the probe calibration fixture, calibrate each individual probe once, connect your probes to the circuit, and disconnect the fixture. Once your probes are in the circuit, there is no need to revisit the fixture until the next calibration interval.

You should familiarize yourself with the following topics:

- **PCF200 Fixture** Overview
- **Probe Connection to PCF200**
- **Probe Calibration Menu**
- **D620 Probe Calibration**

Advanced mode is available:

- **Advanced Mode Probe Calibration Menu**
- **Advanced Probe Calibration**

PCF200 Fixture Overview

Major components of the PCF200 fixture are shown in the following figure:

- SMA male connector Fast Edge input.
- SMA female connector output to AUX IN for 50-ohm termination.
- Clip for connection of Solder-In probes.
- 2-pins header for connection of Square-Pin probes.

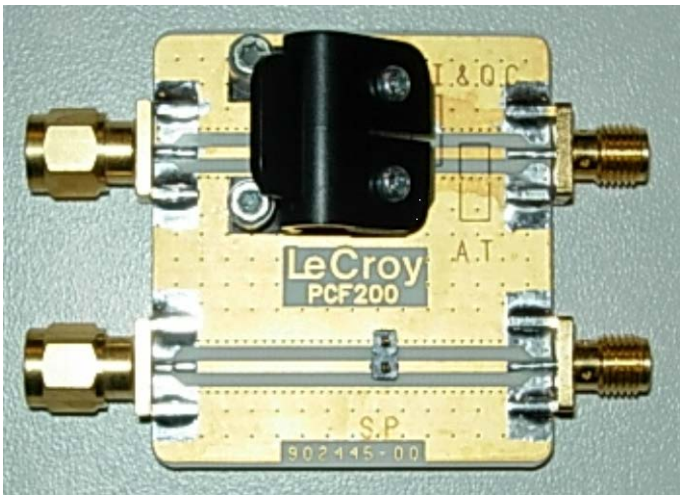


Figure 14. PCF200 Deskew Fixture

A SMA male to BNC male 50-ohm cable is required to perform the calibration.

System assembly is accomplished in the following steps:

1. Connect the BNC end of the 50 Ohm cable to the oscilloscope AUX IN.
2. Connect the SMA end of the 50 Ohm cable to the SMA female connector on the PCF200 fixture.
3. Connect the PCF200 SMA male connector to the oscilloscope Fast Edge SMA output.

The SMA connections should be torqued with an RF torque wrench and must be properly tightened.

Probe Connection to PCF200

The PCF200 provides multiple probe connectors for various kinds of probes. There are 2 circuits depending on the type of probes to calibrate:

- The upper circuit is for Solder-In (SI) and Quick-Connect (QC) probes. This circuit can also be used for AT probes using the designated area to apply the probe tips.
- The lower circuit is for Square-Pin (SP) probes.

Probes are connected electrically in a single-ended arrangement: the positive (+) side of the probe must be connected to the signal trace, while the negative (-) side is connected to the ground plane.

Figure 15. Differential probe properly connected to the fixture (Solder-In configuration)

Probe Calibration Menu

The probe calibration menu can be accessed from the Vertical drop-down menu or from the channel dialog:

Figure 16. Accessing the probe calibration menu

Figure 17. Basic Probes Calibration menu

The information in the probe calibration menu is organized such that each row represents the information for a given channel, and each column represents the calibration information or control for that channel. For each channel, the information and control provided includes:

- The channel number in the colored button icon and the probe type that is installed.
- A **Full Calibration** button, which starts the calibration. Use only with TF-DSQ. DO NOT use with PCF200.
- DC correction information including both gain and offset correction.
- The skew correction.
- A **Clear** button.

Probe

This area shows the type of probe connected to the channel. All other information shown in a given row is associated with that probe.

Full Calibration Button

This button causes the oscilloscope to automatically perform a full DC and deskew calibration. See details of DC Calibration Theory of Operation and Deskew Theory of Operation in TF-DSQ Operation Manual. Use only with TF-DSQ. DO NOT use with PCF200.

Gain & Offset

These fields show the gain and offset applied to the probe. If the probe measures a voltage of V, the new, calibrated voltage is:

$$V_{calibrated} = V \cdot Gain + Offset$$

Note that the offset is in Volts, and the gain is unitless.

The probe DC calibration information can be entered either manually or as the result of an automatic calibration. In the case of automatic calibration, it can be part of the full calibration or it can be a standalone DC calibration executed in advanced mode. When the DC calibration information is a result of an automatic calibration utilizing the TF-DSQ fixture, the information shown is the gain and offset utilized for the currently configured channel sensitivity (volt/division setting; see details of DC Calibration Theory of Operation in the TF-DSQ Operator's Manual on the Teledyne LeCroy website for details). In this case, when the channel sensitivity is altered these values change. **When the DC calibration information is entered manually, it clears any automatic results and replaces them globally with the newly entered values. This means that if new gain and offset numbers are entered manually, these values apply across all sensitivity oscilloscope settings.**

The gain is limited to between 0.8 and 1.2, but the offset is not limited.

Note: It is important to note that some passive probes, and any user-designed probes, do not provide proper probe identification information to the oscilloscope. In these cases, the oscilloscope may not be able to determine the proper attenuation values and you should make sure that the proper attenuation is entered from the channel's **Vertical** setup dialog. Furthermore, the gain entered should be the gain *correction* applied to the system with the correctly entered attenuation.

If used with PCF200, enter values manually.

Skew

This field shows the measured skew between the probe in the specified channel and the reference channel. This can be entered manually or as the result of an automatic calibration. In the case of automatic calibration, it can be the result of a portion of the full calibration or it can be the result of a standalone deskew calibration. Even after the deskew has been performed automatically, the deskew correction can be adjusted manually.

Clear

All probe calibrations can be cleared by pressing this button corresponding to a specific probe.

Calibration Source

This field specifies the signal source used for DC calibrations. When using the PCF200 fixture, specify AUX OUT as the calibration source (even if the PCF200 is connected to Fast Edge output). This signal is not used for deskew.

Calibration Skew Reference

These values specify the channel or external input where the skew reference is supplied. The skew reference is the absolute time reference to which all deskew measurements are made. When the PCF200 fixture is used, select the EXT input.

Recall Calibration

Whenever a probe calibration is applied, the oscilloscope saves the information in a file on the disk. If the oscilloscope must be rebooted for any reason, the probe calibration information is always cleared, but can be manually recalled by pressing this button.

Advanced Mode Checkbox

When the **Advanced Mode** checkbox is unchecked, you have access to the basic probe calibration menu. The basic probe calibration menu shows you only what is absolutely needed to perform a simple calibration of the probes. In other words, it shows you the calibration information and provides the capability to calibrate the probe with a single button press, clear the calibration information, and manually reload the calibration information following an oscilloscope reboot. When the advanced mode button is checked, you have access to the advanced mode probe calibration menu.

This checkbox must be checked for deskew calibration using PCF200.

Advanced Mode Probe Calibration Menu

The advanced mode is entered by checking the advanced mode box in the basic probe calibration menu.

Figure 18. Advanced Mode Probe Calibration menu

Checking this box allows:

- Calibration of gain/offset only
- Calibration of deskew only
- Access to the advanced menu (shown as a tab behind the "Probes Cal" dialog)

Gain/Offset Only

Pressing this button performs only the DC calibration of the probe on the specified channel. See details of DC Calibration Theory of Operation in TF-DSQ Operation Manual. DO NOT use with PCF200 connected to Fast Edge output.

Deskew Only

Pressing this button performs only the deskew calibration of the probe on the specified channel. See details of Deskew Theory of Operation in TF-DSQ Operation Manual.

This is the button to use with PCF200 connected to Fast Edge output.

The Advanced Menu

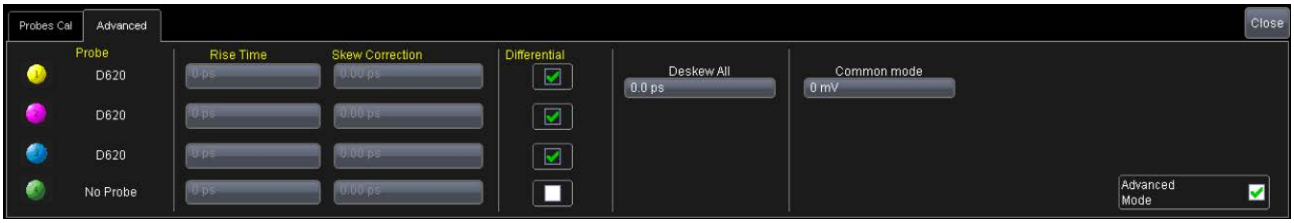


Figure 19. Probes Calibration menu Advanced tab

The Advanced Menu contains information and functionality useful to the advanced user of the PCF200 fixture. These include:

- Rise Time Skew Correction
- Differential(or Single-Ended) probe selection
- Deskew All (or common deskew capability)
- Common mode voltage settings for DC calibration

Rise Time Skew Correction

This field shows the signal risetime and the corresponding skew correction based on the signal risetime.

When probes are deskewed, the risetime measurement of the edge used for deskewing is displayed in the **Rise Time** field corresponding to the probe and probe channel, and an additional skew correction of zero is applied.

The measured risetime of the signals encountered can be entered into the **Rise Time** field, and the oscilloscope automatically calculates and applies a new skew correction value to be utilized in addition to the deskew amount calculated during the deskew calibration procedure. With this use, a finer deskew calibration is performed because the risetimes of the signals measured are now taken into account. Refer to the Deskew Risetime Adjustment Theory of Operation in the TF-DSQ Operator's Manual on the Teledyne LeCroy website for details.

Differential (or Single-Ended) Probe Selection

The PCF200 fixture calibrates probes differentially or in single-ended mode depending on the type of probe used. The selection is done automatically when the probe is detected. If No Probe is detected, the selection is done manually. When calibrating D620 probes, they are automatically detected and Differential is checked.

Deskew All (or Common Skew)

This is the deskew amount applied to all channels. The time entered in this field is the absolute time by which all waveforms displayed by the oscilloscope are delayed in time. This value effectively adjusts the zero time reference of the system. See Deskew Theory of Operation in the TF-DSQ Operation Manual for details.

Common Mode Voltage Selection

Differential probes allow the common mode voltage component to be applied during the DC calibration for improved calibration accuracy in situations where probe gain or offset correction depends on common mode components. See DC Calibration Theory of Operation or Differential and Single-ended Probe Basics in TF-DSQ Operation Manual for details.

Advanced Probe Calibration

When the **Advanced Mode** checkbox is checked, you can perform the DC calibration and the deskew calibration separately by pressing **Gain/Offset Only** or **Deskew Only**.

When performing DC calibration, you have the option to apply a common mode component to the differential DC levels applied to the probe during calibration. See DC Calibration Theory of Operation or Differential and Single-ended Probe Basics in TF-DSQ Operation Manual for details. Use this with TF-DSQ. DO NOT use with PCF200 connected to Fast Edge output.

After performing the deskew calibration, you have the option to apply a common skew value to all channels to adjust the zero time reference of the system.

If you know the risetime of the signals being measured, you can enter the measured risetime of the signals in the **Rise Time** field to obtain a further skew correction that accounts for the risetime. If the risetime entered is less than the risetime measured during the calibration, no correction is applied; otherwise, the system calculates a correction to account for the signal risetime. This makes it important to enter the measured risetime, meaning, the risetime of the signal the oscilloscope measures (or will measure). Refer to the Deskew Risetime Adjustment Theory of Operation in the TF-DSQ Operator's Manual on the Teledyne LeCroy website for details.

D620 Probe Calibration Procedure

The PCF200 fixture is used to calibrate D620 probes. Prior to beginning your measurements

- Assemble the PCF200 fixture
- Attach the fixture, as described in **PCF200 Fixture** Overview.
- Access the Probe Calibration Menu in Advanced Mode

Follow the instructions for each probe used:

- Connect the probe to the oscilloscope channel
- Attach the probe to the PCF200 fixture
- Press the **Deskew Only** button in the Advanced Probe Calibration Menu.
- Wait a few seconds as the probe is calibrated.
- When the calibration completes, remove the probe from the PCF200 fixture

Now you are ready to probe the circuit and perform your measurements. If power is interrupted during your measurements, reboot the oscilloscope and manually recall your settings.

QPHY-DDR2 TEST CONFIGURATIONS

Configurations include variable settings and limit sets as well, not just test selections. See the section for a description of each variable value and its default value. See the **QPHY-DDR2 Limit Sets** section for more information about the limit sets.

1) **Clock tests DDR2-667 (1 Probe)**

This configuration runs all of the clock tests. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- tCK(avg)
- tCK(abs)
- tCH(avg)
- tCL(avg)
- tCH(abs)
- tCL(abs)
- tJIT(duty)
- tJIT(per)
- tJIT(CC)
- tERR(n per)

2) CKdiff-DQse-DQSdiff 667 Write Burst (3 probes)

This configuration runs all of the tests that are run on write bursts of the DDR2 signals in which 3 probes are required. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- Eye Diagram – Write Bursts (Inputs)
- SlewR
- SlewF
- VIH(ac)
- VIH(dc)
- VIL(ac)
- VIL(dc)
- VSWING
- AC Overshoot Peak Amplitude
- AC Overshoot Area above VDDQ
- AC Undershoot Peak Amplitude
- AC Undershoot Area below VSSQ
- tDQSS
- tDQSH
- tDQSL
- tDSS

- tDSH
- tDS(base)
- tDH(base)
- tWPRE
- tWPST

3) CKdiff-DQse-DQSdiff 667 Read Burst (3 probes)

This configuration runs all of the tests that are run on read bursts of the DDR2 signals in which 3 probes are required. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- Eye Diagram – Read Bursts (Outputs)
- SoutR
- SoutF
- tSLMR
- tDQSQ
- tQHS
- tQH
- tDQSCK
- tAC
- tHZ(DQ)
- tLZ(DQ)
- tLZ(DQS)
- tRPRE
- tRPST

4) Eye Diagram (3 Probes Debug)

This configuration runs the Eye Diagram tests on both the read bursts and the write bursts. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- Eye Diagram – Write Bursts (Inputs)
- Eye Diagram – Read Bursts (Outputs)

5) All tests that require 4 Probes

This configuration runs all of the tests that require 4 probes. These are the tests where the DQS is probes single ended, the CK is probes single ended, or the signal under test is an Address, Control or Data Mask line. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

- VID(ac)
- VIX(ac)
- VOX(ac)

- tDS1(base)
- tDH1(base)
- SlewR (on Add/Ctrl signal)
- SlewF (on Add/Ctrl signal)
- VIH(ac) (on Add/Ctrl signal)
- VIH(dc) (on Add/Ctrl signal)
- VIL(ac) (on Add/Ctrl signal)
- VIL(dc) (on Add/Ctrl signal)
- VSWING (on Add/Ctrl signal)
- AC Overshoot Peak Amplitude (on Add/Ctrl signal)
- AC Overshoot Area above VDDQ (on Add/Ctrl signal)
- AC Undershoot Peak Amplitude (on Add/Ctrl signal)
- AC Undershoot Area below VSSQ (on Add/Ctrl signal)
- tIS(base) (on Add/Ctrl signal)
- tIH(base) (on Add/Ctrl signal)

D1) Demo of All Clock tests

This configuration uses the saved waveforms found in the **D:\Waveforms\DDR2** folder and runs all of the clock tests. All of the variables are set to their defaults except **Use Stored Waveforms** is set to **Yes** and **Use Stored Trace for Speed Grade** is set to **Yes**. The limit set in use is DDR2-667. The tests run are:

- tCK(avg)
- tCK(abs)
- tCH(avg)
- tCL(avg)
- tCH(abs)
- tCL(abs)
- tJIT(duty)
- tJIT(per)
- tJIT(CC)
- tERR(n per)

D2) Demo of Eye Diagram (Debug)

This configuration uses the saved waveforms found in the **D:\Waveforms\DDR2** folder and run the Eye Diagram test on the read bursts and the write bursts. All of the variables are set to their defaults except **Use Stored Waveforms** is set to **Yes** and **Use Stored Trace for Speed Grade** is set to **Yes**. The limit set in use is DDR2-667. The tests run are:

- Eye Diagram – Write Bursts (Inputs)
- Eye Diagram – Read Bursts (Outputs)

D3) Demo of All tests

This configuration uses the saved waveforms found in the **D:\Waveforms\DDR2** folder and run all of the tests. All of the variables are set to their defaults except **Use Stored Waveforms** is set to **Yes** and **Use Stored Trace for Speed Grade** is set to **Yes**. The limit set in use is DDR2-667. All supported tests are run.

D4) Demo of All CKdiff-DQSdiff-DQse tests

This configuration uses the saved waveforms found in the **D:\Waveforms\DDR2** folder and run all of the tests requiring probing the clock and strobe signals differentially and the single ended data signal. All of the variables are set to their defaults except **Use Stored Waveforms** is set to **Yes** and **Use Stored Trace for Speed Grade** is set to **Yes**. The limit set in use is DDR2-667. All supported tests are run.

QPHY-DDR2 VARIABLES

General Variables

The following variables are used by all configurations. They can be used in conjunction with the test selection and limit set selection to create custom configurations.

DUT Speed Grade in MT/s

Transfer speed of the DUT. Used to set the oscilloscope timebase and sampling rate, see **Clock Period Per Screen Division** variable for more explanation. Choose between: 400, 533, 667 and 800 MT/s. Default is 667 MT/s.

DQ Signal Name

Select name of data (DQ) SUT. Choose between available DDR signal names. Default is DQ0.

DQS Signal Name

Select name of strobe (DQS) SUT. Choose between available DDR signal names. Default is DQS0.

Clock Signal Name

Select name of clock (CK) SUT. Choose between available DDR signal names. Default is CK.

DUT Power Supply VDDQ

Value of VDDQ used to compute test limits as specified by Jedec standard. Default is 1.8 V.

4th Probe Names

DQSp Signal Name

Select the name of the positive strobe (DQSp) SUT. Choose between available DDR signal names. Default is DQS0p.

DQSn Signal Name

Select the name of the negative strobe (DQSn) SUT. Choose between available DDR signal names. Default is DQS0n.

ADD/CTRL signal name

Select the name of the Address or Control SUT. Choose between available DDR signal names. Default is A0.

Clock Positive Signal Name

Select the name of the positive clock (CKp) SUT. Choose between available DDR signal names. Default is CKp.

Clock Negative Signal Name

Select the name of the negative clock (CKn) SUT. Choose between available DDR signal names. Default is CKn.

DM Signal Name

Select the name of the Data Mask SUT. Choose between available DDR signal names. Default is DM0.

Script Settings

Save Acquired Waveforms

Saved waveforms can be used later in demonstration or optimized version of script. Choose between Yes or No. The default is No. This setting is ignored (no save) if using stored waveforms is enabled and in Demo mode.

Silent mode control

No more interaction with the user when silent mode is on. Choose between Yes or No. Default is No. This is useful to let the test run without interruption in the background.

Stop On Test to review results

When set to **Yes**, the script stops after each test allowing you to view the results. The setup is saved so the oscilloscope settings can be modified by the user. On resume, the setup is recalled. Any new acquisition done may cause the script to produce unexpected results.

Waveform Path

Specify the path on the oscilloscope to save/recall waveforms. When not in **Demo Mode** and when **Save acquired waveforms** is enabled, the waveforms are saved in this folder. When set to **Demo Mode** or when **Use stored trace for pixel clock measure**, waveforms are also available from this folder. The default location is **D:\Waveforms\DDR2**.

Demo Settings

Use Stored Waveforms

When enabled, previously stored DDR2 waveforms is used. Default is No.

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Define format used to set trace names

Stores a saved waveform naming format or convention The choices are **LeCroy** or **Dialog**. The **LeCroy** choice produces waveform names automatically by the software. **Dialog** prompts the user for custom waveform names. The default setting is **LeCroy**.

Use Stored Trace for Speed Grade

This is an optimization used specifically to measure the clock frequency only once. Choose from **Yes** or **No** values, The default selection is **No**.

Advanced Settings

Clock Period per Screen Division

Oscilloscope timebase and sampling rate is set to acquire the given number of clock cycle per display horizontal division at a given **DUT Speed Grad in MT/s** and for a **Max. Number of Samples Per Clock Period**. The default is 3341 clock periods (this gives a 10us/div timebase at 667 MT/s and 3.3MS max for 100 samples per period).

Timebase = [**Clock Period Per Screen Division**] / ([**DUT Speed Grade in MT/s**] / 2 * 1e6)

Maximum Samples = **[Max. Number Of Samples Per Clock Period]** * [**Clock Period Per Screen Division]** * 10

Number of cycles for Clock test

Jedec standard requires 200 cycles for the Clock compliance test.

This is the default value of this variable. Any positive number can be entered.

Max. Number Of Samples Per Clock Period

The oscilloscope timebase and sampling rate is set to acquire the given number of points per clock period. The oscilloscope is always set to at least acquire at 20GS/s. Additionally, if an oscilloscope with greater than 6GHz bandwidth is used, the bandwidth is limited to 6GHz. See the **Clock Period Per Screen Division** topic for more details. Choose between 10;20;50;100;200;500 or 1000. The default value is 100.

Configuration Specific Variables

The following variables are specific to the configuration in which they appear under. Some of these variables appear under multiple configurations.

XX Channel Gain

Allows the user to manually specify the vertical scale in V/div for XX SUT. XX can be Clock, DQ, DQS, DQSn, ADD/CTRL, or DM. Default is 0 for auto-scale.

XX Channel Index

Allows the user to manually specify the channel XX SUT. XX can be Clock, DQ, DQS, DQSn, ADD/CTRL, or DM. Default is 1 for CK, 2 for DQS, 3 for DQ and 4 for others

XX Channel Invert

Allows the user to invert XX SUT. XX can be Clock, DQ, DQS, DQSn, ADD/CTRL, or DM. Default is False.

XX Channel Offset

Allows the user to manually specify the offset in Volts for XX SUT. XX can be Clock, DQ, DQS, DQSn, ADD/CTRL, or DM. Default is 0 for auto-scale.

Select Signal Under Test if many

These variables allow the user to specify which signals to tests for particular tests. The default state is to tests all of the pertinent signals. For the ADD/CTRL tests the default is ADD and for the DM tests the default is DM

Previously measured tHP in seconds
tHP is usually computed from the result of test tCH/tCL. However if a result is not available, the value entered here is used. If this variable is set to 0, then tHP is computed from the DUT Speed Grade in MT/s.

Max Overshoot Peak Amplitude

For address and control signals, the maximum requirements for peak amplitude were reduced from 0.9V to 0.5V. Default value is 0.5 V.

Note: Register vendor data sheets specify the maximum over/undershoot induced in specific RDIMM applications. DRAM vendor data sheets also specify the maximum overshoot/undershoot that their DRAM can tolerate. This allows the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register induces in the specific RDIMM.

QPHY-DDR2 LIMIT SETS

DDR2-400

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 400 MT/s.

DDR2-533

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 533 MT/s.

DDR2-667

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 667 MT/s.

DDR2-800

This corresponds to the JEDEC JESD79-2E DDR2 standard specification limits for 800 MT/s.

DDR2-1066

This corresponds to the JEDEC JESD208 DDR2 standard specification limits for 1066 MT/s.

QPHY-DDR2 TESTS

Clock Tests

All time measure on clock CK are done at level VREF.

tCK(avg), Average Clock Period

tCK(avg) is defined as the average clock period over any 200 consecutive clock periods.

tCK(avg) = SUM(tCKi) / 200 where i=1 to 200

Measured on both the rising and the falling edge.

tCK(abs), Absolute Clock Period

tCK(abs) is defined as the absolute clock period of each of 200 consecutive clock periods.

Measured on both the rising and the falling edge.

tCH(avg), Average High Pulse Width

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

tCH(avg) = SUM(tCHi) / (200 x tCK(avg)) where I = 1 to 200

See Figure 20 as follows.

tCL(avg), Average Low Pulse Width

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

tCL(avg) = SUM(tCLi) / (200 x tCK(avg)) where i=1 to 200

See Figure 20 as follows.

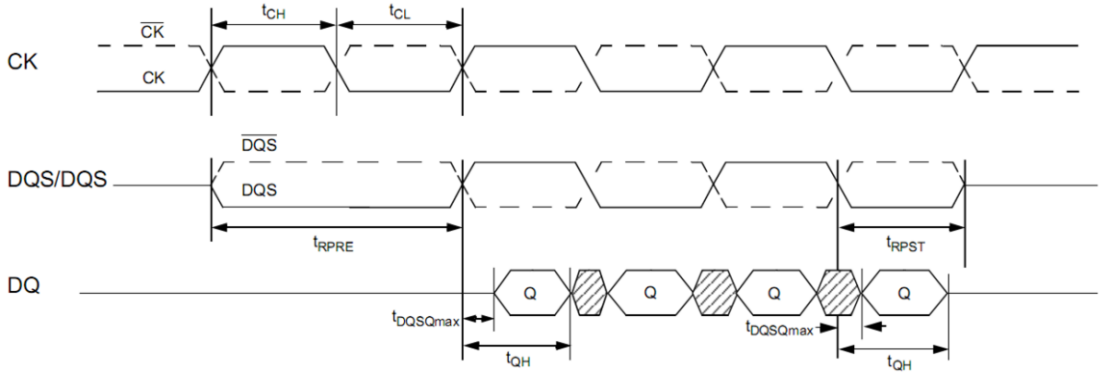


Figure 20. Data output (read) timing [JESD79-2E figure 32]

tCH(abs), Absolute High Pulse Width

tCH(abs) is defined as the absolute high pulse width, of each of 200 consecutive high pulses.

tCL(abs), Absolute Low Pulse Width

tCL(abs) is defined as the absolute low pulse width of each of 200 consecutive low pulses.

tJIT(duty), Half Period Jitter

Applicable only to 667 and 800 MHz device only.

tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter over 200 consecutive cycles.

tCH jitter is the largest deviation of any single tCH from tCH(avg).

tCL jitter is the largest deviation of any single tCL from tCL(avg).

tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}

where,

tJIT(CH) = {tCHi - tCH(avg) where i=1 to 200}

tJIT(CL) = {tCLi - tCL(avg) where i=1 to 200}

tJIT(per), Clock Period Jitter

Applicable only to 667 and 800 MHz device only.

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). This test compares the average clock period (over 200 cycles) with each period inside the window. The smallest and largest values must be within limits.

tJIT(per) = Min/max of {tCKi - tCK(avg)} where i=1 to 200

Measured on both the rising and the falling edge.

There are different limit depending on whether the DLL is already locked or not:

- tJIT(per) defines the single period jitter when the DLL is already locked.
- tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

A configuration variable allows to define which limit to use.

tJIT(cc), Cycle to Cycle Period Jitter

Applicable only to 667 and 800 MHz device only.

tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles. This test compares the smallest and largest values of the difference between any two consecutive clock cycles inside a 200 cycles window.

tJIT(cc) = Min/max of {tCKi+1 – tCKi} where i = 1 to 199

Measured on both the rising and the falling edge.

There are different limit depending on whether the DLL is already locked or not:

- tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
- tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

A configuration variable allows to define which limit to use.

tERR(n per), Cumulative Error

Applicable only to 667 and 800 MHz device only.

tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg). This test compares the average clock period (over 200 cycles) with each n-bit period inside the window. The smallest and largest values must be within limits.

There are 6 different tests:
tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR (6-10per) and tERR (11-50per)

tERR(nper) = Min/max of {SUM(tCKi) - n x tCK(avg)}

where i=1 to n and:

n = 2 for tERR(2per)

n = 3 for tERR(3per)

n = 4 for tERR(4per)

n = 5 for tERR(5per)

$6 \leq n \leq 10$ for tERR(6-10per)

$11 \leq n \leq 50$ for tERR(11-50per)

Measured on both the rising and the falling edge.

Eye Diagram

Write Burst (Inputs)

This is an informational only test that creates the eye diagram of all of the write bursts found in the acquisition.

Read Burst (Outputs)

This is an informational only test that creates the eye diagram of all of the read bursts found in the acquisition.

Electrical Tests

Write Bursts (Inputs)

Slew (Input Slewrate)

This test applies to all input signals.

SlewR and SlewF

Apply to all input signals.

The input signal minimum slew rate is to be maintained over the range from VREF to VIH(ac) min for rising edges (SlewR) and the range from VREF to VIL(ac) max for falling edges (SlewF) of single-ended signal.

For differential signals (e.g. CK - CK#) slew rate for rising edges is measured from CK - CK# = - 250 mV to CK - CK# = + 500 mV (+ 250 mV to - 500 mV for falling edges).

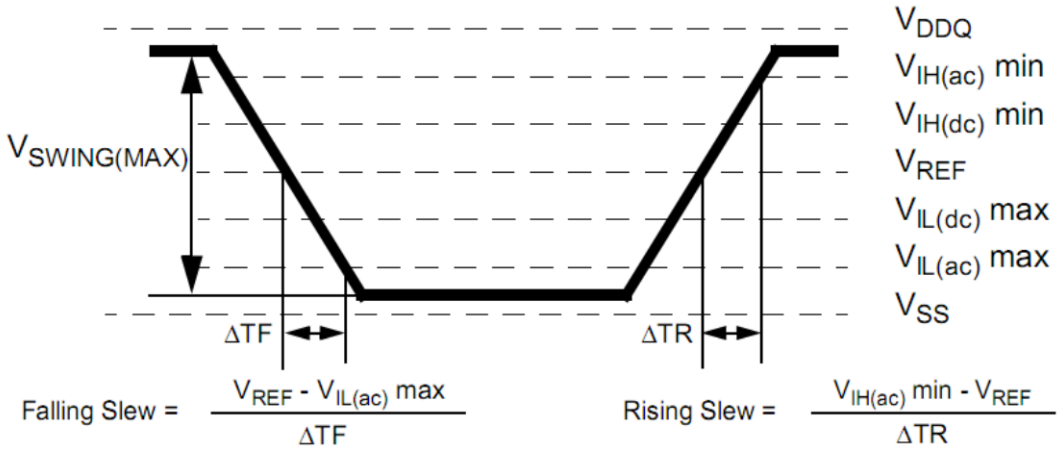


Figure 21. AC input test signal waveform [JESD79-2E figure 73]

Logic Levels

VIH(ac), maximum AC input logic high

Measure the local maximum value from VREF to VREF of the high pulse histogram. If multiple pulses are measured, take the lowest number and the highest number as the worst cases.

The lowest number must be greater than or equal to the minimum limit and the highest number must be less than or equal to the maximum limit.

VIH(dc), minimum DC input logic high

Measure the local minimum and maximum values from the first VIH(ac)min crossing point to the time corresponding to VIH(dc)min crossing a 1V/ns slewrate slope to VREF. If multiple pulses are measured, take the lowest, respectively the highest, number as the worst case.

The local minimum must be greater than or equal to the minimum limit. The local maximum must be less than or equal to the maximum limit.

VIL(ac), maximum AC input logic low

Measure the local minimum value from VREF to VREF of the low pulse histogram. If multiple pulses are measured, take the lowest number and the highest number as the worst cases.

The lowest number must be greater than or equal to the minimum limit and the highest number must be less than or equal to the maximum limit.

VIL(dc), minimum DC input logic low

Measure the local minimum and maximum values from the first VIL(ac)max crossing point to the time corresponding to VIL(dc)max crossing a 1V/ns slewrate slope to VREF. If multiple pulses are measured, take the lowest, respectively the highest, number as the worst case.

The local minimum must be greater than or equal to the minimum limit. The local maximum must be less than or equal to the maximum limit.

VSWING(MAX), input signal maximum peak to peak swing

Measure the peak to peak value of the signal in a given Write frame. .If multiple frames are measured, take, the highest number as the worst case.

The measure must be less than or equal to the limit.

AC Over/Undershoot

AC Overshoot, Maximum peak amplitude

Maximum peak amplitude allowed for overshoot area.

AC Overshoot, Maximum overshoot area above VDDQ

Prerequisite: AC Overshoot maximum peak amplitude, needed to compute area.

Maximum overshoot area above VDDQ.

AC Undershoot, Maximum peak amplitude

Maximum peak amplitude allowed for undershoot area.

AC Undershoot, Maximum overshoot area above VDDQ

Prerequisite: AC Undershoot maximum peak amplitude, needed to compute area.

Maximum undershoot area below VSSQ.

Note: The maximum requirements for peak amplitude were reduced from 0.9V to 0.5V. Register vendor data sheets specify the maximum over/undershoot induced in specific RDIMM applications. DRAM vendor data sheets also specify the maximum overshoot/undershoot that their DRAM can tolerate. This allows the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register induces in the specific RDIMM application. A variable allows this limit to be changed.

Tests Requiring Single Ended Probing of Differential Signal

VID(ac), AC Differential Input Voltage

VID(ac) specifies the input differential voltage | VTR - VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as CK, DQS, LDQS or UDQS). The minimum value is equal to VIH(ac) - VIL(ac). This test requires probing each half of a differential signal. This is only available in the configurations using 4 probes.

VIX(ac), AC Differential Input Cross Point Voltage

The typical value of VIX(ac) is expected to be about 0.5 x VDDQ of the transmitting device and VIX(ac) is expected to track variations in VDDQ. VIX(ac) indicates the voltage at which differential input signals must cross. This test requires probing each half of a differential signal. This is only available in the configurations using 4 probes.

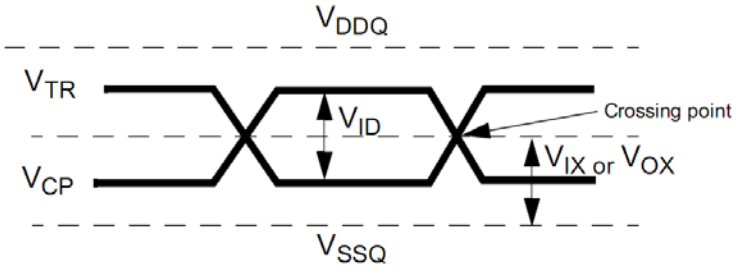


Figure 22. Differential signal levels [JESD79-2E figure 74]

Read Bursts (Outputs)

Sout (Output Slew Rate)

SoutR and SoutF

Apply to all output signals (DQn data signals), but only for 400, 533 and 667 MHz device, not for 800 MHz device.

The output slew rate is measured from VIL(ac) to VIH(ac) for the rising edge and from VIH(ac) to VIL(ac) for the falling edge. DRAM output slew rate specification applies to 400, 533 & 667 MHz speed devices.

PLEASE NOTE THE FOLLOWING:

- Absolute value of the slew rate as measured from (dc) to (dc) >= Slew rate as measured from (ac) to (ac).This is guaranteed by design and characterization.
- Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - DQS#) output slew rate is measured between DQS - DQS# = - 500 mV and DQS - DQS# = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

tSLMR

This is the ratio of the rising edge slewrate to the falling edge slewrate. This is a test recommended by Intel but not reported in the Jedec JESD79-2E standard. Therefore it is not selected in the standard configurations, but only in the All Tests configuration.

Tests Requiring Single Ended Probing of Differential Signal

VOX(ac) , AC Differential Output Cross Point Voltage

The typical value of VOX(ac) is expected to be about 0.5 x VDDQ of the transmitting device and VOX(ac) is expected to track variations in VDDQ . VOX(ac) indicates the voltage at which differential output signals must cross. This test requires probing each half of a differential signal. This is only available in the configurations using 4 probes.

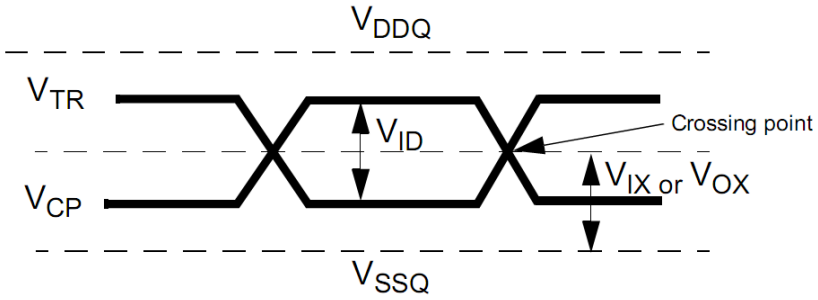


Figure 23. Differential signal levels [JESD79-2E figure 74]

Timing Tests

Read Bursts

tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals

Maximum skew between the DQS line and the associated DQ line within a read burst

Measure timing from DQS at VREF to DQ rising at VIH(ac)min and falling at VIL(ac)max.

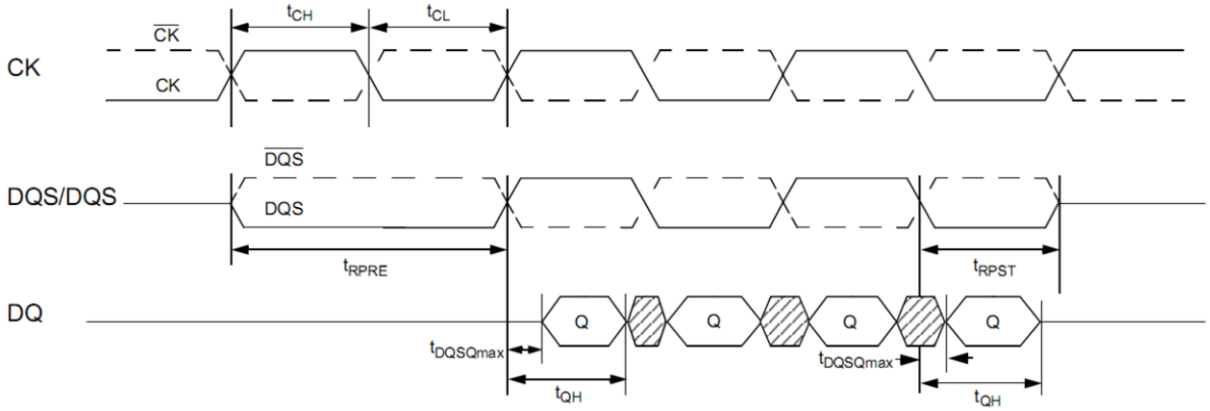


Figure 24. Data output (read) timing [JESD79-2E figure 32]

tHP, CK half pulse width

Prerequisite: needs result of tCL and tCH Clock Tests.

tHP refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). tHP is the minimum of the absolute half period of the actual input clock.

tHP is an input parameter but not an input specification parameter, hence no limits are applied, it is reported as informational only. It is used in conjunction with tQHS to derive the DRAM output timing tQH.

```
tHP = Min ( tCH(abs), tCL(abs) )
where,
tCH(abs) is the minimum of the actual instantaneous clock HIGH time;
tCL(abs) is the minimum of the actual instantaneous clock LOW time;
```

tQHS, DQ hold skew factor

This measures the sum of CK at VREF to DQS at VREF and DQ at VIH(dc) or VIL(dc) to DQS at VREF

tQH, DQ/DQS Output Hold Time From DQS

This measures the timing from DQS at VREF to DQ at VIH(dc) (rising edge) or VIL(dc) (falling edge).

Prerequisite: tHP to compute limit.

tDQSCK, DQS Output Access Time from CK/CK #

Time from CK at VREF level to DQS at VREF level.

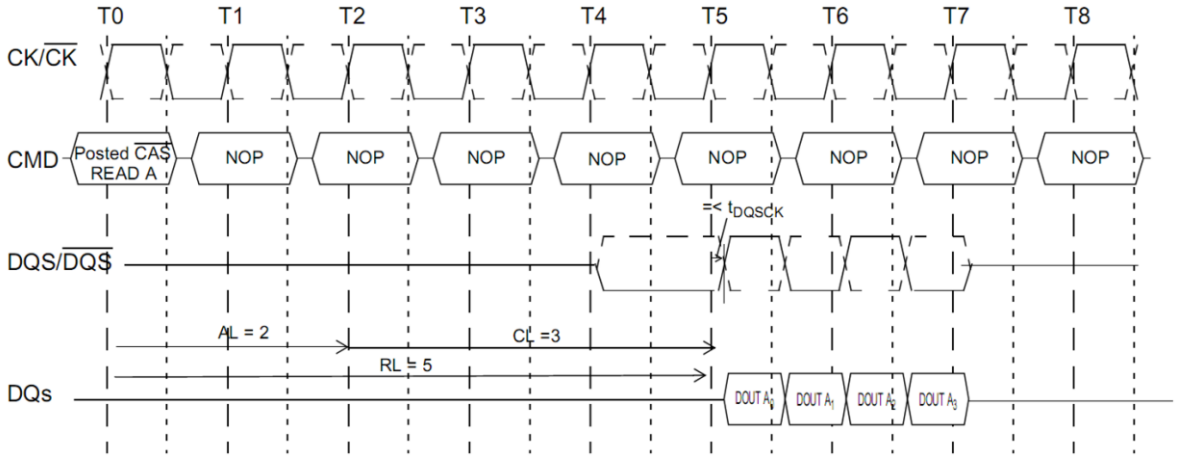


Figure 25. Burst read operation [JESD79-2E figure 33]

This is a measure similar to tDQSS but on the Read frame and on both edges (the result can be negative).

Prerequisite: tERR(6-10per), a derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only for both of the following tests.

tAC, DQ Output Access Time from CK/CK#

Time from CK at VREF level to DQ at VIH(ac) or VIL(ac) level.

Prerequisite: tERR(6-10per), a derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only for both of the following tests.

tHZ(DQ), DQ High Impedance Time From CK/CK#

This is the time from Vref of the CK/CK# signal to the point when the DQ is not being driven anymore (at the end of the burst)

tLZ(DQ), DQ Low-Impedance Time from CK/CK#

This is the time from when the DQ begins to be driven (at the beginning of the burst) to the nearest CK/CK# edge.

tLZ(DQS), DQS Low-Impedance Time from CK/CK#

This is the time from when the DQS begins to be driven (at the beginning of the preamble) to the nearest CK/CK# edge.

tRPRE, Read Preamble

Time from when DQS begins to be driven (at the beginning of the preamble) to when it crosses Vref. This is only measured on a read cycle.

Prerequisite: tJIT(per), a derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only.

tRPST, Read Postamble

Time from when DQS crosses Vref (at the beginning of the postamble) to when DQS stops being driven (at the end of the postamble). This is only measured on a read cycle.

Prerequisite: tJIT(duty), a derating factor is applied to the limit depending on the clock jitter. This is applicable to 667 and 800 MHz device only.

Write Bursts

tDQSS, DQS latching rising transitions to associated CK edge

CK rising edge at VREF level to DQS rising edge at VREF level, see Figure 26.

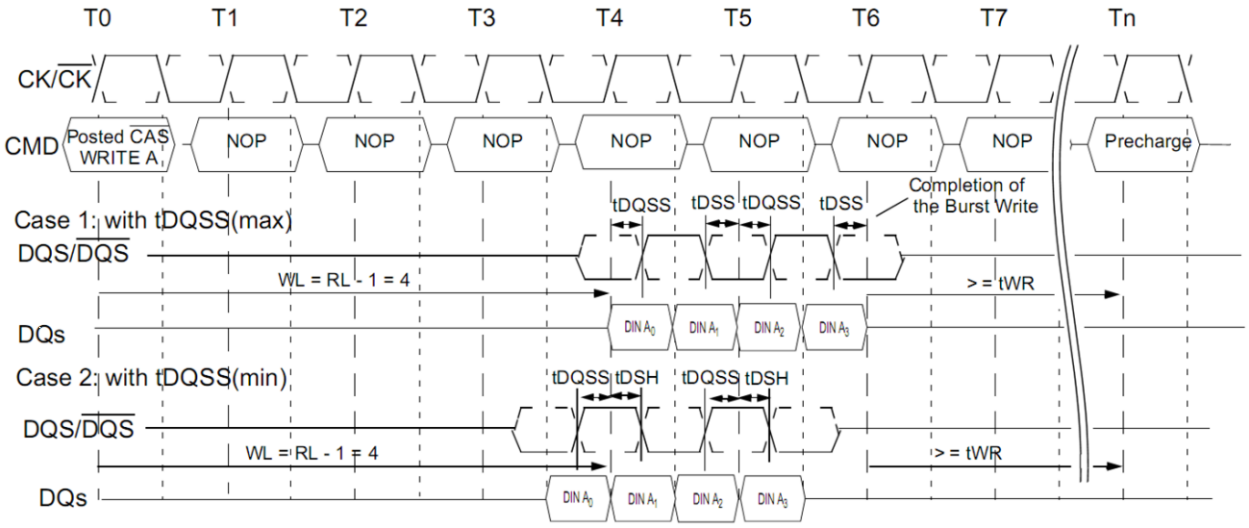


Figure 26. Burst write operation [JESD79-2E figure 39]

tDQSH, DQS Input High Pulse Width

DQS High pulse width at VREF level, see Figure 27.

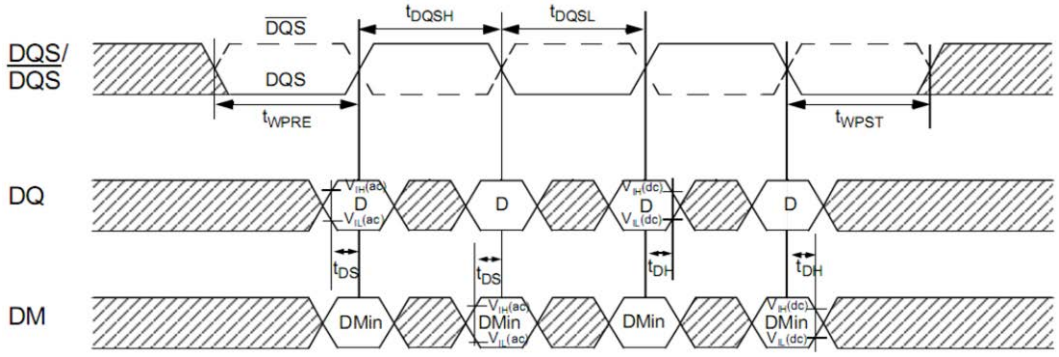


Figure 27. Data input (write) timing [JESD79-2E figure 38]

tDQSL, DQS Input Low Pulse Width

DQS Low pulse width at VREF level, see Figure 27.

tDSS, DQS Falling Edge to CK Setup Time

Time from DQS falling edge at VREF level to CK rising edge at VREF level, see Figure 27.

tDSH, DQS Falling Edge Hold Time from CK

Time from CK rising edge at VREF level to DQS falling edge at VREF level, see Figure 27.

tWPRE, Write Preamble

Time from when DQS begins to be driven (at the beginning of the preamble) to when it crosses Vref. This is only measured on a write cycle.

tWPST, Write Postamble

Time from when DQS crosses Vref (at the beginning of the postamble) to when DQS stops being driven (at the end of the postamble). This is only measured on a write cycle.

Prerequisite: SLEW of DQ and DQS, a derating factor is applied to the limit depending on the signals slewrate. This is applicable for the following four tests.

tDS(base), DQ and DM Input Setup Time

Input waveform timing tDS with differential data strobe enabled, is referenced from the input signal crossing at the VIH(ac)min level to the differential data strobe crosspoint at VREF for a rising signal, and from the input signal crossing at the VIL(ac)max level to the differential data strobe crosspoint at VREF for a falling signal applied to the device under test. See Figure 28 and Figure 29 as follows.

DQS and DQS# signals must be monotonic between VIL(dc)max and VIH(dc)min.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max.

JESD79-2E Specific Note 8 (page 85 to 94) with tables 43 and 44 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

tDH(base), DQ and DM Input Hold Time

Input waveform timing tDH with differential data strobe enabled, is referenced from the differential data strobe crosspoint at VREF to the input signal crossing at the VIH(dc)min level for a falling signal and from the differential data strobe crosspoint at VREF to the input signal crossing at the VIL(dc)max level for a rising signal applied to the device under test. See Figure 28 and Figure 29 as follows.

DQS and DQS# signals must be monotonic between VIL(dc)max and VIH(dc)min.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc).

JESD79-2E Specific Note 8 (page 85 to 94) with tables 43 and 44 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

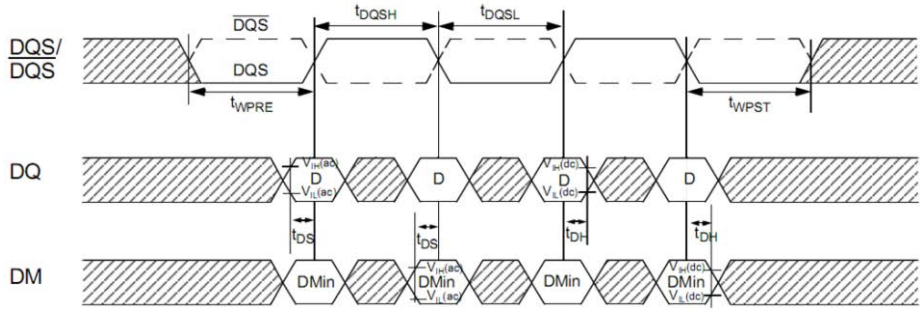


Figure 28. Data input (write) timing [JESD79-2E figure 38]

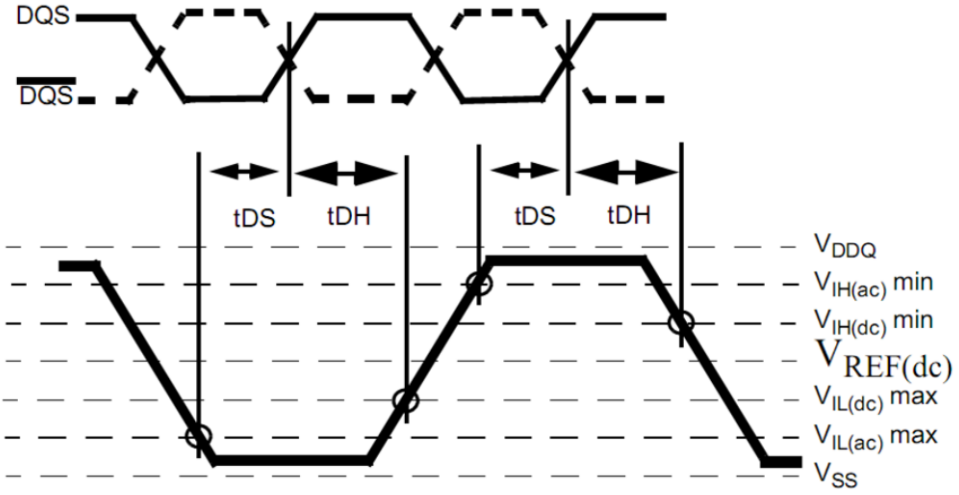


Figure 29. Differential input waveform timing - tDS and tDH [JESD79-2E figure 98]

tDS1(base), DQ and DM input setup time (single-ended strobe)

This test is only applicable only on 400 and 533 MHz devices.

Input waveform timing with single-ended data strobe enabled, is referenced from the input signal crossing at the VIH(ac)min level to the single-ended data strobe crossing VIH(dc)min or VIL(dc)max at the start of its transition for a rising signal, and from the input signal crossing at the VIL(ac)max level to the single-ended data strobe crossing VIH(dc)min or VIL(dc)max at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between VIL(dc)max and VIH(dc)min. See Figure 30 as follows.

Jedec JESD79-2E Specific Note 8 (page 85 to 94) with table 45 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

tDH1(base), DQ and DM input hold time (single-ended strobe)

This test is only applicable only on 400 and 533 MHz devices.

Input waveform timing with single-ended data strobe enabled, is referenced from the input signal crossing at the VIH(dc)min level to the single-ended data strobe crossing VIH(ac)min or VIL(ac)max at the end of its transition for a rising signal, and from the input signal crossing at the VIL(dc)max level to the single-ended data strobe crossing

VIH(ac)min or VIL(ac)max at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between VIL(dc)max and VIH(dc)min. See Figure 30 as follows.

Jedec JESD79-2E Specific Note 8 (page 85 to 94) with table 45 explains the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

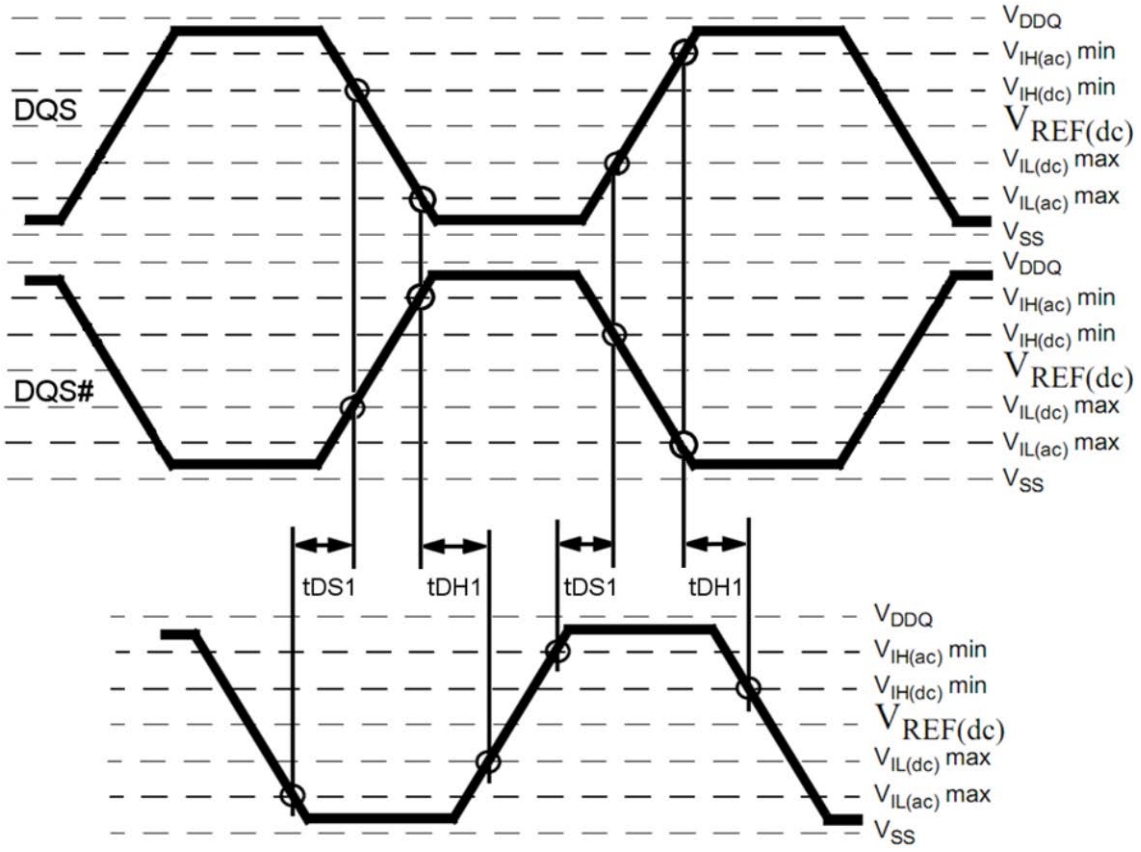


Figure 30. Single-ended input waveform timing - tDS1 and tDH1

The following tests require probing and address or control signal. These tests are only available in the configurations using 4 probes.

Prerequisite: SLEW of CK and Address or Control, a derating factor is applied to the limit depending on the signals slewrate. This is applicable for both of the following tests.

tIS(base) - Address and Control Input Setup Time

Input waveform timing is referenced from the input signal crossing at the VIH(ac)min level to the differential clock crosspoint at VREF for a rising signal, and from the input signal crossing at the VIL(ac)max level to the differential clock crosspoint at VREF for a falling signal applied to the device under test. See Figure 31 as follows.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max.

Jedec JESD79-2E Specific Note 9 (page 95 to 100) with tables 46 and 47 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

tIH(base) - Address and Control Input Hold Time

Input waveform timing is referenced from the input signal crossing at the VIL(dc)max level to the differential clock crosspoint at VREF for a rising signal, and from the input signal crossing at the VIH(dc)min level to the differential clock crosspoint at VREF for a falling signal applied to the device under test. See Figure 31 as follows.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc).

Jedec JESD79-2E Specific Note 9 (page 95 to 100) with tables 46 and 47 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

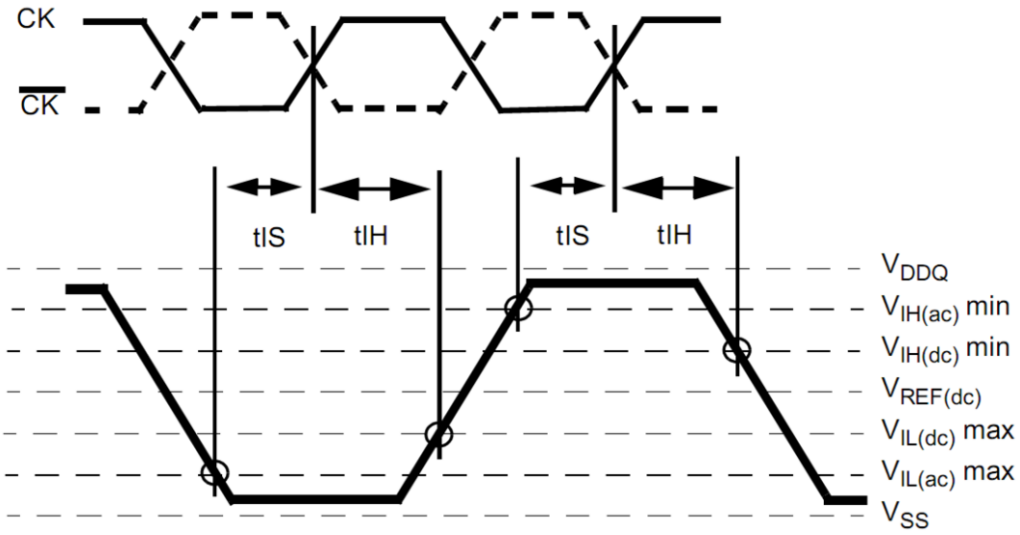


Figure 31. Differential input waveform timing - tIS and tIH [JESD79-2E figure 99]