19-3686; Rev 2; 4/06

EVALUATION KIT AVAILABLE

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

General Description

The MAX5773/MAX5774/MAX5775 32-channel, 14-bit, voltage-output, digital-to-analog converters (DACs) are ideal for applications requiring a high number of programmable voltages. The MAX5773/MAX5774/MAX5775 can be programmed to calibrate the 14-bit input data word for gain and offset errors before updating the DAC output.

An SPI™-/QSPI™-/MICROWIRE™- or DSP-compatible serial interface controls the MAX5773/MAX5774/MAX5775. Each DAC channel has its own input, gain, and offset register. These three registers pass data through one of the two multiplier accumulator units (MACs), resulting in a voltage output corrected for gain and offset error. Each DAC channel has a double-buffered input structure to minimize the digital-noise feedthrough from the digital inputs to the outputs, and allows for synchronous or asynchronous updating of the outputs. The DAC outputs update independently or simultaneously with a single software or hardware command. The MAX5773/MAX5774/MAX5775 also provide a digital output (DOUT) that allows for readback or daisy chaining of multiple devices.

All DAC outputs are buffered and drive 10kΩ in parallel with 100pF. The MAX5773 has a 0 to +10V output range; the MAX5774 has a -2.5V to +7.5V output range; and the MAX5775 has a -5V to +5V output range.

The MAX5773/MAX5774/MAX5775 are available in a 68-pin, 10mm x 10mm, TQFN package and a 64-pin, 12mm x 12mm, TQFP package. The MAX5773/MAX5774/MAX5775 are specified over the 0°C to +85°C temperature range. Refer to the MAX5753/MAX5754/MAX5755 data sheet for similar 14-bit, 32-channel DACs without offset and gain calibration.

Applications

Automatic Test Systems

Optical Router Controls

Industrial Process Controls

Arbitrary Function Generators

Avionics Equipment

Minimum Component Count Analog Systems

Digital Offset/Gain Adjustment

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **Offset and Gain Correction for Each DAC Channel**
- **Guaranteed Monotonic to 14 Bits**
- **32 Individual DACs in a 10mm x 10mm, 68-Pin TQFN Package or 12mm x 12mm, 64-Pin TQFP Package**
- **Output Voltage Ranges**
  0 to +10V (MAX5773)
  -2.5V to +7.5V (MAX5774)
  -5V to +5V (MAX5775)
- **Buffered Voltage Outputs Drive 10kΩ II 100pF**
- **Glitch-Free Power-Up**
- **SPI/QSPI/MICROWIRE- and DSP-Compatible 33MHz Serial Interface**

Ordering Information

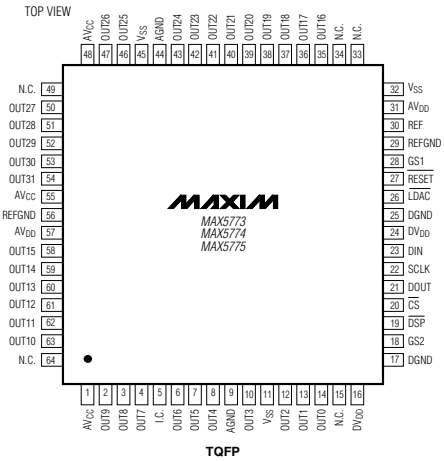
PART	PIN-PACKAGE	OUTPUT VOLTAGE RANGE (V)	PKG CODE
MAX5773UTK*	68 TQFN-EP**	0 to +10	T6800-3
MAX5773UCB*	64 TQFP	0 to +10	C64-12
MAX5774UTK*	68 TQFN-EP**	-2.5 to +7.5	T6800-3
MAX5774UCB	64 TQFP	-2.5 to +7.5	C64-12
MAX5775UTK*	68 TQFN-EP**	-5 to +5	T6800-3
MAX5775UCB*	64 TQFP	-5 to +5	C64-12

Note: *All devices are specified over the 0°C to +85°C temperature range.*

**Future product—contact factory for availability.*

***EP = Exposed paddle.*

Pin Configurations



Pin Configurations continued at end of data sheet.

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

AV_{CC} to V_{SS}, AGND, DGND, REFGND .....-0.3V to +12V
V_{SS} to AGND, DGND.....-6V to +0.3V
AV_{DD} to AGND, DGND, REFGND .....-0.3V to +6V
DV_{DD} to AGND, DGND, REFGND .....-0.3V to AV_{DD}
AGND to DGND.....-0.3V to +0.3V
REF to AGND,
DGND, REFGND ....-0.3V to the lower of (AV_{DD} + 0.3V) and +6V
REFGND to AGND.....-0.3V to +0.3V
Digital Inputs to AGND, DGND,
REFGND .....-0.3V to the lower of (DV_{DD} + 0.3V) and +6V
DOUT to DGND .....-0.3V to the lower of (DV_{DD} + 0.3V) and +6V
OUT_ to V_{SS}.....-0.3V to the lower of (AV_{CC} +0.3V) and +12V
GS1, GS2 to AGND .....-1V to +1V
GS1, GS2 to V_{SS}.....-0.3V to +6V
Maximum Current into REF.....±10mA
Maximum Current into Any Other Pin .....±50mA
Maximum Power Dissipation (T_A = +70°C)
68-Pin TQFN (derate 50.0mW/°C above +70°C) 4.0W
64-Pin TQFP (derate 25.0mW/°C above +70°C).....2.0W
Operating Temperature Range .....0°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5773 (0 to +10V Output Voltage Range)

(AV_{CC} = +10.5V to +11V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = AGND = DGND = REFGND = GS1 = GS2 = 0, V_{REF} = +3.0V, R_L = ∞, C_L = 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		14			Bits
Integral Nonlinearity	INL	(Note 2)		±1	±4	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Offset Error (Without Digital Calibration)	V_{OS}	V_{SS} = -0.5V, AV_{CC} = +10V (Note 3)		±8	±40	mV
Offset Error (with Digital Calibration)	V_{OS-CAL}	V_{SS} = -0.5V, AV_{CC} = +10V		±300		µV
Gain Error (Without Digital Calibration)		(Note 3)		±0.1	±0.5	%FSR
Gain Error (with Digital Calibration)				±0.05		%FSR
Gain Temperature Coefficient				20		ppm FSR/°C
DC Crosstalk		V_{SS} = -0.5V, AV_{CC} = +10V (Note 4)		50	250	µV
DYNAMIC CHARACTERISTICS (f_{SCLK} = 20MHz)						
Output-Voltage Settling Time	t_S	Full-scale change to ±0.5 LSB		20		µs
Voltage-Output Slew Rate				1		V/µs
Digital Feedthrough		(Note 5)		5		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		120		nV-s
DAC-to-DAC Crosstalk		(Note 6)		25		nV-s
Output-Noise Spectral Density at 1kHz		Full-scale code		250		$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS—MAX5773 (0 to +10V Output Voltage Range)(continued)

(AV_{CC} = +10.5V to +11V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = AGND = DGND = REFGND = GS1 = GS2 = 0, V_{REF} = +3.0V, R_L = ∞, C_L = 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG OUTPUTS (OUT0 to OUT31)						
Output-Voltage Range		V_{SS} = -0.5V, AV_{CC} = +10.5V (Note 1)	0		10	V
Resistive Load to Ground			10	50		kΩ
Capacitive Load to Ground					100	pF
DC-Output Impedance				0.1		Ω
Short-Circuit Current		Sourcing, full scale, output connected to AGND		+5		mA
		Sinking, zero scale, output connected to AV_{CC}		-5		
GROUND-SENSE ANALOG INPUTS (GS1 and GS2)						
Input-Voltage Range	V_{GS}	Relative to AGND	-0.5		+0.5	V
Ground-Sense Gain	A_{GS}		0.995	1.000	1.005	V/V
Input Resistance		-0.5V ≤ V_{GS} ≤ +0.5V, V_{SS} = -0.5V	70			kΩ
REFERENCE INPUT (REF)						
Input Resistance			1			MΩ
Reference Input Voltage Range	V_{REF}	Referred to REFGND	2.900	3.000	3.100	V
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{LDAC}$, RESET, $\overline{DSP}$)						
Input-Voltage High	V_{IH}	+2.7V ≤ DV_{DD} ≤ + 3.6V	0.7 x DV_{DD}			V
		+3.6V < DV_{DD} ≤ +5.25V	2.4			
Input-Voltage Low	V_{IL}				0.8	V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	Digital inputs = 0 or DV_{DD}			±1	µA
DIGITAL OUTPUT (DOUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 1mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 0.2mA	0.8 x DV_{DD}			V
Tri-State Leakage Current	I_L				±10	µA
Tri-State Output Capacitance	C_{OUT}			10		pF
POWER REQUIREMENTS (AV_{CC}, V_{SS}, AGND, AV_{DD}, DV_{DD}, DGND)						
Output-Amplifier Positive Supply Voltage	AV_{CC}		10		11	V
Output-Amplifier Negative Supply Voltage	V_{SS}		-0.5		0	V
Output-Amplifier Supply Voltage Difference		AV_{CC} - V_{SS}			11	V
Analog Supply Voltage	AV_{DD}		4.75		5.25	V
Digital Supply Voltage	DV_{DD}		2.7		AV_{DD}	V

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX5773 (0 to +10V Output Voltage Range)(continued)

(AV_{CC} = +10.5V to +11V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = AGND = DGND = REFGND = GS1 = GS2 = 0, V_{REF} = +3.0V, R_L = ∞, C_L = 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Supply Current	AI_{DD}	V_{OUT0} through V_{OUT31} = 0			10	15	mA
		Software shutdown			10		µA
Digital Supply Current	DI_{DD}	DV_{DD} = +5V, V_{IH} = DV_{DD}, V_{IL} = 0, f_{SCLK} = 20MHz, continuous writethrough			2.5	3.5	mA
		DV_{DD} = +5V, V_{IH} = +2.4V, V_{IL} = +0.8V, f_{SCLK} = 20MHz, continuous writethrough			5.0	6.5	
		Software shutdown			75		nA
Output-Amplifier Positive Supply Current	AI_{CC}	V_{OUT0} through V_{OUT31} = 0			4	10	mA
		Software shutdown			20		µA
Output-Amplifier Negative Supply Current	I_{SS}	V_{SS} = -0.5V	V_{OUT0} through V_{OUT31} = 0		-4	-10	mA
			Software shutdown		-20		µA
Power-Supply Rejection Ratio	PSRR				-95		dB

ELECTRICAL CHARACTERISTICS—MAX5774 (-2.5V to +7.5V Output Voltage Range)

(AV_{CC} = +7.75V to +8.25V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = -2.75V to -3.25V, AGND = DGND = REFGND = GS1 = GS2 = 0, program the offset DAC to 1000h. V_{REF} = +3.0V, R_L = ∞, C_L= 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		14			Bits
Integral Nonlinearity	INL	(Note 2)		±1	±4	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Offset Error (Without Digital Calibration)	V_{OS}	V_{SS} = -3.25V, AV_{CC} = +7.75V (Note 3)		±8	±40	mV
Offset Error (with Digital Calibration)	V_{OS-CAL}	V_{SS} = -3.25V, AV_{CC} = +7.75V		±300		µV
Gain Error (Without Digital Calibration)		(Note 3)		±0.1	±0.5	%FSR
Gain Error (with Digital Calibration)				±0.05		%FSR
Gain Temperature Coefficient				20		ppm FSR/°C
DC Crosstalk		V_{SS} = -3.25V, AV_{CC} = +7.75V (Note 4)		50	250	µV
DYNAMIC CHARACTERISTICS (f_{SCLK} = 20MHz)						
Output-Voltage Settling Time	t_S	Full-scale change to ±0.5 LSB		20		µs
Voltage-Output Slew Rate				1		V/µs
Digital Feedthrough		(Note 5)		5		nV-s

ELECTRICAL CHARACTERISTICS—MAX5774 (-2.5V to +7.5V Output Voltage Range) (continued)

(AV_{CC} = +7.75V to +8.25V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = -2.75V to -3.25V, AGND = DGND = REFGND = GS1 = GS2 = 0, program the offset DAC to 1000h. V_{REF} = +3.0V, R_L = ∞, C_L= 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital-to-Analog Glitch Impulse		Major carry transition		120		nV-s
DAC-to-DAC Crosstalk		(Note 6)		25		nV-s
Output-Noise Spectral Density at 1kHz		Full-scale code		250		nV/√Hz
ANALOG OUTPUTS (OUT0 to OUT31)						
Output Voltage Range		V_{SS} = -2.75V, AV_{CC} = +7.75V (Note 1)	-2.5		+7.5	V
Resistive Load to Ground			10	50		kΩ
Capacitive Load to Ground					100	pF
DC Output Impedance				0.1		Ω
Short-Circuit Current		Sourcing, full scale, output connected to AGND		+5		mA
		Sinking, zero scale, output connected to AV_{CC}		-5		
GROUND-SENSE ANALOG INPUTS (GS1 and GS2)						
Input-Voltage Range	V_{GS}	Relative to AGND	-0.5		+0.5	V
Ground-Sense Gain	A_{GS}		0.993	1.000	1.005	V/V
Input Resistance		-0.5V ≤ V_{GS} ≤ +0.5V, V_{SS} = -2.75V	70			kΩ
REFERENCE INPUT (REF)						
Input Resistance			1			MΩ
Reference Input Voltage Range	V_{REF}	Referred to REFGND	2.900	3.000	3.100	V
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{LDAC}$, $\overline{RESET}$, DSP)						
Input-Voltage High	V_{IH}	+2.7V ≤ DV_{DD} ≤ +3.6V	0.7 x DV_{DD}			V
		+3.6V < DV_{DD} ≤ +5.25V	2.4			
Input-Voltage Low	V_{IL}				0.8	V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	Digital inputs = 0 or DV_{DD}			±1	µA
DIGITAL OUTPUT (DOUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 1mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 0.2mA	0.8 x DV_{DD}			V
Tri-State Leakage Current	I_L				±10	µA
Tri-State Output Capacitance	C_{OUT}			10		pF
POWER REQUIREMENTS (AV_{CC}, V_{SS}, AGND, AV_{DD}, DV_{DD}, DGND)						
Output-Amplifier Positive Supply Voltage	AV_{CC}		7.50		8.25	V

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX5774 (-2.5V to +7.5V Output Voltage Range) (continued)

(AV_{CC} = +7.75V to +8.25V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = -2.75V to -3.25V, AGND = DGND = REFGND = GS1 = GS2 = 0, program the offset DAC to 1000h. V_{REF} = +3.0V, R_L = ∞, C_L= 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Amplifier Negative Supply Voltage	V_{SS}		-3.25		-2.50	V
Output-Amplifier Supply Voltage Difference		AV_{CC} - V_{SS}			11	V
Analog Supply Voltage	AV_{DD}		4.75		5.25	V
Digital Supply Voltage	DV_{DD}		2.7		AV_{DD}	V
Analog Supply Current	AI_{DD}	V_{OUT0} through V_{OUT31} = 0		10	15	mA
		Software shutdown		10		µA
Digital Supply Current	DI_{DD}	DV_{DD} = +5V,V_{IH} = DV_{DD}, V_{IL} = 0, f_{SCLK} = 20MHz, continuous writethrough		2.0	3.0	mA
		DV_{DD} = +5V,V_{IH} = +2.4V, V_{IL} = +0.8V, f_{SCLK} = 20MHz, continuous writethrough		4.5	6.0	
		Software shutdown		75		nA
Output-Amplifier Positive Supply Current	AI_{CC}	V_{OUT0} through V_{OUT31} = 0		4	8	mA
		Software shutdown		20		µA
Output-Amplifier Negative Supply Current	I_{SS}	V_{SS} = -2.75V; V_{OUT0} through V_{OUT31} = 0		-4	-10	mA
		V_{SS} = -2.75V; Software shutdown		-20		µA
Power-Supply Rejection Ratio	PSRR			-95		dB

ELECTRICAL CHARACTERISTICS—MAX5775 (-5V to +5V Output Voltage Range)

(AV_{CC} = +5.25V to +5.5V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = -5.25V to -5.5V, AGND = DGND = REFGND = GS1 = GS2 = 0, program the offset DAC to 2000h. V_{REF} = +3.0V, R_L = ∞, C_L = 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		14			Bits
Integral Nonlinearity	INL	(Note 2)		±1	±4	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Offset Error (Without Digital Calibration)	V_{OS}	V_{SS} = -5.25V, AV_{CC} = +5.25V (Note 3)		±8	±40	mV
Offset Error (with Digital Calibration)	V_{OS-CAL}	V_{SS} = -5.25V, AV_{CC} = +5.25V		±300		µV
Gain Error (Without Digital Calibration)		(Note 3)		±0.1	±0.5	%FSR
Gain Error (with Digital Calibration)				±0.05		%FSR
Gain Temperature Coefficient				20		ppm FSR/°C

ELECTRICAL CHARACTERISTICS—MAX5775 (-5V to +5V Output Voltage Range) (continued)

(AV_{CC} = +5.25V to +5.5V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = -5.25V to -5.5V, AGND = DGND = REFGND = GS1 = GS2 = 0, program the offset DAC to 2000h. V_{REF} = +3.0V, R_L = ∞, C_L = 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Crosstalk		V_{SS} = -5.50V, AV_{CC} = +5.25V (Note 4)		50	250	µV
DYNAMIC CHARACTERISTICS (f_{SCLK} = 20MHz)						
Output-Voltage Settling Time	t_S	Full-scale change to ±0.5 LSB		20		µs
Voltage-Output Slew Rate				1		V/µs
Digital Feedthrough		(Note 5)		5		nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		120		nV-s
DAC-to-DAC Crosstalk		(Note 6)		25		nV-s
Output-Noise Spectral Density at 1kHz		Full-scale code		250		nV/√Hz
ANALOG OUTPUTS (OUT0 to OUT31)						
Output-Voltage Range		V_{SS} = -5.25V, AV_{CC} = +5.25V (Note 1)	-5		+5	V
Resistive Load to Ground			10	50		kΩ
Capacitive Load to Ground					100	pF
DC Output Impedance				0.1		Ω
Short-Circuit Current		Sourcing, full scale, output connected to AGND		+5		mA
		Sinking, zero scale, output connected to AV_{CC}		-5		
GROUND-SENSE ANALOG INPUTS (GS1 and GS2)						
Input-Voltage Range	V_{GS}	Relative to AGND	-0.5		+0.5	V
Ground-Sense Gain	A_{GS}		0.995	1.000	1.005	V/V
Input Resistance		-0.5V ≤ V_{GS} ≤ +0.5V, V_{SS} = -5.25V	70			kΩ
REFERENCE INPUT (REF)						
Input Resistance			1			MΩ
Reference Input Voltage Range	V_{REF}	Referred to REFGND	2.900	3.000	3.100	V
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{LDAC}$, $\overline{RESET}$, $\overline{DSP}$)						
Input-Voltage High	V_{IH}	+2.7V ≤ DV_{DD} ≤ +3.6V	0.7 x DV_{DD}			V
		+3.6V < DV_{DD} ≤ 5.25V	2.4			
Input-Voltage Low	V_{IL}				0.8	V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	Digital inputs = 0 or DV_{DD}			±1	µA
DIGITAL OUTPUT (DOUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 1mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 0.2mA	0.8 x DV_{DD}			V

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX5775 (-5V to +5V Output Voltage Range) (continued)

(AV_{CC} = +5.25V to +5.5V (Note 1), AV_{DD} = +5V ±5%, DV_{DD} = +2.7V to AV_{DD}, V_{SS} = -5.25V to -5.5V, AGND = DGND = REFGND = GS1 = GS2 = 0, program the offset DAC to 2000h. V_{REF} = +3.0V, R_L = ∞, C_L = 50pF referenced to V_{SS}, T_A = T_{MIN} to T_{MAX}, SCLK = 0, all offset and gain registers = 0000h, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Tri-State Leakage Current	I_L					±10	µA
Tri-state Output Capacitance	C_{OUT}				10		pF
POWER REQUIREMENTS (AV_{CC}, V_{SS}, AGND, AV_{DD}, DV_{DD}, DGND)							
Output-Amplifier Positive Supply Voltage	AV_{CC}			4.75		5.50	V
Output-Amplifier Negative Supply Voltage	V_{SS}			-5.50		-4.75	V
Output-Amplifier Supply Voltage Difference		AV_{CC} - V_{SS}				11	V
Analog Supply Voltage	AV_{DD}			4.75		5.25	.V
Digital Supply Voltage	DV_{DD}			2.7		AV_{DD}	V
Analog Supply Current	AI_{DD}	V_{OUT0} through V_{OUT31} = 0			10	15	mA
		Software shutdown			10		µA
Digital Supply Current	DI_{DD}	DV_{DD} = +5V, V_{IH} = DV_{DD}, V_{IL} = 0, f_{SCLK} = 20MHz, continuous writethrough			2.5	3.5	mA
		DV_{DD} = +5V, V_{IH} = +2.4V, V_{IL} = +0.8V, f_{SCLK} = 20MHz, continuous writethrough			5.0	6.5	
		Software shutdown			75		nA
Output-Amplifier Positive Supply Current	AI_{CC}	V_{OUT0} through V_{OUT31} = 0			4	10	mA
		Software shutdown			20		µA
Output-Amplifier Negative Supply Current	I_{SS}	V_{SS} = -5.25V	V_{OUT0} through V_{OUT31} = 0		-4	-10	mA
			Software shutdown		-20		µA
Power-Supply Rejection Ratio	PSRR				-95		dB

TIMING CHARACTERISTICS

(Figures 1 and 2, AV_{DD} = +4.75V to +5.25V, **DV_{DD} = +4.75V to +5.25V**, AGND = DGND = REFGND = GS1 = GS2 = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCLK}		0		33	MHz
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}		10			ns
SCLK Fall to $\overline{CS}$ Fall Setup Time	t_{SCS}		6			ns

TIMING CHARACTERISTICS (continued)

(Figures 1 and 2, AV_{DD} = +4.75V to +5.25V, **DV_{DD} = +4.75V to +5.25V**, AGND = DGND = REFGND = GS1 = GS2 = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSS}		5			ns
$\overline{CS}$ Rise to SCLK Fall	t_{CS1}	At end of cycle in SPI mode only	15			ns
SCLK Fall to $\overline{CS}$ Rise Setup Time	t_{CS2}		0			ns
DIN to SCLK Fall Setup Time	t_{DS}		10			ns
DIN to SCLK Fall Hold Time	t_{DH}		2			ns
SCLK Fall to DOUT Fall	t_{SCL}	Load capacitance = 20pF			20	ns
SCLK Fall to DOUT Rise	t_{SDH}	Load capacitance = 20pF			20	ns
$\overline{CS}$ Pulse-Width High	t_{CSPWH}		50			ns
$\overline{CS}$ Pulse-Width Low	t_{CSPWL}	(Note 7)	20			ns
$\overline{LDAC}$ Pulse-Width Low	$t_{\overline{LDAC}}$		20			ns
$\overline{RESET}$ Pulse-Width Low	$t_{\overline{CLR}}$		50			ns

TIMING CHARACTERISTICS

(Figures 1 and 2, AV_{DD} = +4.75V to +5.25V, **DV_{DD} = +2.7V to +5.25V**, AGND = DGND = REFGND = GS1 = GS2 = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCLK}		0		25	MHz
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}		10			ns
SCLK Fall to $\overline{CS}$ Fall Setup Time	t_{SCS}		10			ns
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSS}		10			ns
$\overline{CS}$ Rise to SCLK Fall	t_{CS1}	At end of cycle in SPI mode only	18			ns
SCLK Fall to $\overline{CS}$ Rise Setup Time	t_{CS2}		0			ns
DIN to SCLK Fall Setup Time	t_{DS}		10			ns
DIN to SCLK Fall Hold Time	t_{DH}		2			ns
SCLK Fall to DOUT Fall	t_{SCL}	Load capacitance = 20pF			25	ns
SCLK Fall to DOUT Rise	t_{SDH}	Load capacitance = 20pF			25	ns
$\overline{CS}$ Pulse-Width High	t_{CSPWH}		50			ns
$\overline{CS}$ Pulse-Width Low	t_{CSPWL}	(Note 7)	20			ns
$\overline{LDAC}$ Pulse-Width Low	$t_{\overline{LDAC}}$		20			ns
$\overline{RESET}$ Pulse-Width Low	$t_{\overline{CLR}}$		50			ns

Note 1: AV_{CC} should be at least 0.25V higher than the maximum output voltage required from the DAC.

Note 2: Linearity guaranteed for full code range.

Note 3: Offset error is measured at code 0. Gain error is measured at code 3FFFh.

Note 4: DC crosstalk is the change in the output level of one DAC at midscale in response to the full-scale output change of all other DACs.

Note 5: Digital feedthrough is a measure of the impulse injected into the analog outputs from the digital control inputs when the device is not being written to. It is measured with a worst-case change on the digital inputs.

Note 6: DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog output change at another converter.

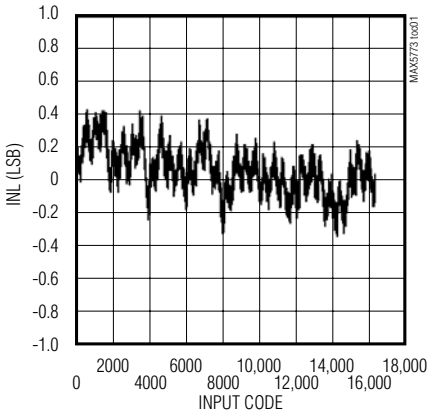
Note 7: In DSP mode, maintain the maximum $\overline{CS}$ pulse width low to ≤ 16 SCLK cycles.

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

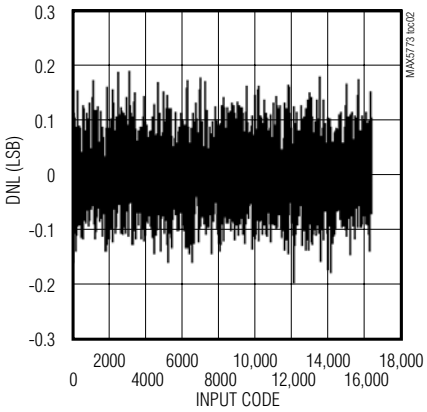
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

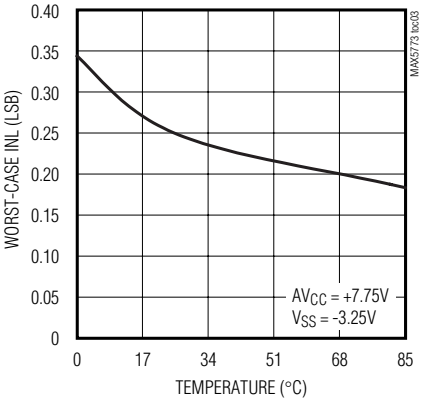
INTEGRAL NONLINEARITY vs. INPUT CODE



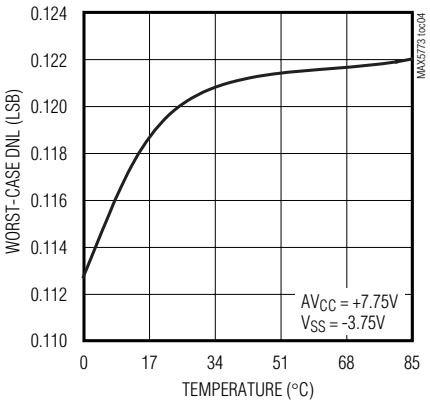
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



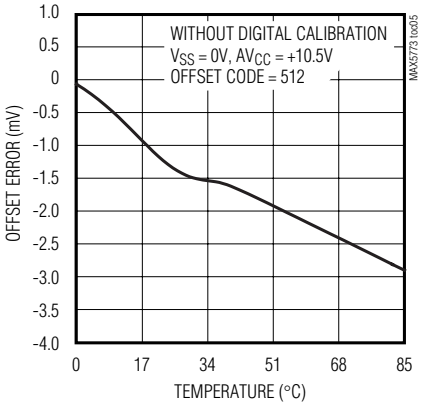
WORST-CASE INL vs. TEMPERATURE



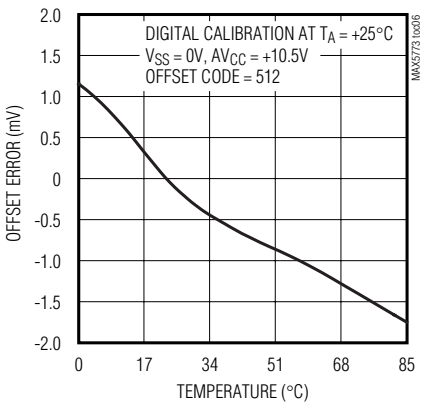
WORST-CASE DNL vs. TEMPERATURE



OFFSET ERROR vs. TEMPERATURE



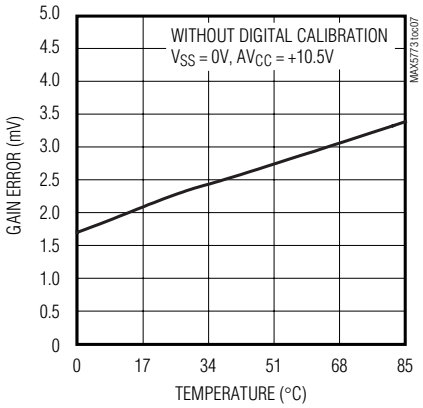
OFFSET ERROR vs. TEMPERATURE



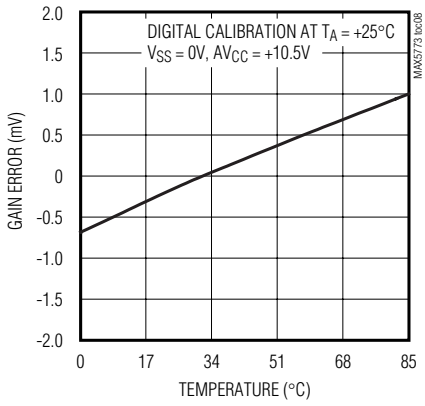
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

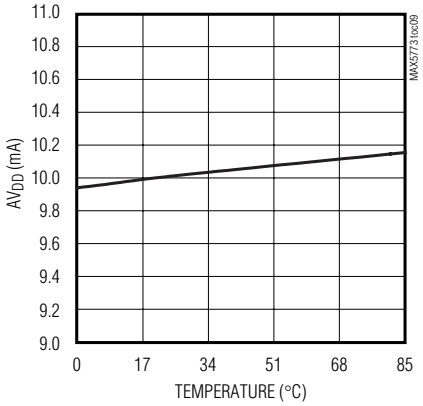
GAIN ERROR vs. TEMPERATURE



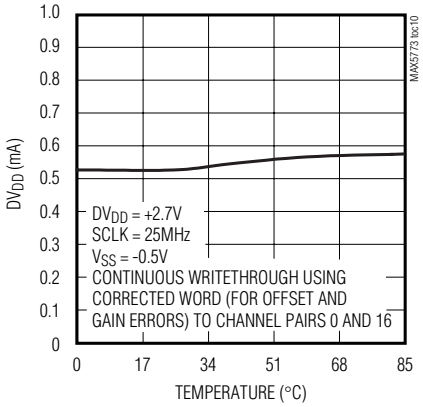
GAIN ERROR vs. TEMPERATURE



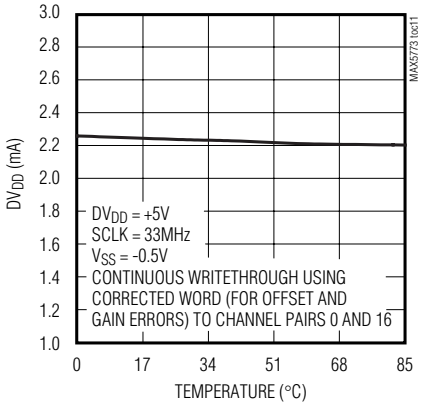
ANALOG SUPPLY CURRENT vs. TEMPERATURE



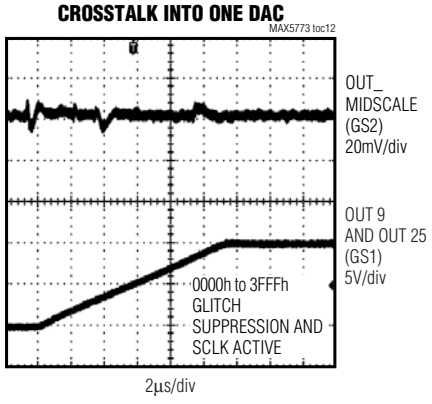
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



DIGITAL SUPPLY CURRENT vs. TEMPERATURE



CHANNEL-TO-CHANNEL CROSSTALK FOR A DAC PAIR SWITCHING AND RESULTING CROSSTALK INTO ONE DAC

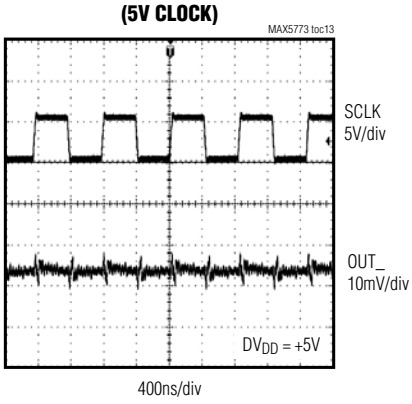


32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

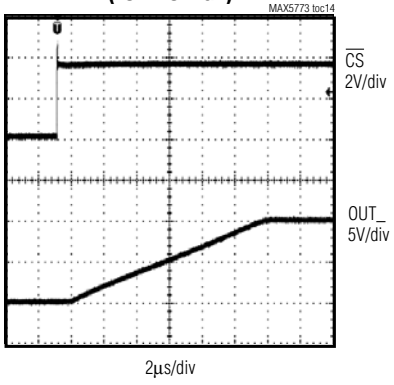
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

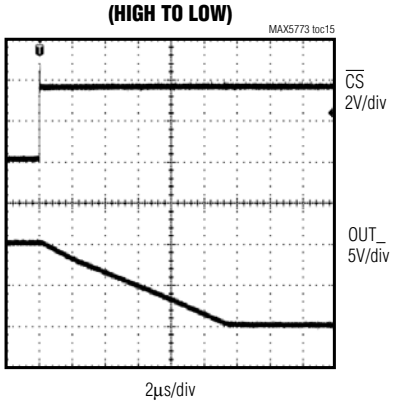
DIGITAL FEEDTHROUGH (5V CLOCK)



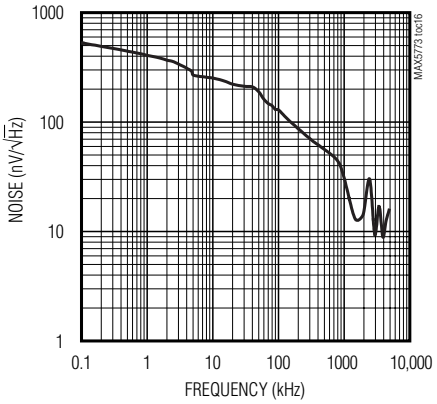
LARGE-SIGNAL STEP RESPONSE (LOW TO HIGH)



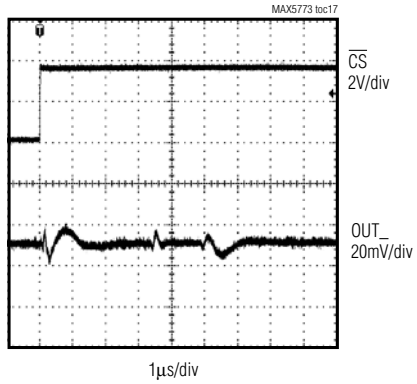
LARGE-SIGNAL STEP RESPONSE (HIGH TO LOW)



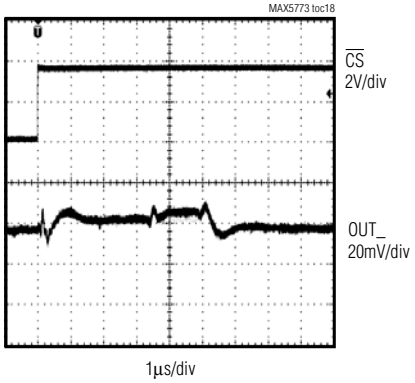
NOISE VOLTAGE DENSITY



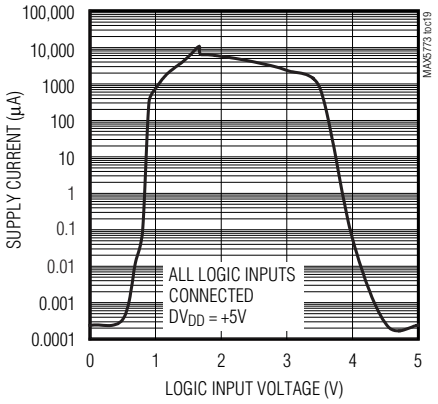
MAJOR CARRY TRANSITION 1FFFh TO 2000h WITH GLITCH SUPPRESSION



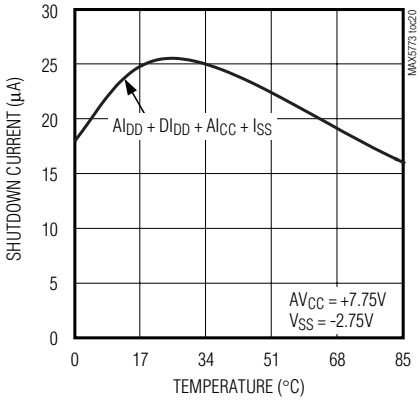
MAJOR CARRY TRANSITION 2000h TO 1FFFh WITH GLITCH SUPPRESSION



DV_{DD} SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



TOTAL SUPPLY SHUTDOWN CURRENT vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
68 TQFN	64 TQFP		
1, 16, 34, 35, 36, 51, 52, 53, 68	15, 33, 34, 49, 64	N.C.	No Connection. Not internally connected.
2, 50, 59	1, 48, 55	AV_{CC}	Output-Amplifier Positive Supply Input. Bypass to AGND with a 0.1µF capacitor.
3	2	OUT9	DAC9 Buffered Analog Output Voltage
4	3	OUT8	DAC8 Buffered Analog Output Voltage
5	4	OUT7	DAC7 Buffered Analog Output Voltage
6	5	I.C.	Internally Connected. Do not make any connections to I.C.
7	6	OUT6	DAC6 Buffered Analog Output Voltage
8	7	OUT5	DAC5 Buffered Analog Output Voltage
9	8	OUT4	DAC4 Buffered Analog Output Voltage
10, 46	9, 44	AGND	Analog Ground
11	10	OUT3	DAC3 Buffered Analog Output Voltage
12, 33, 47	11, 32, 45	V_{SS}	Bypass to AGND with a 0.1µF capacitor
13	12	OUT2	DAC2 Buffered Analog Output Voltage
14	13	OUT1	DAC1 Buffered Analog Output Voltage
15	14	OUT0	DAC0 Buffered Analog Output Voltage
17, 25	16, 24	DV_{DD}	Digital Power-Supply Input. Bypass to DGND with a 0.1µF capacitor.
18, 26	17, 25	DGND	Digital Ground
19	18	GS2	Ground-Sense Analog Input 2. Offsets the DAC amplifier outputs OUT0, OUT1, OUT2, OUT16, OUT17, and OUT18 by ±0.5V to compensate for a remote system ground potential difference.
20	19	$\overline{DSP}$	Digital Serial-Interface Mode-Select Input. Drive low for DSP interface mode. Drive high for SPI interface mode.
21	20	$\overline{CS}$	Active-Low Digital Chip-Select Input
22	21	DOUT	Digital Serial Data Output. Use DOUT to daisy chain or read the contents of the internal registers. DOUT data clocks out on the falling edge of SCLK, MSB first.
23	22	SCLK	Digital Serial Clock Input
24	23	DIN	Digital Serial Data Input. Data clocks in on the falling edge of SCLK.
27	26	$\overline{LDAC}$	Active-Low Digital Load DAC Input. Drive this asynchronous input low to transfer the contents of the input register to their respective DAC registers and update all DAC outputs accordingly.
28	27	$\overline{RESET}$	Active-Low Reset Input. Drive this asynchronous input low to initiate a power-on reset. See the *Power-On Reset* section for further information.
29	28	GS1	Ground-Sense Analog Input 1. Offsets the DAC amplifier outputs OUT3–OUT15 and OUT19–OUT31 by ±0.5V to compensate for a remote system ground potential difference.
30, 60	29, 56	REFGND	Reference Ground

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

Pin Description

PIN		NAME	FUNCTION
68 TQFN	64 TQFP		
31	30	REF	Analog Reference Voltage Input. Connect a +3V reference to REF and bypass to REFGND with a 0.1µF capacitor.
32, 61	31, 57	AV_{DD}	Analog Power-Supply Input. Bypass to AGND with a 0.1µF capacitor.
37	35	OUT16	DAC16 Buffered Analog Output Voltage
38	36	OUT17	DAC17 Buffered Analog Output Voltage
39	37	OUT18	DAC18 Buffered Analog Output Voltage
40	38	OUT19	DAC19 Buffered Analog Output Voltage
41	39	OUT20	DAC20 Buffered Analog Output Voltage
42	40	OUT21	DAC21 Buffered Analog Output Voltage
43	41	OUT22	DAC22 Buffered Analog Output Voltage
44	42	OUT23	DAC23 Buffered Analog Output Voltage
45	43	OUT24	DAC24 Buffered Analog Output Voltage
48	46	OUT25	DAC25 Buffered Analog Output Voltage
49	47	OUT26	DAC26 Buffered Analog Output Voltage
54	50	OUT27	DAC27 Buffered Analog Output Voltage
55	51	OUT28	DAC28 Buffered Analog Output Voltage
56	52	OUT29	DAC29 Buffered Analog Output Voltage
57	53	OUT30	DAC30 Buffered Analog Output Voltage
58	54	OUT31	DAC31 Buffered Analog Output Voltage
62	58	OUT15	DAC15 Buffered Analog Output Voltage
63	59	OUT14	DAC14 Buffered Analog Output Voltage
64	60	OUT13	DAC13 Buffered Analog Output Voltage
65	61	OUT12	DAC12 Buffered Analog Output Voltage
66	62	OUT11	DAC11 Buffered Analog Output Voltage
67	63	OUT10	DAC10 Buffered Analog Output Voltage
EP	—	EP	Exposed Paddle. Connect to V_{SS}.

Detailed Description

The MAX5773/MAX5774/MAX5775 are 32-channel, 14-bit, voltage-output DACs. All devices accept a +3.0V external reference input at REF. An internal offset DAC allows all outputs to be offset up to -5V (see Table 1).

A 33MHz SPI-/QSPI-/MICROWIRE- or DSP-compatible serial interface (see Figure 1) controls the MAX5773/MAX5774/MAX5775. Use $\overline{DSP}$ to select the DSP mode or the SPI/QSPI/MICROWIRE mode.

Each DAC has a double-buffered input structure to minimize the digital-noise feedthrough from the digital inputs to the outputs. The two buffers are organized as an input register followed by a DAC register. Input registers update the DAC registers independently or simultaneously with a single software or hardware command. Each DAC channel has its own offset and gain registers that calibrate offset and gain errors for a given channel. The MAX5773/MAX5774/MAX5775 are divided into two banks of 16 channels to provide real-time calibration of channel pairs. Channel bank pairs are ordered as (bank 0:bank 1) OUT0:OUT16, OUT1:OUT17 … OUT14:OUT30, OUT15:OUT31.

An offset DAC allows all the outputs to be offset up to -5V and dual ground-sensing inputs (GS1 and GS2) allow the output voltages to be referenced to remote

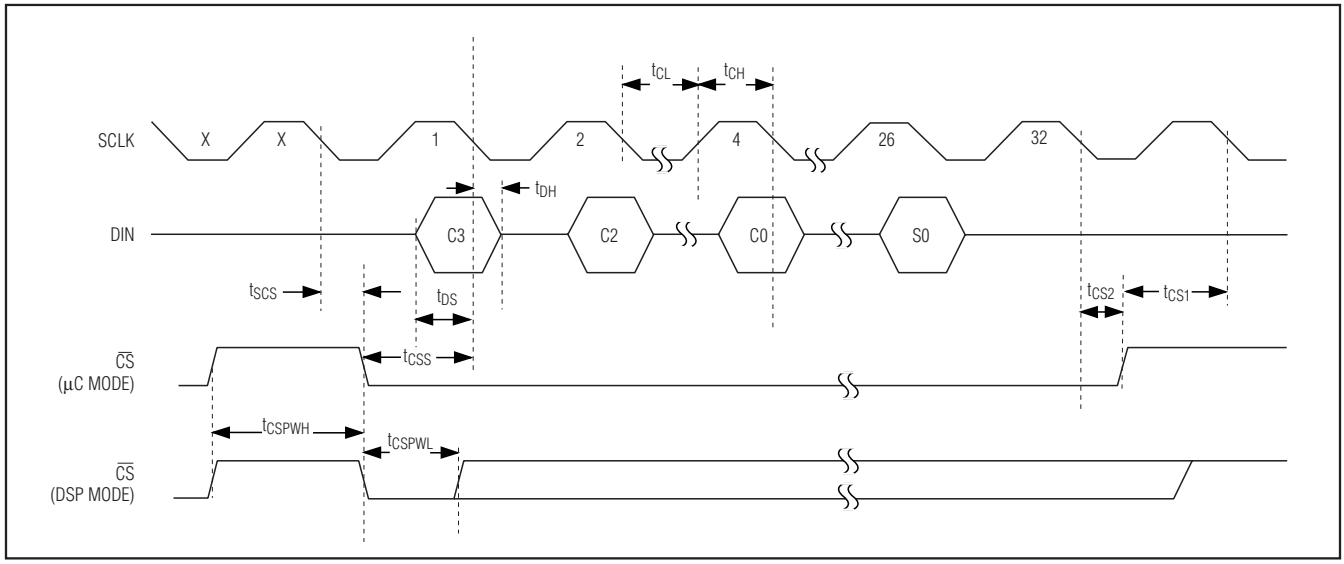


Figure 1. Serial-Interface Timing

Table 1. Offset DAC Codes

PART	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S1*	S0*
MAX5773	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MAX5774	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MAX5775	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**S1 = S0 = 0 for proper operation.*

grounds (see the Functional Diagram). Three output channels of each channel bank (bank 0 and bank 1) are referenced to GS2 (OUT0, OUT1, OUT2 in bank 0, and OUT16, OUT17, OUT18 in bank 1). All other output channels are referenced to GS1.

The MAX5773/MAX5774/MAX5775 analog and digital sections have separate power inputs (AV_{DD} and DV_{DD}). Separate power inputs are also provided for the output buffers (AV_{CC} and V_{SS}). Proprietary deglitch circuitry prevents output glitches at power-up and eliminates the need for power sequencing. A software-shutdown mode facilitates efficient power management. When shut down, the MAX5773/MAX5774/MAX5775 consume 50µA (typ) of supply current.

The MAX5773/MAX5774/MAX5775 have a 5µs (typ) wake-up time from shutdown mode to normal DAC operation.

All DACs provide buffered outputs that can drive 10kΩ in parallel with 100pF. The MAX5773 has a 0 to +10V output range; the MAX5774 has a -2.5V to +7.5V output range; and the MAX5775 has a -5V to +5V output range.

External Reference Input (REF)

The REF voltage sets the full-scale output voltage for all 32 DACs. REF accepts a +3.0V ±3% input. Reference voltages outside these limits result in a degradation of device performance.

REF is a buffered input. The input impedance is 1MΩ minimum and it does not vary with code. Use a high-accuracy, low-noise voltage reference such as the MAX6126AASA30 (3ppm/°C temperature drift and 0.02% initial accuracy) to improve static accuracy. REF does not accept AC signals.

Ground Sense (GS1 and GS2)

The MAX5773/MAX5774/MAX5775 include ground-sense inputs (GS1 and GS2) that allow the output voltages to be referenced to a remote ground. The ground-sense input GS1 is connected to channels OUT3–OUT15 (bank 0) and to channels OUT19–OUT31 (bank 1). The ground-sense input GS2 is connected to channels OUT0, OUT1, OUT2 (bank 0), and OUT16, OUT17, OUT18 (bank 1). Channels connected to the same ground sense can be accessed in pairs. For example, OUT0 and OUT16 can

32-Channel, 14-Bit, Voltage-Output DACs with Serial Interface

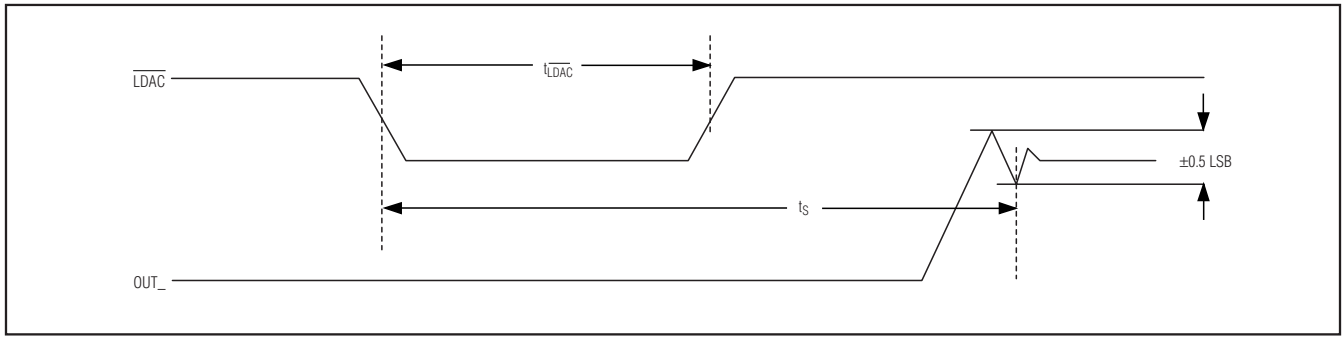


Figure 2. LDAC Timing

be accessed as a pair (see Figure 3 for pairing of output channels).

The ground-sense input voltage range (V_{GS1} or V_{GS2}) is -0.5V to +0.5V with respect to AGND. V_{GS} is added to the output voltage with unity gain. Ensure that the resulting output voltage is within the valid output voltage range set by the power supplies. Refer to the *Output Amplifiers (OUT0–OUT31)* section for the effect of the ground-sense inputs on the DAC outputs.

Offset DAC

The MAX5773/MAX5774/MAX5775 feature an offset DAC that determines the output voltage range. While each device provides an allowable output voltage range, the offset DAC determines the endpoint voltages of the range. Table 1 shows the offset DAC code necessary for each device's output-voltage range.

The MAX5773/MAX5774/MAX5775 offset DAC can be programmed with any of the three output voltage ranges. The specifications in the *Electrical Characteristics* table are only guaranteed (production tested) for the offset code associated with each particular part number.

The offset DAC is summed with the GS_ input voltage (see the *Functional Diagram*). Any change in the offset DAC affects all 32 DACs.

The offset DAC is also double buffered with an input and DAC register.

Software commands for the MAC-bypass for all channels and load-DAC for all channels do not affect the offset DAC.

The data format for writing to the offset DAC is: control bits C3–C0 = 0011, address bits A5–A0 = 110000, 14 data bits (and S1, S0), and 6 don't-care bits as shown in Table 2.

Table 2. Offset DAC Input Data Format

CONTROL BITS	ADDRESS BITS	DATA BITS	DON'T-CARE BITS
C3–C0	A5–A0	D13–D0 and S1, S0*	6 Don't-Care Bits
0011	110000	See Table 1	XXXXXX

**S1 = S0 = 0 for proper 14-bit operation.*

Table 3. Software Load-DAC Input Data Format

CONTROL BITS	ADDRESS BITS	DATA BITS	DON'T-CARE BITS
C3–C0	A5–A0	D13–D0 and S1, S0*	6 Don't-Care Bits
0010	111111	XXXXXXXXXX XXXX00	XXXXXX

**S1 = S0 = 0 for proper 14-bit operation.*

Output Amplifiers (OUT0–OUT31)

All DAC outputs are internally buffered. The internal buffers provide gain, improved load regulation, and glitch suppression for the DAC outputs. The output buffers slew at 1V/µs and can drive 10kΩ in parallel with 100pF. The output buffers are powered by AV_{CC} and V_{SS}. AV_{CC} and V_{SS} determine the maximum output voltage range of the device.

The input code, the voltage reference, the offset DAC output, the voltage on GS1 (or GS2), and the gain of the output amplifier determine the output voltage. Calculate V_{OUT} as follows:

$$V_{OUT} = \frac{GAIN \times V_{REF} \times (DAC\ CODE - OFFSET\ DAC\ CODE)}{2^{14}} + V_{GS\_}$$

CHANNEL-BANK SELECTION

ADDRESS BITS		CHANNEL BANK(S) SELECTED
A5	A4	
0	0	CHANNEL BANK 0
0	1	CHANNEL BANK 1
1	0	BOTH CHANNEL BANKS
1	1	OFFSET CHANNEL AND ALL CHANNEL OPERATION

INPUT REGISTER, DAC REGISTER, GAIN REGISTER, AND OFFSET REGISTER ACCESS*

BANK 0		BANK 1		BANK 0 AND BANK 1		ADDRESS BITS			
A5	A4	A5	A4	A5	A4	A3	A2	A1	A0
0	0	0	1	1	0				
CHANNEL 0		CHANNEL 16		CHANNEL 0 AND CHANNEL 16		0	0	0	0
CHANNEL 1		CHANNEL 17		CHANNEL 1 AND CHANNEL 17		0	0	0	1
CHANNEL 2		CHANNEL 18		CHANNEL 2 AND CHANNEL 18		0	0	1	0
CHANNEL 3		CHANNEL 19		CHANNEL 3 AND CHANNEL 19		0	0	1	1
CHANNEL 4		CHANNEL 20		CHANNEL 4 AND CHANNEL 20		0	1	0	0
CHANNEL 5		CHANNEL 21		CHANNEL 5 AND CHANNEL 21		0	1	0	1
CHANNEL 6		CHANNEL 22		CHANNEL 6 AND CHANNEL 22		0	1	1	0
CHANNEL 7		CHANNEL 23		CHANNEL 7 AND CHANNEL 23		0	1	1	1
CHANNEL 8		CHANNEL 24		CHANNEL 8 AND CHANNEL 24		1	0	0	0
CHANNEL 9		CHANNEL 25		CHANNEL 9 AND CHANNEL 25		1	0	0	1
CHANNEL 10		CHANNEL 26		CHANNEL 10 AND CHANNEL 26		1	0	1	0
CHANNEL 11		CHANNEL 27		CHANNEL 11 AND CHANNEL 27		1	0	1	1
CHANNEL 12		CHANNEL 28		CHANNEL 12 AND CHANNEL 28		1	1	0	0
CHANNEL 13		CHANNEL 29		CHANNEL 13 AND CHANNEL 29		1	1	0	1
CHANNEL 14		CHANNEL 30		CHANNEL 14 AND CHANNEL 30		1	1	1	0
CHANNEL 15		CHANNEL 31		CHANNEL 15 AND CHANNEL 31		1	1	1	1

**CHANNEL PAIR ACCESS (BANK 0 AND BANK 1) ONLY PERMITTED FOR WRITETHROUGH, MAC-BYPASS, AND LOAD-DAC COMMANDS.*

ACCESSING OFFSET CHANNEL AND ALL CHANNELS (ADDRESS BITS A5 AND A4 = 11)

ADDRESS BITS				REGISTER SELECTED
A3	A2	A1	A0	
0	0	0	0	OFFSET CHANNEL
0001 THROUGH 1110				UNUSED
1	1	1	1	ALL CHANNELS (SOFTWARE LOAD-DAC AND MAC-BYPASS COMMANDS ONLY)

ACCESSING CONFIGURATION REGISTER (CONTROL BITS C3–C0 = 1100 OR 1101, ADDRESS BITS A5 AND A4 = 00)

ADDRESS BITS				REGISTER SELECTED
A3	A2	A1	A0	
0	0	0	0	CONFIGURATION REGISTER (SEE TABLE 8)
0001 THROUGH 1111				UNUSED

Figure 3. Address Space When Accessing DAC Channel Register(s), Offset Register(s), Gain Register(s), and Special Registers

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GAIN = 10/3 for the MAX5773/MAX5774/MAX5775.

Load-DAC ($\overline{LDAC}$) Input

The MAX5773/MAX5774/MAX5775 feature an active-low $\overline{LDAC}$ input that allows the outputs (OUT_) to update asynchronously. Keep $\overline{LDAC}$ high during normal operation (when the device is controlled only through the serial interface). Drive $\overline{LDAC}$ low to simultaneously update all DAC outputs with data from their respective input registers. Figure 2 shows the $\overline{LDAC}$ timing with respect to OUT_.

A software command can also perform the $\overline{LDAC}$ operation. To initiate $\overline{LDAC}$ by software, set control bits C3–C0 = 0010, address bits A5–A0 = 111111, and all data bits to don't care. See Table 3 for the data format. This operation updates all DAC outputs simultaneously. The software load-DAC command for all channels does not affect the offset DAC.

Software MAC-Bypass

The MAX5773/MAX5774/MAX5775 feature a software MAC-bypass command that loads data into the DAC directly from DIN. Software MAC-bypass loads one DAC, a pair of DACs, or all 32 DACs with a data word (D13–D0 and S1, S0) entered at DIN and the selected DAC output(s) are simultaneously updated. Software MAC-bypass bypasses gain and offset calibration, sending the input data directly to the DAC register immediately updating the selected DAC outputs. After executing MAC-bypass on a channel(s), previously calibrated data can be reloaded into the DAC by executing software load-DAC or hardware $\overline{LDAC}$ (see Figure 4). Using software MAC-bypass, the DAC output(s) can be set to the ground-sense value or any arbitrary value within the DAC output voltage range.

To activate software MAC-bypass, set control bits C3–C0 = 0111. The address bits (A5–A0) select the DAC(s) to be updated and the data bits (D13–D0) control the DAC output voltage value. Table 4 shows the input data format for the software-controlled MAC-bypass command.

Reset ($\overline{RESET}$)

The MAX5773/MAX5774/MAX5775 feature an active-low $\overline{RESET}$ logic input that asynchronously sets all the registers to code 0000h (power-up state). The serial interface can also issue a software-reset command. Setting the control bits C3–C0 = 1111 performs the same function as driving the logic input $\overline{RESET}$ low. Table 5 shows the reset data format for the software-controlled reset command. The software reset does not work in daisy-chain mode. Reprogram the offset DAC after asserting a software or hardware reset.

Table 4. MAC-Bypass Data Format

CONTROL BITS	ADDRESS BITS	DATA BITS	DON'T-CARE BITS
C3–C0	A5–A0	D13–D0 and S1, S0*	6 Don't-Care Bits
0111	See Figure 3	D13–D0, S1, S0*	XXXXXX

**S1 = S0 = 0 for proper 14-bit operation.*

Table 5. Reset Data Format

CONTROL BITS	ADDRESS BITS	DATA BITS	DON'T-CARE BITS
C3–C0	A5–A0	D13–D0 and S1, S0*	6 Don't-Care Bits
1111	XXXXXX	XXXXXXXXXX XXXX00	XXXXXX

**S1 = S0 = 0 for proper 14-bit operation.*

Table 6. Serial Data Format

CONTROL BITS	ADDRESS BITS	DATA BITS	6 DON'T-CARE BITS
MSB			LSB
C3–C0	A5–A0	D13–D0 and S1, S0*	XXXXXX

**S1 = S0 = 0 for proper 14-bit operation.*

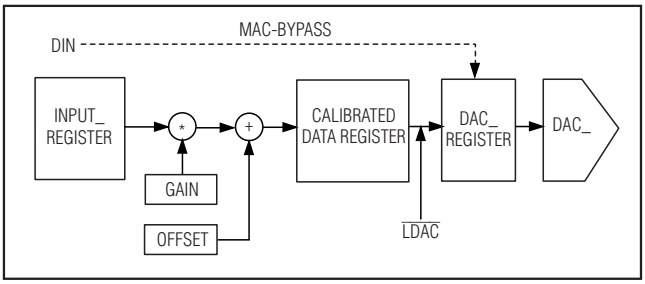

Figure 4. MAC-Bypass Functional Diagram

Serial Interface

The MAX5773/MAX5774/MAX5775 allow channel updates either individually or in pairs. This is achieved by dividing the 32 channels into two channel banks, with 16 channels in each bank. Channel bank 0 contains output channels OUT0–OUT15 and channel bank 1 contains channels OUT16–OUT31. A channel from bank 0 is paired with a channel from bank 1 and is ordered as OUT0:OUT16, OUT1:OUT17...OUT14:OUT30, OUT15:OUT31.

A 3-wire SPI-/QSPI-/MICROWIRE- and DSP-compatible serial interface controls the MAX5773/MAX5774/MAX5775. The interface requires a

32-bit command word to control the device. The command word consists of 4 control bits, 6 address bits, 14 data bits (and S1, S0 = 00), and 6 don't-care bits. Table 6 shows the general serial data format. The control bits control various write and read commands, as well as the load DAC and MAC-bypass commands. Table 8 shows the control-bit functions. The address bits select the register(s) to update. Figure 3 shows the address functions. The data bits control the voltage value of the DAC outputs. DIN data is clocked in at the falling edge of SCLK (Figure 1).

Table 7. Gain and Offset Register Input Data Format

REGISTER	CONTROL BITS (C3–C0)	ADDRESS BITS (A5–A0)	DATA BITS (D13–D0 AND S1, S0*)	6 DON'T-CARE BITS
Offset Register	1001	See Figure 3	See Table 10	XXXXXX
Gain Register	1000	See Figure 3	See Table 9	XXXXXX

**S1 = S0 = 0 for proper 14-bit operation.*

Table 8. Control-Bit Functions

4 CONTROL BITS				CONTROL-BIT DESCRIPTION
C3	C2	C1	C0	
0	0	0	0	No operation (NOP). No internal registers change state. The NOP command can be passed to DOUT depending on the state of the configuration register. Address bits A5–A0 and data bits D13–D0 are ignored.
0	0	0	1	This instruction writes and calibrates the 14-bit input data word for gain and offset errors. Drive $\overline{LDAC}$ low or use a software load-DAC command to update the selected DAC outputs.
0	0	1	0	Software load-DAC command. Updates the output of the selected DAC channel(s). Depending on the address bits, this command updates one DAC output, a pair of DAC outputs, or all the DAC outputs simultaneously. Data bits D13–D0 are ignored.
0	0	1	1	This instruction writes and calibrates the 14-bit input data word for gain and offset errors and immediately updates the DAC outputs for the selected address.
0	1	0	0	Read command. Depending on the address bits, one of the input register values is read back through DOUT. Data bits D13–D0 are ignored. See the *Daisy-Chain Operation* section.
0	1	0	1	Reserved; do not use.
0	1	1	0	Reserved; do not use.
0	1	1	1	MAC-bypass command. Depending on the address bits, one, two, or all DAC registers are loaded with a 14-bit data word at DIN. The input data is not calibrated for gain and offset errors (see the *MAC-Bypass* section). Selected DAC output(s) are immediately updated.
1	0	0	0	Loads D13–D0 into one or two of the gain register(s) for the selected address. The data for the selected address is calibrated for gain error. Drive $\overline{LDAC}$ low or use a software load-DAC command to update the selected DAC outputs.
1	0	0	1	Loads D13–D0 into one or two of the offset register(s) for the selected address. The data for the selected address is calibrated for offset error. Drive $\overline{LDAC}$ low or use a software load-DAC command to update the selected DAC outputs.
1	0	1	0	Read command. Reads one of the gain registers and presents the data at DOUT.
1	0	1	1	Read command. Reads one of the offset registers and presents the data at DOUT.
1	1	0	0	Write command. Loads D13–D0 into the configuration register.
1	1	0	1	Read command. Reads the contents of the configuration register.
1	1	1	0	Read command. Reads the DAC register for the selected address.
1	1	1	1	Reset instruction.

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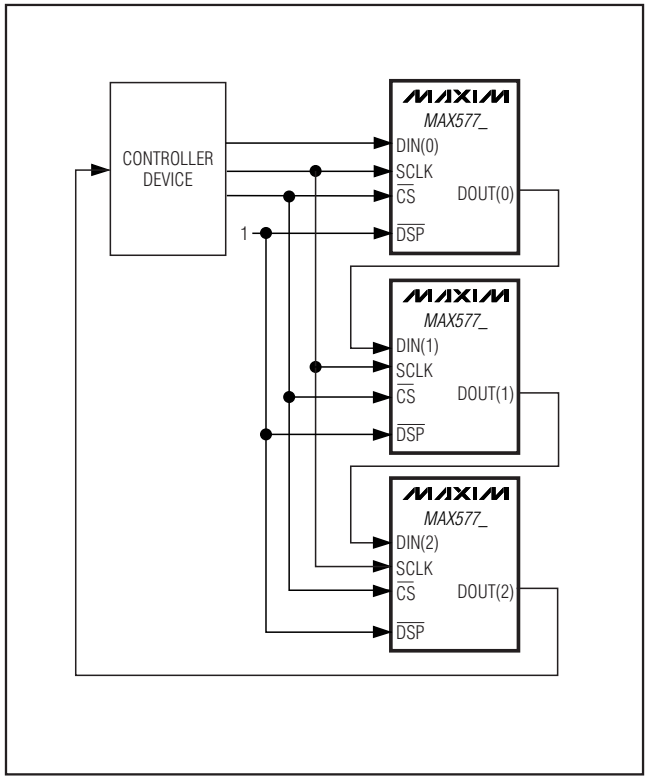

Figure 5. Daisy-Chain Configuration

Table 9. Gain Register Code Values

CODE (DATA BITS D13–D0)	GAIN VALUE
0000h	Unity Gain
0001h	0.000061
0002h	0.00012
:	:
1FFFh	0.499938
2000h	0.5
:	:
3FFEh	0.999877
3FFFh	0.999938

Table 10. Offset Register Code Values

CODE (DATA BITS D13–D0)	OFFSET VALUE*
1FFFh	FS/2 - 1 LSB
:	:
0001h	+1 LSB
0000h	0
3FFFh	-1 LSB
:	:
2000h	-FS/2

**1 LSB = FS/2^{14}*

Gain and Offset Registers

The MAX5773/MAX5774/MAX5775 contain a gain and offset register associated with each channel to correct real-time gain and offset errors associated with each channel. The gain and offset registers can be accessed individually or in pairs.

The gain word range is limited between 0 and 1. The gain word is an unsigned 14-bit data word. A gain word of 0000h is a special mapping to provide a gain of absolute one, i.e., no gain correction. For all the other gain word codes, the amount of gain correction varies proportionally to the gain word's decimal value. For example, a gain word of 0001h is equivalent to a gain of 0.5^{14} and a gain of 3FFFh is equivalent to $1 - 0.5^{14}$ (see Table 9). To access the gain register, set control bits C3–C0 = 1000 (see Tables 7 and 8).

The offset has a range from -FS/2 to + (FS/2 - 1 LSB). The offset word is a 14-bit data word represented in two's complement. For example, an offset word equivalent to 1FFFh would provide an offset of FS/2 - 1 LSB and offset word of 2000h would provide an offset of -FS/2 (see Table 10). To access the offset register, set control bits C3–C0 = 1001 (see Tables 7 and 8).

Configuration Register

The configuration register controls the advanced features of the MAX5773/MAX5774/MAX5775. Write to the configuration register by setting control bits C3–C0 = 1100 and address bits 000000. Table 11 shows the configuration register data format for the D13–D0 data bits. Table 12 shows the commands controlled by the configuration register.

DSP Mode ($\overline{DSP}$)

The MAX5773/MAX5774/MAX5775 provide a hardware-selectable DSP-interface mode. The active-low $\overline{DSP}$ logic input selects the microcontroller (µC)-interface or DSP-interface mode. Drive $\overline{DSP}$ high for µC-interface mode. Drive $\overline{DSP}$ low for DSP-interface mode. DSP mode, when active, allows chip select ($\overline{CS}$) to go high before the entire 32-bit command word is clocked in. Figure 1 illustrates serial timing for both µC- and DSP-interface modes.

SING

When SING = 0, the MAX5773/MAX5774/MAX5775 are in daisy-chain mode. For daisy-chain operation, set $\overline{DSP}$ high (µC mode) and SING = 0.

Table 11. Configuration Register Data Format

14 DATA BITS															
D13	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**S1**	**S0**
ERRF	SING	GLT	DT	SHDN	X	X	X	X	X	X	X	X	X	X	X

X = Don't care.

Table 12. Configuration Register Commands

DATA BIT	NAME	DESCRIPTION
D13	ERRF	Error flag. ERRF goes logic high when an invalid command is attempted. ERRF is cleared each time the configuration register is read back to DOUT. Reset-register commands C3–C0 = 1111 reset ERRF. Conditions that trigger ERRF include: • Attempted read of a wrong or invalid address bits A5–A0 • Access to reserved addresses The default is logic low (no error flags); ERRF is read only.
D12	SING	Single device. SING determines daisy-chain or stand-alone mode. Logic high sets the device to operate in stand-alone mode or in parallel with other devices. Only 14 data bits (and S1, S0 = 00) are output to DOUT when SING is logic high. When SING is logic low, the entire 32-bit command word is output to DOUT. The default is logic low (daisy-chain mode). For daisy-chain operation, set SING to logic low and $\overline{DSP}$ must be set high (µC mode). SING is read/write.
D11	GLT	Glitch-suppression enable. The MAX5773/MAX5774/MAX5775 feature glitch-suppression circuitry on the analog outputs that minimizes the output glitch during a major carry transition. A logic low disables the internal glitch-suppression circuitry. Logic high enables glitch suppression, suppressing up to a 120nV-s glitch impulse on the DAC outputs. Default is logic low (glitch suppression is disabled). GLT is read/write.
D10	DT	Digital output enable. A logic low enables DOUT. Logic high disables DOUT. Disabling DOUT reduces power consumption and digital noise feedthrough to the DAC outputs from the DOUT output buffer. Default is logic-low (DOUT enabled); DT is read/write.
D9	SHDN	Shutdown. A logic high shuts down all 32 DACs. The logic interface remains active, and the data is retained in the DAC and input registers. Read/write operations can be performed while the device is shut down; however, no changes can occur at the device outputs. Logic-low powers up all 32 DACs. Upon waking up (5µs (typ)), the DAC outputs return to the last stored value in the DAC registers. Default is logic low (normal operation). SHDN is read/write.
D8–D0 and S1, S0	X	Don't care.

In daisy-chain operation, DOUT follows DIN after 32 clock cycles for a write command. For a read command, DOUT provides only the 14 data bits (and S1, S0) in the next cycle following the $\overline{CS}$ falling edge. Data is provided MSB first at DOUT on the falling edge of SCLK.

When SING = 1, the device is in stand-alone mode. To reduce the time it takes to read data out, the read data is provided MSB first at DOUT on the last 16 cycles of the current command word. The device acts on an incoming command word independent of the rising edge of $\overline{CS}$. SING functionality is ignored in DSP mode.

Daisy-Chain Operation

Daisy chain any number of the MAX5773/MAX5774/MAX5775 devices by connecting the DOUT of one device to DIN of another. Set $\overline{DSP}$ high and SING = 0 for all devices in the daisy chain (see Figure 5).

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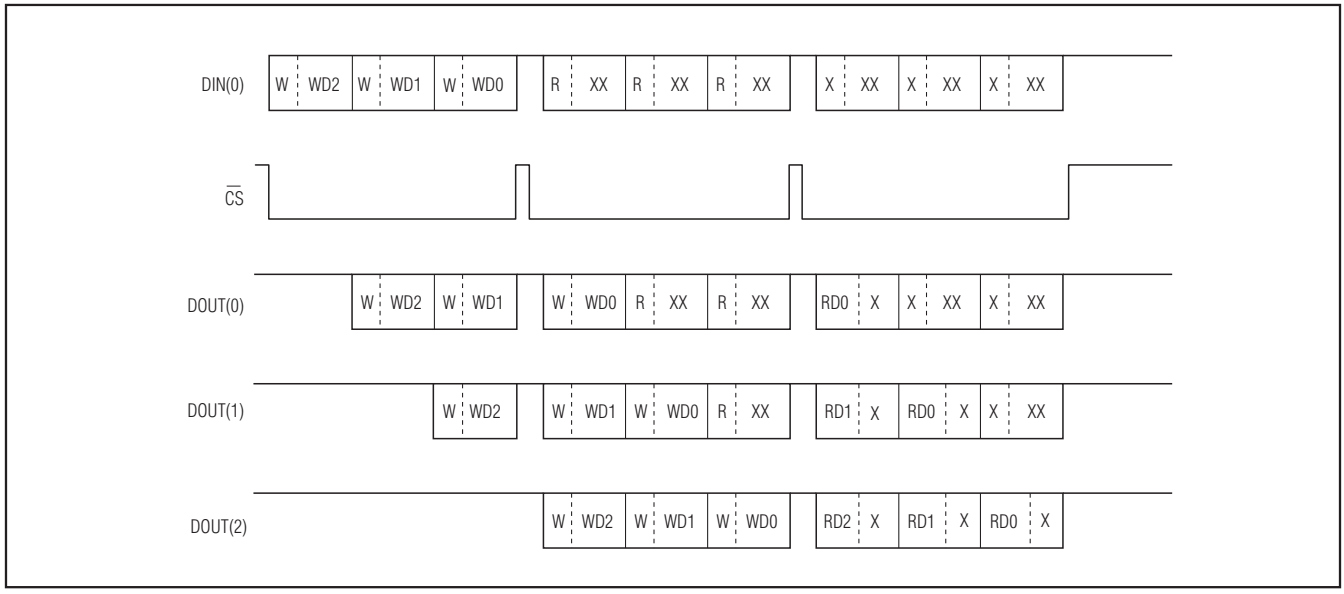

Figure 6. Example 1 of a Daisy-Chain Data Sequence

W/WD0 = 32-bit word with a write command; WD0 writes data for device 0. The 0 refers to the position in the daisy chain (0 is closest to the bus master). Devices 1 and 2 are devices further down the chain.
RDn/X = 32-bit word with a 14-bit read output from from device "n" followed by don't-care bits.
X = Don't care (for X in the data or command position).

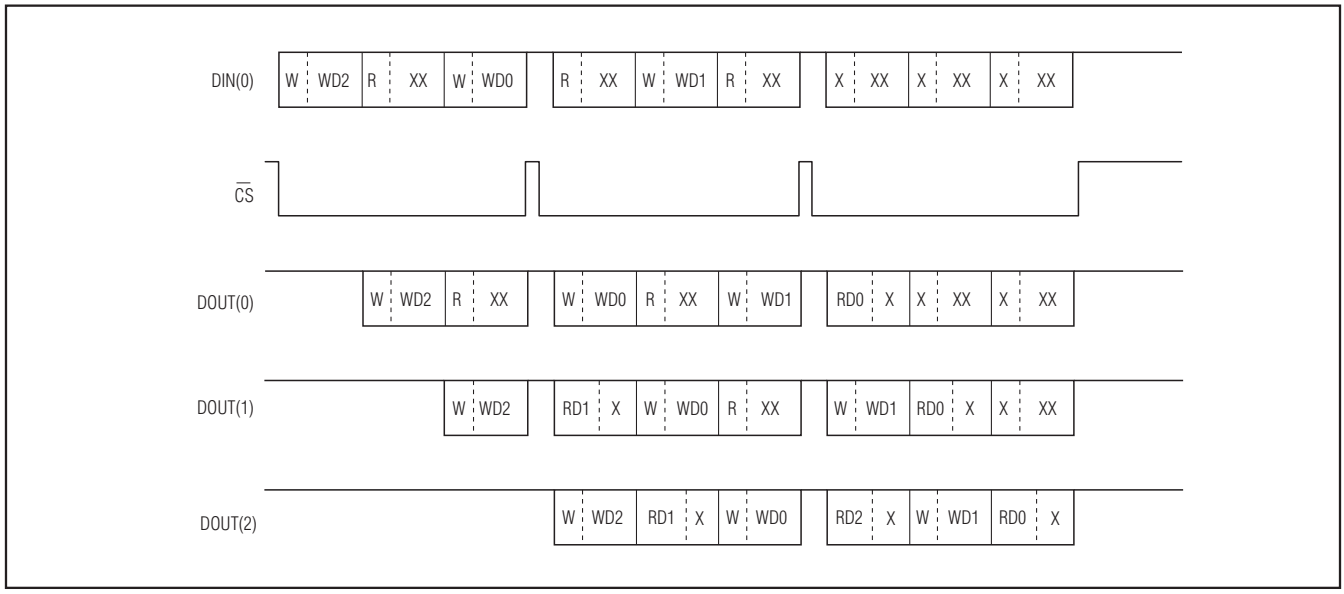

Figure 7. Example 2 of a Daisy-Chain Data Sequence

W/WD0 = 32-bit word with a write command; WD0 writes data for device 0. The 0 refers to the position in the daisy chain (0 is closest to the bus master). Devices 1 and 2 are devices further down the chain.
RDn/X = 32-bit word with a 14-bit read output from from device "n" followed by don't-care bits.
X = Don't care (for X in the data or command position).

The MAX5773/MAX5774/MAX5775 support daisy-chain connections of multiple devices. The default (power-up) configuration for the MAX5773/MAX5774/MAX5775 assumes that the device may be part of a daisy chain of devices (SING = 0 and $\overline{DSP}$ = 1). For a write command, DOUT follows DIN after 32 clock cycles in the default configuration. Figures 6 and 7 show examples of daisy-chain data sequences.

Data Readback

Read the contents of the MAX5773/MAX5774/MAX5775 DAC and configuration registers at DOUT by issuing a read-data command. Control bits C3–C0 configure the device for the read-data modes (see Table 8). The address bits select the register(s) to be read. The contents of the register(s) are clocked out MSB first at DOUT on the falling edge of SCLK. The output data format depends on the status of $\overline{DSP}$ and SING. Table 13 shows the manner in which data is written to DOUT.

Shutdown Mode

The MAX5773/MAX5774/MAX5775 feature a software-controlled, low-power shutdown mode.

Setting bit 9 of the configuration register to a logic high, disables the analog section of the device, forcing the outputs to go high impedance. In shutdown, supply current is reduced to 50µA typical. Data stored in the DAC and input registers is retained, and the device outputs return to their previous values upon exiting shutdown. Wake-up time is 5µs (typ). The serial interface remains active while the device is in shutdown.

Power-Up State

The MAX5773/MAX5774/MAX5775 monitor the four power supplies and maintain the output buffers in a known state until sufficient voltage is available to ensure that no output glitches occur. Once the minimum voltage threshold has been exceeded, the device outputs come up in the clear state (all outputs = 0).

Applications Information

Automatic Test Equipment (ATE) Applications

The MAX5773/MAX5774/MAX5775 include many features suited for ATE applications. These devices are the most highly integrated level-setting solution available for high-density pin electronics boards, and provide the output voltage ranges required by most ATE applications. The offset DAC simultaneously adjusts the voltage range of all 32 DACs, allowing optimization to the application. The remote-sense feature (GS1 and GS2) allows the pin electronic voltages to be referenced to the ground potential at the DUT site. An integrated offset and gain feature eliminates the need for costly external circuitry.

The pipelined register architecture allows all 32 DACs to be updated simultaneously. This is valuable during test setups, as all values in the tester can be set and then updated in unison with a single command. Accessing the serial interface or the $\overline{LDAC}$ input updates all 32 DACs simultaneously.

The low output noise of the MAX5773/MAX5774/MAX5775 allows direct connection to the pin electronics, eliminating the cost and PC board area of external filtering.

Modern pin electronics integrated circuits (PEICs) are typically fabricated on high-speed processes with low breakdown voltages. Some devices require external protection on their reference inputs to satisfy absolute maximum ratings. The MAX5773/MAX5774/MAX5775 feature outputs that are almost rail-to-rail allowing the AV_{CC} and V_{SS} supplies to be set to voltages within the absolute maximum ratings of the PEIC to guarantee that the PEIC is protected in all situations.

Power Supplies, Bypassing, Decoupling, and Layout

Grounding and power-supply decoupling strongly influence device performance. Digital signals can couple through the reference input, power supplies, and ground connection. Proper grounding and layout can reduce digital feedthrough and crosstalk. For noisy environments, bypass all power supplies with a 0.1µF and 1µF on each pin, as close to the device as possible.

The MAX5773/MAX5774/MAX5775 have four separate power supplies. AV_{DD} powers the internal analog circuitry (except for the output buffers), and DV_{DD} powers the digital section of the device. AV_{CC} and V_{SS} power the output buffers.

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Table 13. Read-Data Modes with SING and $\overline{DSP}$ Controls

$\overline{DSP}$	SING	CONFIGURATION	READ DATA AT DOUT
0	X	Stand-alone DSP mode	DOUT provides the 14 data bits only (and S1, S0). The 14 data bits (and S1, S0) are clocked out MSB first at DOUT, on the last 16 clock edges of the current read command word. See Figures 8, 9, and 10.
1	0	Standard daisy-chain configuration µC mode	For write commands, DOUT follows DIN after 32 clocks. The entire 32-bit write command word (both command word and data) is clocked out MSB first at DOUT. For read commands, the 14 data bits (and S1, S0) of the selected register are valid at DOUT starting with the first clock falling edge after the falling edge of $\overline{CS}$ (see Figures 6 and 7).
1	1	Stand-alone µC mode	DOUT provides the 14 data bits (and S1, S0) of the selected register from the current read command word. The 14 data bits (and S1, S0) are clocked out MSB first at DOUT on the last 16 clock edges of the current read command word (see Figures 8, 9 and 10).

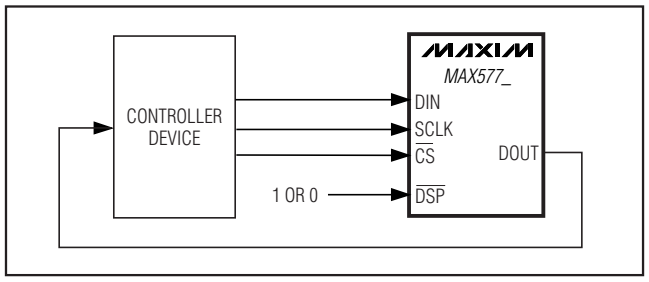


Figure 8. Stand-Alone Configuration

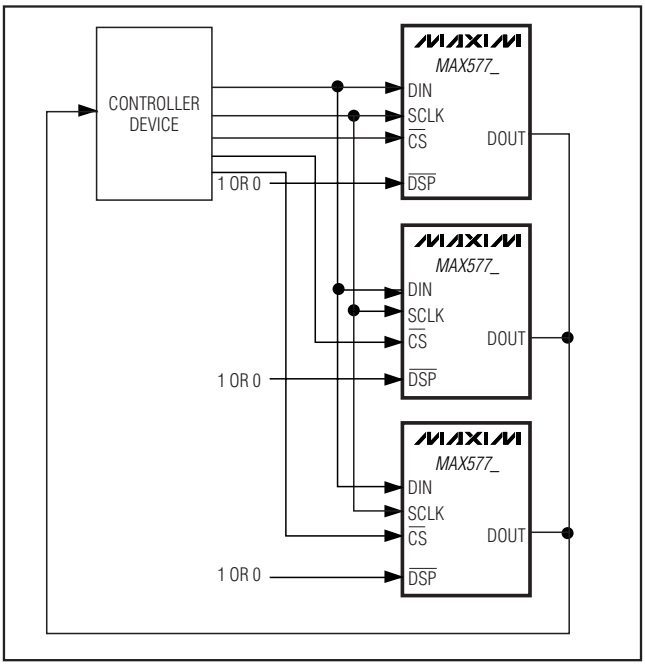


Figure 9. Example of a Parallel Configuration with Readback

Chip Information

PROCESS: BiCMOS

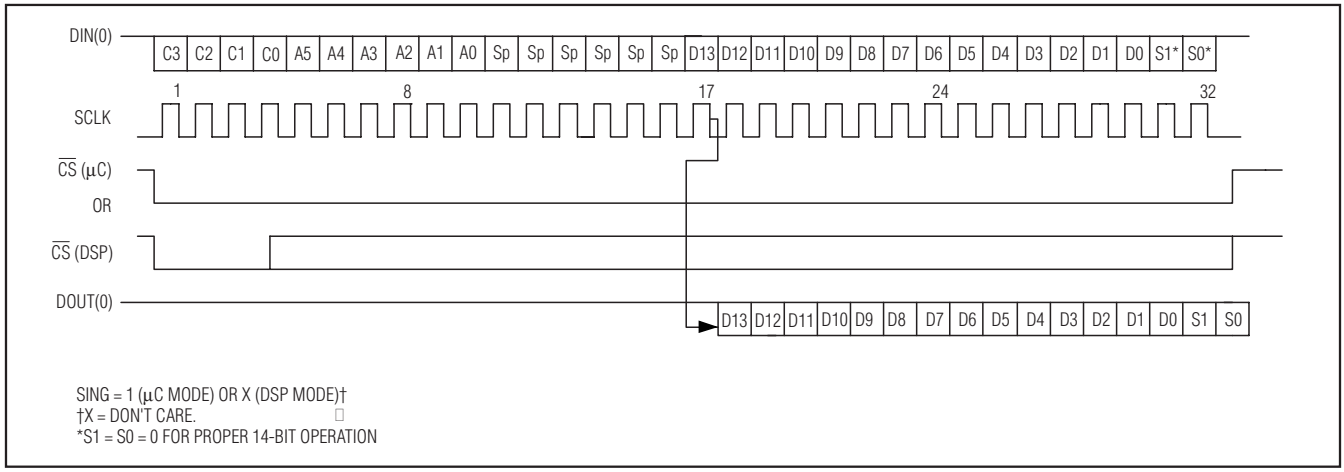
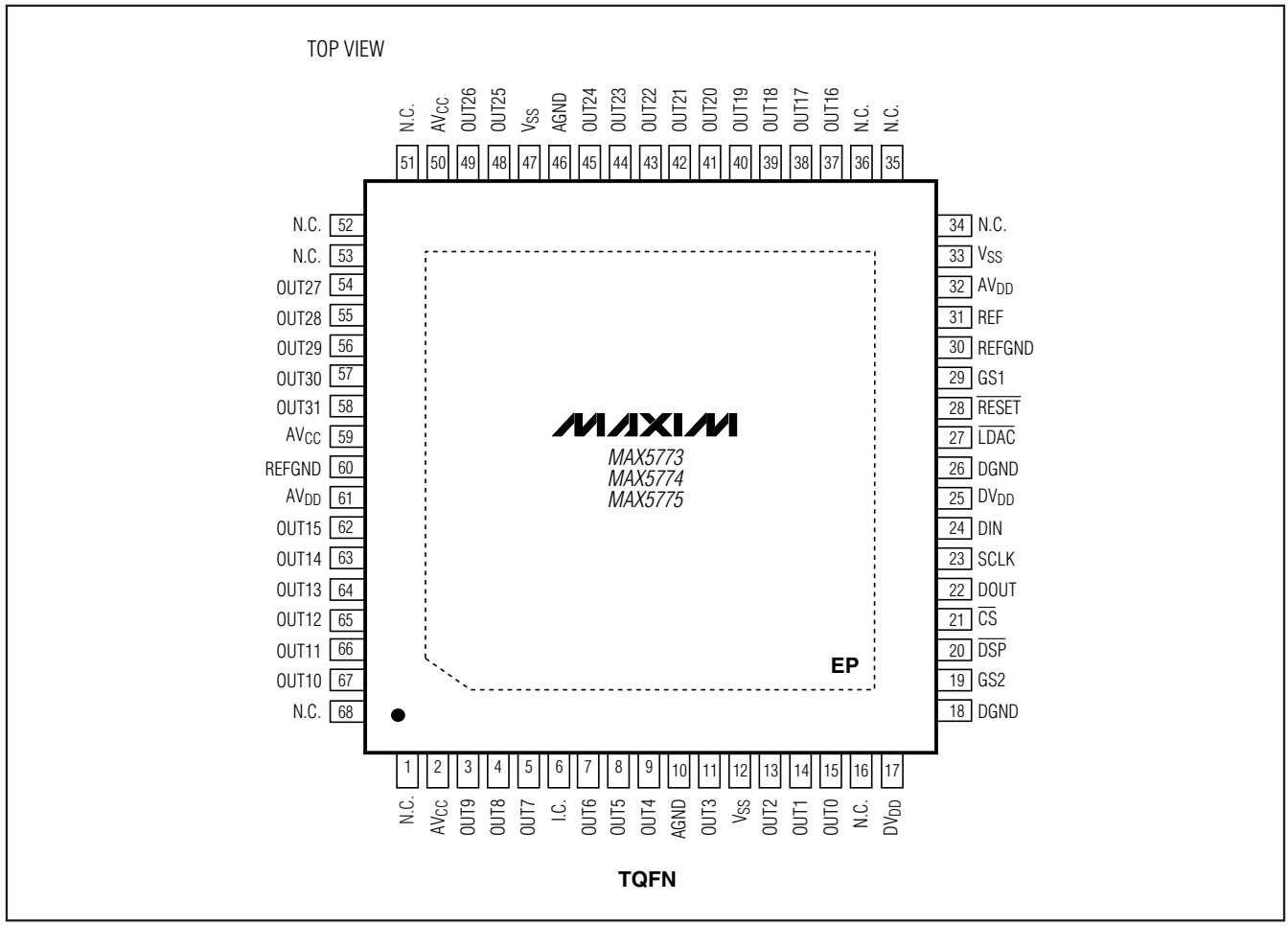


Figure 10. Read Data Timing When Not Daisy Chained

Pin Configurations (continued)



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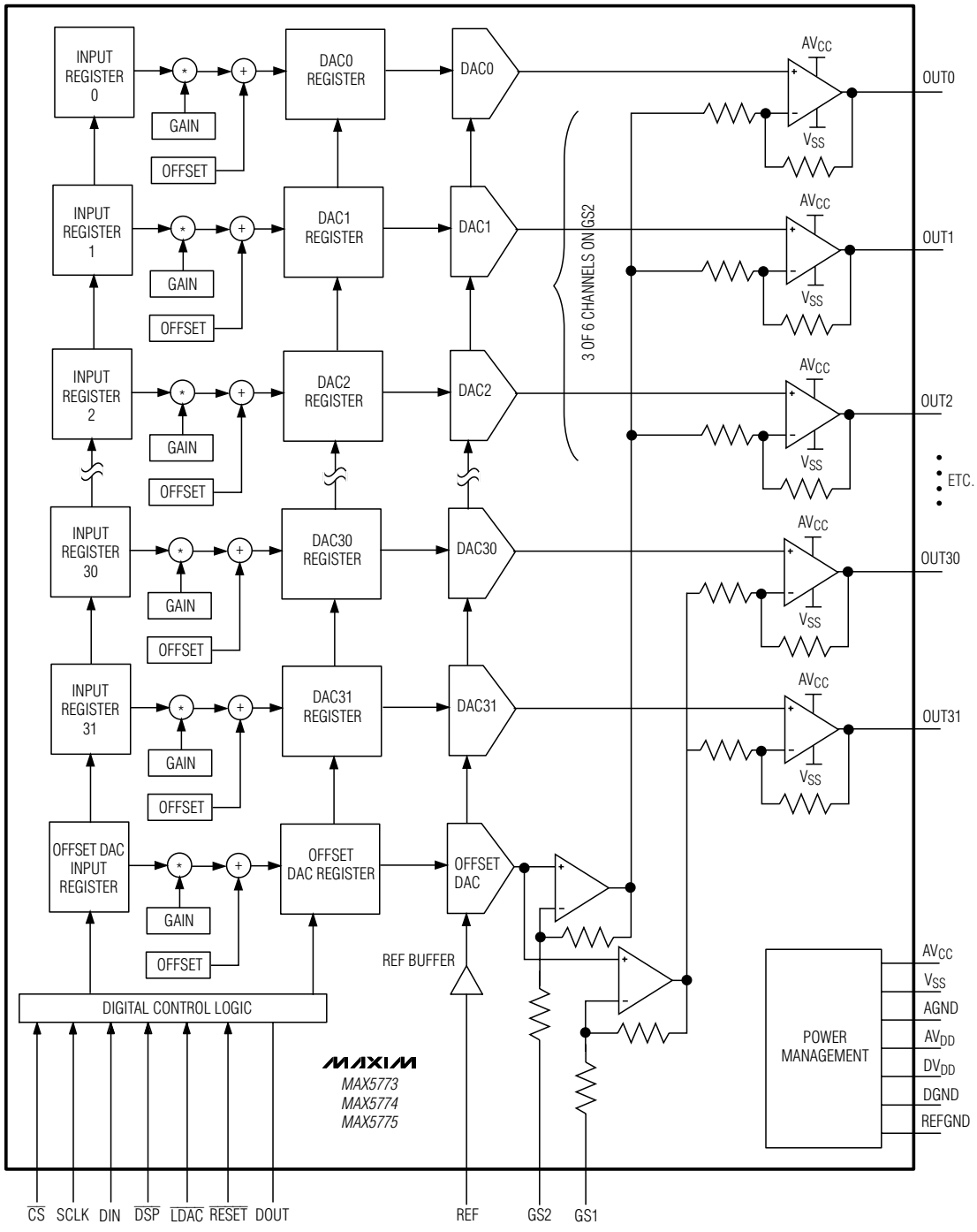
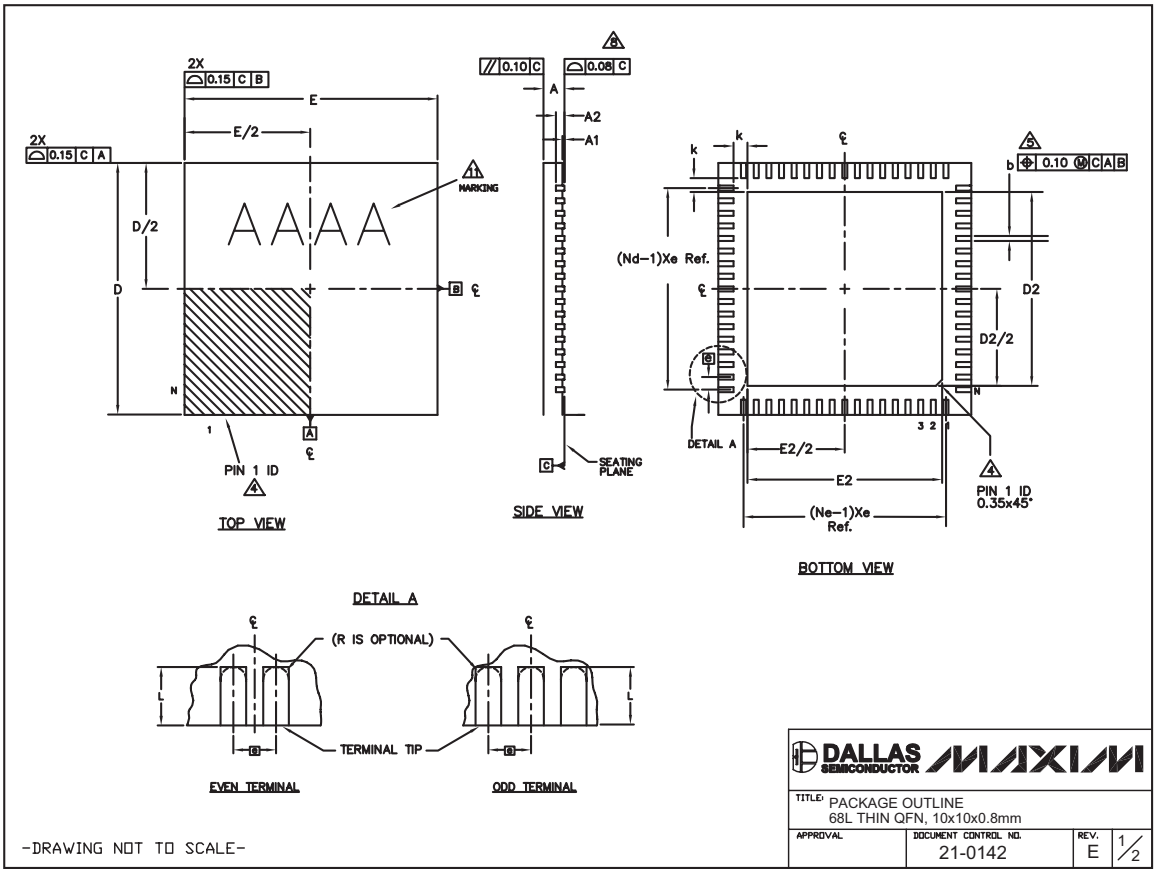
Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	68L 10x10			NOTE
REF.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
A1	0.00	0.01	0.05	
A2		0.20 REF		
b	0.20	0.25	0.30	
D	9.90	10.00	10.10	
E	9.90	10.00	10.10	
e		0.50 BSC.		
k	0.25	-	-	
L	0.45	0.55	0.65	
N		68		
ND		17		
NE		17		
JEDEC		WNND-2		

EXPOSED PAD VARIATIONS						
PKG. CODE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T6800-2	7.60	7.70	7.80	7.60	7.70	7.80
T6800-3	7.60	7.70	7.80	7.60	7.70	7.80
T6800-4	7.60	7.70	7.80	7.60	7.70	7.80
T6800-5	5.70	5.80	5.90	5.70	5.80	5.90

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO-220.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 68L THIN QFN, 10x10x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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