TEA1795T

GreenChip synchronous rectifier controller

Rev. 1 — 4 November 2010 Product data sheet

1. General description

The TEA1795T is a member of the new generation of Synchronous Rectifier (SR) controller ICs for switched mode power supplies. Its high level of integration enables the design of a cost-effective power supply with a minimum number of external components.

The TEA1795T is a dedicated controller IC for synchronous rectification on the secondary side of resonant converters. It has two driver stages for driving the SR MOSFETs, which are rectifying the outputs of the central tap secondary transformer windings.

The two gate driver stages have their own sensing inputs and operate independently of each other.

The TEA1795T is fabricated in a Silicon On Insulator (SOI) process.

2. Features and benefits

2.1 Distinctive features

- Accurate synchronous rectification functionality
- Wide supply voltage range (8.5 V to 38 V)
- Separate sense inputs for sensing the drain and source voltage of each SR MOSFET
- High level of integration, resulting in a minimum external component count
- High driver output voltage of 10 V to drive all MOSFET brands to the lowest R_{DSon}

2.2 Green features

- Low current consumption
- High system efficiency from no load to full load

2.3 Protection features

- UnderVoltage Protection (UVP)

3. Applications

The TEA1795T is intended for resonant power supplies. In such applications, it can drive two external synchronous rectifier MOSFETs which replace diodes for the rectification of the voltages on the two secondary windings of the transformer. It can be used in applications such as:

- Adapters
- ATX power supplies

- Server power supplies
- LCD television
- Plasma television

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1795T/N1	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

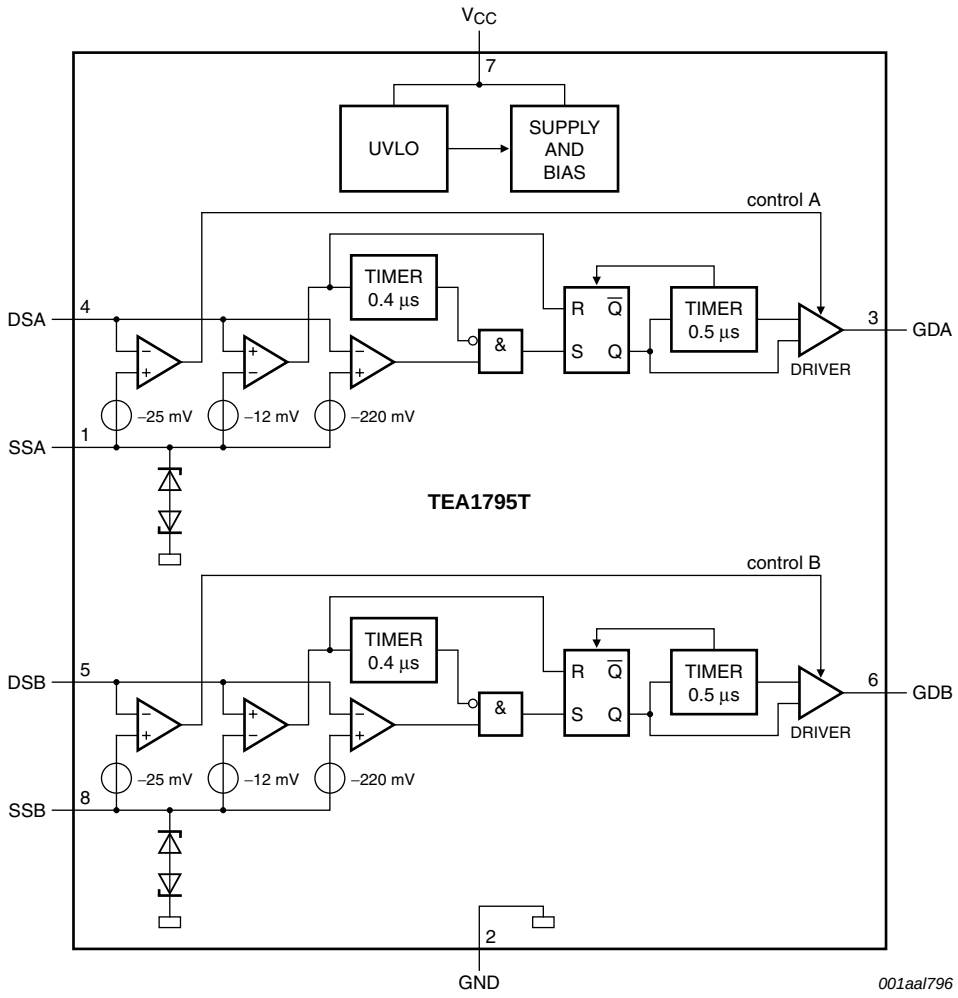


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

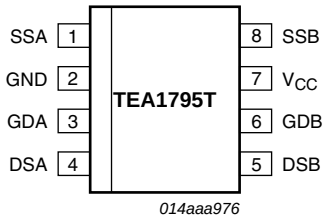


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SSA	1	source sense input MOSFET A
GND	2	ground
GDA	3	gate driver output MOSFET A
DSA	4	drain sense input for synchronous timing MOSFET A
DSB	5	drain sense input for synchronous timing MOSFET B
GDB	6	gate driver output MOSFET B
V_{CC}	7	supply voltage
SSB	8	source sense input MOSFET B

7. Functional description

7.1 Introduction

The TEA1795T is a controller for synchronous rectification to be used in resonant applications. It can drive two synchronous rectifier MOSFETs on the secondary side of the central tap transformer winding. A typical configuration is shown in Figure 3.

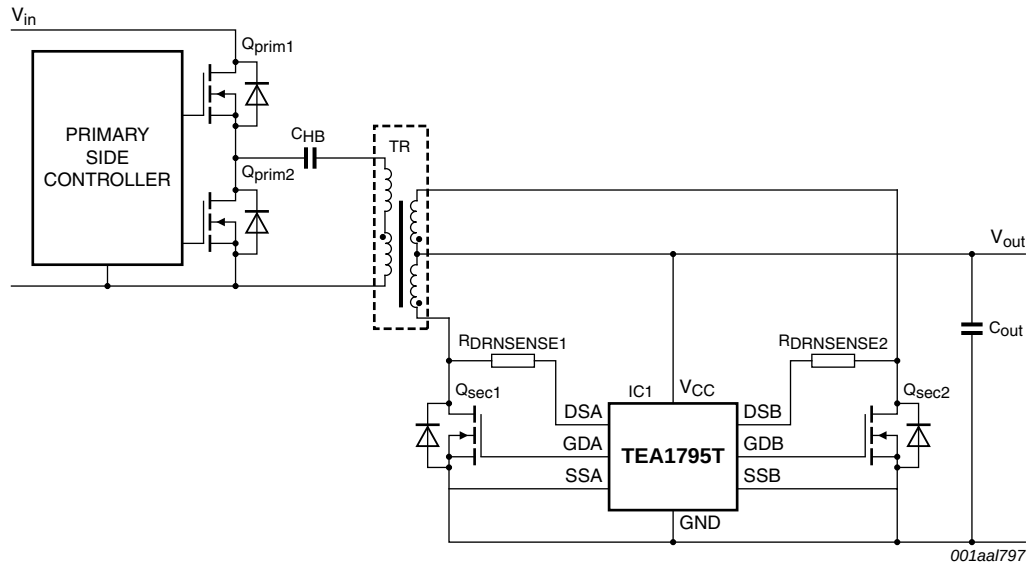


Fig 3. TEA1795T: typical configuration

7.2 Start-up and UnderVoltage LockOut (UVLO)

The IC leaves the UVLO state and activates the synchronous rectifier circuitry when the voltage on the V_{CC} pin is above $V_{startup}$ (8.5 V typical). When the voltage drops below 8.0 V (typical), the UVLO state is reentered and the SR MOSFET gate driver outputs are actively kept low.

7.3 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

7.4 Synchronous rectification (DSA, SSA, DSB and SSB pins)

The voltages present between the drain and source terminals of the SR MOSFETs are used to derive the timing for the gate drive signal. The IC senses the voltage difference between the drain sense (pins DSA and DSB) and the source sense (pins SSA and SSB) connections. When this voltage difference is lower than $V_{act(drv)}$ (−220 mV typical), the corresponding gate driver output voltage is driven high and the external SR MOSFET is switched on.

When the external SR MOSFET is switched on, the input signals on the drain sense pins and source sense pins are ignored during the minimum synchronous rectification active time ($t_{act(sr)(min)}$, 520 ns typical). This minimizes false switch-off due to the sensing of high frequency ringing signals at the start of the conduction phase.

Once this minimum synchronous rectification active time has ended, the IC monitors the difference between the drain sense inputs and the source sense inputs. When the difference is higher than $V_{reg(drv)}$ (−25 mV typical), the gate driver output voltage is regulated to maintain this −25 mV difference between the drain sense pins and the source sense pins. As a result, the SR MOSFET can be switched off quickly when the current through the external SR MOSFET reaches zero.

The zero current is detected by sensing a $V_{deact(drv)}$ (−12 mV typical) difference between the drain sense pins and the source sense pins (see Figure 4). A synchronous rectification off-timer ($t_{off(sr)(min)}$, 400 ns typical) is started and the next switching cycle can only be started when the synchronous rectification off-timer has finished.

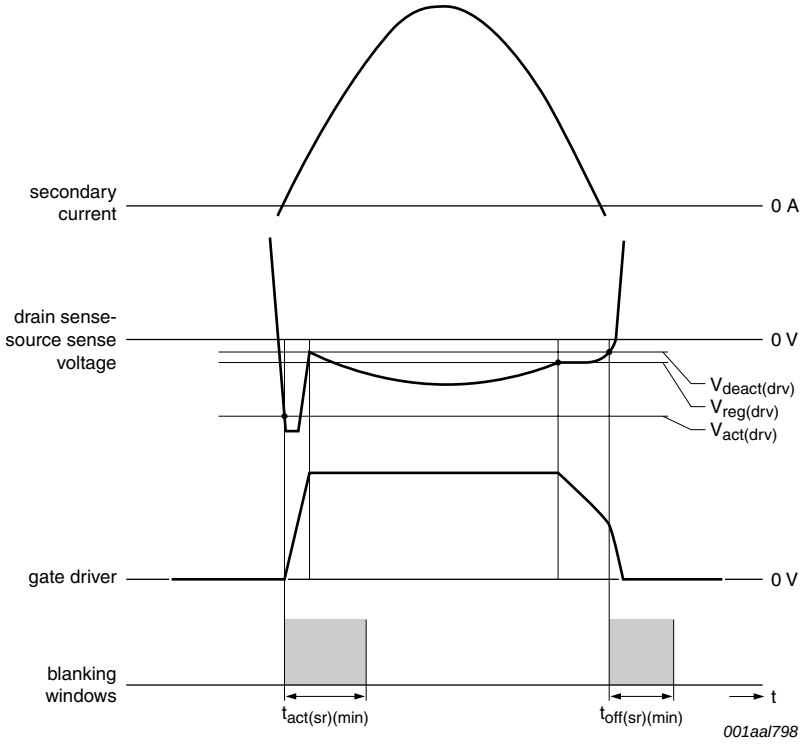


Fig 4. Synchronous rectification signals

7.5 Gate driver (GDA and GDB pins)

The gate driver circuit to the gate of the external SR MOSFET has a source capability of typically 400 mA and a sink capability of typically 2.7 A. This allows fast turn-on and turn-off of the external SR MOSFET for efficient operation. The source stage is coupled to the timer (see Figure 1). When the timer has finished, the source capability is reduced to a small current (4 mA typical) capable of keeping the driver output voltage at its level.

The output voltage of the driver is limited to 10 V (typical). This high output voltage drives all MOSFET brands to the minimum on-state resistance.

During start-up conditions ($V_{CC} < V_{startup}$) and UVLO the driver output voltage is actively pulled low.

7.6 Source sense (SSA and SSB pins)

The IC is equipped with additional source sense pins (SSA and SSB). These pins are used for the measurement of the drain-to-source voltage of the external SR MOSFET. This drain-to-source voltage determines the timing of the gate driver. The source sense input should be connected as close as possible to the source pin of the external SR MOSFET to minimize timing errors, caused by voltage difference on PCB tracks, due to parasitic inductance in combination with large dI/dt values.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	continuous	–0.4	+38	V
$V_{sense(D)A}$	drain sense voltage A	continuous	-	120	V
$V_{sense(D)B}$	drain sense voltage B	continuous	-	120	V
Currents					
$I_{drv(G)A}$	gate driver current A	δ < 10 %	–0.8	+3.0	A
$I_{drv(G)B}$	gate driver current B	δ < 10 %	–0.8	+3.0	A
$I_{I(DSA)}$	input current on pin DSA		–3	-	mA
$I_{I(DSB)}$	input current on pin DSB		–3	-	mA
$I_{I(SSA)}$	input current on pin SSA		–1	+1	mA
$I_{I(SSB)}$	input current on pin SSB		–1	+1	mA
General					
P_{tot}	total power dissipation	T_{amb} < 80 °C	-	0.45	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–40	+150	°C
ElectroStatic Discharge voltage (ESD)					
V_{ESD}	electrostatic discharge voltage	class 2			
		human body model [1]	-	2000	V
		machine model [2]	-	200	V
		charged device model	-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	150	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	100	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage management (pin V_{CC})							
$V_{startup}$	start-up voltage			8.2	8.5	8.8	V
V_{hys}	hysteresis voltage		[1]	-	0.5	-	V
$I_{CC(oper)}$	operating supply current	V_{CC} = 8 V (V_{CC} < $V_{startup}$)		-	0.35	-	mA
		f_{sw} = 200 kHz; no load on pins GDA and GDB		-	1.85	-	mA
Synchronous rectification sense input (pins DSA/SSA and pins DSB/SSB)							
$V_{act(drv)}$	driver activation voltage	$V_{sense(S)A}$ = 0 V; $V_{sense(S)B}$ = 0 V		–260	–220	–180	mV
$V_{reg(drv)}$	driver regulation voltage	$V_{sense(S)A}$ = 0 V; $V_{sense(S)B}$ = 0 V		–33	–25	–17	mV
$V_{deact(drv)}$	driver deactivation voltage	$V_{sense(S)A}$ = 0 V; $V_{sense(S)B}$ = 0 V	[2]	-	–12	-	mV
$V_{I(cm)}$	common-mode input voltage	pins SSA and SSB		–0.7	-	+0.7	V
$t_{d(act)(drv)}$	driver activation delay time	$V_{sense(S)A}$ = 0 V; $V_{sense(S)B}$ = 0 V; $V_{sense(D)A}$ = falling from +0.5 V to –0.5 V; $V_{sense(D)B}$ = falling from +0.5 V to –0.5 V		-	100	-	ns
$t_{d(deact)(drv)}$	driver deactivation delay time	$V_{sense(S)A}$ = 0 V; $V_{sense(S)B}$ = 0 V; $V_{sense(D)A}$ = rising from –0.35 V to +0.5 V; $V_{sense(D)B}$ = rising from –0.35 V to +0.5 V		-	35	-	ns
$t_{act(sr)(min)}$	minimum synchronous rectification active time			415	520	625	ns
$t_{off(sr)(min)}$	minimum synchronous rectification off-time			310	400	490	ns
Gate driver (pins GDA/GDB)							
I_{source}	source current	V_{CC} = 15 V; pins GDA/GDB = 2 V; during minimum synchronous rectification active time		–0.46	–0.4	–0.34	A
		V_{CC} = 15 V; pins GDA/GDB = 5 V; minimum synchronous rectification active time has ended		-	–4	-	mA
I_{sink}	sink current	V_{CC} = 15 V					
		pins GDA/GDB = 2 V		1	1.4	-	A
		pins GDA/GDB = 9.5 V		2.2	2.7	-	A
$V_{o(max)}$	maximum output voltage	V_{CC} = 15 V		-	10	12	V
Switching							
$f_{sw(max)}$	maximum switching frequency			500	-	-	kHz

[1] The V_{CC} stop voltage is $V_{startup} - V_{hys}$.

[2] The $V_{deact(drv)}$ level is always above the $V_{reg(drv)}$ level.

11. Application information

A switched mode power supply with the TEA1795T consists of a primary side half bridge, a transformer, a resonant capacitor and an output stage. In the output stage SR MOSFETs are used to obtain low conduction loss rectification. These SR MOSFETs are controlled by the TEA1795T.

The timing for the synchronous rectifier switch is derived from the voltage difference between the corresponding drain sense and source sense pins. The resistor in the drain sense connection is needed to protect the TEA1795T against excessive voltages. These resistors should typically be 1 kΩ. Higher values might impair correct timing, lower values may not provide sufficient protection.

Special attention should be paid to the connection of the drain sense and source sense pins. The voltages measured on these pins are used for the timing of the gate driver output. Wrong measurement results in wrong timing. The connections to these pins should not interfere with the power wiring. The power wiring conducts currents with high dI/dt values. This can easily cause measurement errors resulting from induced voltages due to parasitic inductances. The separate source sense pins make it possible to sense the source voltage of the external MOSFETs directly, without having to use the current carrying power ground tracks for this.

11.1 Application diagram resonant application

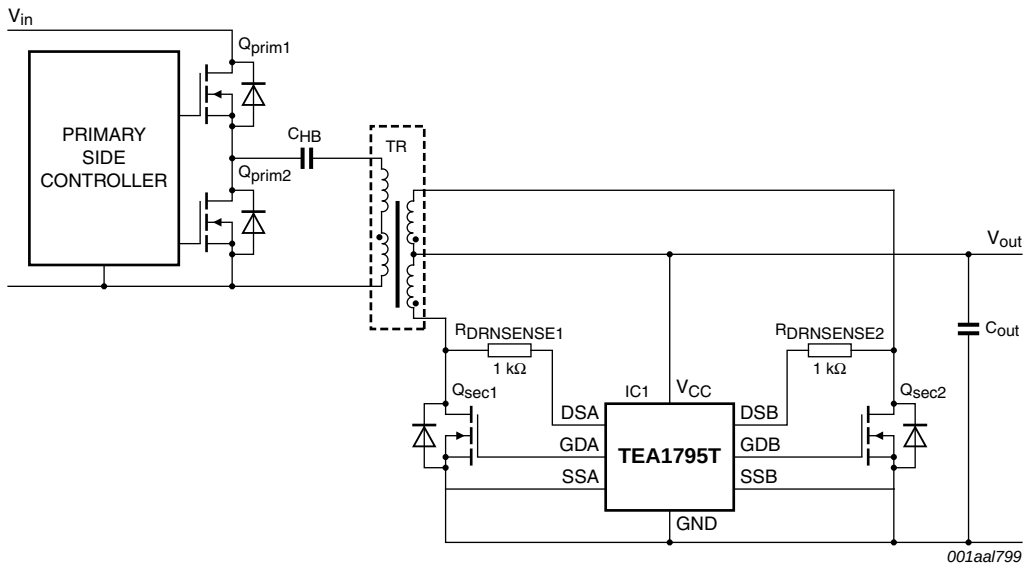


Fig 5. Typical resonant application with TEA1795T

11.2 Application diagram multi-output flyback application

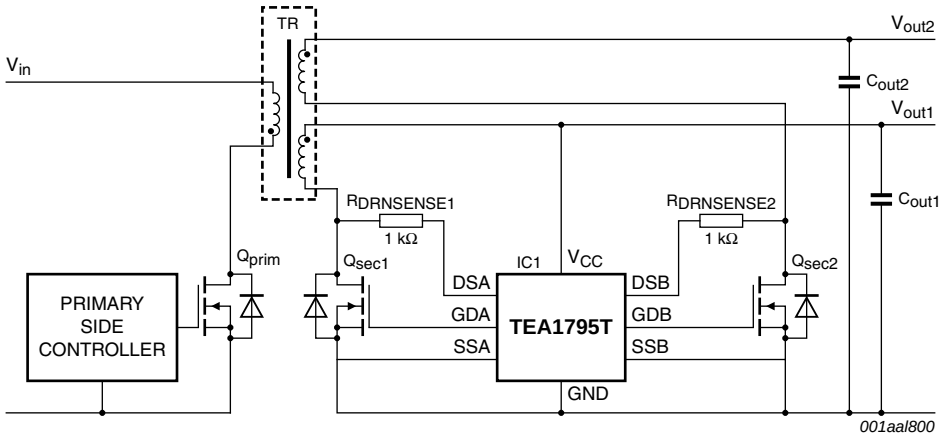
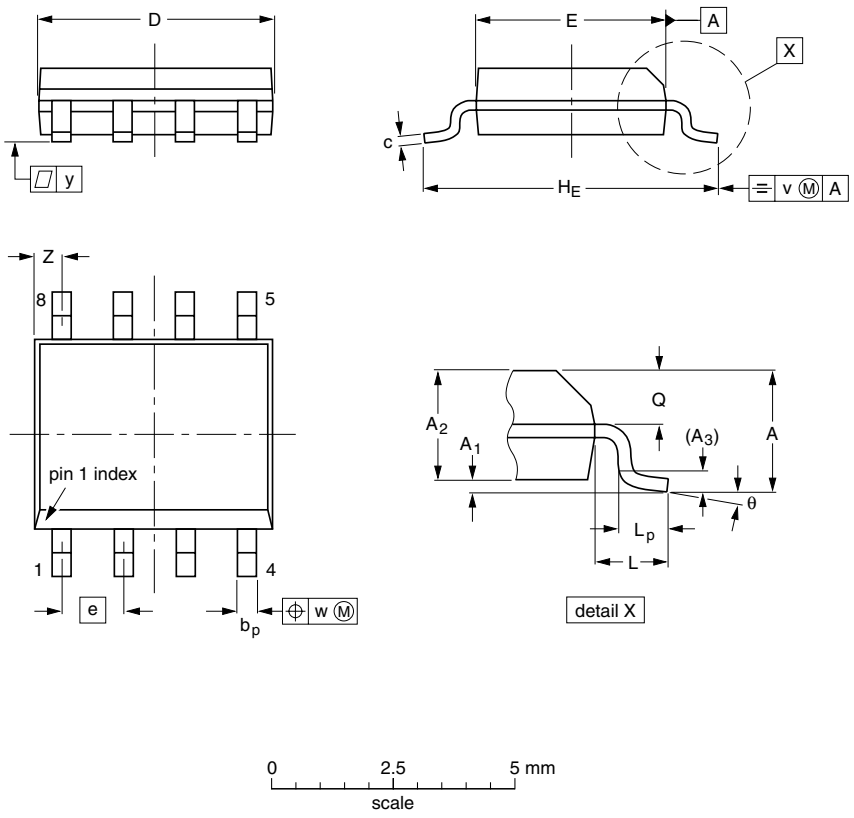


Fig 6. Multi-output flyback application with TEA1795T

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT096-1 (SO8)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1795T v.1	20101104	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

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