

MC74LVX573

Octal D-Type Latch with 3-State Outputs

With 5 V-Tolerant Inputs

The MC74LVX573 is an advanced high speed CMOS octal latch with 3-state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

Features

- High Speed: $t_{PD} = 6.4$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V;
Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant



ON Semiconductor®

<http://onsemi.com>

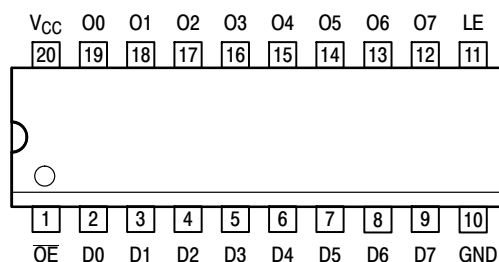


**SOIC-20
DW SUFFIX
CASE 751D**



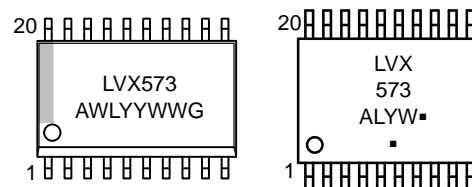
**TSSOP-20
DT SUFFIX
CASE 948E**

PIN ASSIGNMENT



20-Lead (Top View)

MARKING DIAGRAMS



SOIC-20

TSSOP-20

- LVX573 = Specific Device Code
- A = Assembly Location
- WL, L = Wafer Lot
- Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74LVX573

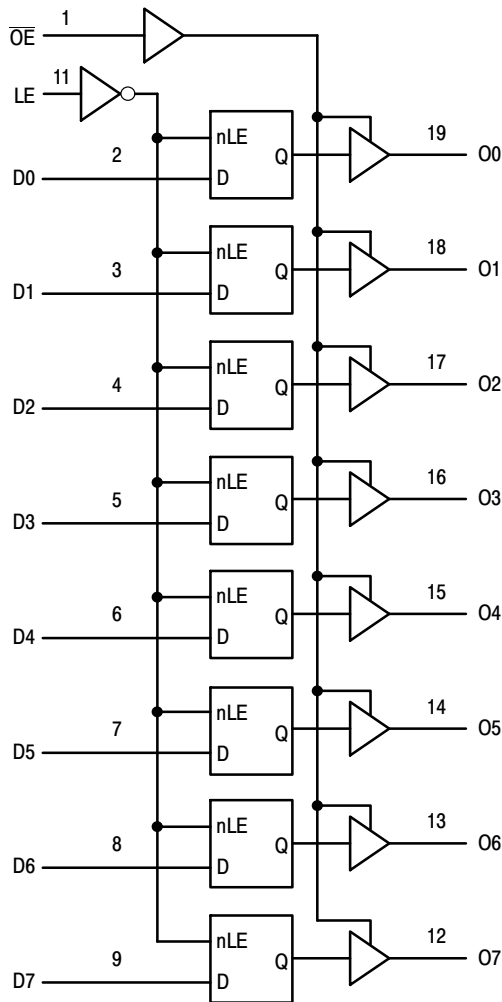


Figure 1. Logic Diagram

Table 1. PIN NAMES

Pins	Function
\overline{OE}	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

INPUTS			OUTPUTS	OPERATING MODE
OE	LE	Dn	On	
L	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	
L	L	h	H	Latched (Latch Enabled) Read Latch
L	L	l	L	
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H	H	H	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	
H	L	h	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; NC = No Change, State Prior to the Latch Enable High-to-Low Transition; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; For I_{CC} Reasons DO NOT FLOAT Inputs.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{in}	DC Input Voltage	-0.5 to +7.0	V
V_{out}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation	180	mW
T_{stg}	Storage Temperature	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MC74LVX573

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = -50 μA I _{OH} = -50 μA I _{OH} = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{in}	Input Leakage Current	V _{in} = 5.5 V or GND	3.6			±0.1		±1.0	μA
I _{OZ}	Maximum 3-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	3.6			±0.2 5		±2.5	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = -40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay LE to O	V _{CC} = 2.7 V C _L = 15 pF C _L = 50 pF		8.2 10.7	15.6 19.1	1.0 1.0	18.5 22.0	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		6.4 8.9	10.1 13.6	1.0 1.0	12.0 15.5	
t _{PLH} , t _{PHL}	Propagation Delay D to O	V _{CC} = 2.7 V C _L = 15 pF C _L = 50 pF		7.6 10.1	14.5 18.0	1.0 1.0	17.5 21.0	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		5.9 8.4	9.3 12.8	1.0 1.0	11.0 14.5	
t _{PZL} , t _{PZH}	Output Enable Time OE to O	V _{CC} = 2.7 V R _L = 1 kΩ C _L = 15 pF C _L = 50 pF		7.8 10.3	15.0 18.5	1.0 1.0	18.5 22.0	ns
		V _{CC} = 3.3 ± 0.3 V R _L = 1 kΩ C _L = 15 pF C _L = 50 pF		6.1 8.6	9.7 13.2	1.0 1.0	12.0 15.5	
t _{PLZ} , t _{PHZ}	Output Disable Time OE to O	V _{CC} = 2.7 V R _L = 1 kΩ C _L = 50 pF		12.1	19.1	1.0	22.0	ns
		V _{CC} = 3.3 ± 0.3 V R _L = 1 kΩ C _L = 50 pF		10.1	13.6	1.0	15.5	
t _{OSHL} , t _{OSLH}	Output-to-Output Skew (Note 1)	V _{CC} = 2.7 V V _{CC} = 3.3 ± 0.3 V C _L = 50 pF C _L = 50 pF			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

MC74LVX573

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T _A = 25°C			T _A = -40 to 85°C		Unit
		Min	Typ	Max	Min	Max	
C _{in}	Input Capacitance		4	10		10	pF
C _{out}	Maximum 3-State Output Capacitance		6				pF
C _{PD}	Power Dissipation Capacitance (Note 2)		29				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 3.3 V, Measured in SOIC Package)

Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.5	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.5	-0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions	T _A = 25°C		T _A = -40 to 85°C	Unit
			Typ	Limit	Limit	
t _{w(h)}	Minimum Pulse Width, LE	V _{CC} = 2.7 V V _{CC} = 3.3 ± 0.3 V		6.5 5.0	7.5 5.0	ns
t _{su}	Minimum Setup Time, D to LE	V _{CC} = 2.7 V V _{CC} = 3.3 ± 0.3 V		5.0 3.5	5.0 3.5	ns
t _h	Minimum Hold Time, D to LE	V _{CC} = 2.7 V V _{CC} = 3.3 ± 0.3 V		1.5 1.5	1.5 1.5	ns

MC74LVX573

SWITCHING WAVEFORMS

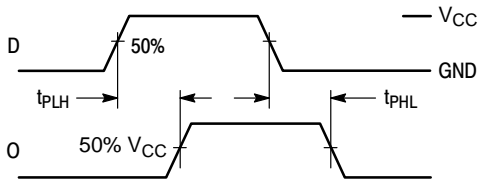


Figure 2.

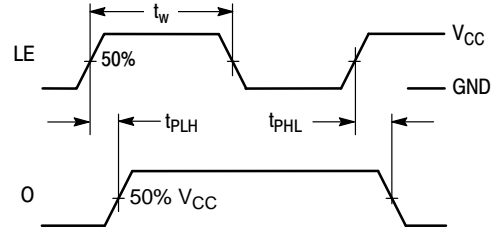


Figure 3.

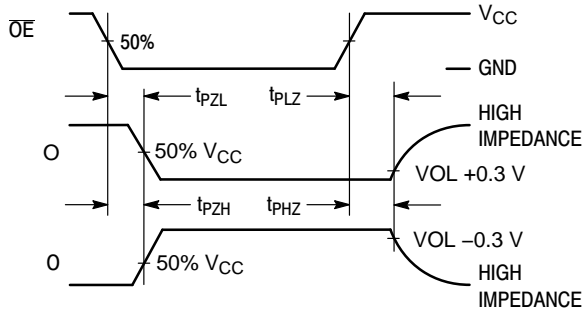


Figure 4.

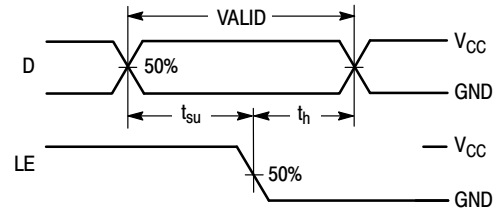
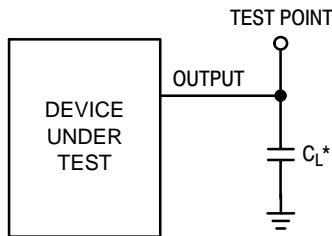


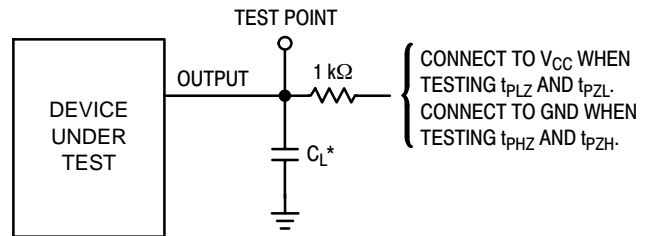
Figure 5.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 6. Propagation Delay Test Circuit



*Includes all probe and jig capacitance

Figure 7. 3-State Test Circuit

ORDERING INFORMATION

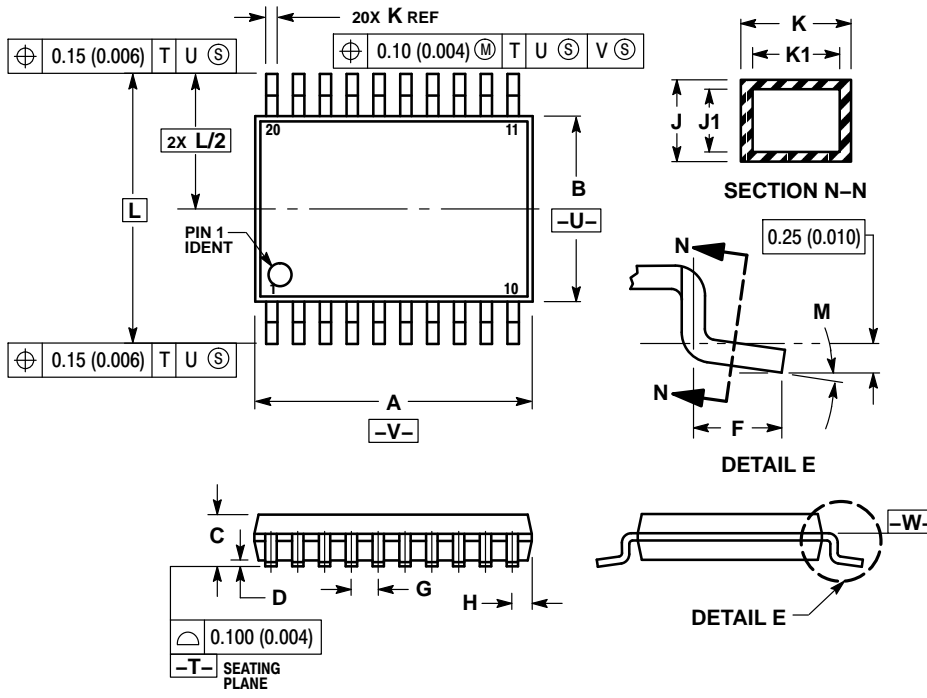
Device	Package	Shipping†
MC74LVX573DWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel
MC74LVX573DTG	TSSOP-20 (Pb-Free)	75 Units / Rail
MC74LVX573DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74LVX573

PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

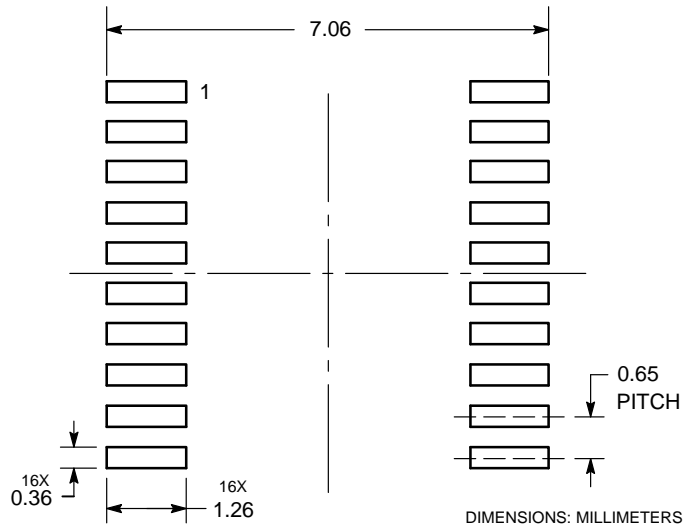


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

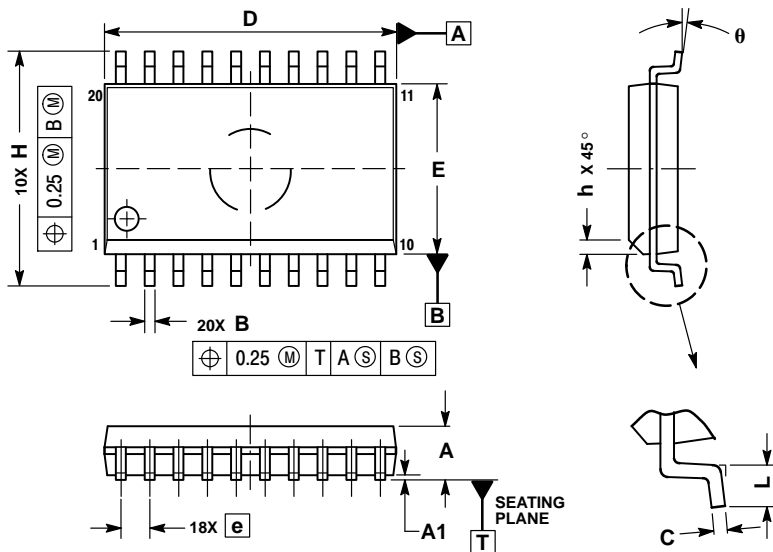


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74LVX573

PACKAGE DIMENSIONS


SOIC-20
CASE 751D-05
ISSUE G



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative